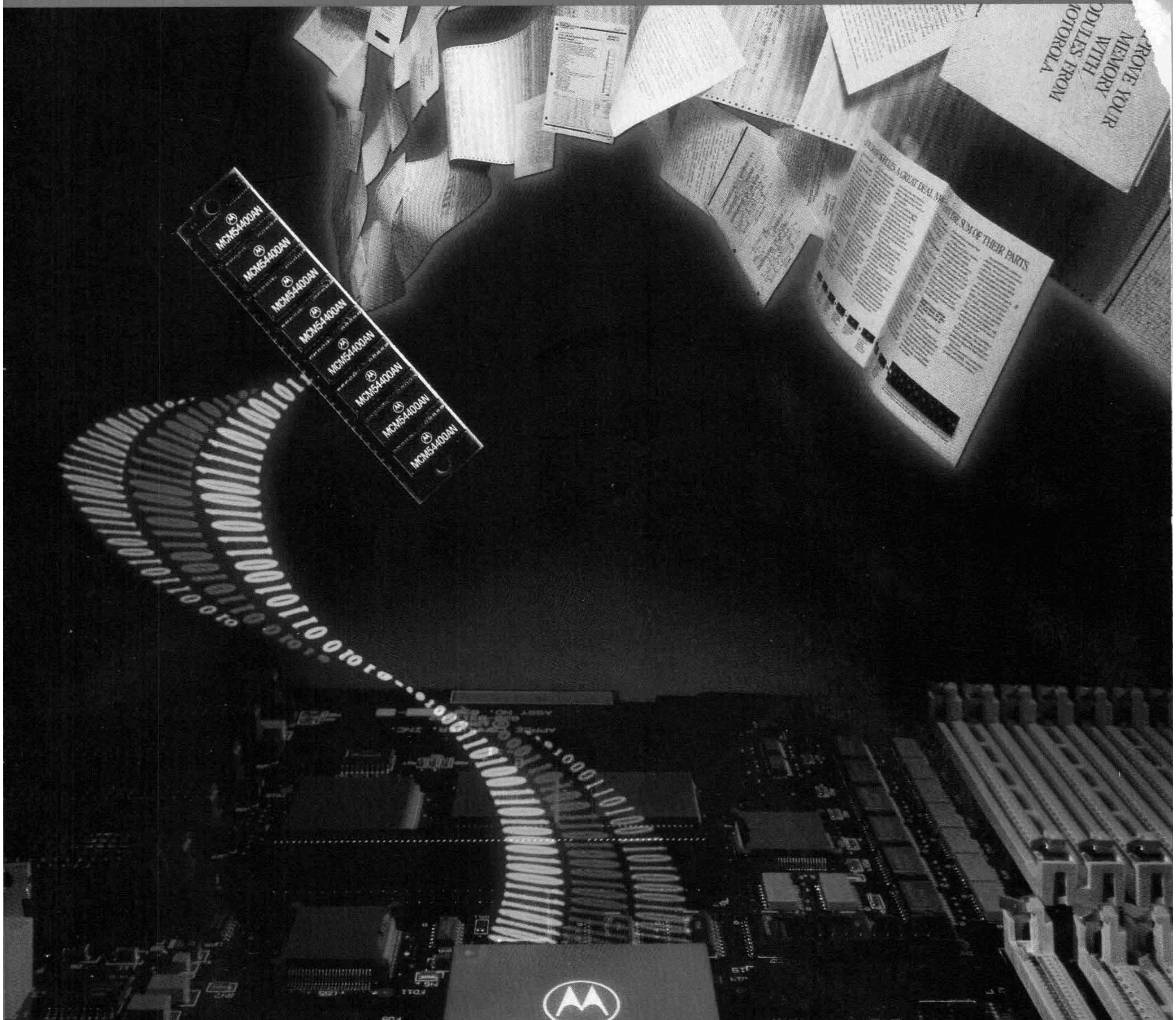
MOTOROLA

DL155/D

Dynamic RAMs

& Memory Modules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PROVE YOUR
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Selector Guide and Cross Reference

CMOS 1M Dynamic RAMs

CMOS 4M Dynamic RAMs

CMOS 16M Dynamic RAMs

Dynamic RAM Modules

General Memory Devices

Military Products

Reliability Information

Applications Information

Mechanical Data

DATA CLASSIFICATION

Product Preview

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Dynamic RAM Data

Motorola has developed a broad range of reliable dynamic RAMs and Memory Modules for virtually any digital data processing system application. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, a selector guide and a cross reference are included to simplify the task of choosing the best combination of circuits for optimum system architecture.

For information on Fast Static RAM devices, please refer to DL156/D. For information on Military Memory devices, please contact your Motorola representative.

New Motorola memories are being introduced continually. For the latest releases, additional technical information, and pricing, please contact your nearest authorized Motorola distributor or Motorola Sales Office. A complete listing of distributors and sales offices is included at the back of this book.

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TABLE OF CONTENTS

ALPHANUMERIC INDEX viii

CHAPTER 1 — SELECTOR GUIDE AND CROSS REFERENCE

Selector Guide 1-3
Cross Reference 1-11

CHAPTER 2 — CMOS 1M DYNAMIC RAMs

MCM411000 2-3
MCM414256 2-16
MCM511000A 2-29
MCM511000B 2-44
MCM511001A 2-59
MCM511002A 2-74
MCM514256A 2-89
MCM514256B 2-104
MCM514258A 2-119

CHAPTER 3 — CMOS 4M DYNAMIC RAMs

MCM44100 3-3
MCM44400 3-20
MCM54100A 3-38
MCM54100A-C 3-57
MCM54101A 3-75
MCM54102A 3-92
MCM54170B 3-114
MCM54190B 3-149
MCM54260B 3-184
MCM54280B 3-213
MCM54400A 3-241
MCM54400A-C 3-261
MCM54402A 3-281
MCM54800A 3-303

CHAPTER 4 — CMOS 16M DYNAMIC RAMs

MCM516100 4-3
MCM516400 4-3
MCM517400 4-3

CHAPTER 5 — DYNAMIC RAM MODULES

DRAM MODULES ORGANIZED x 8 BITS

256K x 8 256KB MCM84256 5-3
1M x 8 1MB MCM81000 5-15
MCM81430 5-27
4M x 8 4MB MCM84000 5-39
MCM84030 5-39
16M x 8 16MB MCM81600 5-51

TABLE OF CONTENTS (Continued)

DRAM MODULES ORGANIZED x 9 BITS

256K x 9 256KB MCM94256 5-53
1M x 9 1MB MCM91000 5-65
MCM91430 5-77
4M x 9 4MB MCM94000 5-88
MCM94030 5-88
16M x 9 16MB MCM91600 5-100

DRAM MODULES ORGANIZED x 32 BITS

256K x 32 256KB MCM32256 5-102
512K x 32 512KB MCM32512 5-114
1M x 32 1MB MCM32130 5-126
2M x 32 2MB MCM32230 5-138
4M x 32 4MB MCM32400 5-150
8M x 32 8MB MCM32800 5-152

DRAM MODULES ORGANIZED x 36 BITS

256K x 36 256KB MCM36256 5-155
512K x 36 512KB MCM36512 5-167
1M x 36 1MB MCM36100 5-179
2M x 36 2MB MCM36200 5-191
4M x 36 4MB MCM36400 5-203
8M x 36 8MB MCM36800 5-206

DRAM MODULES ORGANIZED x 40 BITS

256K x 40 256KB MCM40256 5-209
512K x 40 512KB MCM40512 5-225
1M x 40 1MB MCM40100 5-241
2M x 40 2MB MCM40200 5-257
4M x 40 4MB MCM40400 5-273
8M x 40 8MB MCM40800 5-276

DRAM MODULES ORGANIZED x 72 BITS

1M x 72 1MB MCM72100 5-279
2M x 72 2MB MCM72200 5-282
4M x 72 4MB MCM72400 5-285
8M x 72 8MB MCM72800 5-288

CHAPTER 6 — GENERAL MEMORY DEVICES

MCM2018A 6-3
MCM2814 6-8
MCM60L256A-C 6-23
MCM60L256A-V 6-31

CHAPTER 7 — MILITARY PRODUCTS

CHAPTER 8 — RELIABILITY INFORMATION

Reliability Information 8-2

TABLE OF CONTENTS (Concluded)

CHAPTER 9 — APPLICATIONS INFORMATION

AN968 Page, Nibble, and Static Column Modes: High-Speed, Serial-Access Options on 1M-Bit + DRAMs 9-3
AN987 DRAM Refresh Modes 9-7
AN1124 1M to 4M DRAM Upgrading 9-9
AN1125 DRAM Interface to the MC88200 M Bus 9-11
AN1127 High Speed DRAM Design for the 40 MHz MC68EC030 9-50
AN1202 Battery Backup of Self-Refreshing Dynamic Random Access Memory 9-67

CHAPTER 10 — MECHANICAL DATA

Case Outlines 10-3
TRMEM 10-15

SALES OFFICES

ALPHANUMERIC INDEX — DRAM AND FSRAM

Device	Org	Access Time (ns)	Comments	Page
MCM2018A	2K x 8	35/45/55		6-3
MCM2814	256 x 8		Byte programmable serial EEPROM	6-8
MCM3264A	64K x 32	15/20	Perfect for 32-bit system; JEDEC standard.	DL156
MCM36B32	32K x 36	12/14/19/24	BurstRAM module for i486	DL156
MCM36B64	64K x 36	12/14/19/24	BurstRAM module for i486	DL156
MCM36M32	32K x 36	12/14/19/24	BurstRAM module for 68040	DL156
MCM36M64	64K x 36	12/14/19/24	BurstRAM module for 68040	DL156
MCM4464	64K x 36	12/15/17	1M byte R4000 cache module	DL156
MCM6205C	32K x 9	15/17/20/25/35		DL156
MCM62L05C	32K x 9	20/25/35	Low standby current	DL156
MCM6206C	32K x 8	15/17/20/25/35		DL156
MCM62L06C	32K x 8	20/25/35	Low standby current	DL156
MCM62V06D	32K x 8	25/35	First 3.3 V Fast SRAM	DL156
MCM62L07	256K x 1	20/25/35	Battery backup appl. Idr = 50 µA; Main memory appl. Isb2 = 100 µA	DL156
MCM6207C	256K x 1	15/20/25		DL156
MCM62L07C	256K x 1	20/25/35	Battery backup appl. Idr = 50 µA; Main memory appl. Isb2 = 100 µA	DL156
MCM62L08	64K x 4	20/25/35	Low standby current	DL156
MCM6208C	64K x 4	15/20/25/35		DL156
MCM62L08C	64K x 4	20/25/35	Low standby current	DL156
MCM62L09	64K x 4	20/25/35	Low standby current; output enable	DL156
MCM6209C	64K x 4	15/20/25/35	Output enable	DL156
MCM62L09C	64K x 4	20/25/35	Low standby current; output enable	DL156
MCM6226A	128K x 8	20/25/35/45		DL156
MCM62L26A	128K x 8	25/35/45	Low standby current	DL156
MCM6227A	1M x 1	20/25/35/45	Separate I/O	DL156
MCM62L27A	1M x 1	25/35/45	Separate I/O	DL156
MCM6229A	256K x 4	20/25/35/45	Output enable	DL156
MCM62L29A	256K x 4	25/35/45	Low standby current; output enable	DL156
MCM6246	512K x 8	25/30/35		DL156
MCM6249	1M x 4	25/30/35		DL156
MCM6264C	8K x 8	12/15/20/25/35		DL156
MCM6265C	8K x 9	12/15/20/25/35		DL156
MCM6268	4K x 4	20/25/35/45/55		DL156
MCM6269	4K x 4	20/25/35		DL156
MCM6270	4K x 4	20/25/35	Fast output enable access time = 10/12/14 ns	DL156
MCM6287B	64K x 1	12/15/20/25/35	Mainframe applications; also use for parity	DL156
MCM6288C	16K x 4	12/15/20/25/35		DL156
MCM6290C	16K x 4	10/12/15/20/25/35	Output enable; 10 ns SOJ only	DL156
MCM6293	16K x 4	20/25	Synchronous; pipelined	DL156
MCM6294	16K x 4	20/25	Synchronous; pipelined; output enable	DL156
MCM6295	16K x 4	25/30	Synchronous; output enable	DL156
MCM6705A	32K x 9	10/12	Evolutionary pinout	DL156
MCM6706A	32K x 8	8/10/12	Use for new quals and designs; evolutionary pinout	DL156
MCM6706R	32K x 8	6/7/8	Use for new quals and designs; revolutionary pinout	DL156

Device	Org	Access Time (ns)	Comments	Page
MCM6708A	64K x 4	8/10/12	Use for new quals and designs	DL156
MCM6709A	64K x 4	8/10/12	Use for new quals and designs; output enable	DL156
MCM6709R	64K x 4	6/7/8	Use for new quals and designs; revolutionary pinout; output enable	DL156
MCM6726	128K x 8	10/12/15	Revolutionary pinout	DL156
MCM6726A	128K x 8	8/10/12/15	Revolutionary pinout	DL156
MCM6727	1M x 1	10/12/15	Separate I/O; revolutionary pinout	DL156
MCM6727A	1M x 1	8/10/12/15	Separate I/O; revolutionary pinout	DL156
MCM6728	256K x 4	10/12/15	Revolutionary pinout	DL156
MCM6728A	256K x 4	8/10/12/15	Revolutionary pinout	DL156
MCM6729	256K x 4	10/12/15	Output enable; revolutionary pinout	DL156
MCM6729A	256K x 4	8/10/12/15	Output enable; revolutionary pinout	DL156
MCM8256	256K x 8	15/20	JEDEC standard module	DL156
MCM32128	128K x 32	20/25/35	JEDEC standard module	DL156
MCM32130	1M x 32	60/70/80	Fast page mode cycle time = 45/50 ns	5-126
MCM32230	2M x 32	60/70/80	Fast page mode cycle time = 45/50 ns	5-138
MCM32256	256K x 32	70/80	Fast page mode cycle time = 40/45 ns	5-102
MCM32257	256K x 32	20/25/35	8M bit module	DL156
MCM32400	4M x 32	60/70/80	Fast page mode cycle time = 40/45/50 ns	5-150
MCM32512	512K x 32	70/80	Fast page mode cycle time = 40/45 ns	5-114
MCM32800	8M x 32	60/70/80	Fast page mode cycle time = 40/45/50 ns	5-152
MCM36100	1M x 36	70/80	MCM32130 with parity application	5-179
MCM36200	2M x 36	70/80	MCM32256 with parity application	5-191
MCM36256	256K x 36	70/80	MCM32400 with parity application	5-155
MCM36232	2 x 32K x 36	15/20	Designed for parity applications	DL156
MCM36400	4M x 36	60/70/80	MCM32230 with parity application	5-203
MCM36512	512K x 36	70/80	MCM32800 with parity application	5-167
MCM36800	8M x 36	60/70/80	MCM32512 with parity application	5-206
MCM40100	1M x 40	60/70/80	MCM32100 with error correction applications	5-241
MCM40200	2M x 40	60/70/80	MCM32200 with error correction applications	5-257
MCM40256	256K x 40	70/80	MCM32256 with error correction applications	5-209
MCM40400	4M x 40	60/70/80	MCM32400 with error correction applications	5-273
MCM40512	512K x 40	70/80	MCM32800 with error correction applications	5-255
MCM40800	8M x 40	60/70/80	MCM32512 with error correction applications	5-276
MCM44100	4M x 1	60/70/80	Fast page mode cycle time = 50/55/55 ns	3-3
MCM44256	256K x 36	12/15/17	4M byte R4000 cache module	DL156
MCM44400	1M x 4	60/70/80	Fast page mode cycle time = 50/55/55 ns	3-20
MCM54100A	4M x 1	60/70/80	Fast page mode cycle time = 50/55/55 ns	3-38
MCM54100A-C	4M x 1	70/80	Industrial temperature range = (- 40 to + 84 °C)	3-57
MCM54101A	4M x 1	60/70/80	Nibble mode cycle time = 40/40/40 ns	3-75
MCM54102A	4M x 1	60/70/80	Static column mode cycle time = 35/40/45 ns	3-92
MCM54170B	256K x 16	70/80/100	Fast page mode, 1 CAS, 2W, 1024 refresh	3-114
MCM54190B	256K x 16	70/80/100	Fast page mode, 2 CAS, 1W, 512 refresh	3-149
MCM54260B	256K x 16	70/80/100	Fast page mode, 1 CAS, 2W, 1024 refresh	3-184
MCM54280B	256K x 16	70/80/100	Fast page mode, 2 CAS, 1W, 512 refresh	3-213

Device	Org	Access Time (ns)	Comments	Page
MCM54400A	1M x 4	60/70/80	Fast page mode cycle time = 45/45/50 ns	3-241
MCM54400A-C	1M x 4	70/80	Industrial temperature range = (- 40 to + 85° C)	3-261
MCM54402A	1M x 4	60/70/80	Static column mode cycle time = 35/40/45 ns	3-281
MCM54800A	512K x 8	70/80	Fast page mode cycle time = 50/60 ns	3-303
MCM56824A	8K x 24	20/25/35	DSPRAM for DSP56001 applications	DL156
MCM60L256A-C	32K x 8	100	Industrial temperature range (- 40 to + 85° C). low power	6-23
MCM60L256A-V	32K x 8	100	Extended temperature range (- 40 to + 105° C), low power	6-31
MCM62110	32K x 9	15/17/20	Dual I/O's for 88110 and other microprocessor applications	DL156
MCM62486A	32K x 9	11/12/14/19/24	i486 synchronous BurstRAM cache	DL156
MCM62820A	8K x 20	17/23	Designed for MIPS R3000 cache	DL156
MCM62940A	32K x 9	11/12/14/19/24	68040 synchronous BurstRAM cache	DL156
MCM62950A	32K x 9	15/20/25	RISC-CISC synchronous cache	DL156
MCM62963A	4K x 10	30	Synchronous; output registers	DL156
MCM62973A	4K x 12	18/20	Synchronous; output registers	DL156
MCM62974A	4K x 12	18/20	Synchronous; output registers; output enable	DL156
MCM62975A	4K x 12	25/30	Synchronous; output enable	DL156
MCM62980	64K x 4	15/20	Synchronous; registered address	DL156
MCM62981	64K x 4	15/20	ParityRAM; synchronous; registered address	DL156
MCM62982	64K x 4	12/15	Synch; registered address and outputs for 2 stage pipeline	DL156
MCM62983	64K x 4	12/15	ParityRAM; synch; registered address and outputs for 2 stage pipeline	DL156
MCM62990A	16K x 16	12/15/20/25	Designed for advanced RISC-CISC applications	DL156
MCM62995A	16K x 16	12/15/20/25	DSP96000 and MIPS R3000 applications; Address and data input latches	DL156
MCM62996	16K x 16	12/15/20/25	Choice of 5 V or 3.3 V power supplies for output buffers	DL156
MCM67Q004	1M x 4	8	Synchronous; Separate I/O	DL156
MCM67A618	64K x 18	12/15/20	Asynchronous; latched address	DL156
MCM67B618	64K x 18	11/14/19	Burst counter; asynch output enable; i486/P5 BurstRAM	DL156
MCM67C618	64K x 18	9	Burst counter; asynch output enable; i486/P5 BurstRAM	DL156
MCM67F618	64K x 18	12/15	CISC sync; reg. to latch; registered output and chip enable	DL156
MCM67M618	64K x 18	11/14/19	Burst counter; asynch output enable; 68040 BurstRAM	DL156
MCM67P618	64K x 18	6/8/10/12	RISC; sync pipelined; reg. to reg; registered output and chip enable	DL156
MCM67W618	64K x 18	12/15/20	Asynch w/ byte enable	DL156
MCM67F804	256K x 4	12/15	Synch; secondary cache RISC; 3.3 V output levels	DL156
MCM67P804	256K x 4	10/12	Synch; secondary cache RISC; 3.3 V output levels	DL156
MCM67Q804	256K x 4	10/12	Graphics; secondary cache RISC; revolutionary pinout; 3.3 V output	DL156
MCM72100	1M x 72	60/70/80	64 bit data bus and 8 bit for EDC	5-279
MCM72200	2M x 72	60/70/80	64 bit data bus and 8 bit for EDC	5-282
MCM72400	4M x 72	60/70/80	64 bit data bus and 8 bit for EDC	5-285
MCM72800	8M x 72	60/70/80	64 bit data bus and 8 bit for EDC	5-288
MCM81000	1M x 8	70/80	Fast page mode cycle time = 40/45 ns	5-15
MCM81100	1M x 8	20/25/35	8M bit byte module	DL156
MCM81430	1M x 8	60/70/80	Two chip derivative of MCM81000	5-27
MCM81600	16M x 8	60/70/80	Fast page mode cycle time = 40/45/50 ns	5-51
MCM84000	4M x 8	60/70/80	Fast page mode cycle time = 45/50 ns	5-39
MCM84030	4M x 8	60/70/80	Low height (0.52 in) version of MCM8L4000	5-39

Device	Org	Access Time (ns)	Comments	Page
MCM84256	256K x 8	70/80	Fast page mode cycle time = 40/45 ns	5-3
MCM91000	1M x 9	70/80	Fast page mode cycle time = 40/45 ns	5-65
MCM91430	1M x 9	60/70/80	Three chip derivative of MCM91000	5-77
MCM91600	16M x 9	60/70/80	Fast page mode cycle time = 40/45/50 ns	5-100
MCM94000	4M x 9	60/70/80	Fast page mode cycle time = 45/50 ns	5-88
MCM94030	4M x 9	60/70/80	Low height 4M x 9 using MCM54100AN DRAM	5-88
MCM94256	256K x 9	70/80	Fast page mode cycle time = 40/45 ns	5-53
MCM101510	1M x 1	10/12	100K ECL compatible @ - 5.2 V; separate I/O	DL156
MCM101514	256K x 4	10/12	100K ECL compatible @ - 5.2 V; separate I/O	DL156
MCM101520	4M x 1	10/12/15	100K ECL compatible @ - 5.2 V	DL156
MCM101524	1M x 4/2M x 2	10/12/15	100K ECL compatible @ - 5.2 V	DL156
MCM411000	1M x 1	70/80	Fast page mode cycle time = 50/55 ns	2-3
MCM414256	256K x 4	70/80	Fast page mode cycle time = 50/55 ns	2-16
MCM511000A	1M x 1	70/80	Fast page mode cycle time = 40 ns	2-29
MCM511000B	1M x 1	60	Fast page mode cycle time = 40/45 ns	2-44
MCM511001A	1M x 1	70/80	Nibble mode access time = 35/35 ns	2-59
MCM511002A	1M x 1	70/80	Static column mode access time = 40/45 ns	2-74
MCM514256A	256K x 4	70/80	Fast page mode cycle time = 40/45 ns	2-89
MCM514256B	256K x 4	60	Fast page mode cycle time = 40 ns	2-104
MCM514258A	256K x 4	70/80	Static column mode access time = 40/45 ns	2-119
MCM516100	16M x 1	60/70/80	Fast page mode cycle time = 40/45/50 ns 4K; refresh	4-3
MCM516400	4M x 4	60/70/80	Fast page mode cycle time = 40/45/50 ns 4K; refresh	4-3
MCM517400	4M x 4	60/70/80	Fast page mode cycle time = 40/45/50 ns; 4K refresh	4-3

NOTES:
1. "Evolutionary pinout" refers to in-line packages with corner power/ground pins.
2. "Revolutionary pinout" refers to in-line packages with center power/ground pins.
3. DL156 is the Fast Static RAM BiCMOS, CMOS, and Module Data Book, which is available now from LDC.

DYNAMIC RAM SELECTOR GUIDE

Org	Motorola Part Number	Package Information 300 mil DIP	300 mil SOJ	400 mil SOJ	100 mil ZIP	300 mil TSOP	400 mil TSOP	Address Access (ns Max)	Op Current (mA Max)	Low Power	Industrial Temp
1M X 1	MCM411000-70	18	20/26		20			70	80		
	MCM411000-80	18	20/26		20			80	70		
	MCM41L1000-70	18	20/26		20			70	80	•	
	MCM41L1000-80	18	20/26		20			80	70	•	
	MCM511000A-70	18	20/26		20			70	80		
	MCM511000A-80	18	20/26		20			80	70		
	MCM51L1000A-70	18	20/26		20			70	80	•	
	MCM51L1000A-80	18	20/26		20			80	70	•	
	MCM511000B-60		20/26		20			60	90		
	MCM511001A-70	18	20/26		20			70	80		
	MCM511001A-80	18	20/26		20			80	70		
	MCM511002A-70	18	20/26		20			70	80		
	MCM511002A-80	18	20/26		20			80	70		
256K X 4	MCM414256-70	20	20/26		20			70	80		
	MCM414256-80	20	20/26		20			80	70		
	MCM41L4256-70	20	20/26		20			70	80	•	
	MCM41L4256-80	20	20/26		20			80	70	•	
	MCM514256A-70	20	20/26		20			70	80		
	MCM514256A-80	20	20/26		20			80	70		
	MCM51L4256A-70	20	20/26		20			70	80	•	
	MCM51L4256A-80	20	20/26		20			80	70	•	
	MCM514256A-C70							70	85		•
	MCM514256A-C80							80	75		•
	MCM51L4256A-C70							70	85	•	•
	MCM51L4256A-C80							80	75	•	•
	MCM514256B-60		20/26		20			60	90		
	MCM514258A-70	20	20/26		20			70	80		
	MCM514258A-80	20	20/26		20			80	70		
4M X 1	MCM34100A-60		20/26					60	120		
	MCM34100A-70		20/26					70	100		

DYNAMIC RAM SELECTOR GUIDE (cont.)

Org	Motorola Part Number	Package Information						Address Access (ns Max)	Op Current (mA Max)	Low Power	Industrial Temp
		300 mil DIP	300 mil SOJ	400 mil SOJ	100 mil ZIP	300 mil TSOP	400 mil TSOP				
4M X 1 (cont.)	MCM34100A-80		20/26					80	80		
	MCM44100-60		20/26		20			60	120		
	MCM44100-70		20/26		20			70	100		
	MCM44100-80		20/26		20			80	85		
	MCM4L4100-60		20/26		20			60	120	•	
	MCM4L4100-70		20/26		20			70	100	•	
	MCM4L4100-80		20/26		20			80	85	•	
	MCM54100A-60		20/26		20	20/26		60	120		
	MCM54100A-70		20/26		20	20/26		70	100		
	MCM54100A-80		20/26		20	20/26		80	85		
	MCM5L4100A-60		20/26		20	20/26		60	120	•	
	MCM5L4100A-70		20/26		20	20/26		70	100	•	
	MCM5L4100A-80		20/26		20	20/26		80	85	•	
	MCM54100A-C70		20/26		20			70	100		•
	MCM54100A-C80		20/26		20			80	85		•
1M X 4	MCM34400A-60		26					60	120		
	MCM34400A-70		26					70	100		
	MCM34400A-80		26					80	85		
	MCM44400-60		20/26		20			60	120		
	MCM44400-70		20/26		20			70	100		
	MCM44400-80		20/26		20			80	85		
	MCM4L4400-60		20/26		20			60	120	•	
	MCM4L4400-70		20/26		20			70	100	•	
	MCM4L4400-80		20/26		20			80	85	•	
	MCM54400A-60		20/26		20			60	120		
	MCM54400A-70		20/26		20			70	100		
	MCM54400A-80		20/26		20			80	85		
	MCM5L4400A-60		20/26		20			60	120	•	
	MCM5L4400A-70		20/26		20			70	100	•	
	MCM5L4400A-80		20/26		20			80	85	•	

DYNAMIC RAM SELECTOR GUIDE (cont.)

		Package Information						Address	Op		
Org	Motorola Part Number	300 mil DIP	300 mil SOJ	400 mil SOJ	100 mil ZIP	300 mil TSOP	400 mil TSOP	Access (ns Max)	Current (mA Max)	Low Power	Industrial Temp
1M X 4	MCM54400A-C70		20/26		20			70	100		•
(cont.)	MCM54400A-C80		20/26		20			80	85		•
512K X 8	MCM34800A-70			28				70	105		
	MCM34800A-80			28				80	90		
	MCM34L800A-70			28				70	105	•	
	MCM34L800A-80			28				80	90	•	
	MCM54800A-70			28			28	70	105		
	MCM54800A-80			28			28	80	90		
	MCM5L4800A-70			28			28	70	105	•	
	MCM5L4800A-80			28			28	80	90	•	
	MCM5V4800A-70			28			28	70	105		
	MCM5V4800A-80			28			28	80	90		
256K X 16	MCM34170A-60			40				60	140		
	MCM34170A-70			40				70	120		
	MCM34170A-80			40				80	105		
	MCM34260A-80			40				80	140		
	MCM34260A-10			40				100	120		
	MCM54170B-70			40				70	75		
	MCM54170B-80			40				80	65		
	MCM54170B-10			40				100	60		
	MCM54260B-70			40				70	100		
	MCM54260B-80			40				80	85		
	MCM54260B-10			40				100	75		
	MCM54270B-70			40				70	100		
	MCM54270B-80			40				80	85		
	MCM54270B-10			40				100	75		
256K X 18	MCM34190A-60			40				60	140		
	MCM34190A-70			40				70	120		
	MCM34190A-80			40				80	105		
	MCM34280A-80			40				80	140		

DYNAMIC RAM SELECTOR GUIDE (cont.)

Org	Motorola Part Number	Package Information 300 mil DIP	300 mil SOJ	400 mil SOJ	100 mil ZIP	300 mil TSOP	400 mil TSOP	Address Access (ns Max)	Op Current (mA Max)	Low Power	Industrial Temp
256K X 18	MCM34280A-10			40				100	120		
(cont.)	MCM54190B-70			40				70	75		
	MCM54190B-80			40				80	65		
	MCM54190B-10			40				100	60		
	MCM54280B-70			40				70	110		
	MCM54280B-80			40				80	95		
	MCM54280B-10			40				100	85		
	MCM54290B-70			40				70	110		
	MCM54290B-80			40				80	95		
	MCM54290B-10			40				100	85		
16M X 1	MCM516100-60			24/28			24/28	60	90		
	MCM516100-70			24/28			24/28	70	80		
	MCM516100-80			24/28			24/28	80	70		
4M X 4	MCM516400-60			24/28			24/28	60	90		
	MCM516400-70			24/28			24/28	70	80		
	MCM516400-80			24/28			24/28	80	70		
	MCM517400-60			24/28			24/28	60	90		
	MCM517400-70			24/28			24/28	70	80		
	MCM517400-80			24/28			24/28	80	70		

DYNAMIC RAM SELECTOR GUIDE (cont.)

			Package Information									Address	Op
Org	Byte Density	Motorola Part Number	Pins	AS	ASG	L	LH	S	SG	SH	SHG	Access (ns Max)	Current (mA Max)
256K X 8	256 KB	MCM84256-70	30	•								70	160
		MCM84256-80	30	•								80	140
1M X 8	1 MB	MCM81430-60	30			•		•				60	240
		MCM81430-70	30			•		•				70	220
		MCM81430-80	30			•		•				80	170
4M X 8	4 MB	MCM84000-60	30	•		•						60	960
		MCM84000-70	30	•		•						70	800
		MCM84000-80	30	•		•						80	680
		MCM84030-60	30				•					60	960
		MCM84030-70	30				•					70	800
		MCM84030-80	30				•					80	680
16M X 8	16 MB	MCM81600-60	30			•		•				60	960
		MCM81600-70	30			•		•				70	800
		MCM81600-80	30			•		•				80	680
256K X 9	256 KB	MCM94256-70	30	•								70	225
		MCM94256-80	30	•								80	195
1M X 9	1 MB	MCM91430-60	30			•		•				60	330
		MCM91430-70	30			•		•				70	280
		MCM91430-80	30			•		•				80	240
4M X 9	4 MB	MCM94000-60	30	•		•						60	1080
		MCM94000-70	30	•		•						70	900
		MCM94000-80	30	•		•						80	765
		MCM94030-60	30				•					60	1080
		MCM94030-70	30				•					70	900
		MCM94030-80	30				•					80	765
16M X 9	16 MB	MCM91600-60	30			•		•				60	680
		MCM91600-70	30			•		•				70	900
		MCM91600-80	30			•		•				80	765
1M X 18	2 MB	MCM18100-60	72	•	•							60	240
		MCM18100-70	72	•	•							70	220

DYNAMIC RAM SELECTOR GUIDE (cont.)

Org	Byte Density	Motorola Part Number	Package Information									Address Access (ns Max)	Op Current (mA Max)
			Pins	AS	ASG	L	LH	S	SG	SH	SHG		
2M X 18	4 MB	MCM18100-80	72	•	•							80	170
		MCM18200-60	72					•	•			60	240
		MCM18200-70	72					•	•			70	220
		MCM18200-80	72					•	•			80	170
4M X 18	8 MB	MCM18400-60	72	•	•							60	240
		MCM18400-70	72	•	•							70	220
		MCM18400-80	72	•	•							80	170
8M X 18	16 MB	MCM18800-60	72					•	•			60	240
		MCM18800-70	72					•	•			70	220
		MCM18800-80	72					•	•			80	170
256K X 32	1 MB	MCM32256-70	72	•	•							70	640
		MCM32256-80	72	•	•							80	560
512K X 32	2 MB	MCM32512-70	72	•	•							70	656
		MCM32512-80	72	•	•							80	576
1M X 32	4 MB	MCM32130-60	72							•	•	60	960
		MCM32130-70	72							•	•	70	800
		MCM32130-80	72							•	•	80	680
2M X 32	8 MB	MCM32230-60	72							•	•	60	976
		MCM32230-70	72							•	•	70	816
		MCM32230-80	72							•	•	80	696
4M X 32	14 MB	MCM32400-60	72					•	•			60	976
		MCM32400-70	72					•	•			70	816
		MCM32400-80	72					•	•			80	696
8M X 32	32 MB	MCM32800-60	72					•	•			60	976
		MCM32800-70	72					•	•			70	816
		MCM32800-80	72					•	•			80	696
256K X 36	1 MB	MCM36256-70	72					•	•			70	940
		MCM36256-80	72					•	•			80	820
		MCM36512-70	72					•	•			70	964
		MCM36512-80	72					•	•			80	844

DYNAMIC RAM SELECTOR GUIDE (cont.)

			Package Information									Address	Op
Org	Byte Density	Motorola Part Number	Pins	AS	ASG	L	LH	S	SG	SH	SHG	Access (ns Max)	Current (mA Max)
1M X 36	4 MB	MCM36100-60	72	•	•							60	1320
		MCM36100-70	72	•	•							70	1120
		MCM36100-80	72	•	•							80	960
2M X 36	8 MB	MCM36200-60	72	•	•							60	1344
		MCM36200-70	72	•	•							70	1144
		MCM36200-80	72	•	•							80	984
4M X 36	16 MB	MCM36400-60	72					•	•			60	1440
		MCM36400-70	72					•	•			70	1200
		MCM36400-80	72					•	•			80	1020
8M X 36	32 MB	MCM36800-60	72					•	•			60	1464
		MCM36800-70	72					•	•			70	1224
		MCM36800-80	72					•	•			80	1044
256K X 40	1 MB	MCM40256-70	72	•	•							70	800
		MCM40256-80	72	•	•							80	700
512K X 40	2 MB	MCM40512-70	72	•	•							70	820
		MCM40512-80	72	•	•							80	720
1M X 40	4 MB	MCM40100-60	72	•	•							60	1200
		MCM40100-70	72	•	•							70	1000
		MCM40100-80	72	•	•							80	850
2M X 40	8 MB	MCM40200-60	72	•	•							60	1220
		MCM40200-70	72	•	•							70	1020
		MCM40200-80	72	•	•							80	870
4M X 40	16 MB	MCM40400-60	72					•	•			60	1200
		MCM40400-70	72					•	•			70	1000
		MCM40400-80	72					•	•			80	850
8M X 40	32 MB	MCM40800-60	72					•	•			60	1220
		MCM40800-70	72					•	•			70	1020
		MCM40800-80	72					•	•			80	870
1M X 72	8 MB	MCM72100-60	100						•			60	2360
		MCM72100-70	100						•			70	2000

DYNAMIC RAM SELECTOR GUIDE (cont.)

Org	Byte Density	Motorola Part Number	Package Information									Address Access (ns Max)	Op Current (mA Max)
			Pins	AS	ASG	L	LH	S	SG	SH	SHG		
1M X 72	8 MB	MCM72100-80	100						•			80	1730
2M X 72	16 MB	MCM72200-60	100						•			60	2596
		MCM72200-70	100						•			70	2236
		MCM72200-80	100						•			80	1966
4M X 72	32 MB	MCM72400-60	100						•			60	2360
		MCM72400-70	100						•			70	2000
		MCM72400-80	100						•			80	1730
8M X 72	64 MB	MCM72800-60	100						•			60	2596
		MCM72800-70	100						•			70	2236
		MCM72800-80	100						•			80	1966

AS = SIMM (Board Revision)
ASG = Gold Pad SIMM (Board Revision)
L = SIP
LH = Low Height SIP
S = SIMM
SH = Short Height SIMM
SHG = Short Height Gold Pad SIMM
SG = Gold Pad SIMM

CROSS REFERENCE

DYNAMIC RAMs

DENSE-PAC	MOTOROLA
V56C100	MCM511000A
DPD1MX8	MCM81000
DPD1MX9	MCM91000
VM55C104K36	MCM36256
VM55C1042K3	MCM36152

FUJITSU	MOTOROLA
MB81C1000	MCM511000A
MB81C1001	MCM511001A
MB81C1003	MCM511002A
MB81C4256	MCM514256A
MB81C4258	MCM514258A
MB814100	MCM54100A
MB814400	MCM54400A
MB85230	MCM81000
MB85235	MCM91000

GOLDSTAR	MOTOROLA
GM71C1000	MCM511000A
GM71C4256	MCM514256A
GM71C4100A	MCM54100A
GM71C4400A	MCM54400A

HITACHI	MOTOROLA
HM511000	MCM511000A
HM511001	MCM511001A
HM511002	MCM511002A
HM514100	MCM54100A
HM514101	MCM54101A
HM514256	MCM514256A
HM514258	MCM514258A
HM514400	MCM54400A
HB56D136B	MCM36100
HB56D25636	MCM36256
HB56D51236	MCM36512

INTEL	MOTOROLA
P21010	MCM511000A
P21014	MCM514256A
P21040	MCM54100A
SM21019	MCM91000

MICRON	MOTOROLA
MT4C1004	MCM54100A
MT4C1005	MCM54101A
MT4C1006	MCM54102A
MT4C1024	MCM511000A
MT4C1025	MCM511001A
MT4C1026	MCM511002A
MT4C4001	MCM54400A
MT4C4003	MCM54402A
MT4C4256	MCM514256A
MT4C4258	MCM514258A
MT8C36256	MCM36256
MT8C36512	MCM36512
MT8C8024	MCM81000
MT8C9024	MCM91000

MITSUBISHI	MOTOROLA
M5M44100	MCM54100A
M5M44101	MCM54101A
M5M44102	MCM54102A
M5M44400	MCM54400A
M5M44402	MCM54402A
M5M44C256	MCM514256A
M5M4C1001	MCM511001A
M5M4C1002	MCM511002A
MH1M08A	MCM81000
MH1M09A	MCM91000

NEC	MOTOROLA
μPD421000	MCM511000A
μPD421001	MCM511001A
μPD421002	MCM511002A
μPD424256	MCM514256A
μPD424258	MCM514258A
MC-421000A36	MCM36100
MC-421000A40	MCM40100
MC-421000A8	MCM81000
MC-421000A9	MCM91000
MC-422000A36	MCM36200
MC-422000A40	MCM40200
MC-424100A8	MCM84000
MC-424100A9	MCM94000
MC-424256A36	MCM36256
MC-424512A36	MCM36512
MC-424512A40	MCM40512
μPD424100	MCM54100A

NEC (cont.)	MOTOROLA (cont.)
μPD42101	MCM54101A
μPD42102	MCM54102A
μPD42400	MCM54400A
μPD42402	MCM54402A

NMB	MOTOROLA
AAA1M104	MCM514256A
AAA4M100	MCM54100A

PANASONIC	MOTOROLA
MN41C1000	MCM511000A
MN41C4000	MCM54100A
MN41C4001	MCM54101A
MN41C4002	MCM54102A
MN41C41000	MCM54400A
MN41C41002	MCM54402A
MN41C4256	MCM514256A

SAMSUNG	MOTOROLA
KM41C1000	MCM511000A
KM41C1001	MCM511001A
KM41C1002	MCM511002A
KM44C4000	MCM54400A
KM41C4001	MCM54101A
KM41C4002	MCM54102A
KM44C1000	MCM54400A
KM44C256	MCM514256A
KM44C258	MCM514258A
KMM36256	MCM36512
KMM36512	MCM36512
KMM581000	MCM81000
KMM591000	MCM91000

SIEMENS	MOTOROLA
HYB514100	MCM54100A
HYB514256	MCM514256A
HYB514400	MCM54400A
HYM910005	MCM91000A

TEXAS INSTRUMENTS	MOTOROLA
TMS44C256	MCM514256A
TMS4C1024	MCM511000A
TMS4C1025	MCM511001A
TMS4C1027	MCM511002A
TMS44100	MCM54100A
TMS44101	MCM54101A
TMS44400	MCM54400A
TM024EAD9	MCM91000
TM024GAD8	MCM81000
TM124BBK32	MCM32100
TM124MBK35	MCM36100
TM256BBK32	MCM32256
TM256KBK36	MCM36256
TM4100EBD9	MCM94000
TM4100GBD8	MCM84000
TM512CBK32	MCM32512
TM512LBK36	MCM36512

TOSHIBA	MOTOROLA
TC511000	MCM511000A
TC511001	MCM511001A
TC511002	MCM511002A
TC514100	MCM54100A
TC514101	MCM54101A
TC514102	MCM54102A
TC514256	MCM514256A
TC514258	MCM514258A
TC514400	MCM54400A
TC514402	MCM54402A
THM3625600A	MCM36256
THM365120A	MCM36512
THM81000A	MCM81000
THM91000A	MCM91000

CMOS 1M Dynamic RAMs

MCM411000 2-3
MCM414256 2-16
MCM511000A 2-29
MCM511000B 2-44
MCM511001A 2-59
MCM511002A 2-74
MCM514256A 2-89
MCM514256B 2-104
MCM514258A 2-119

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM411000
MCM41L1000

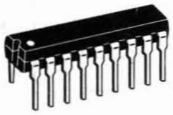
1M x 1 CMOS Dynamic RAM

Page Mode

The MCM411000 is a 1.0µ CMOS high-speed dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM411000 requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil dual-in-line plastic package (DIP) and a 300 mil SOJ plastic package.

- Three-State Data Output
- Common I/O with Early Write
- Fast Page Mode
- TTL-Compatible Inputs and Output
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM411000 = 8 ms
  MCM41L1000 = 64 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC})
  MCM411000-70 and MCM41L1000-70 = 70 ns (Max)
  MCM411000-80 and MCM41L1000-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM411000-70 and MCM41L1000-70 = 440 mW (Max)
  MCM411000-80 and MCM41L1000-80 = 385 mA (Max)
- Low Standby Power Dissipation:
  MCM411000 and MCM41L1000 = 11 mW (Max, TTL Levels)
  MCM411000 = 5.5 mW (Max, CMOS Levels)
  MCM41L1000 = 1.65 mW (Max, CMOS Levels)



P PACKAGE
300 MIL PLASTIC
CASE 707B-01

J PACKAGE
300 MIL SOJ
CASE 822B-01

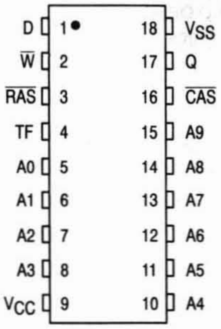
Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836A-01

PIN NAMES

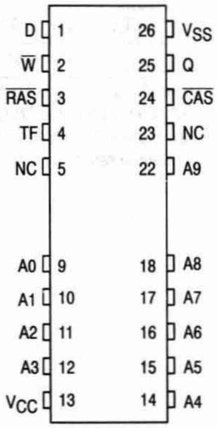
A0 – A9	Address Inputs
D	Data Input
Q	Data Output
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENTS

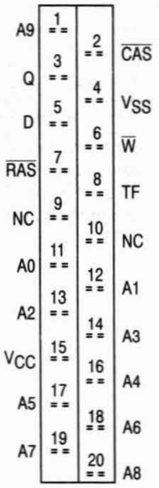
DUAL-IN-LINE


D 1 18 VSS
W 2 17 Q
RAS 3 16 CAS
TF 4 15 A9
A0 5 14 A8
A1 6 13 A7
A2 7 12 A6
A3 8 11 A5
VCC 9 10 A4

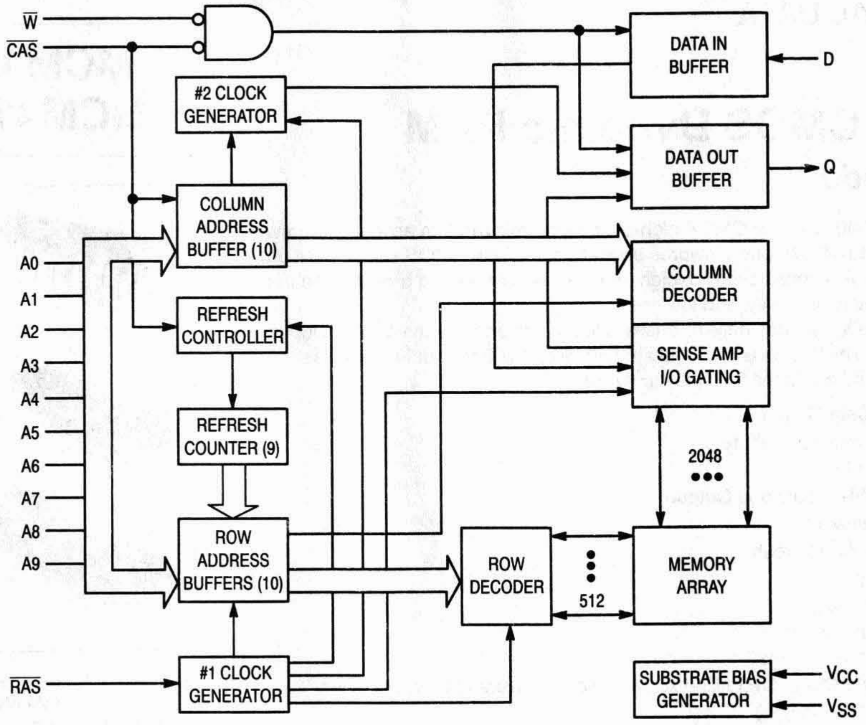
SMALL OUTLINE


D 1 26 VSS
W 2 25 Q
RAS 3 24 CAS
TF 4 23 NC
NC 5 22 A9
A0 9 18 A8
A1 10 17 A7
A2 11 16 A6
A3 12 15 A5
VCC 13 14 A4

ZIG-ZAG IN-LINE


A9 1
2 CAS
Q 3
4 VSS
D 5
6 W
RAS 7
8 TF
NC 9
10 NC
A0 11
12 A1
A2 13
14 A3
VCC 15
16 A4
A5 17
18 A6
A7 19
20 A8

BLOCK DIAGRAM



W
CAS
#2 CLOCK GENERATOR
COLUMN ADDRESS BUFFER (10)
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
REFRESH CONTROLLER
REFRESH COUNTER (9)
ROW ADDRESS BUFFERS (10)
RAS
#1 CLOCK GENERATOR
DATA IN BUFFER
D
DATA OUT BUFFER
Q
COLUMN DECODER
SENSE AMP I/O GATING
2048
ROW DECODER
512
MEMORY ARRAY
SUBSTRATE BIAS GENERATOR
VCC
VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Test Function Input Voltage	$V_{in(TF)}$	– 1 to V_{CC} + 0.5 V	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V
Test Function Input Voltage	$V_{IH(TF)}$	– 1.0	—	V_{CC} + 0.5	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM411000-70 and MCM41L1000-70, t_{RC} = 140 ns	I_{CC1}	—	80	mA	1, 2
MCM411000-80 and MCM41L1000-80, t_{RC} = 160 ns		—	70		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycle	I_{CC3}			mA	1, 2
MCM411000-70 and MCM41L1000-70, t_{RC} = 140 ns		—	80		
MCM411000-80 and MCM41L1000-80, t_{RC} = 160 ns		—	60		
V_{CC} Power Supply Current During Fast Page Mode Cycle	I_{CC4}			mA	1, 3, 4
MCM411000-70 and MCM41L1000-70, t_{PC} = 50 ns		—	70		
MCM411000-80 and MCM41L1000-80, t_{PC} = 55 ns		—	50		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM411000	I_{CC5}	—	1.0	mA	
MCM41L1000		—	300	µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	1
MCM411000-70 and MCM41L1000-70, t_{RC} = 140 ns		—	70		
MCM411000-80 and MCM41L1000-80, t_{RC} = 160 ns		—	60		
V_{CC} Power Supply Current, Battery Back-Up Mode — MCM41L1000 only (t_{RC} = 125 µs; t_{RAS} = 1 µs, $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0 – A9, $\overline{W}$, D = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	—	300	µA	3
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable)	I_{CC8}	—	5	mA	1
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Measured with one address transition per page mode cycle.
4. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	D, A0 – A9	C_{in}	5	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, TF		7	
Output Capacitance	Q	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM411000-70 MCM41L1000-70		MCM411000-80 MCM41L1000-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	140	—	160	—	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	165	—	190	—	ns	7
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	—	55	—	ns	
Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	75	—	85	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	70	—	80	ns	7, 8
Access Time from $\overline{CAS}$ (Typ. = 16 ns @ 70°C)	t_{CELQV}	t_{CAC}	—	20	—	25	ns	7, 9
Access Time from Column Address	t_{AVQA}	t_{AA}	—	35	—	40	ns	7, 10
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	45	—	50	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	12
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	25	10,000	ns	13
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	22	55	ns	14
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	17	40	ns	15
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	12	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	20	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	40	—	42	—	ns	16

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. TF pin must be either at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
7. Measured with a current load equivalent to 2 TTL (–200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \le t_{RCD}$ (max).
9. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
10. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Transition times are measured between V_{IH} and V_{IL}.
13. t_{RASP} is determined by the $\overline{RAS}$ pulse width in the fast page mode cycle.
14. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled by t_{AA}.
16. t_{AR}, t_{WCR} and t_{DHR} referenced to t_{RAD} (min)

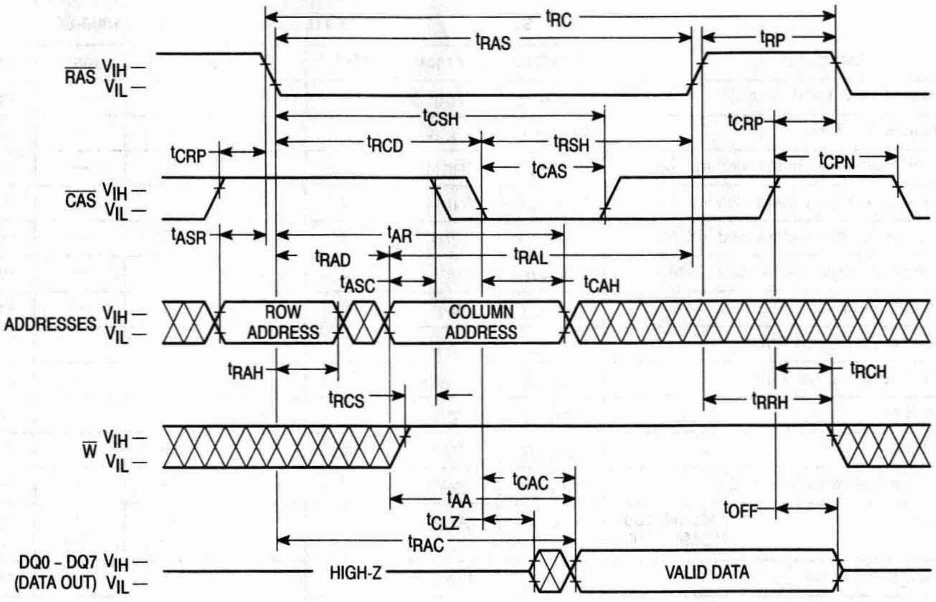
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM411000-70 MCM41L1000-70		MCM411000-80 MCM41L1000-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	17
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	10	—	10	—	ns	17
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	15	—	20	—	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELWH}	t_{WCR}	40	—	42	—	ns	16
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	18, 19
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	20	—	ns	18, 19
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	40	—	42	—	ns	16
Refresh Period MCM411000 MCM41L1000	t_{RVRV}	t_{RFSH}	— —	8 64	— —	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	19, 20
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	20	—	25	—	ns	20
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	70	—	80	—	ns	20
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	35	—	40	—	ns	20
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	10	—	10	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t_{REHCEH}	t_{RHCP}	45	—	50	—	ns	

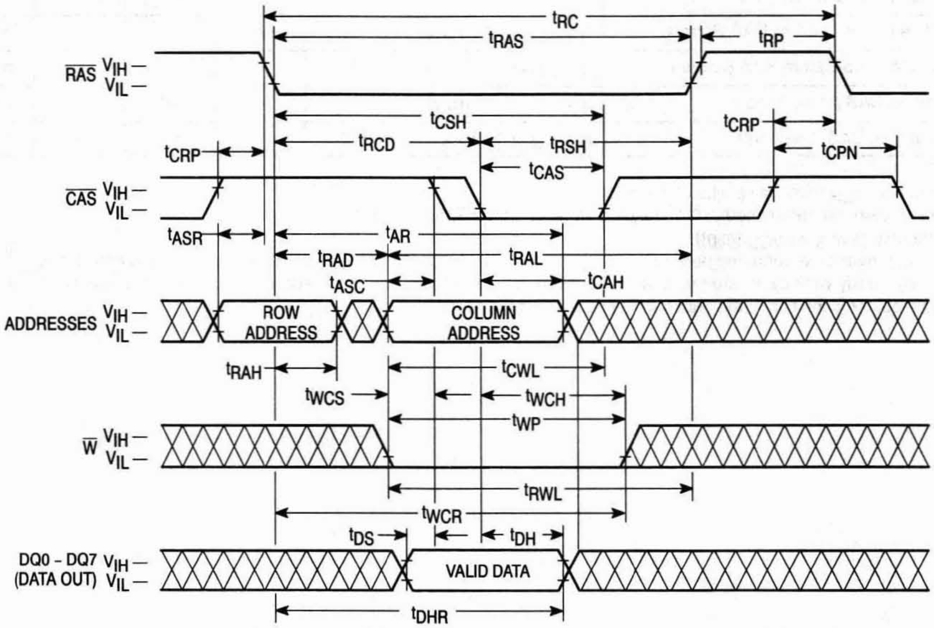
NOTES:

17. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
18. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles.
19. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
20. t_{WCS} is not a restrictive operating parameter; it is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

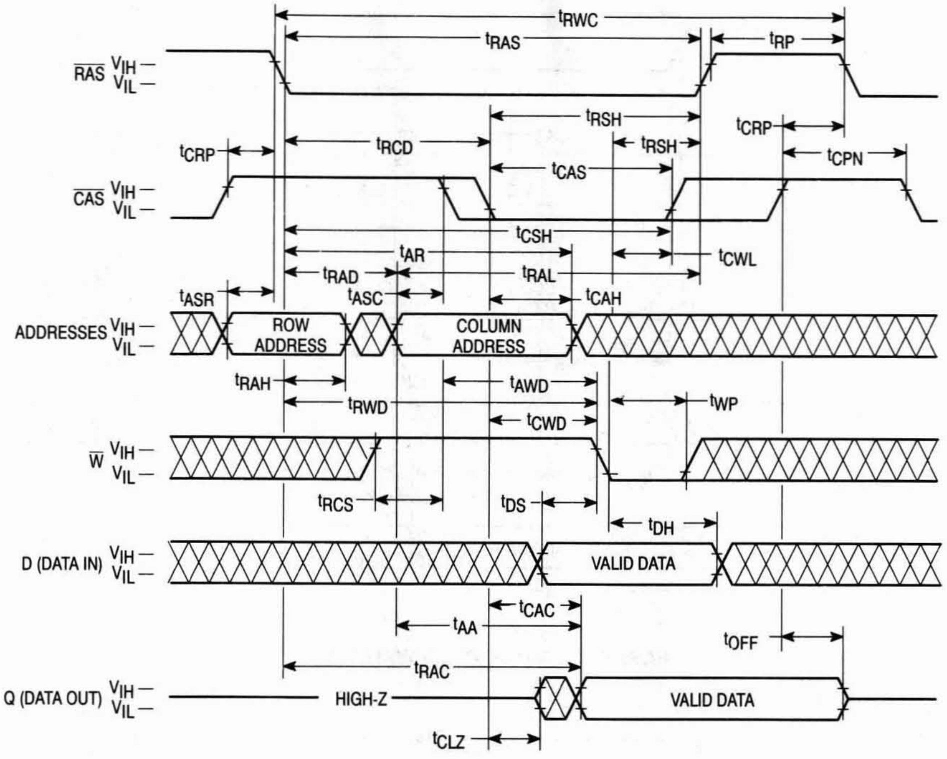
READ CYCLE


tRC
tRAS
tRP
RAS VIH — VIL —
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
tCPN
CAS VIH — VIL —
tASR
tAR
tRAD
tRAL
tASC
tCAH
ADDRESSES VIH — VIL —
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W VIH — VIL —
tCAC
tAA
tOFF
tCLZ
tRAC
DQ0 - DQ7 VIH — (DATA OUT) VIL —
HIGH-Z
VALID DATA

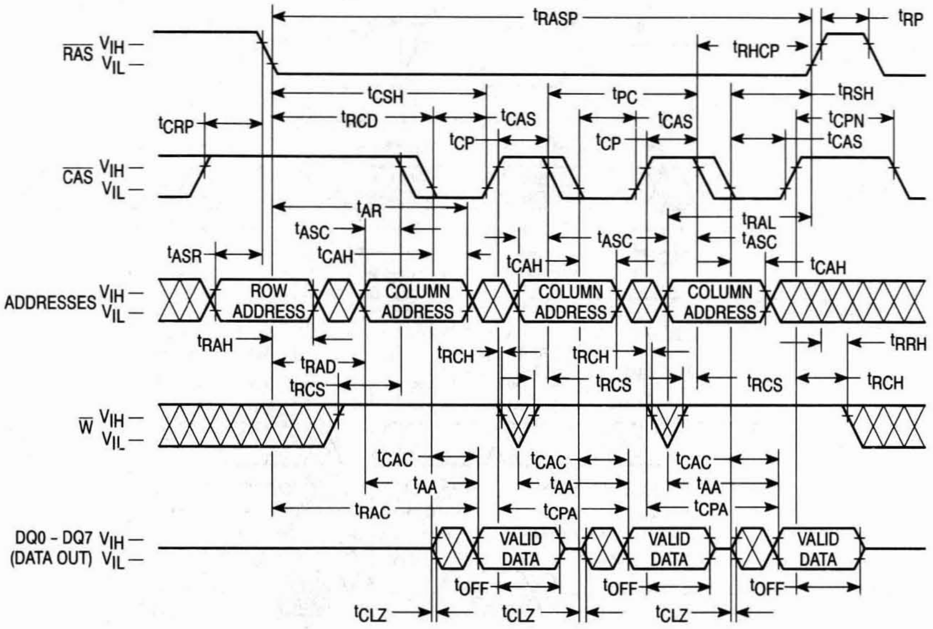
EARLY WRITE CYCLE


tRC
tRAS
tRP
RAS VIH — VIL —
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
tCPN
CAS VIH — VIL —
tASR
tAR
tRAD
tRAL
tASC
tCAH
ADDRESSES VIH — VIL —
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWP
W VIH — VIL —
tRWL
tWCR
tDS
tDH
DQ0 - DQ7 VIH — (DATA OUT) VIL —
VALID DATA
tDHR

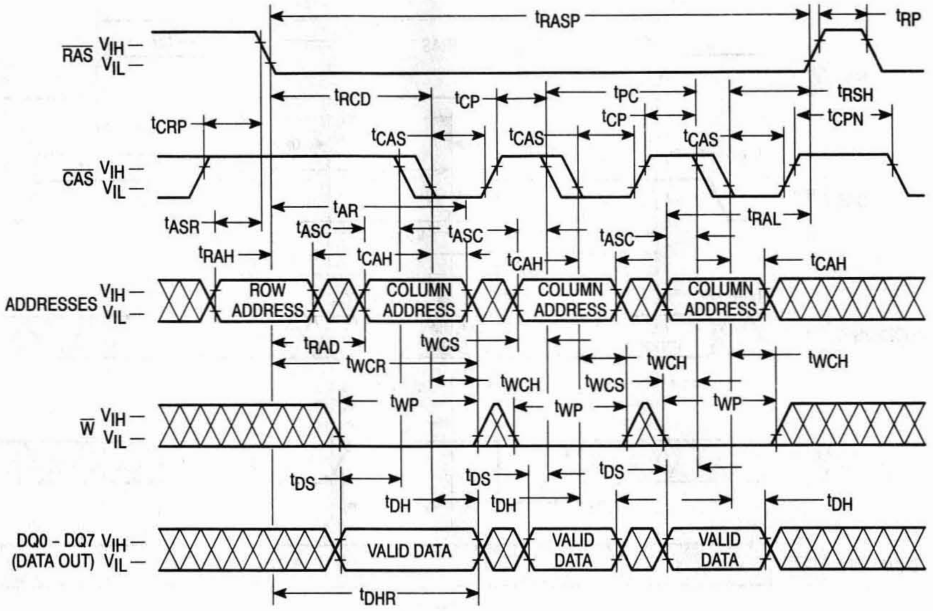
READ-WRITE CYCLE


tRWC
tRAS
tRP
RAS VIH VIL
tRSH
tCRP
tRCD
tRSH
tCRP
tCPN
tCAS
CAS VIH VIL
tCSH
tAR
tCWL
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tAWD
tRWD
tWP
tCWD
W VIH VIL
tRCS
tDS
tDH
D (DATA IN) VIH VIL
VALID DATA
tCAC
tAA
tOFF
tRAC
Q (DATA OUT) VIH VIL
HIGH-Z
VALID DATA
tCLZ

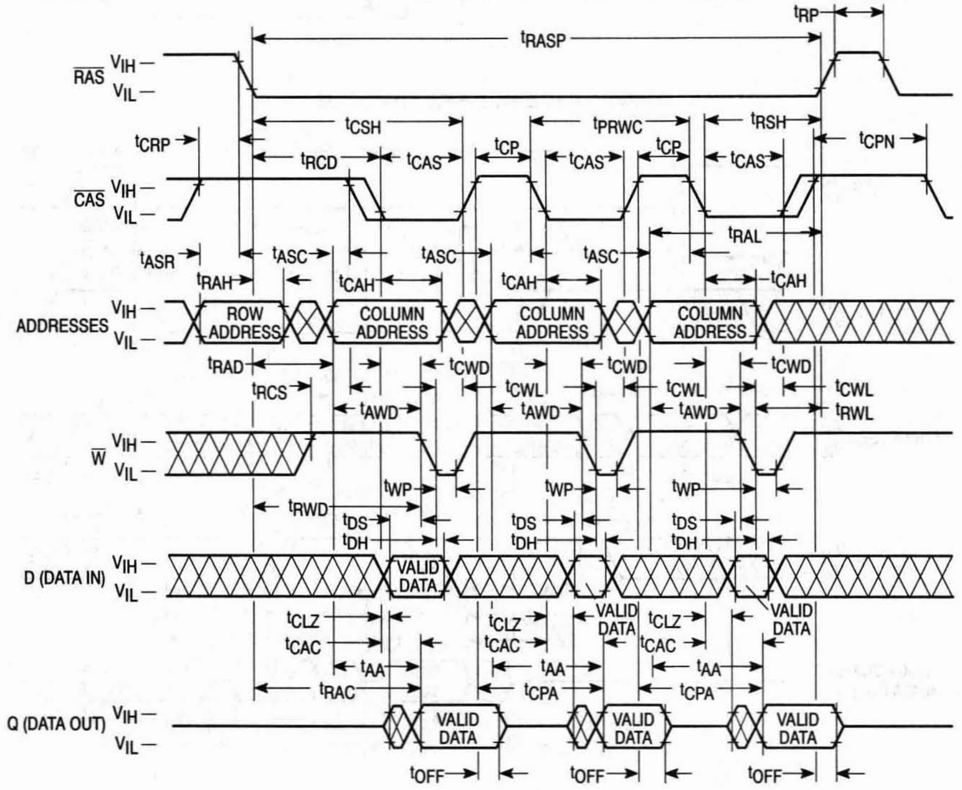
FAST PAGE MODE READ CYCLE


tRASP
tRP
RAS VIH VIL
tRHCP
tCSH
tPC
tRSH
tCRP
tRCD
tCAS
tCAS
tCPN
tCP
tCP
tCAS
CAS VIH VIL
tAR
tRAL
tASC
tASC
tASC
tASR
tCAH
tCAH
tCAH
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAH
tRRH
tRCH
tRCH
tRAD
tRCS
tRCS
tRCS
tRCH
W VIH VIL
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
DQ0 - DQ7 VIH (DATA OUT) VIL
VALID DATA
VALID DATA
VALID DATA
tOFF
tOFF
tOFF
tCLZ
tCLZ
tCLZ

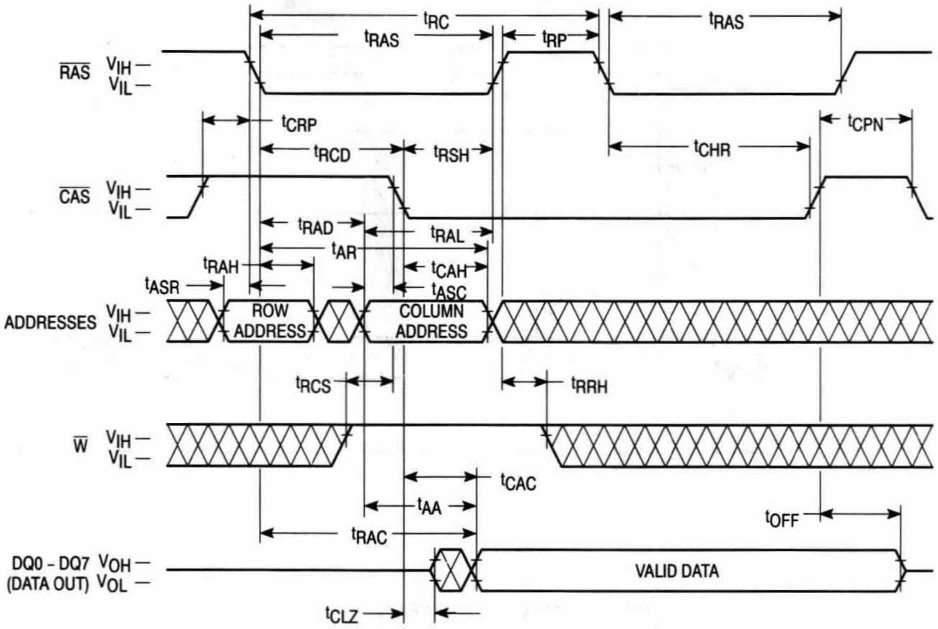
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)


RAS
VIH —
VIL —
CAS
VIH —
VIL —
ADDRESSES
VIH —
VIL —
W
VIH —
VIL —
DQ0 - DQ7
(DATA OUT)
VIH —
VIL —
tRASP
tRP
tRCD
tCP
tPC
tRSH
tCRP
tCP
tCPN
tCAS
tCAS
tCAS
tAR
tRAL
tASR
tASC
tASC
tASC
tRAH
tCAH
tCAH
tCAH
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tWCS
tWCR
tWCH
tWCH
tWCS
tWCH
tWP
tWP
tWP
tDS
tDS
tDS
tDH
tDH
tDH
VALID DATA
VALID DATA
VALID DATA
tDHR

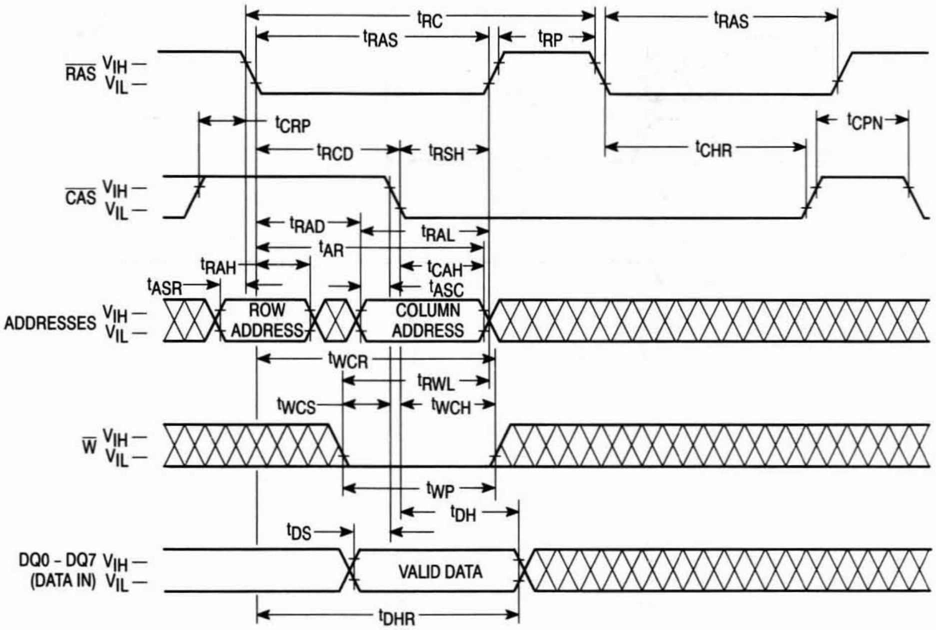
FAST PAGE MODE READ-WRITE CYCLE


RAS
VIH —
VIL —
CAS
VIH —
VIL —
ADDRESSES
VIH —
VIL —
W
VIH —
VIL —
D (DATA IN)
VIH —
VIL —
Q (DATA OUT)
VIH —
VIL —
tRP
tRASP
tCSH
tPRWC
tRSH
tCRP
tCP
tCP
tCPN
tRCD
tCAS
tCAS
tCAS
tRAL
tASR
tASC
tASC
tASC
tRAH
tCAH
tCAH
tCAH
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tCWD
tCWD
tCWD
tRCS
tCWL
tCWL
tCWL
tAWD
tAWD
tAWD
tRWL
tWP
tWP
tWP
tRWD
tDS
tDS
tDS
tDH
tDH
tDH
VALID DATA
VALID DATA
VALID DATA
tCLZ
tCLZ
tCLZ
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
VALID DATA
VALID DATA
VALID DATA
tOFF
tOFF
tOFF

HIDDEN REFRESH CYCLE (READ)

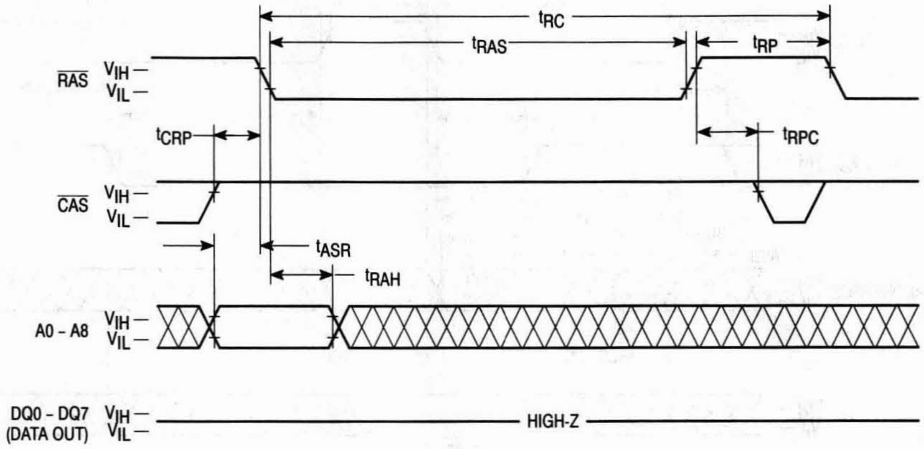

tRC
tRAS
tRP
tRAS
RAS VIH — VIL —
tCRP
tCPN
tRCD
tRSH
tCHR
CAS VIH — VIL —
tRAD
tRAL
tAR
tRAH
tCAH
tASR
tASC
ADDRESSES VIH — VIL —
ROW ADDRESS
COLUMN ADDRESS
tRCS
tRRH
W VIH — VIL —
tCAC
tAA
tOFF
tRAC
DQ0 - DQ7 VOH —
(DATA OUT) VOL —
VALID DATA
tCLZ

HIDDEN REFRESH CYCLE (EARLY WRITE)


tRC
tRAS
tRP
tRAS
RAS VIH — VIL —
tCRP
tCPN
tRCD
tRSH
tCHR
CAS VIH — VIL —
tRAD
tRAL
tAR
tRAH
tCAH
tASR
tASC
ADDRESSES VIH — VIL —
ROW ADDRESS
COLUMN ADDRESS
tWCR
tRWL
tWCS
tWCH
W VIH — VIL —
tWP
tDH
tDS
DQ0 - DQ7 VIH —
(DATA IN) VIL —
VALID DATA
tDHR

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

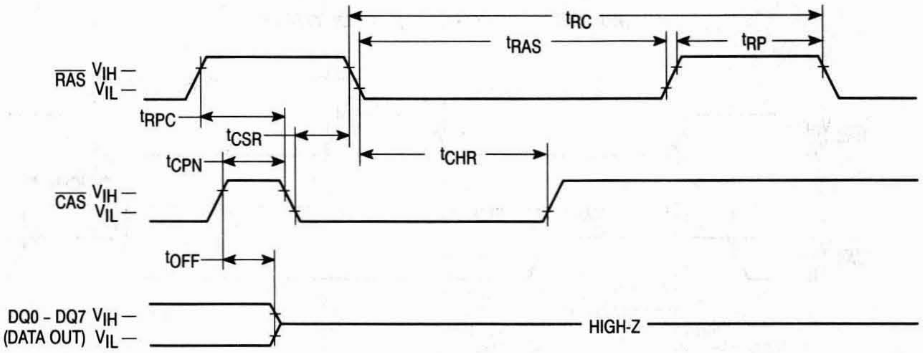
($\overline{\text{W}}$ and A8 are Don't Care)



tRC
tRAS
tRP
RAS VIH — VIL —
tCRP
tRPC
CAS VIH — VIL —
tASR
tRAH
A0 - A8 VIH — VIL —
DQ0 - DQ7 (DATA OUT) VIH — VIL —
HIGH-Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{W}}$ and A0 – A8 are Don't Care)



tRC
tRAS
tRP
RAS VIH — VIL —
tRPC
tCSR
tCPN
tCHR
CAS VIH — VIL —
tOFF
DQ0 - DQ7 (DATA OUT) VIH — VIL —
HIGH-Z

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are two other variations in addressing the 1M RAM: **$\overline{\text{RAS}}$-only refresh cycle** and **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle**. Both are discussed in separate sections that follows.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read modes.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. However, $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ clock active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for a minimum of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but Q may be indeterminate — see note 20 of AC Operating Conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the 1M dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum of t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). A read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). The operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}.

Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM411000 require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM411000. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM411000 and 64 milliseconds on the MCM41L1000.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh**, **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh**, and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

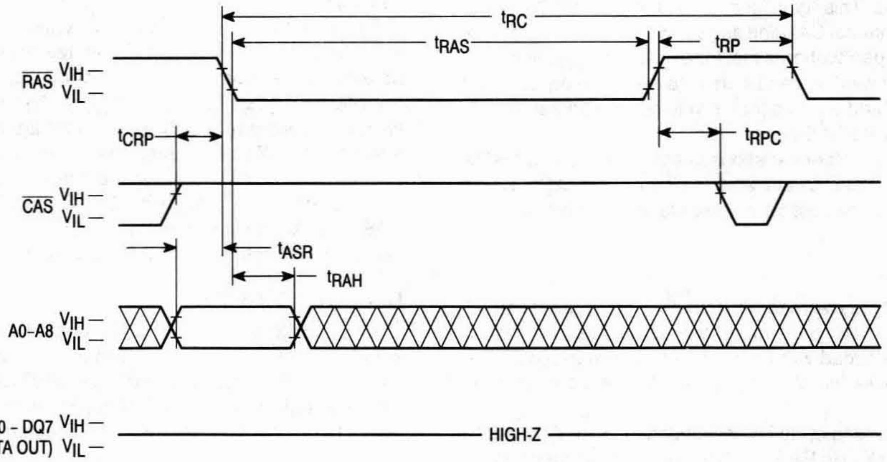
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

($\overline{\text{W}}$ and A8 are Don't Care)



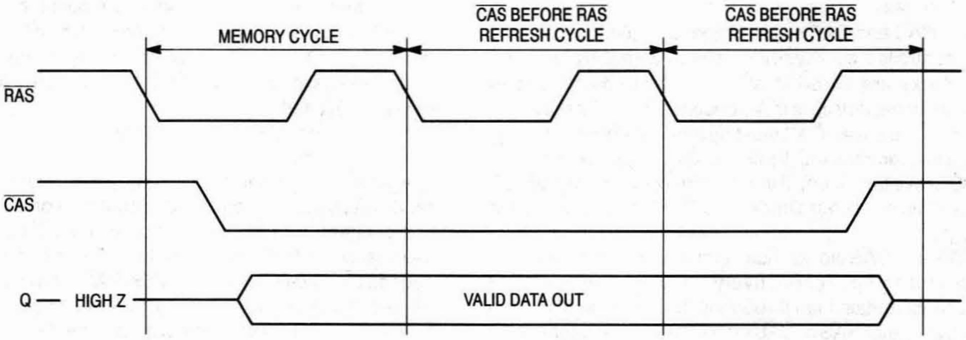


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM **411000 or 41L1000** **X** **XX** **XX**

Motorola Memory Prefix — MCM

Part Number — 411000 or 41L1000

Package (P = 300 mil Plastic DIP, J = 300 mil SOJ, Z = Plastic ZIP) — X

Speed (70 = 70 ns, 80 = 80 ns) — XX

Shipping Method (R2 = Tape and Reel, Blank = Rails) — XX

Full Part Numbers —

MCM411000P70
MCM411000P80
MCM41L1000P70
MCM41L1000P80

MCM411000J70
MCM411000J80
MCM41L1000J70
MCM41L1000J80

MCM411000J70R2
MCM411000J80R2
MCM41L1000J70R2
MCM41L1000J80R2

MCM411000Z70
MCM411000Z80
MCM41L1000Z70
MCM41L1000Z80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

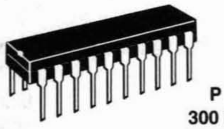
MCM414256
MCM41L4256

256K x 4 CMOS Dynamic RAM
Page Mode

The MCM414256 is a 1.0µ CMOS high-speed, dynamic random access memory. It is organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM414256 requires only nine address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil dual-in-line package (DIP) and a 300 mil SOJ plastic package.

- Three-State Data Output
- Fast Page Mode
- TTL-Compatible Inputs and Output
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM414256 = 8 ms
  MCM41L4256 = 64 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC})
  MCM414256-70 and MCM41L4256-70 = 69 ns (Max)
  MCM414256-80 and MCM41L4256-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM414256-70 and MCM41L4256-70 = 440 mW (Max)
  MCM414256-80 and MCM41L4256-80 = 385 mA (Max)
- Low Standby Power Dissipation:
  MCM414256 and MCM41L4256 = 11 mW (Max), TTL Levels
  MCM414256 = 5.5 mW (Max), CMOS Levels
  MCM41L4256 = 1.65 mW (Max), CMOS Levels



P PACKAGE
300 MIL PLASTIC
CASE 738C-01

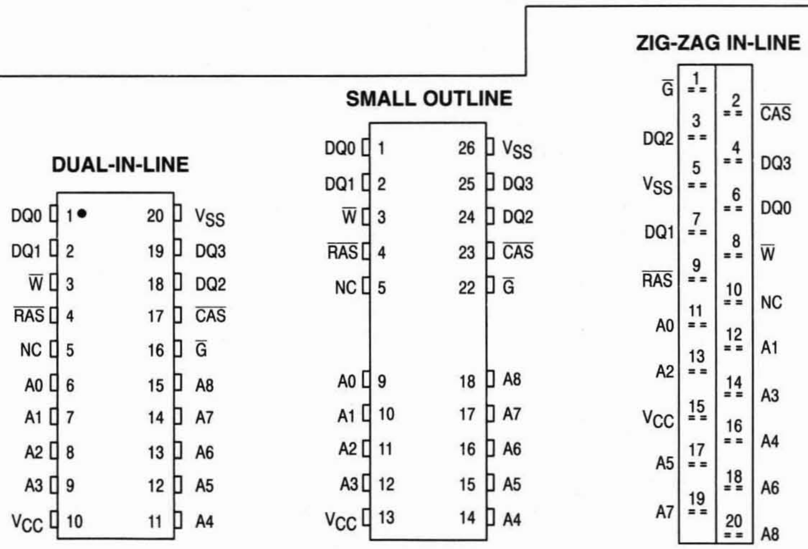
J PACKAGE
300 MIL SOJ
CASE 822B-01

Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836A-01

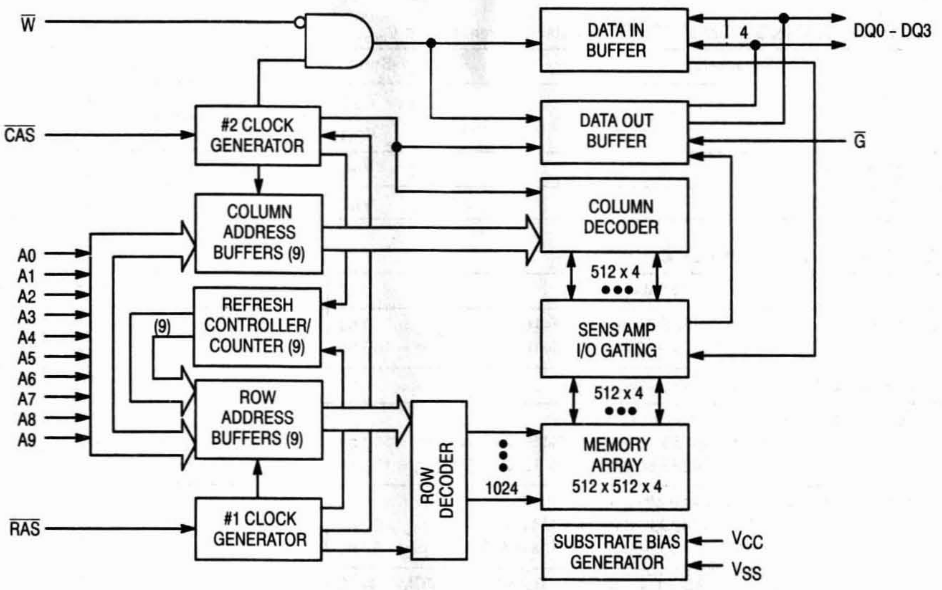
PIN NAMES

A0 – A8	Address Inputs
DQ0 – DQ3	Data Input/Output
$\overline{\text{G}}$	Output Enable
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENTS


DUAL-IN-LINE
DQ0 1 20 VSS
DQ1 2 19 DQ3
W 3 18 DQ2
RAS 4 17 CAS
NC 5 16 G
A0 6 15 A8
A1 7 14 A7
A2 8 13 A6
A3 9 12 A5
VCC 10 11 A4
SMALL OUTLINE
DQ0 1 26 VSS
DQ1 2 25 DQ3
W 3 24 DQ2
RAS 4 23 CAS
NC 5 22 G
A0 9 18 A8
A1 10 17 A7
A2 11 16 A6
A3 12 15 A5
VCC 13 14 A4
ZIG-ZAG IN-LINE
G 1
2 CAS
DQ2 3
4 DQ3
VSS 5
6 DQ0
DQ1 7
8 W
RAS 9
10 NC
A0 11
12 A1
A2 13
14 A3
VCC 15
16 A4
A5 17
18 A6
A7 19
20 A8

BLOCK DIAGRAM



W̄
CAS̄
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
RAS̄
#2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (9)
REFRESH CONTROLLER/ COUNTER (9)
(9)
ROW ADDRESS BUFFERS (9)
#1 CLOCK GENERATOR
ROW DECODER
1024
DATA IN BUFFER
DATA OUT BUFFER
COLUMN DECODER
512 x 4
SENS AMP I/O GATING
512 x 4
MEMORY ARRAY 512 x 512 x 4
SUBSTRATE BIAS GENERATOR
4
DQ0 - DQ3
Ḡ
VCC
VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM414256-70 and MCM41L4256-70, t_{RC} = 140 ns MCM414256-80 and MCM41L4256-80, t_{RC} = 160 ns	I_{CC1}	— —	80 70	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{\text{RAS}}$ only Refresh Cycle MCM414256-70 and MCM41L4256-70, t_{RC} = 140 ns MCM414256-80 and MCM41L4256-80, t_{RC} = 160 ns	I_{CC3}	 — —	 80 70	mA	1,2
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM414256-70 and MCM41L4256-70, t_{PC} = 50 ns MCM414256-80 and MCM41L4256-80, t_{PC} = 55 ns	I_{CC4}	 — —	 80 60	mA	1, 3
V_{CC} Power Supply Current (Standby) ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = V_{CC} – 0.2 V) MCM414256 MCM41L4256	I_{CC5}	— —	1.0 300	mA μA	
V_{CC} Power Supply Current During $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle MCM414256-70 and MCM41L4256-70, t_{RC} = 140 ns MCM414256-80 and MCM41L4256-80, t_{RC} = 160 ns	I_{CC6}	 — —	 80 70	mA	1
V_{CC} Power Supply Current, Battery Back-Up Mode — MCM41L4256 Only (t_{RC} = 125 μs, t_{RAS} = 1 μs, $\overline{\text{CAS}}$ = $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle or 0.2 V; A0 – A9, $\overline{\text{W}}$, D = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	—	300	μA	2
V_{CC} Power Supply Current (Standby) $\overline{\text{RAS}}$ = V_{IH}, $\overline{\text{CAS}}$ = V_{IL}	I_{CC8}	—	5	mA	1
Input Leakage Current (0 V ≤ V_{in} ≤ 7.0 V)	$I_{lkg(I)}$	– 10	10	μA	
Output Leakage Current ($\overline{\text{CAS}}$ = V_{IH}, 0 V ≤ V_{out} ≤ 7.0 V)	$I_{lkg(O)}$	– 10	10	μA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Address can be changed less than three times while $\overline{\text{RAS}}$ = V_{IL}.
3. Measured with one address transition per page mode cycle.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A8	C_{in}	5	pF
	$\overline{\text{W}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$		7	
Output Capacitance($\overline{\text{CAS}}$ = V_{IH} to Disable Output)	DQ0 – DQ3	C_{out}	10	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM414256-70 MCM41L4256-70		MCM414256-80 MCM41L4256-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	140	—	160	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RMW}	190	—	220	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	—	55	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRMW}	100	—	110	—	ns	
Access Time from RAS	t_{RELQV}	t_{RAC}	—	70	—	80	ns	6, 7
Access Time from CAS	t_{CELQV}	t_{CAC}	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	6, 9
Access Time from Precharge CAS	t_{CEHQV}	t_{CPA}	—	45	—	50	ns	6
CAS to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
RAS Precharge Time	t_{REHREL}	t_{RP}	60	—	70	—	ns	
RAS Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	ns	
RAS Hold Time	t_{CELREH}	t_{RSH}	20	—	25	—	ns	
CAS Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
CAS Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	25	10,000	ns	
RAS to CAS Delay Time	t_{RELCEL}	t_{RCD}	20	50	22	55	ns	11
RAS to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	17	40	ns	12
CAS to RAS Precharge Time	t_{CEHREL}	t_{CRP}	10	—	10	—	ns	
CAS Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	ns	
CAS Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	12	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	20	—	ns	
Column Address Hold Time Referenced to RAS	t_{RELAX}	t_{AR}	40	—	42	—	ns	
Column Address to RAS Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	

NOTES: (continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100 µs is required after power-up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max), $t_{RAD} \le t_{RAD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max), $t_{RAD} \le t_{RAD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max), $t_{RCD} \le t_{RCD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled by t_{AA}.

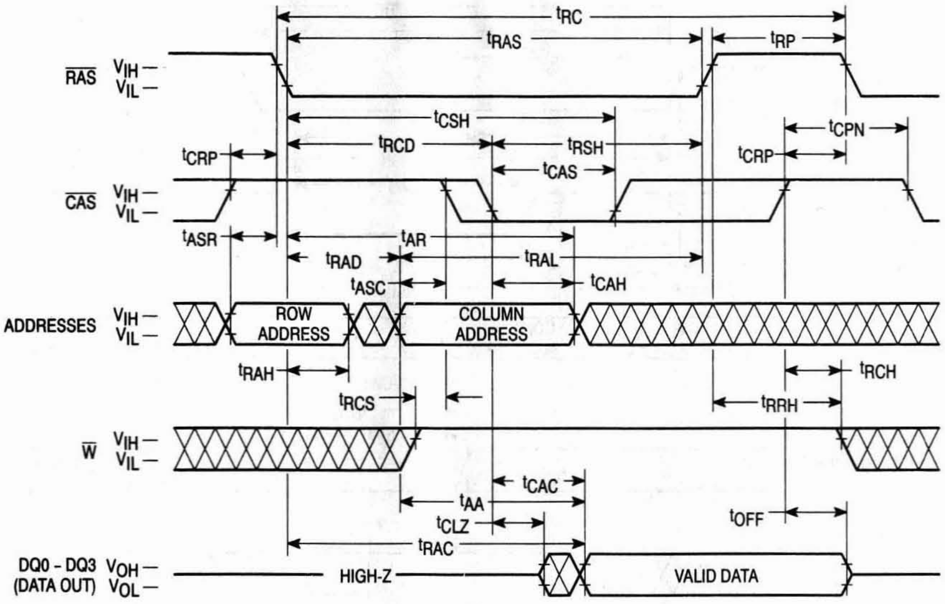
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM414256-70 MCM41L4256-70		MCM414256-80 MCM41L4256-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t_{CEHREH}	t_{RHCP}	50	—	50	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	10	—	10	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	15	—	20	—	ns	
Write Command Hold Time Reference to $\overline{\text{RAS}}$	t_{RELWH}	t_{WCR}	40	—	42	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	20	—	ns	14
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	40	—	42	—	ns	
Refresh Period MCM414256 MCM41L4256	t_{RVRV}	t_{RFSH}	— —	8 64	— —	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	16
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	45	—	55	—	ns	15
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	95	—	110	—	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	60	—	70	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	10	—	10	—	ns	
$\overline{\text{G}}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	25	ns	
$\overline{\text{G}}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{\text{G}}$	t_{GHQZ}	t_{GZ}	—	20	—	20	ns	
$\overline{\text{G}}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	25	—	ns	

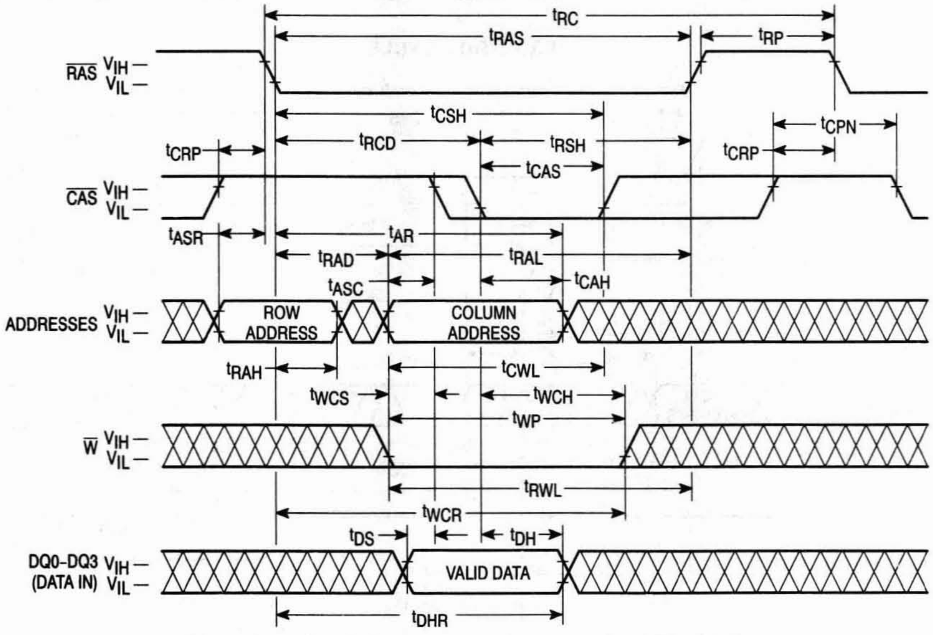
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are reference to $\overline{\text{CAS}}$ leading edge in random write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as an electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

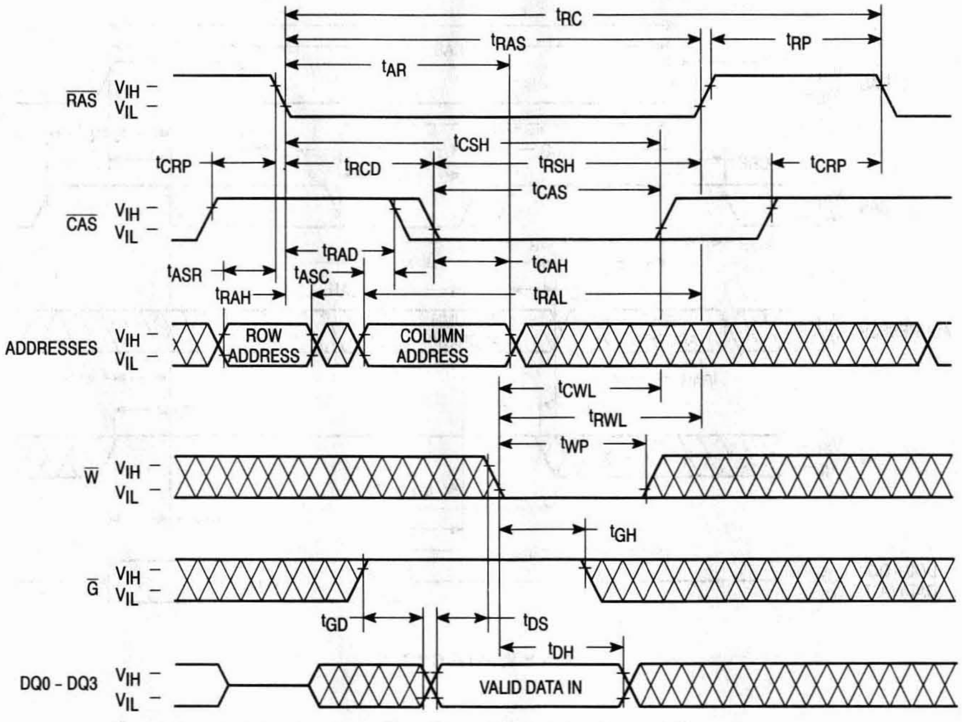
READ CYCLE


tRC
tRAS
tRP
RAS VIH — VIL —
tCSH
tCPN
tCRP
tRCD
tRSH
tCRP
tCAS
CAS VIH — VIL —
tASR
tAR
tRAD
tRAL
tASC
tCAH
ADDRESSES VIH — VIL —
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W VIH — VIL —
tCAC
tAA
tOFF
tCLZ
tRAC
DQ0 - DQ3 VOH — (DATA OUT) VOL —
HIGH-Z
VALID DATA

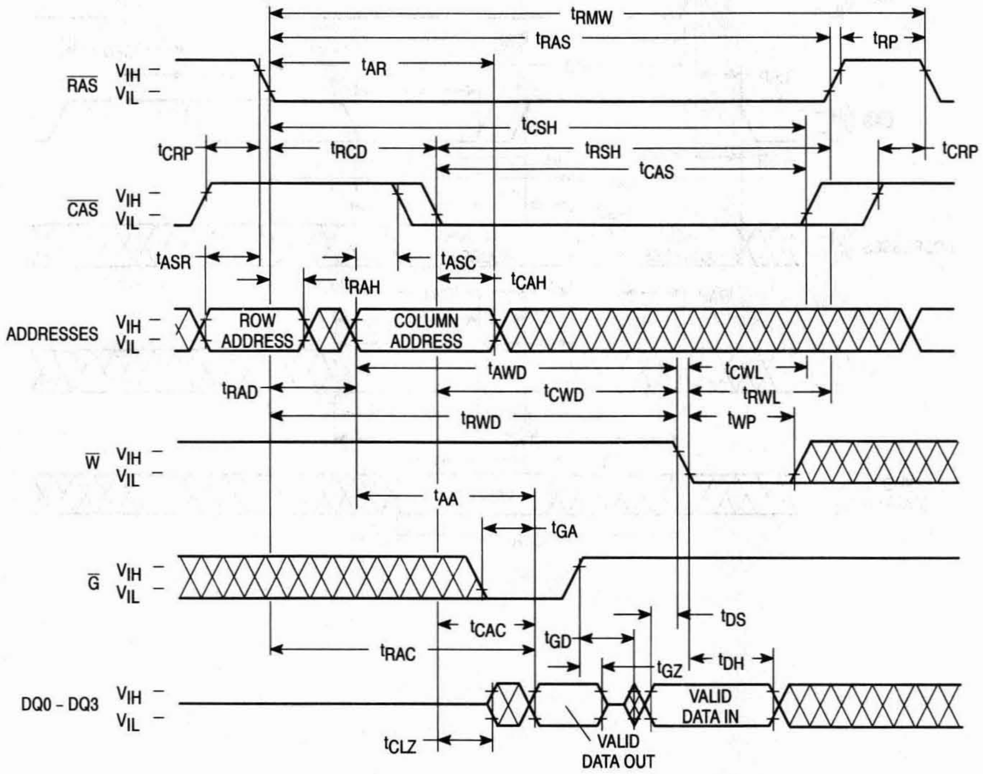
EARLY WRITE CYCLE


tRC
tRAS
tRP
RAS VIH — VIL —
tCSH
tCPN
tCRP
tRCD
tRSH
tCRP
tCAS
CAS VIH — VIL —
tASR
tAR
tRAD
tRAL
tASC
tCAH
ADDRESSES VIH — VIL —
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWP
W VIH — VIL —
tRWL
tWCR
tDS
tDH
DQ0-DQ3 VIH — (DATA IN) VIL —
VALID DATA
tDHR

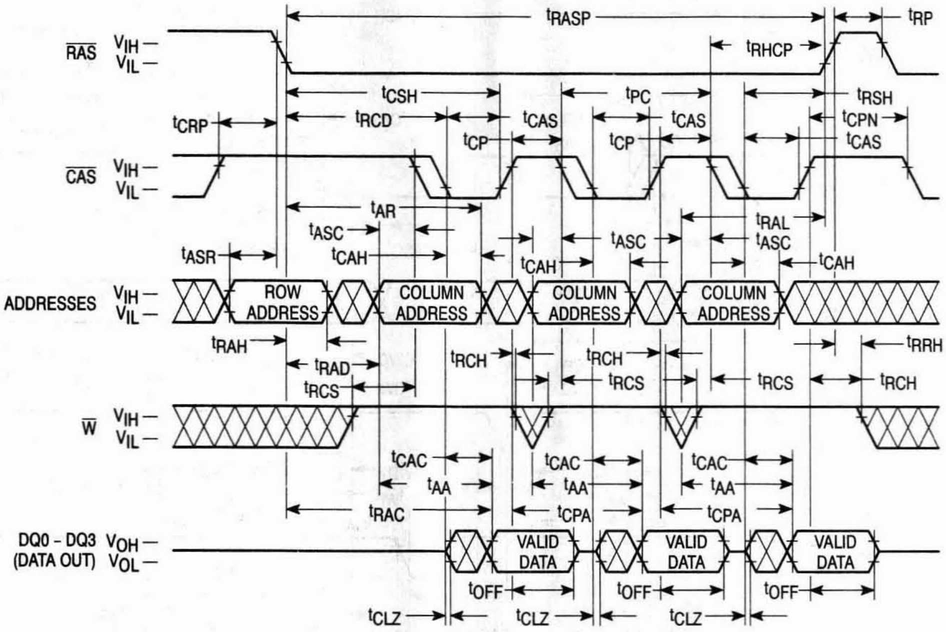
$\overline{G}$ CONTROLLED LATE WRITE CYCLE


t_{RC}
t_{RAS}
t_{RP}
t_{AR}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
t_{RAD}
t_{ASR}
t_{ASC}
t_{CAH}
t_{RAH}
t_{RAL}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{CWL}
t_{RWL}
t_{WP}
$\overline{W}$
t_{GH}
$\overline{G}$
t_{GD}
t_{DS}
t_{DH}
DQ0 – DQ3
VALID DATA IN

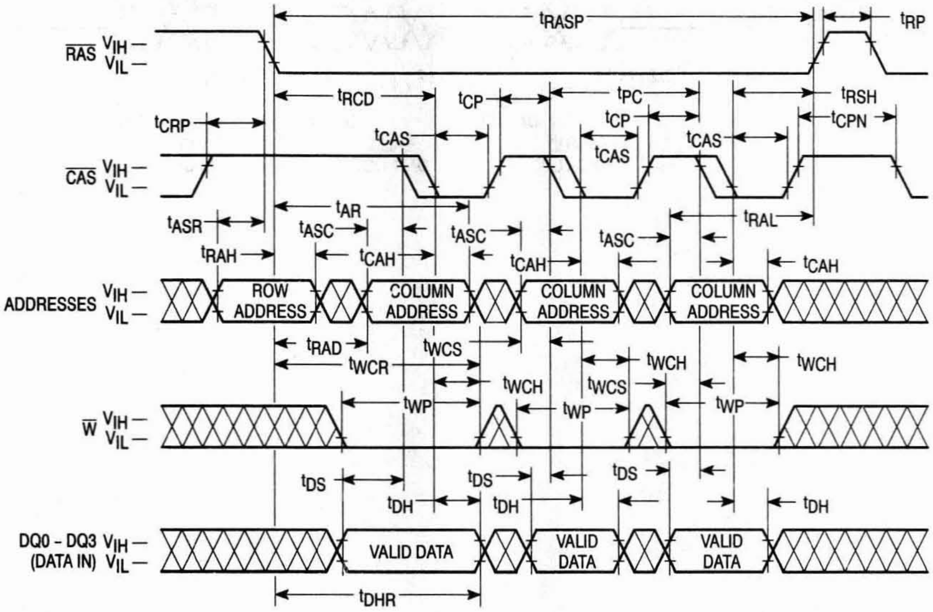
READ-WRITE CYCLE


t_{RMW}
t_{RAS}
t_{RP}
t_{AR}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{AWD}
t_{CWL}
t_{RAD}
t_{CWD}
t_{RWL}
t_{RWD}
t_{WP}
$\overline{W}$
t_{AA}
t_{GA}
$\overline{G}$
t_{DS}
t_{CAC}
t_{GD}
t_{RAC}
t_{GZ}
t_{DH}
DQ0 – DQ3
VALID DATA IN
t_{CLZ}
VALID DATA OUT

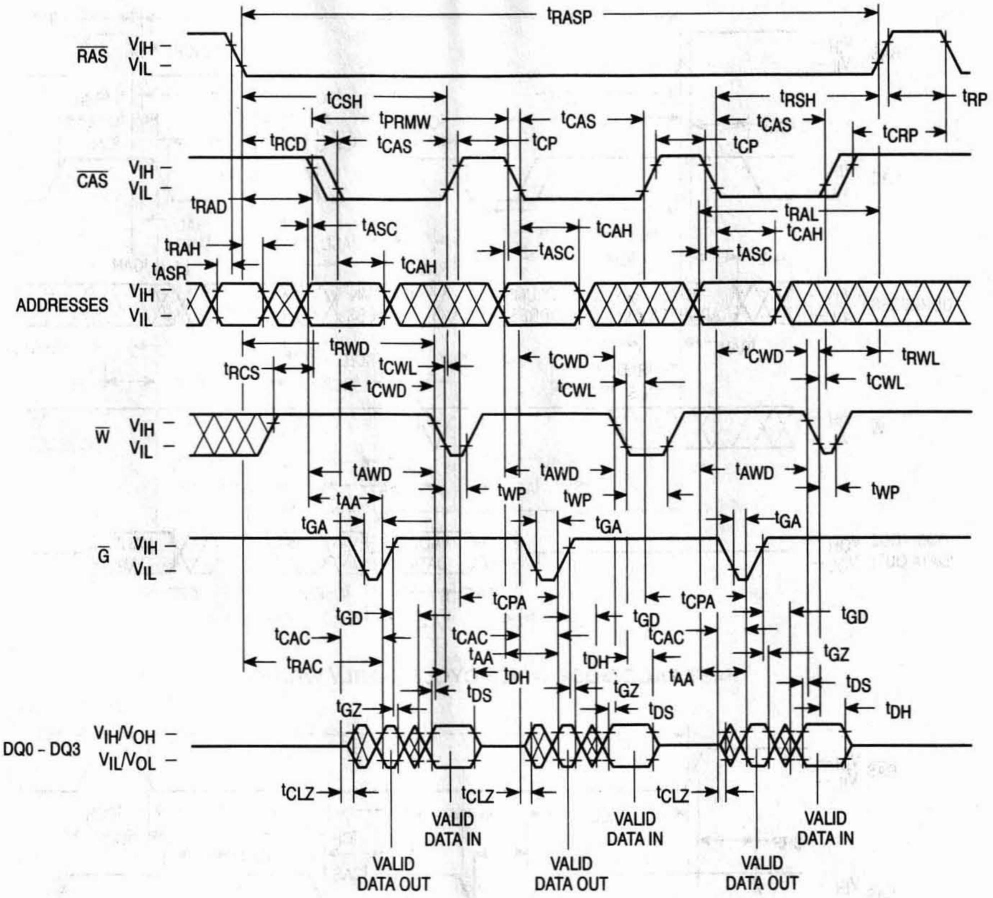
FAST PAGE MODE READ CYCLE


RAS
VIH
VIL
CAS
VIH
VIL
ADDRESSES
VIH
VIL
W
VIH
VIL
DQ0 - DQ3
(DATA OUT)
VOH
VOL
tRASP
tRP
tRHCP
tCSH
tPC
tRSH
tCRP
tRCD
tCAS
tCAS
tCPN
tCP
tCP
tCAS
tAR
tRAL
tASC
tASC
tASC
tASR
tCAH
tCAH
tCAH
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAH
tRRH
tRCH
tRCH
tRAD
tRCS
tRCS
tRCS
tRCH
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
VALID DATA
VALID DATA
VALID DATA
tOFF
tOFF
tOFF
tCLZ
tCLZ
tCLZ

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

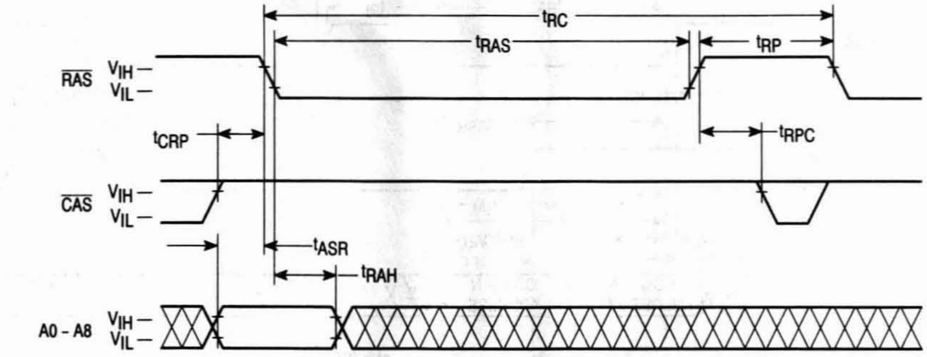

RAS
VIH
VIL
CAS
VIH
VIL
ADDRESSES
VIH
VIL
W
VIH
VIL
DQ0 - DQ3
(DATA IN)
VIH
VIL
tRASP
tRP
tRCD
tCP
tPC
tRSH
tCRP
tCP
tCPN
tCAS
tCAS
tCAS
tAR
tRAL
tASR
tASC
tASC
tASC
tRAH
tCAH
tCAH
tCAH
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tWCS
tWCR
tWCH
tWCS
tWCH
tWCH
tWP
tWP
tWP
tDS
tDS
tDS
tDH
tDH
tDH
VALID DATA
VALID DATA
VALID DATA
tDHR

FAST PAGE MODE READ-WRITE CYCLE


t_{RASP}
$\overline{RAS}$
V_{IH} –
V_{IL} –
t_{CSH}
t_{RSH}
t_{RP}
t_{PRMW}
t_{CAS}
t_{CAS}
t_{CAS}
t_{CRP}
t_{RCD}
t_{CP}
t_{CP}
$\overline{CAS}$
V_{IH} –
V_{IL} –
t_{RAD}
t_{RAL}
t_{ASC}
t_{CAH}
t_{CAH}
t_{RAH}
t_{ASC}
t_{ASC}
t_{CAH}
t_{ASR}
ADDRESSES
V_{IH} –
V_{IL} –
t_{RWD}
t_{CWD}
t_{CWD}
t_{RWL}
t_{RCS}
t_{CWL}
t_{CWD}
t_{CWL}
t_{CWL}
$\overline{W}$
V_{IH} –
V_{IL} –
t_{AWD}
t_{AWD}
t_{AWD}
t_{WP}
t_{WP}
t_{WP}
t_{AA}
t_{GA}
t_{GA}
t_{GA}
$\overline{G}$
V_{IH} –
V_{IL} –
t_{CPA}
t_{CPA}
t_{GD}
t_{GD}
t_{GD}
t_{CAC}
t_{CAC}
t_{CAC}
t_{AA}
t_{DH}
t_{RAC}
t_{DH}
t_{AA}
t_{GZ}
t_{DS}
t_{GZ}
t_{GZ}
t_{DS}
t_{DS}
t_{DH}
DQ0 – DQ3
V_{IH}/V_{OH} –
V_{IL}/V_{OL} –
t_{CLZ}
t_{CLZ}
t_{CLZ}
VALID DATA IN
VALID DATA IN
VALID DATA IN
VALID DATA OUT
VALID DATA OUT
VALID DATA OUT

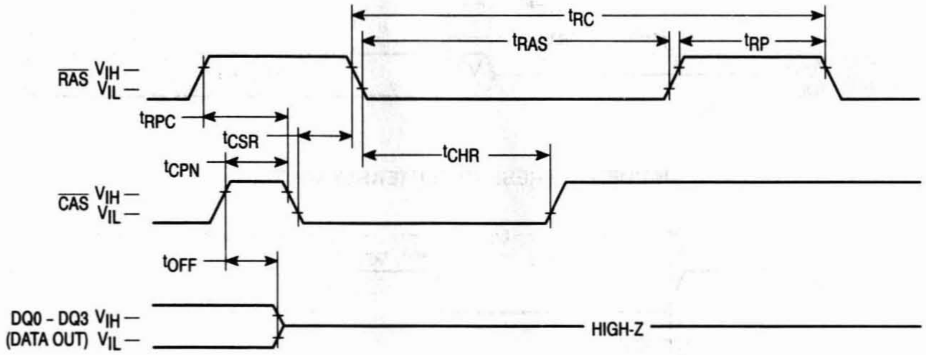
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

($\overline{\text{W}}$ and $\overline{\text{G}}$ are Don't Care)

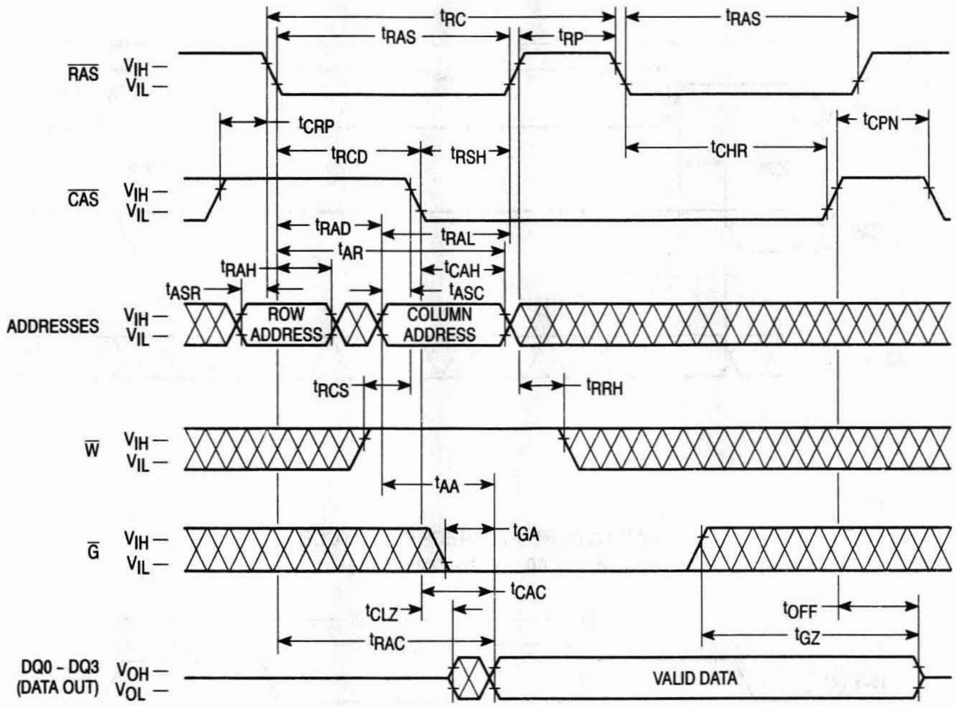

t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$ V_{IH} — V_{IL} —
t_{CRP}
t_{RPC}
$\overline{CAS}$ V_{IH} — V_{IL} —
t_{ASR}
t_{RAH}
A0 - A8 V_{IH} — V_{IL} —

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

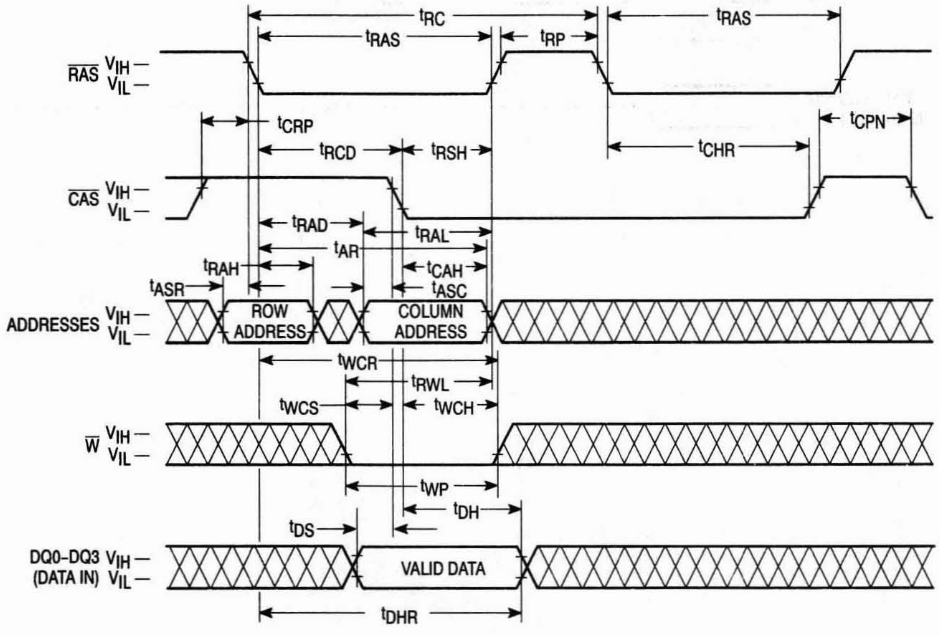
($\overline{\text{W}}$ and A0 – A8 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$ V_{IH} — V_{IL} —
t_{RPC}
t_{CSR}
t_{CHR}
t_{CPN}
$\overline{CAS}$ V_{IH} — V_{IL} —
t_{OFF}
DQ0 - DQ3 V_{IH} —
(DATA OUT) V_{IL} —
HIGH-Z

HIDDEN REFRESH CYCLE (READ)


t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$
V_{IH} —
V_{IL} —
t_{CRP}
t_{CPN}
t_{RCD}
t_{RSH}
t_{CHR}
$\overline{CAS}$
V_{IH} —
V_{IL} —
t_{RAD}
t_{RAL}
t_{AR}
t_{RAH}
t_{CAH}
t_{ASR}
t_{ASC}
ADDRESSES
V_{IH} —
V_{IL} —
ROW ADDRESS
COLUMN ADDRESS
t_{RCS}
t_{RRH}
$\overline{W}$
V_{IH} —
V_{IL} —
t_{AA}
t_{GA}
$\overline{G}$
V_{IH} —
V_{IL} —
t_{CAC}
t_{CLZ}
t_{OFF}
t_{GZ}
t_{RAC}
DQ0 - DQ3 (DATA OUT)
V_{OH} —
V_{OL} —
VALID DATA

HIDDEN REFRESH CYCLE (EARLY WRITE)


t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$
V_{IH} —
V_{IL} —
t_{CRP}
t_{CPN}
t_{RCD}
t_{RSH}
t_{CHR}
$\overline{CAS}$
V_{IH} —
V_{IL} —
t_{RAD}
t_{RAL}
t_{AR}
t_{RAH}
t_{CAH}
t_{ASR}
t_{ASC}
ADDRESSES
V_{IH} —
V_{IL} —
ROW ADDRESS
COLUMN ADDRESS
t_{WCR}
t_{RWL}
t_{WCS}
t_{WCH}
$\overline{W}$
V_{IH} —
V_{IL} —
t_{WP}
t_{DH}
t_{DS}
DQ0-DQ3 (DATA IN)
V_{IH} —
V_{IL} —
VALID DATA
t_{DHR}

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe ($\overline{\text{RAS}}$) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 bit locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This gate feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are two other variations in addressing the 256K x 4 RAM: **$\overline{\text{RAS}}$-only refresh cycle** and **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{\text{CAS}}$ and output enable ($\overline{\text{G}}$) control read access times: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum and $\overline{\text{G}}$ must be active $t_{RAC}-t_{GA}$ (both minimum) after $\overline{\text{RAS}}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{\text{G}}$ active transition does not occur in time, read access time is determined by either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for a minimum of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clocks are active. When either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} or t_{GZ} after inactive transition.

WRITE CYCLE

The DRAM may be written with any of four cycles; early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers disabled, effectively disabling $\overline{\text{G}}$.

A late write cycle (referred to as $\overline{\text{G}}$ controlled write) occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + t_T) \le t_{RAS}$, if timing minimums t_{RCD}, t_{RWL}, and t_T are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but Q may be indeterminate — see note 15 of AC Operating Conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 512 column locations on a selected row of the 256K x 4 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum of t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). The operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM414256 require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM414256. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM414256 and 64 milliseconds on the MCM41L4256.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **RAS-only refresh**, **CAS before RAS refresh**, and **Hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1).

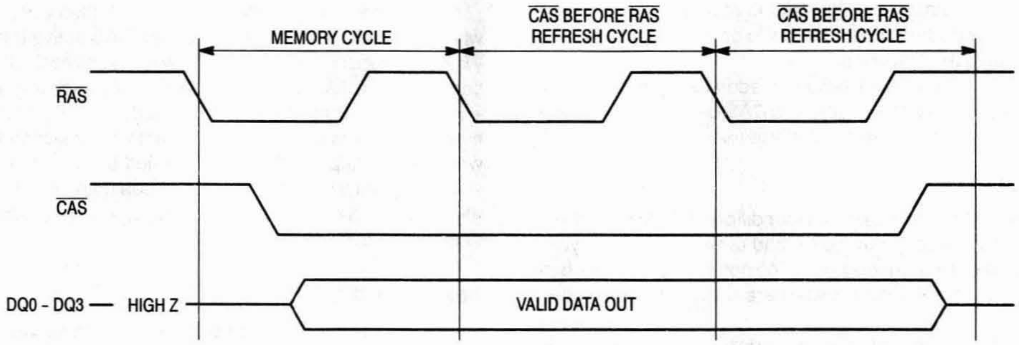


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION

(Order by Full Part Number)

MCM 414256 or 41L4256 X XX XX

Motorola Memory Prefix — MCM
Part Number — 414256 or 41L4256
Shipping Method (R2 = Tape and Reel, Blank = Rails)
Speed (70 = 70 ns, 80 = 80 ns)
Package (P = 300 mil Plastic DIP, J = 300 mil SOJ, Z = 300 mil ZIP)

Full Part Numbers —	MCM414256P70	MCM414256J70	MCM414256J70R2	MCM414256Z70
	MCM414256P80	MCM414256J80	MCM414256J80R2	MCM414256Z80
	MCM41L4256P70	MCM41L4256J70	MCM41L4256J70R2	MCM41L4256Z70
	MCM41L4256P80	MCM41L4256J80	MCM41L4256J80R2	MCM41L4256Z80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

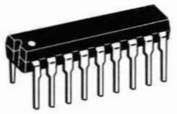
MCM511000A
MCM51L1000A

1M x 1 CMOS Dynamic RAM
Page Mode, Commercial and Industrial Temperature Range

The MCM511000A is a 1.0µ CMOS high-speed dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

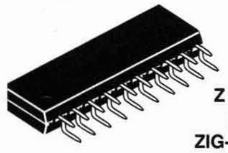
The MCM511000A requires only ten address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil dual-in-line plastic package (DIP), a 300 mil SOJ plastic package, and a 100 mil zig-zag in-line package (ZIP).

- Two Temperature Ranges: Commercial — 0°C to 70°C
  Industrial — – 40°C to + 85°C
- Three-State Data Output
- Common I/O with Early Write
- Fast Page Mode
- Test Mode
- TTL-Compatible Inputs and Output
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh: MCM511000A = 8 ms
  MCM51L1000A = 64 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM511000A-70 and MCM51L1000A-70 = 70 ns (Max)
  MCM511000A-80 and MCM51L1000A-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM511000A-70 and MCM51L1000A-70 = 440 mW (Max)
  MCM511000A-80 and MCM51L1000A-80 = 385 mW (Max)
- Low Standby Power Dissipation:
  MCM511000A and MCM51L1000A = 11 mW (Max, TTL Levels)
  MCM511000A = 5.5 mW (Max, CMOS Levels)
  MCM51L1000A = 1.1 mW (Max, CMOS Levels)



P PACKAGE
300 MIL PLASTIC
CASE 707A-01

J PACKAGE
300 MIL SOJ
CASE 822-03



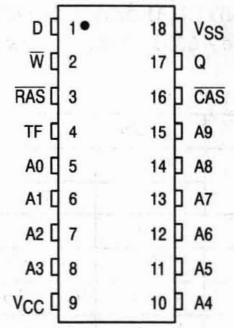
Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836-02

PIN NAMES

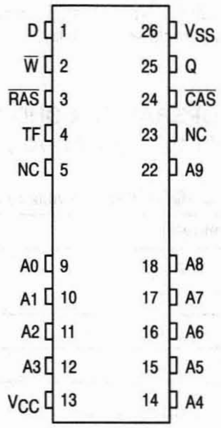
A0 – A9	Address Input
D	Data Input
Q	Data Output
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power Supply (+5 V)
V_{SS}	Ground
TF	Test Function Enable
NC	No Connection

PIN ASSIGNMENTS

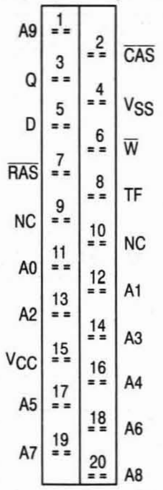
DUAL-IN-LINE


D 1
W 2
RAS 3
TF 4
A0 5
A1 6
A2 7
A3 8
VCC 9
18 VSS
17 Q
16 CAS
15 A9
14 A8
13 A7
12 A6
11 A5
10 A4

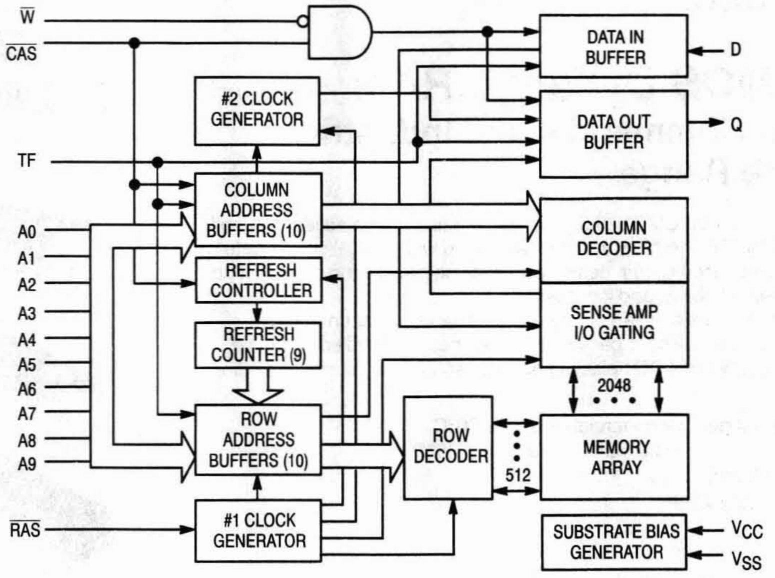
SMALL OUTLINE


D 1
W 2
RAS 3
TF 4
NC 5
A0 9
A1 10
A2 11
A3 12
VCC 13
26 VSS
25 Q
24 CAS
23 NC
22 A9
18 A8
17 A7
16 A6
15 A5
14 A4

ZIG-ZAG IN-LINE


A9 1
2 CAS
Q 3
4 VSS
D 5
6 W
RAS 7
8 TF
NC 9
10 NC
A0 11
12 A1
A2 13
14 A3
VCC 15
16 A4
A5 17
18 A6
A7 19
20 A8

BLOCK DIAGRAM


W
CAS
TF
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
RAS
#2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (10)
REFRESH CONTROLLER
REFRESH COUNTER (9)
ROW ADDRESS BUFFERS (10)
#1 CLOCK GENERATOR
ROW DECODER
512
DATA IN BUFFER
D
DATA OUT BUFFER
Q
COLUMN DECODER
SENSE AMP I/O GATING
2048
MEMORY ARRAY
SUBSTRATE BIAS GENERATOR
VCC
VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Test Function Input Voltage	$V_{in\ (TF)}$	– 1 to + 10.5	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range Commercial Industrial	T_A	0 to + 70 – 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C and – 40 to + 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V
Test Function Input High Voltage	$V_{IH(TF)}$	V_{CC} + 4.5	—	10.5	V
Test Function Input Low Voltage	$V_{IL(TF)}$	– 1.0	—	V_{CC} + 1.0	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	1
MCM511000A-70 and MCM51L1000A-70, t_{RC} = 130 ns, T_A = 0 to 70°C		—	80		
MCM511000A-80 and MCM51L1000A-80, t_{RC} = 150 ns, T_A = 0 to 70°C		—	70		
MCM511000A-C70 and MCM51L1000A-C70, t_{RC} = 130 ns, T_A = – 40 to + 85°C		—	85		
MCM511000A-C80 and MCM51L1000A-C80, t_{RC} = 150 ns, T_A = – 40 to + 85°C		—	75		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}			mA	
MCM511000A and MCM51L1000A, T_A = 0 to 70°C		—	2		
MCM511000A-C and MCM51L1000A-C, T_A = – 40 to + 85°C		—	3		
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	1
MCM511000A-70 and MCM51L1000A-70, t_{RC} = 130 ns, T_A = 0 to 70°C		—	80		
MCM511000A-80 and MCM51L1000A-80, t_{RC} = 150 ns, T_A = 0 to 70°C		—	70		
MCM511000A-C70 and MCM51L1000A-C70, t_{RC} = 130 ns, T_A = – 40 to + 85°C		—	85		
MCM511000A-C80 and MCM51L1000A-C80, t_{RC} = 150 ns, T_A = – 40 to + 85°C		—	75		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	1, 2
MCM511000A-70 and MCM51L1000A-70, t_{PC} = 40 ns, T_A = 0 to 70°C		—	60		
MCM511000A-80 and MCM51L1000A-80, t_{PC} = 45 ns, T_A = 0 to 70°C		—	50		
MCM511000A-C70 and MCM51L1000A-C70, t_{PC} = 40 ns, T_A = – 40 to + 85°C		—	65		
MCM511000A-C80 and MCM51L1000A-C80, t_{PC} = 45 ns, T_A = – 40 to + 85°C		—	55		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}				
MCM511000A, T_A = 0 to 70°C and MCM511000A-C, T_A = – 40 to + 85°C		—	1.0	mA	
MCM51L1000A, T_A = 0 to 70°C		—	200	µA	
MCM51L1000A-C, T_A = – 40 to + 85°C		—	400	µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	1
MCM511000A-70 and MCM51L1000A-70, t_{RC} = 130 ns, T_A = 0 to 70°C		—	80		
MCM511000A-80 and MCM51L1000A-80, t_{RC} = 150 ns, T_A = 0 to 70°C		—	70		
MCM511000A-C70 and MCM51L1000A-C70, t_{RC} = 130 ns, T_A = – 40 to + 85°C		—	85		
MCM511000A-C80 and MCM51L1000A-C80, t_{RC} = 150 ns, T_A = – 40 to + 85°C		—	75		
V_{CC} Power Supply Current, Battery Backup Mode (t_{RC} = 125 µs, t_{RAS} = 1 µs, $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V, A0 – A9, $\overline{W}$, D = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}			µA	1
MCM51L1000A, T_A = 0 to 70°C		—	300		
MCM51L1000A-C, T_A = – 40 to + 85°C		—	500		
Input Leakage Current (Except TF) (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	– 10	10	µA	
Input Leakage Current (TF) (0 V ≤ V_{in} (TF) ≤ V_{CC} + 0.5 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	– 10	10	µA	
Test Function Input Current (V_{CC} + 4.5 V ≤ V_{in} (TF) ≤ V_{CC} ≤ 10.5 V)	$I_{in\ (TF)}$	—	1	mA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	D, A0 – A9	C_{in}	5	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, TF		7	
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C and – 40 to + 85°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511000A-70 MCM51L1000A-70		MCM511000A-80 MCM51L1000A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	155	—	175	—	ns	6
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	65	—	70	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	ns	7, 8
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	7, 10
Access Time from $\overline{\text{CAS}}$ Precharge	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	7
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge (Page Mode Cycle Only)	t_{CELREH}	t_{RHCP}	35	—	40	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	ns	12
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	ns	13
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C and – 40°C ≤ T_A ≤ + 85°C) is ensured.
7. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \le t_{RCD}$ (max).
9. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
10. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

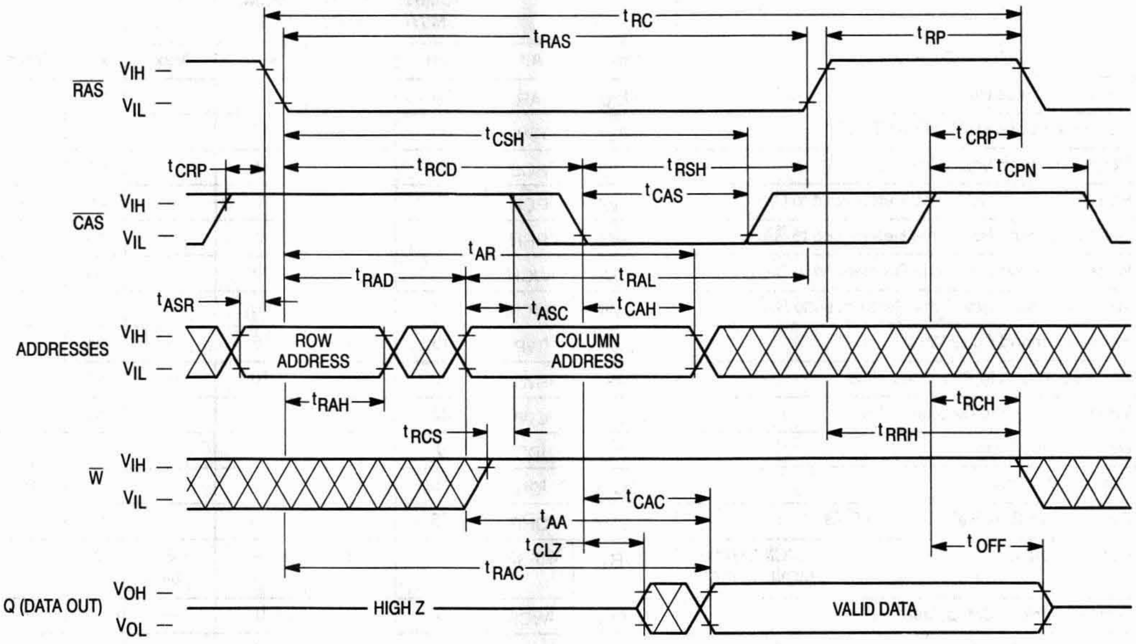
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM511000A-70 MCM51L1000A-70		MCM511000A-80 MCM51L1000A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Column Address Hold Time Referenced to RAS	t_{RELAX}	t_{AR}	55	—	60	—	ns	
Column Address to RAS Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to CAS	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	14
Read Command Hold Time Referenced to RAS	t_{REHWX}	t_{RRH}	0	—	0	—	ns	14
Write Command Hold Time Referenced to CAS	t_{CELWH}	t_{WCH}	15	—	15	—	ns	
Write Command Hold Time Referenced to RAS	t_{RELWH}	t_{WCR}	55	—	60	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to RAS Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to CAS Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	15
Data in Hold Time Referenced to RAS	t_{RELDX}	t_{DHR}	55	—	60	—	ns	
Refresh Period MCM511000A MCM51L1000A	t_{RVRV}	t_{RFSH}	— —	8 64	— —	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	16
CAS to Write Delay	t_{CELWL}	t_{CWD}	20	—	20	—	ns	16
RAS to Write Delay	t_{RELWL}	t_{RWD}	70	—	80	—	ns	16
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	35	—	40	—	ns	16
CAS Precharge to Write Delay Time	t_{CEHWL}	t_{CPWD}	35	—	40	—	ns	16
CAS Setup Time for CAS Before RAS Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	ns	
CAS Hold Time for CAS Before RAS Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	ns	
CAS Precharge to CAS Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
CAS Precharge Time for CAS Before RAS Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	ns	
CAS Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	ns	
Test Mode Enable Setup Time Referenced to RAS	t_{TEHREL}	t_{TES}	0	—	0	—	ns	
Test Mode Enable Hold Time Referenced to RAS	t_{REHTEL}	t_{TEHR}	0	—	0	—	ns	
Test Mode Enable Hold Time Referenced to CAS	t_{CEHTEL}	t_{TEHC}	0	—	0	—	ns	

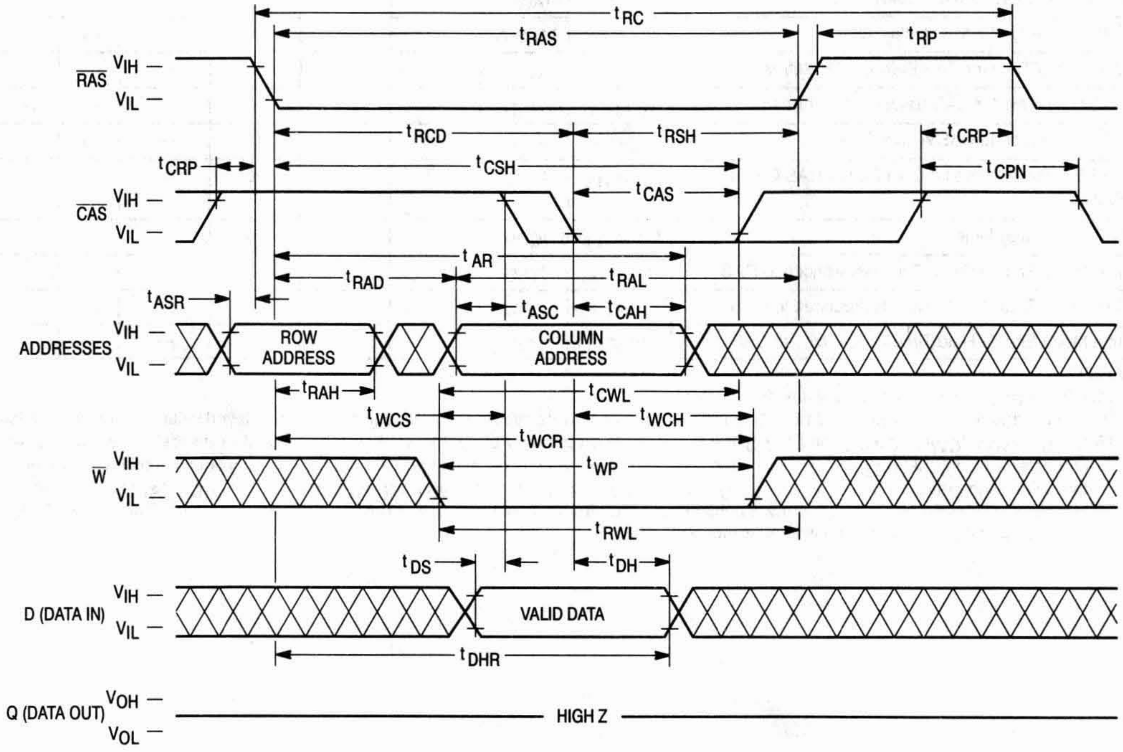
NOTES:

14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to CAS leading edge in early write cycles and to W leading edge in delayed write or read-write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

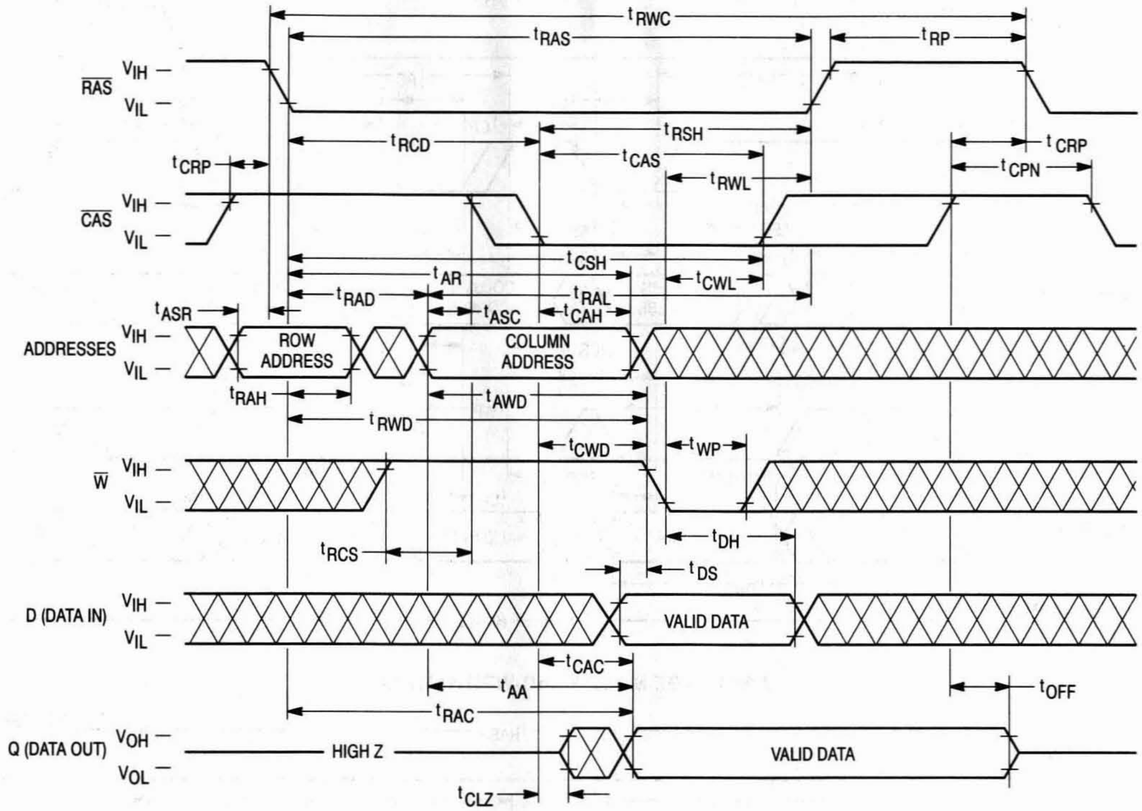
READ CYCLE


t_{RC}
t_{RAS}
t_{RP}
V_{IH}
$\overline{RAS}$
V_{IL}
t_{CSH}
t_{CRP}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CPN}
t_{CAS}
V_{IH}
$\overline{CAS}$
V_{IL}
t_{AR}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
V_{IH}
ADDRESSES
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RAH}
t_{RCH}
t_{RCS}
t_{RRH}
V_{IH}
$\overline{W}$
V_{IL}
t_{CAC}
t_{AA}
t_{CLZ}
t_{OFF}
t_{RAC}
V_{OH}
Q (DATA OUT)
V_{OL}
HIGH Z
VALID DATA

EARLY WRITE CYCLE

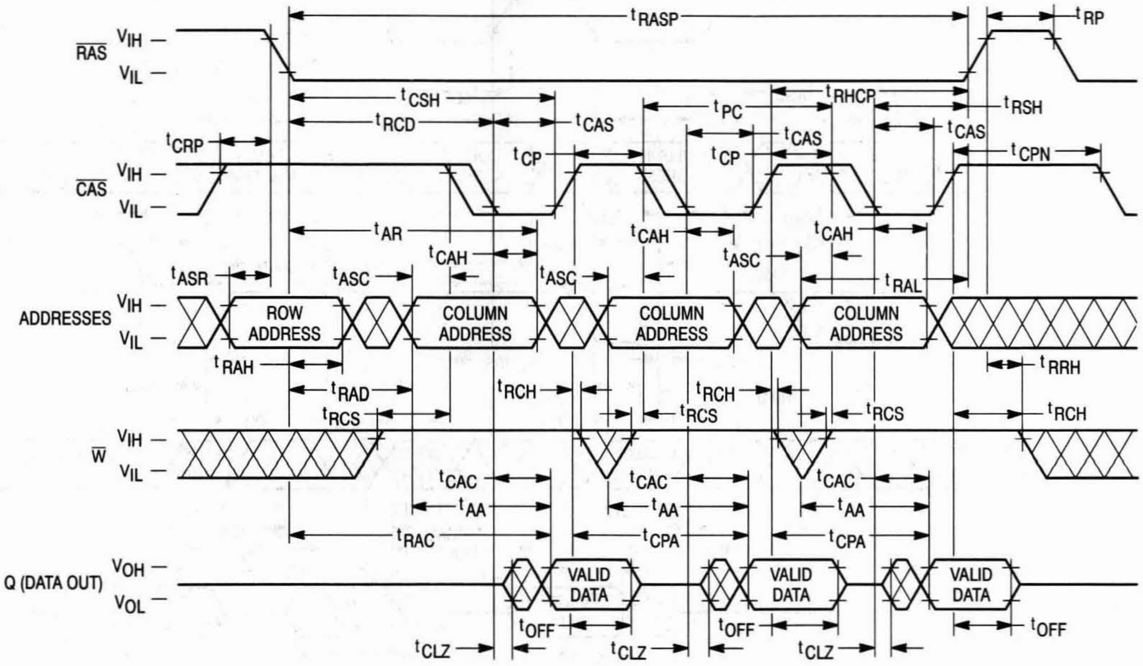

t_{RC}
t_{RAS}
t_{RP}
V_{IH}
$\overline{RAS}$
V_{IL}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CRP}
t_{CSH}
t_{CPN}
t_{CAS}
V_{IH}
$\overline{CAS}$
V_{IL}
t_{AR}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
V_{IH}
ADDRESSES
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RAH}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WCR}
V_{IH}
$\overline{W}$
V_{IL}
t_{WP}
t_{RWL}
t_{DS}
t_{DH}
V_{IH}
D (DATA IN)
V_{IL}
VALID DATA
t_{DHR}
V_{OH}
Q (DATA OUT)
V_{OL}
HIGH Z

READ-WRITE CYCLE



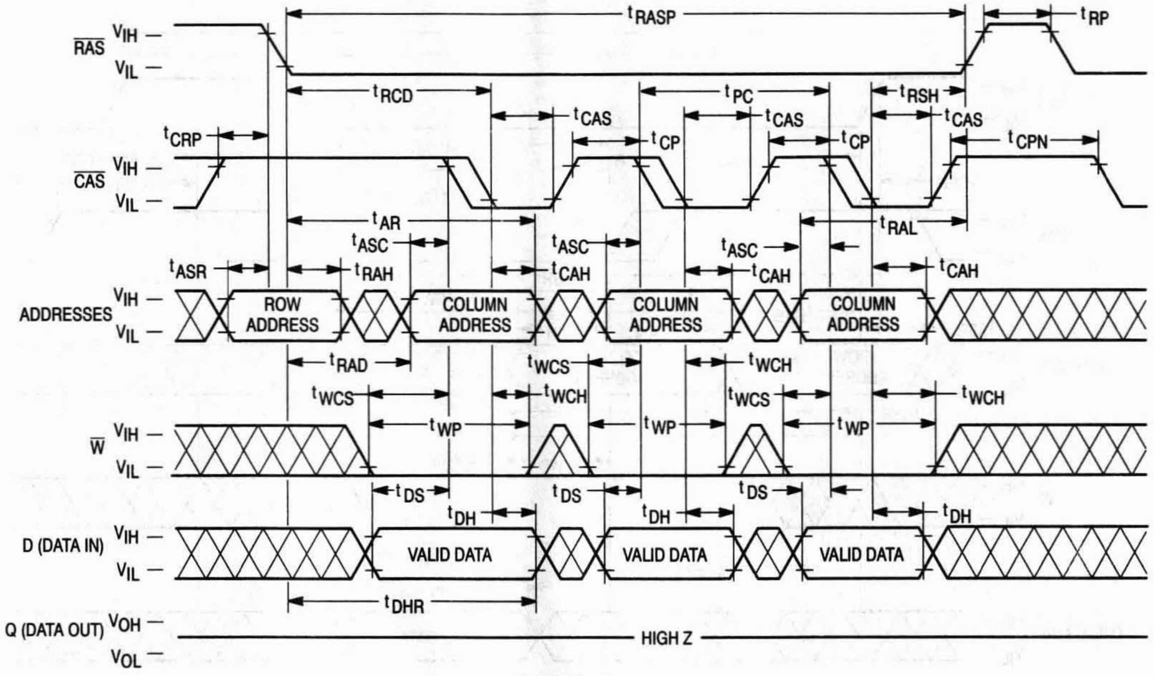
tRWC
tRAS
tRP
RAS
VIH
VIL
tRSH
tCRP
tRCD
tCAS
tCPN
tRWL
CAS
tCSH
tAR
tCWL
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tRAH
tAWD
tRWD
tCWD
tWP
W
tDH
tRCS
tDS
D (DATA IN)
VALID DATA
tCAC
tAA
tOFF
tRAC
Q (DATA OUT)
VOH
VOL
HIGH Z
tCLZ

FAST PAGE MODE READ CYCLE

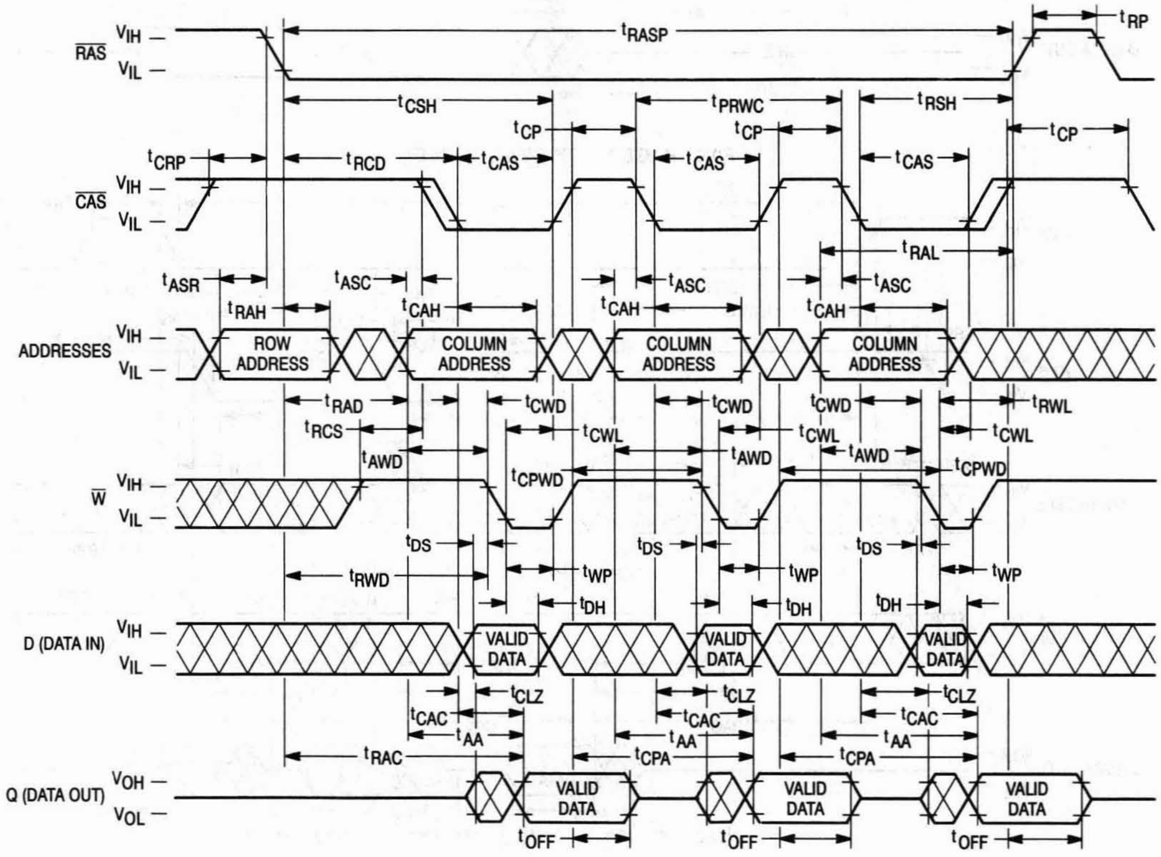


tRASP
tRP
RAS
VIH
VIL
tCSH
tRHCP
tRSH
tRCD
tCAS
tPC
tCAS
tCAS
tCRP
tCP
tCP
tCPN
CAS
tAR
tCAH
tCAH
tCAH
tASC
tASR
tASC
tASC
tRAL
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAH
tRRH
tRAD
tRCH
tRCH
tRCS
tRCS
tRCS
tRCH
W
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
Q (DATA OUT)
VOH
VOL
VALID DATA
VALID DATA
VALID DATA
tOFF
tOFF
tOFF
tCLZ
tCLZ
tCLZ

FAST PAGE MODE EARLY-WRITE CYCLE

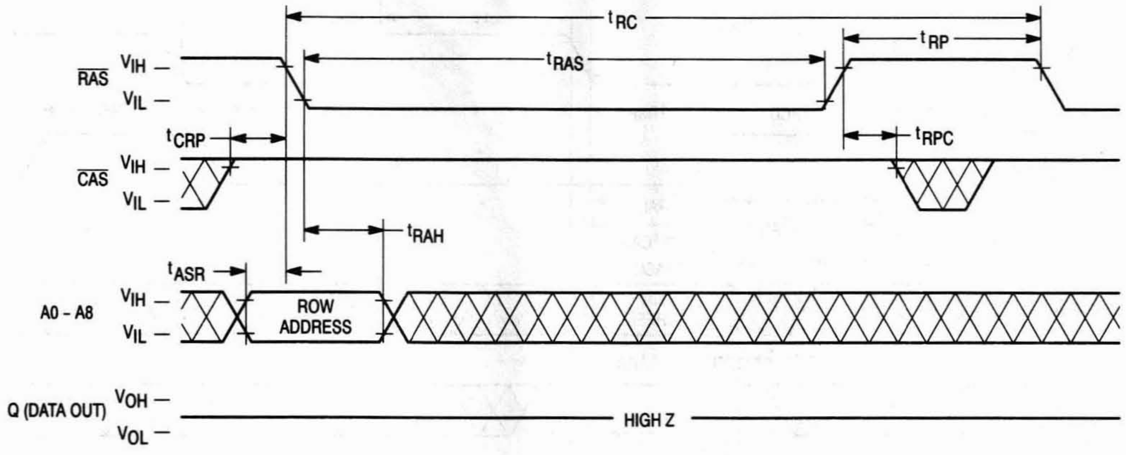

RAS
CAS
ADDRESSES
W
D (DATA IN)
Q (DATA OUT)
VIH
VIL
VOH
VOL
tRASP
tRP
tRCD
tPC
tRSH
tCAS
tCRP
tCP
tCPN
tAR
tRAL
tASC
tASR
tRAH
tCAH
ROW ADDRESS
COLUMN ADDRESS
tRAD
tWCS
tWCH
tWP
tDS
tDH
VALID DATA
tDHR
HIGH Z

FAST PAGE MODE READ-WRITE CYCLE


RAS
CAS
ADDRESSES
W
D (DATA IN)
Q (DATA OUT)
VIH
VIL
VOH
VOL
tRASP
tRP
tCSH
tPRWC
tRSH
tCP
tCRP
tRCD
tCAS
tRAL
tASR
tASC
tRAH
tCAH
ROW ADDRESS
COLUMN ADDRESS
tRAD
tCWD
tRWL
tRCS
tCWL
tAWD
tCPWD
tDS
tRWD
tWP
tDH
VALID DATA
tCLZ
tCAC
tAA
tRAC
tCPA
tOFF

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

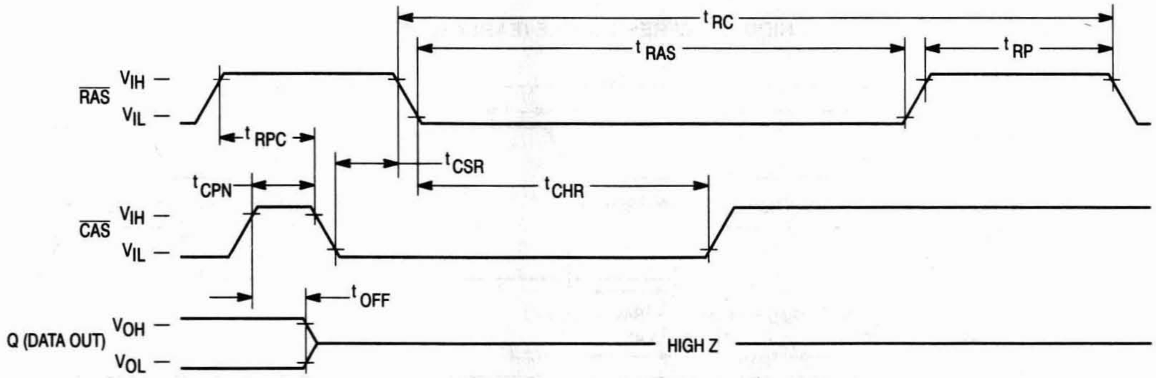
($\overline{\text{W}}$ and A9 are Don't Care)



t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
A0 - A8
V_{IH}
V_{IL}
ROW ADDRESS
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

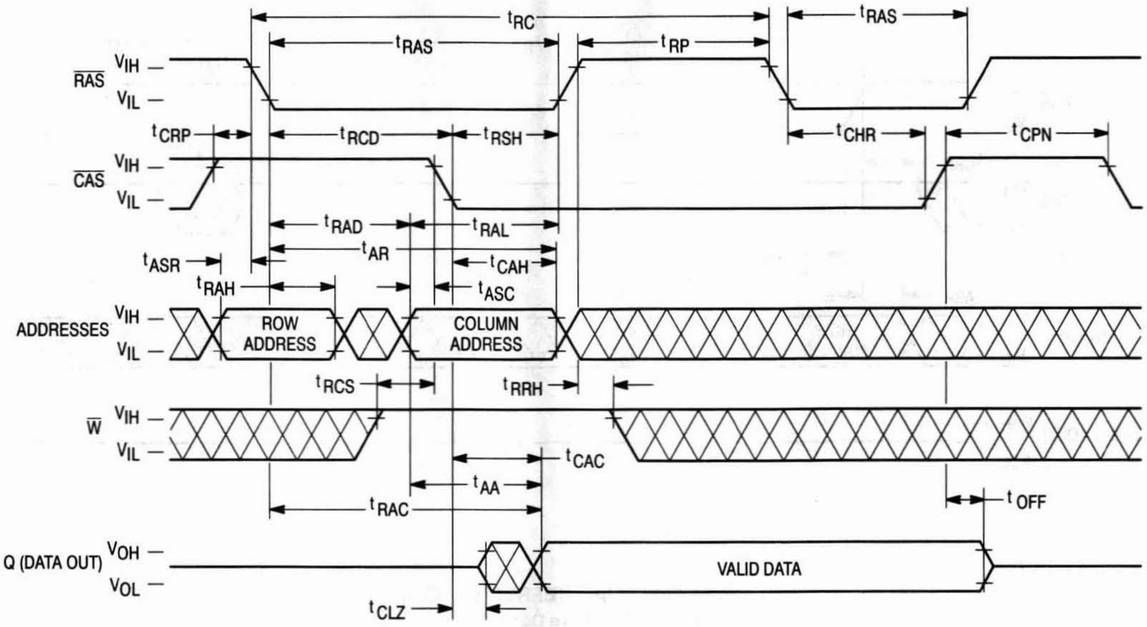
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{W}}$ and A0 – A9 are Don't Care)



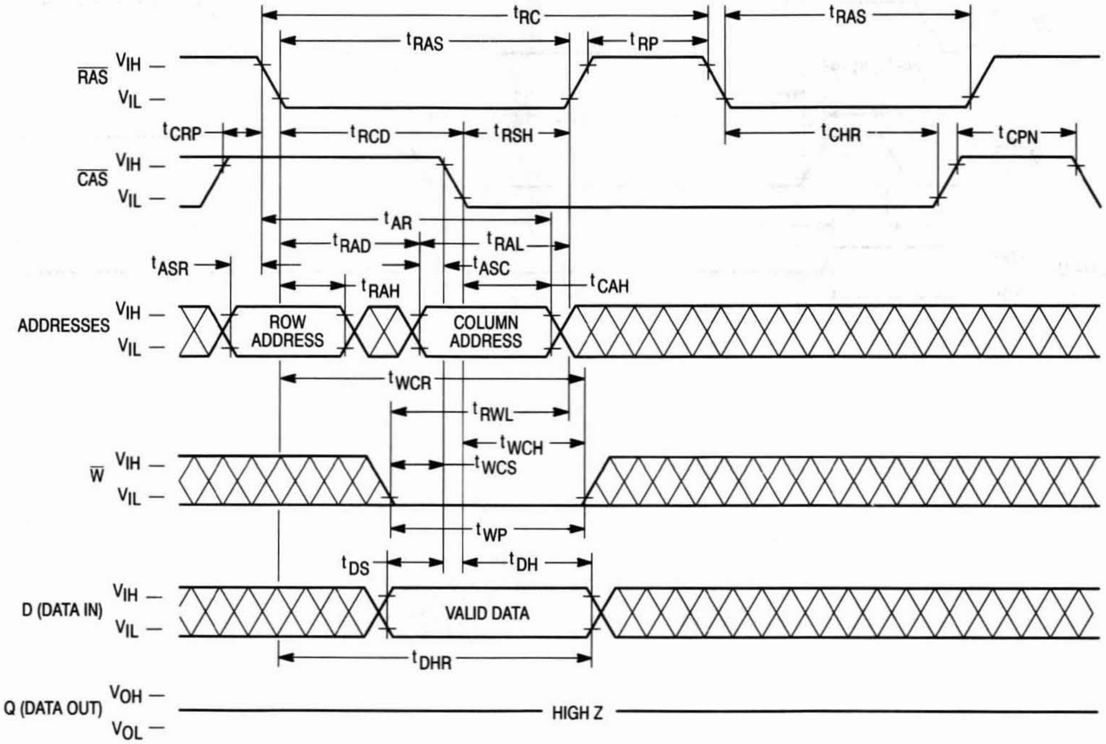
t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RPC}
t_{CSR}
t_{CPN}
t_{CHR}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{OFF}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

HIDDEN REFRESH CYCLE (READ)



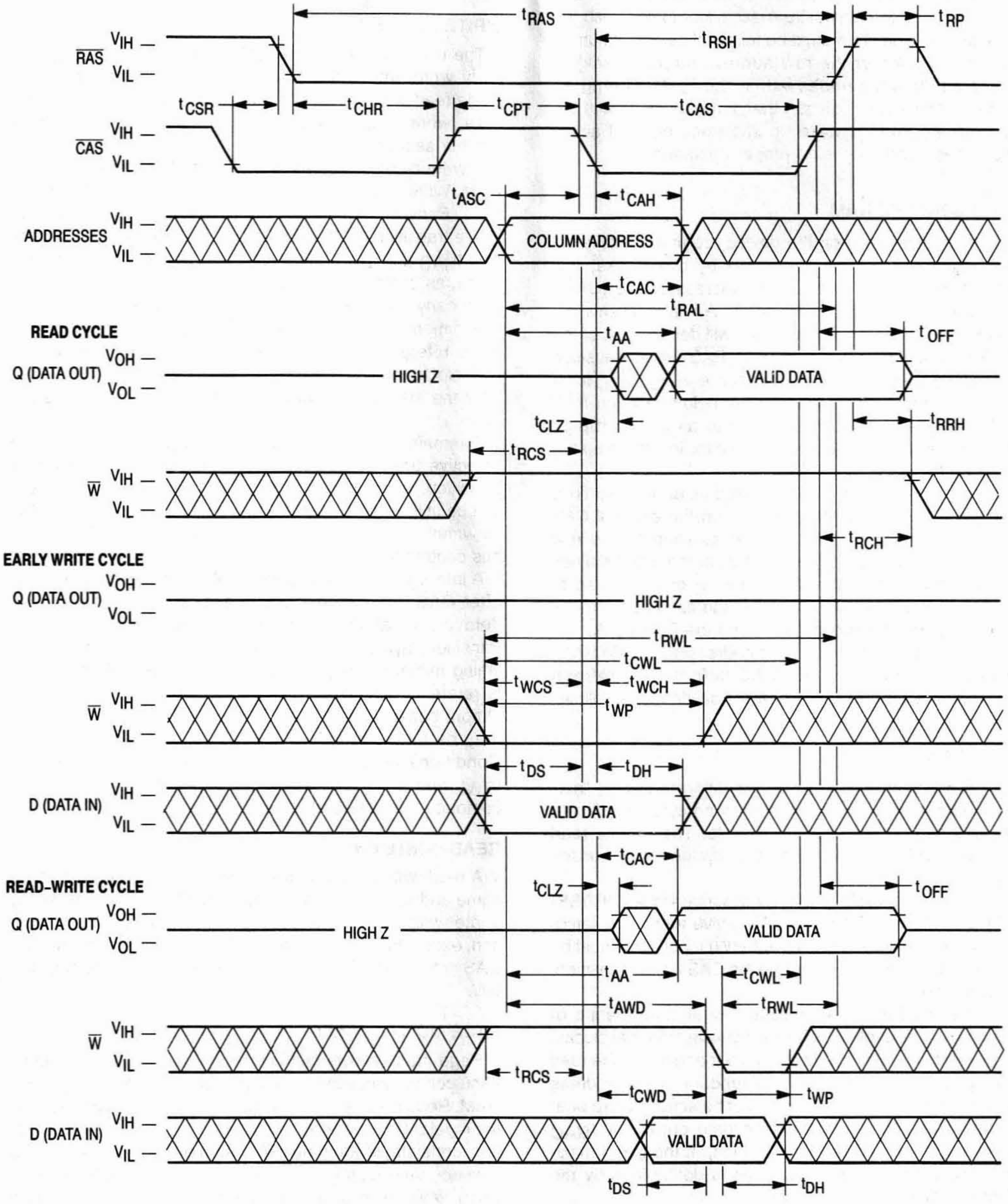
t_{RC}
t_{RAS}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CPN}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAD}
t_{RAL}
t_{AR}
t_{ASR}
t_{CAH}
t_{RAH}
t_{ASC}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RCS}
t_{RRH}
$\overline{W}$
V_{IH}
V_{IL}
t_{CAC}
t_{AA}
t_{RAC}
t_{OFF}
Q (DATA OUT)
V_{OH}
V_{OL}
VALID DATA
t_{CLZ}

HIDDEN REFRESH CYCLE (EARLY WRITE)



t_{RC}
t_{RAS}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CPN}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{AR}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{WCR}
t_{RWL}
t_{WCH}
t_{WCS}
$\overline{W}$
V_{IH}
V_{IL}
t_{WP}
t_{DS}
t_{DH}
D (DATA IN)
V_{IH}
V_{IL}
VALID DATA
t_{DHR}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



t_{RAS}
t_{RP}
t_{RSH}
$\overline{\text{RAS}}$ V_{IH} — V_{IL} —
t_{CSR}
t_{CHR}
t_{CPT}
t_{CAS}
$\overline{\text{CAS}}$ V_{IH} — V_{IL} —
t_{ASC}
t_{CAH}
ADDRESSES V_{IH} — V_{IL} —
COLUMN ADDRESS
t_{CAC}
t_{RAL}
READ CYCLE
t_{AA}
t_{OFF}
Q (DATA OUT) V_{OH} — V_{OL} —
HIGH Z
VALID DATA
t_{CLZ}
t_{RRH}
t_{RCS}
$\overline{\text{W}}$ V_{IH} — V_{IL} —
t_{RCH}
EARLY WRITE CYCLE
Q (DATA OUT) V_{OH} — V_{OL} —
HIGH Z
t_{RWL}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{\text{W}}$ V_{IH} — V_{IL} —
t_{DS}
t_{DH}
D (DATA IN) V_{IH} — V_{IL} —
VALID DATA
t_{CAC}
READ-WRITE CYCLE
t_{CLZ}
t_{OFF}
Q (DATA OUT) V_{OH} — V_{OL} —
HIGH Z
VALID DATA
t_{AA}
t_{CWL}
t_{AWD}
t_{RWL}
$\overline{\text{W}}$ V_{IH} — V_{IL} —
t_{RCS}
t_{CWD}
t_{WP}
D (DATA IN) V_{IH} — V_{IL} —
VALID DATA
t_{DS}
t_{DH}

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are two other variations in addressing the 1M RAM: **$\overline{\text{RAS}}$-only refresh cycle** and **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. However, $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ clock active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but Q may be indeterminate — see note 16 of AC Operating Conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the 1M dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum of t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM511000A require refresh every 8 milliseconds while refresh time for the MCM51L1000A is 64 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM511000A and 124.8 microseconds for the MCM51L1000A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM511000A and 64 milliseconds on the MCM51L1000A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other mehtods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **Hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

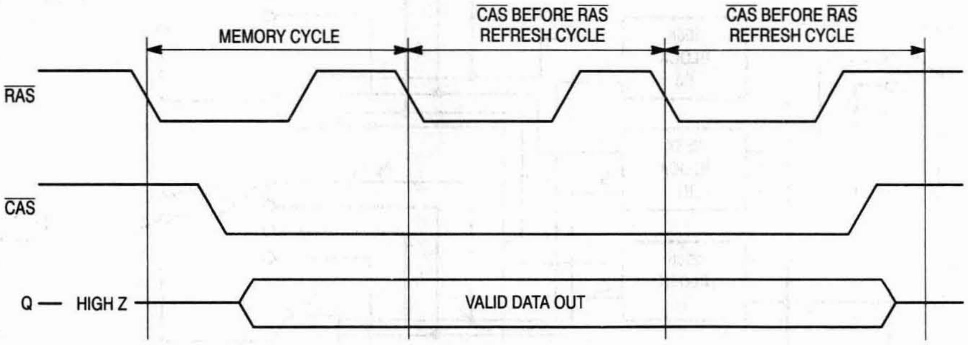


Figure 1. Hidden Refresh Cycle

TEST MODE

Internal organization of this device (256K x 4) allows it to be tested as if it were a 256K x 1 DRAM. Only nine of the ten addresses (A0 – A8) are used in test mode; A9 is internally disabled. A test mode write cycle writes data, D (data in), to a bit in each of the four 256K x 1 blocks (B0 – B3), in parallel. A test mode cycle reads a bit in each of the four blocks. If data is the same in all four bits, Q (data out) is the same as the data in each bit. If data is not the same in all four bits, Q is high Z. See truth table and test mode block diagram.

Test mode can be used in any timing cycle, including page mode cycles. The test mode function is enabled by holding the "TF" pin on "super voltage" for the specified period (t_{TES}, t_{TEHR}, t_{TEHC}; see **TEST MODE CYCLE**).

"Super voltage" = V_{CC} + 4.5 V

where

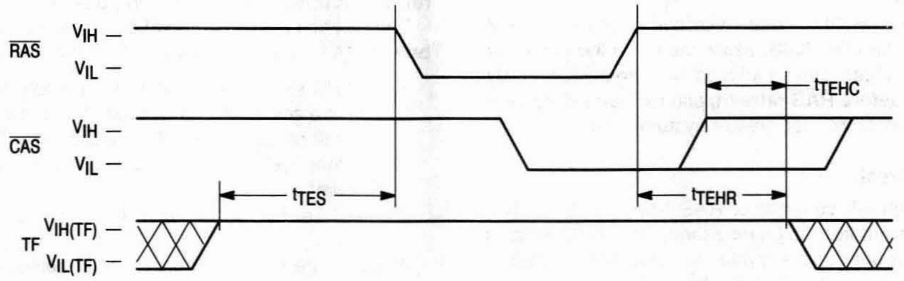
4.5 V < V_{CC} < 5.5 V and maximum voltage = 10.5 V.

A9 is ignored in test mode. In normal operation, the "TF" pin must either be connected to V_{IL}, or left open.

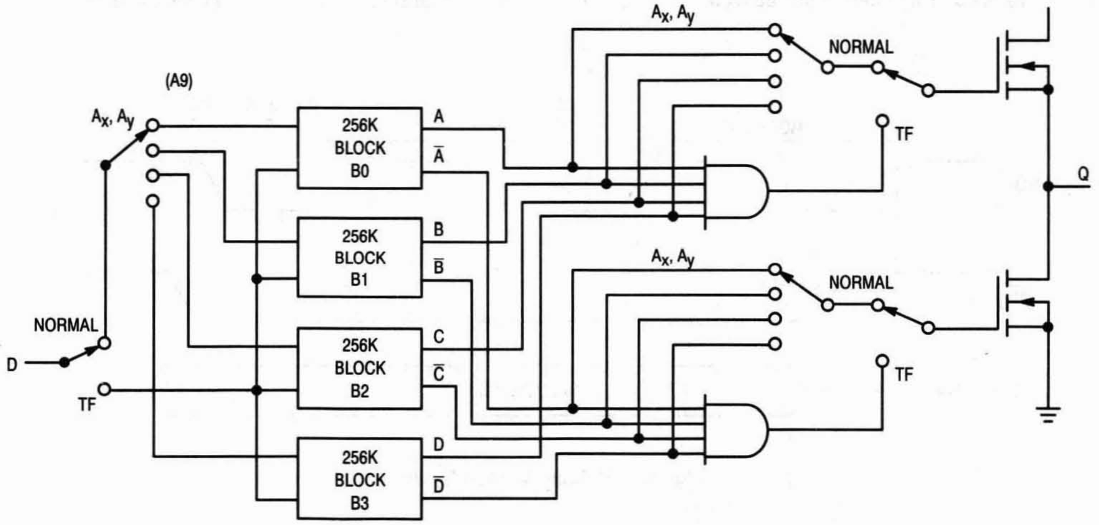
Test Mode Truth Table

D	B0	B1	B2	B3	Q
0	0	0	0	0	0
1	1	1	1	1	1
—	Any Other				High-Z

TEST MODE BLOCK DIAGRAM


$\overline{RAS}$
V_{IH} —
V_{IL} —
$\overline{CAS}$
V_{IH} —
V_{IL} —
t_{TES}
t_{TEHR}
t_{TEHC}
TF
$V_{IH(TF)}$ —
$V_{IL(TF)}$ —

TEST MODE BLOCK DIAGRAM


(A9)
A_x, A_y
NORMAL
D
TF
256K BLOCK B0
256K BLOCK B1
256K BLOCK B2
256K BLOCK B3
A
$\overline{A}$
B
$\overline{B}$
C
$\overline{C}$
D
$\overline{D}$
A_x, A_y
NORMAL
TF
A_x, A_y
NORMAL
TF
Q

ORDERING INFORMATION
(Order by Full Part Number)

MCM 511000A or 51L1000A X X XX XX

Motorola Memory Prefix — MCM

Part Number — 511000A or 51L1000A

Shipping Method (R2 = Tape and Reel, Blank = Rails)

Speed (70 = 70 ns, 80 = 80 ns)

Temperature (Blank = 0 to 70°C, C = – 40 to + 85°C)

Package (P = 300 mil Plastic DIP, J = 300 mil SOJ,
Z = Plastic ZIP)

Commercial Temperature Range 0 to 70°C

Full Part Numbers—	MCM511000AP70	MCM511000AJ70	MCM511000AJ70R2	MCM511000AZ70
	MCM511000AP80	MCM511000AJ80	MCM511000AJ80R2	MCM511000AZ80
	MCM51L1000AP70	MCM51L1000AJ70	MCM51L1000AJ70R2	MCM51L1000AZ70
	MCM51L1000AP80	MCM51L1000AJ80	MCM51L1000AJ80R2	MCM51L1000AZ80

Industrial Temperature Range – 40 to + 85°C

MCM511000APC70	MCM511000AJC70	MCM511000AJC70R2	MCM511000AZC70
MCM511000APC80	MCM511000AJC80	MCM511000AJC80R2	MCM511000AZC80
MCM51L1000APC70	MCM51L100AJC70	MCM51L100AJC70R2	MCM51L1000AZC70
MCM51L1000APC80	MCM51L100AJC80	MCM51L100AJC80R2	MCM51L1000AZC80

NOTE: Low Power Industrial Temperature SOJ device part numbers are one character shorter than corresponding PDIP or ZIP part numbers.

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

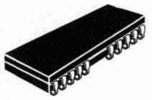
MCM511000B
MCM51L1000B

1M x 1 CMOS Dynamic RAM
Page Mode

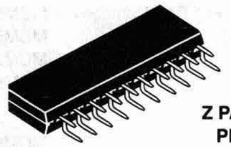
The MCM511000B is a 0.8µ CMOS high-speed dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM511000B requires only ten address lines; row and column address inputs are multiplexed. The device is packaged in a 300 mil SOJ plastic package, and a 100 mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Common I/O with Early Write
- Fast Page Mode
- Test Mode
- TTL-Compatible Inputs and Output
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh: MCM511000B = 8 ms
  MCM51L1000B = 64 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM511000B-60 and MCM51L1000B-60 = 60 ns (Max)
- Low Active Power Dissipation:
  MCM511000B-60 and MCM51L1000B-60 = 495 mW (Max)
- Low Standby Power Dissipation:
  MCM511000B and MCM51L1000B = 11 mW (Max, TTL Levels)
  MCM511000B = 5.5 mW (Max, CMOS Levels)
  MCM51L1000B = 1.1 mW (Max, CMOS Levels)



N PACKAGE
300 MIL SOJ
CASE 822-03

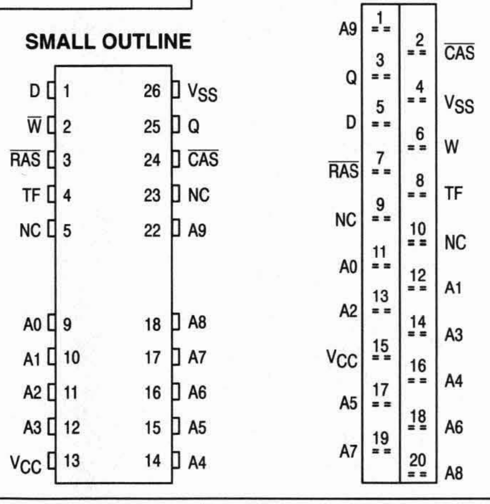


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836-02

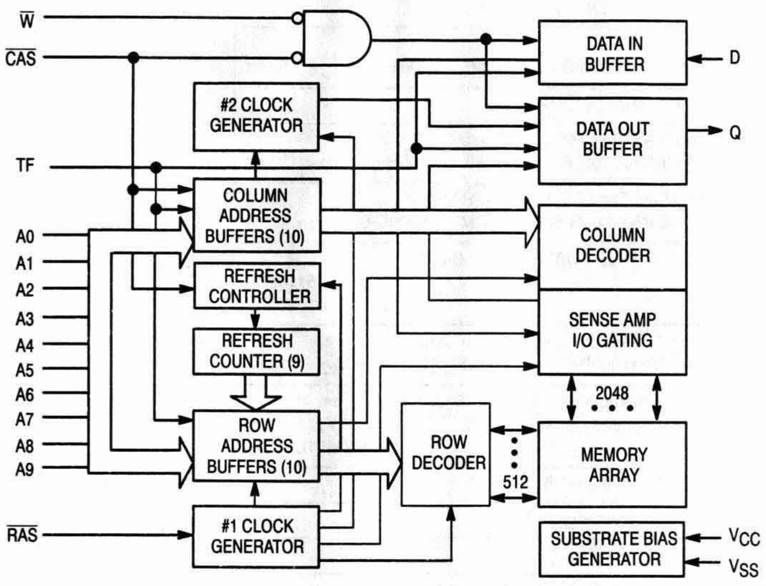
PIN NAMES

A0 – A9	Address Input
D	Data Input
Q	Data Output
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
TF	Test Function Enable
NC	No Connection

PIN ASSIGNMENTS


ZIG-ZAG IN-LINE
SMALL OUTLINE
D 1
W̄ 2
RAS̄ 3
TF 4
NC 5
A0 9
A1 10
A2 11
A3 12
VCC 13
26 VSS
25 Q
24 CAS̄
23 NC
22 A9
18 A8
17 A7
16 A6
15 A5
14 A4
A9 1
2 CAS̄
Q 3
4 VSS
D 5
6 W
RAS̄ 7
8 TF
NC 9
10 NC
A0 11
12 A1
A2 13
14 A3
VCC 15
16 A4
A5 17
18 A6
A7 19
20 A8

BLOCK DIAGRAM


W̄
CAS̄
TF
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
RAS̄
#2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (10)
REFRESH CONTROLLER
REFRESH COUNTER (9)
ROW ADDRESS BUFFERS (10)
#1 CLOCK GENERATOR
ROW DECODER
512
DATA IN BUFFER
D
DATA OUT BUFFER
Q
COLUMN DECODER
SENSE AMP I/O GATING
2048
MEMORY ARRAY
SUBSTRATE BIAS GENERATOR
V_{CC}
V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Test Function Input Voltage	$V_{in\ (TF)}$	– 1 to + 10.5	V
Data Output Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V
Test Function Input High Voltage	$V_{IH\ (TF)}$	V_{CC} + 4.5	—	10.5	V
Test Function Input Low Voltage	$V_{IL\ (TF)}$	–1.0	—	V_{CC} + 1.0	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM511000B-60 and MCM51L1000B-60, t_{RC} = 110 ns	I_{CC1}	—	90	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}	—	2	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles ($\overline{CAS} = V_{IH}$) MCM511000B-60 and MCM51L1000B-60, t_{RC} = 110 ns	I_{CC3}	—	90	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS} = V_{IL}$) MCM511000B-60 and MCM51L1000B-60, t_{PC} = 40 ns	I_{CC4}	—	60	mA	2, 3
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V) MCM511000B MCM51L1000B	I_{CC5}	— —	1.0 200	mA µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM511000B-60 and MCM51L1000B-60, t_{RC} = 110 ns	I_{CC6}	—	90	mA	2
V_{CC} Power Supply Current, Battery Backup Mode (t_{RC} = 125 µs, t_{RAS} = 1 µs, $\overline{CAS} = \overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V, A0 – A9, $\overline{W}$, D = $V_{CC} - 0.2$ V or 0.2 V) MCM51L1000B	I_{CC7}	—	300	µA	2
Input Leakage Current (Except TF) (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	– 10	10	µA	
Input Leakage Current (TF) (0 V ≤ V_{in} (TF) ≤ V_{CC} + 0.5 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current ($\overline{CAS} = V_{IH}$, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	– 10	10	µA	
Test Function Input Current (V_{CC} + 4.5 V ≤ V_{in} (TF) ≤ V_{CC} ≤ 10.5 V)	$I_{in\ (TF)}$	—	1	mA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	D, A0 – A9	C_{in}	5	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, TF		7	
I/O Capacitance ($\overline{CAS} = V_{IH}$ to Disable Output)	Q	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511000B-60 MCM51L1000B-60		Unit	Notes
	Std	Alt	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	135	—	ns	6
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	ns	
Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	65	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	60	ns	7, 8
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	ns	7, 10
Access Time from $\overline{\text{CAS}}$ Precharge	t_{CEHQV}	t_{CPA}	—	35	ns	7
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge (Page Mode Cycle Only)	t_{CELREH}	t_{RHCP}	35	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	ns	12
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	ns	13
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
7. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \le t_{RCD}$ (max).
9. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
10. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

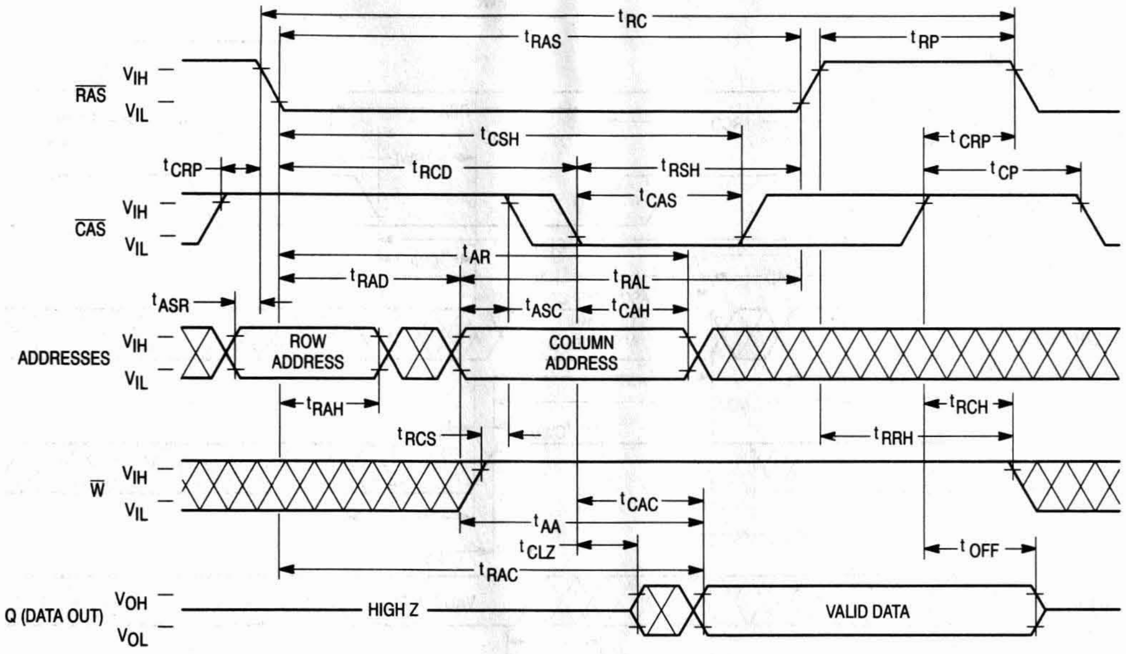
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM511000B-60 MCM51L1000B-60		Unit	Notes
	Std	Alt	Min	Max		
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELAX}	t_{AR}	50	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	ns	14
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	ns	14
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELWH}	t_{WCR}	45	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	ns	15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	ns	15
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	50	—	ns	
Refresh Period MCM511000B MCM51L1000B	t_{RVRV}	t_{RFSH}	— —	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	ns	16
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	20	—	ns	16
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	60	—	ns	16
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	30	—	ns	16
$\overline{\text{CAS}}$ Precharge to Write Delay Time	t_{CEHWL}	t_{CPWD}	35	—	ns	16
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	30	—	ns	
Test Mode Enable Setup Time Referenced to $\overline{\text{RAS}}$	t_{TEHREL}	t_{TES}	0	—	ns	
Test Mode Enable Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHTEL}	t_{TEHR}	0	—	ns	
Test Mode Enable Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHTEL}	t_{TEHC}	0	—	ns	

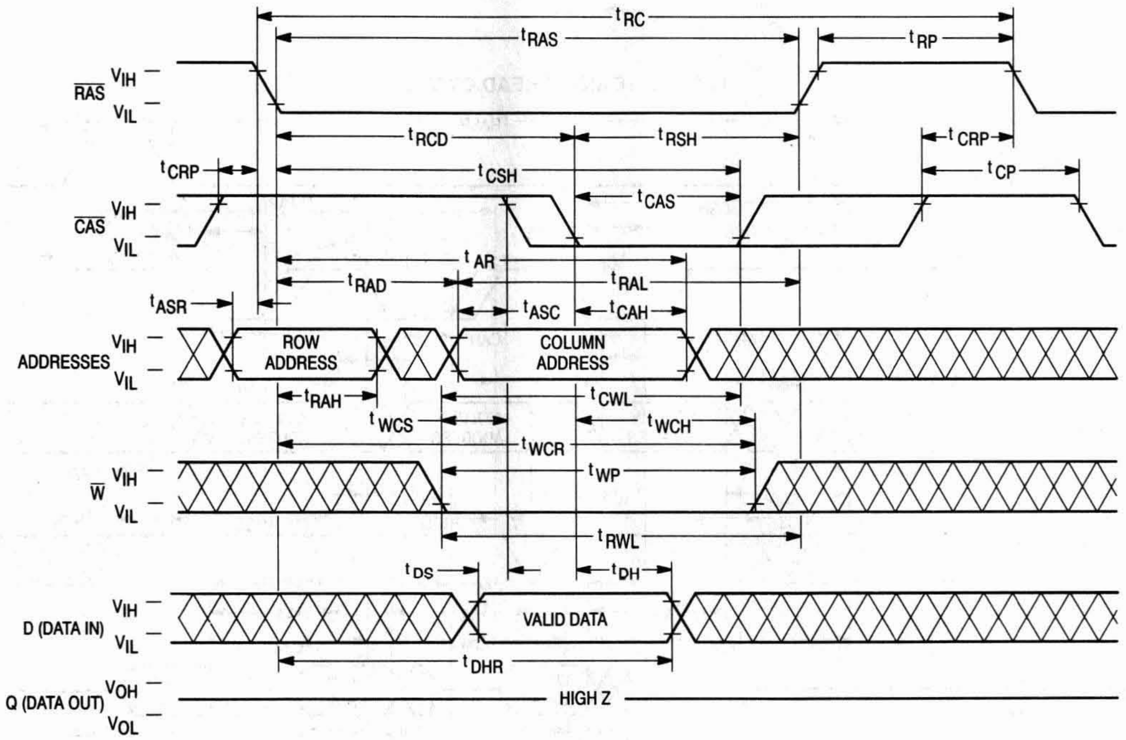
NOTES:

14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in delayed write or read-write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

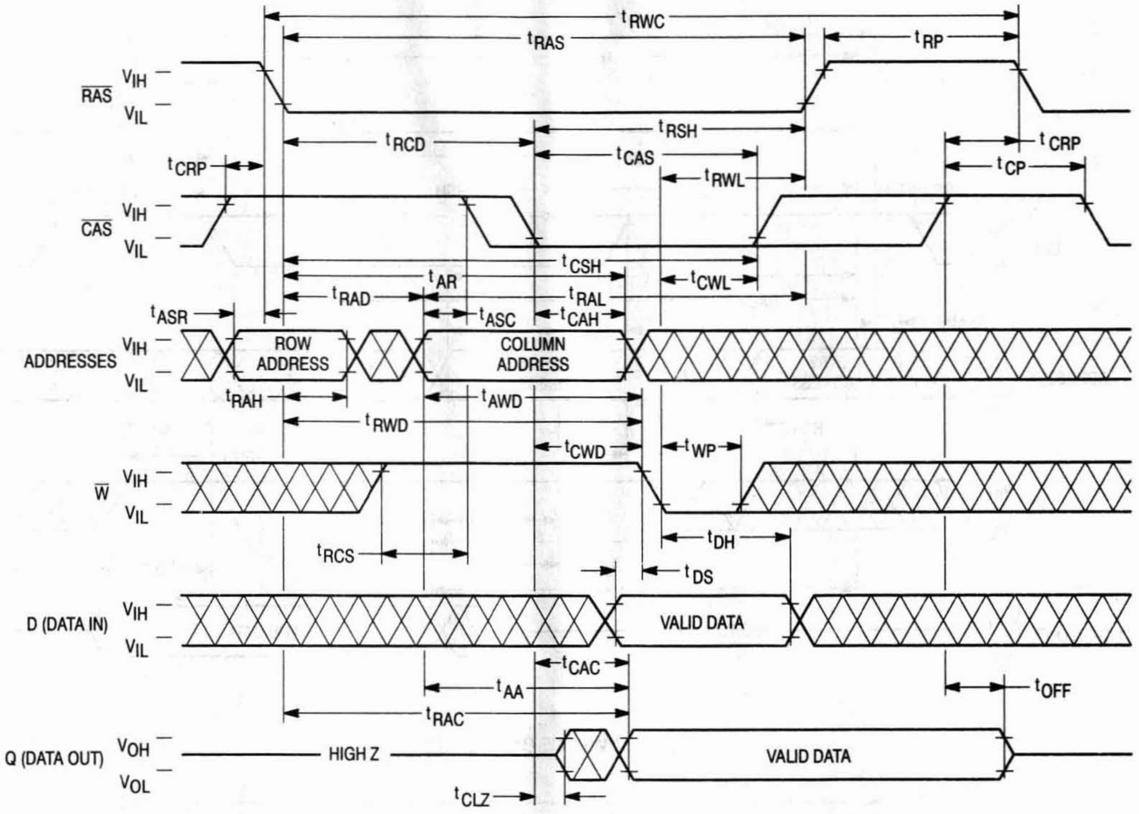
READ CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tCRP
tRCD
tRSH
tCP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W
VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
Q (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA

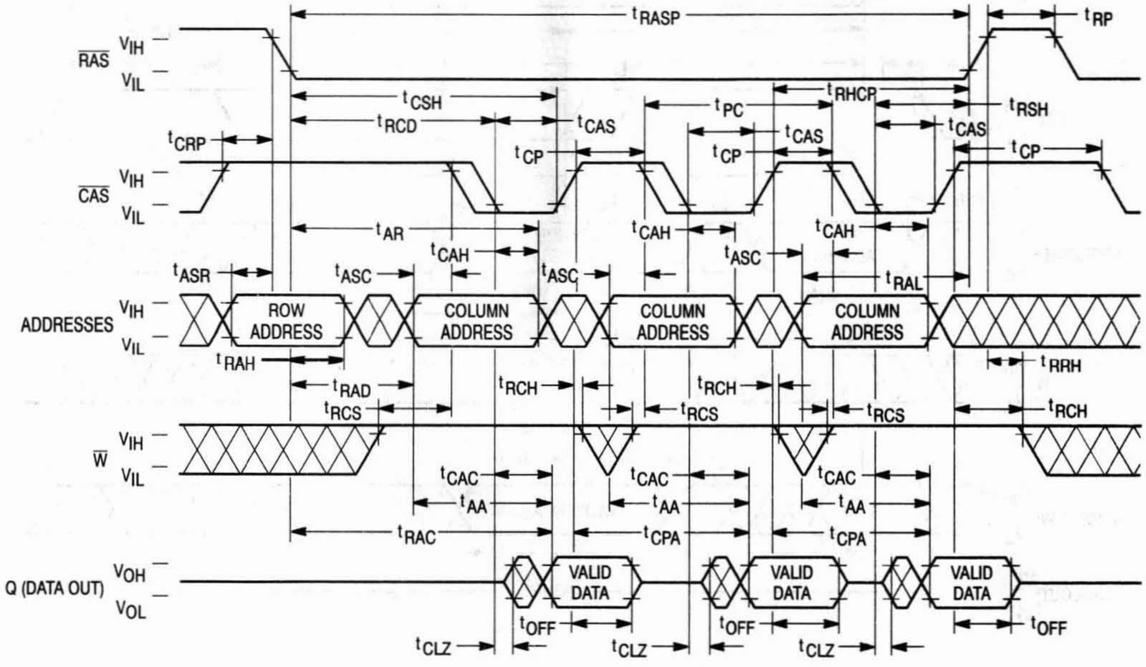
EARLY WRITE CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tRCD
tRSH
tCRP
tCRP
tCSH
tCP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWCR
tWP
W
VIH
VIL
tRWL
tDS
tDH
D (DATA IN)
VIH
VIL
VALID DATA
tDHR
Q (DATA OUT)
VOH
VOL
HIGH Z

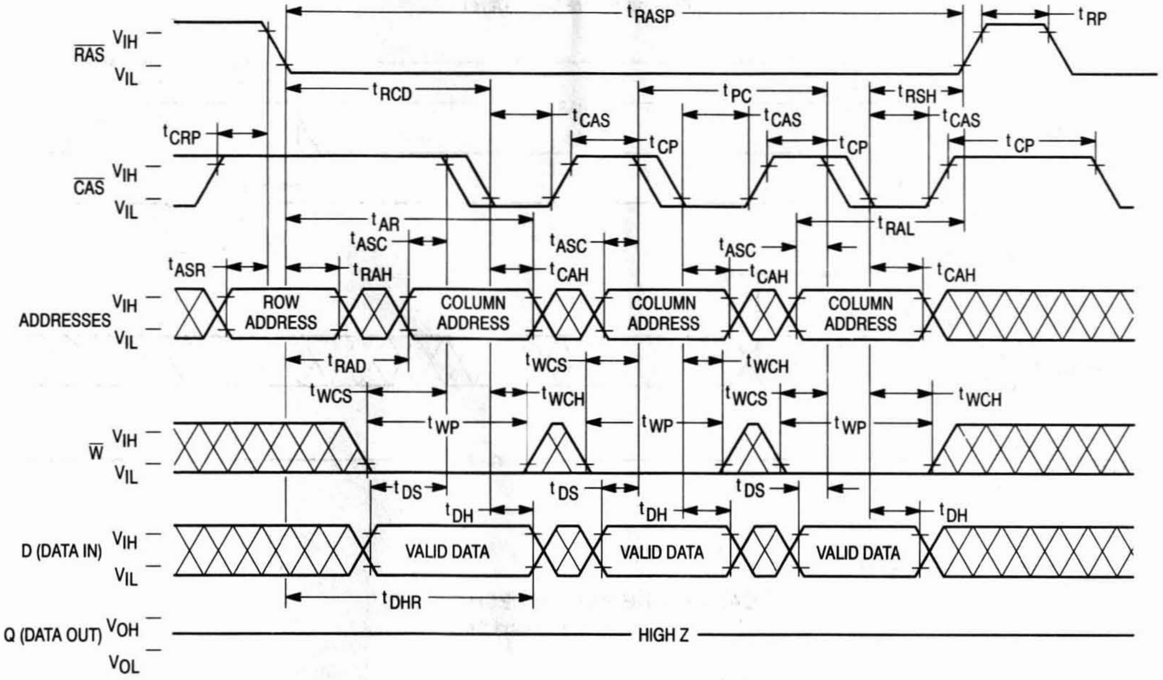
READ-WRITE CYCLE


t_{RWC}
t_{RAS}
t_{RP}
RAS
V_{IH}
V_{IL}
t_{RCD}
t_{RSH}
t_{CAS}
t_{RWL}
t_{CRP}
t_{CP}
CAS
t_{CSH}
t_{AR}
t_{CWL}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{RAH}
t_{AWD}
t_{RWD}
t_{CWD}
t_{WP}
W
t_{DH}
t_{RCS}
t_{DS}
D (DATA IN)
VALID DATA
t_{CAC}
t_{AA}
t_{OFF}
t_{RAC}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z
VALID DATA
t_{CLZ}

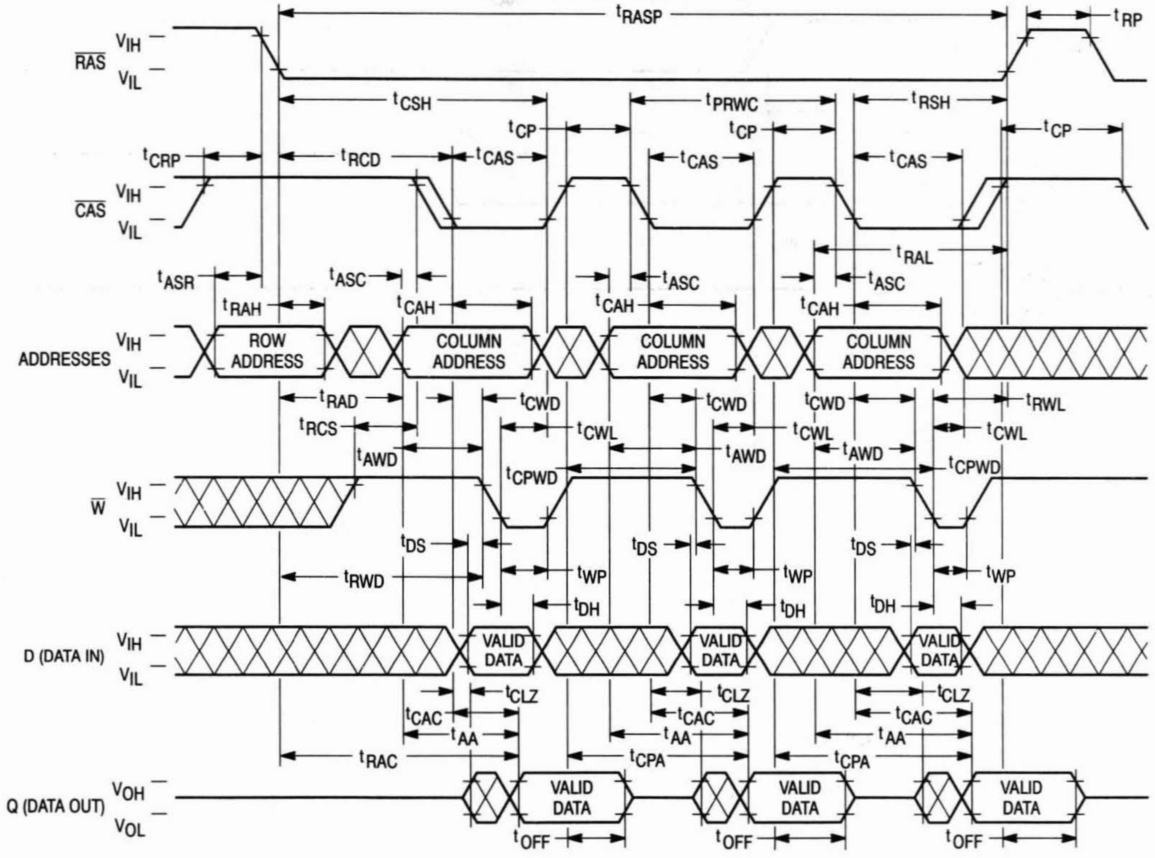
FAST PAGE MODE READ CYCLE


t_{RASP}
t_{RP}
RAS
V_{IH}
V_{IL}
t_{CSH}
t_{RHCP}
t_{RSH}
t_{PC}
t_{RCD}
t_{CAS}
t_{CAS}
t_{CAS}
t_{CRP}
t_{CP}
t_{CP}
t_{CP}
CAS
t_{AR}
t_{CAH}
t_{CAH}
t_{CAH}
t_{ASC}
t_{ASC}
t_{ASC}
t_{ASR}
t_{RAL}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
t_{RAH}
t_{RRH}
t_{RAD}
t_{RCH}
t_{RCH}
t_{RCH}
t_{RCS}
t_{RCS}
t_{RCS}
W
t_{CAC}
t_{CAC}
t_{CAC}
t_{AA}
t_{AA}
t_{AA}
t_{RAC}
t_{CPA}
t_{CPA}
Q (DATA OUT)
V_{OH}
V_{OL}
VALID DATA
VALID DATA
VALID DATA
t_{OFF}
t_{OFF}
t_{OFF}
t_{CLZ}
t_{CLZ}
t_{CLZ}

FAST PAGE MODE EARLY WRITE CYCLE

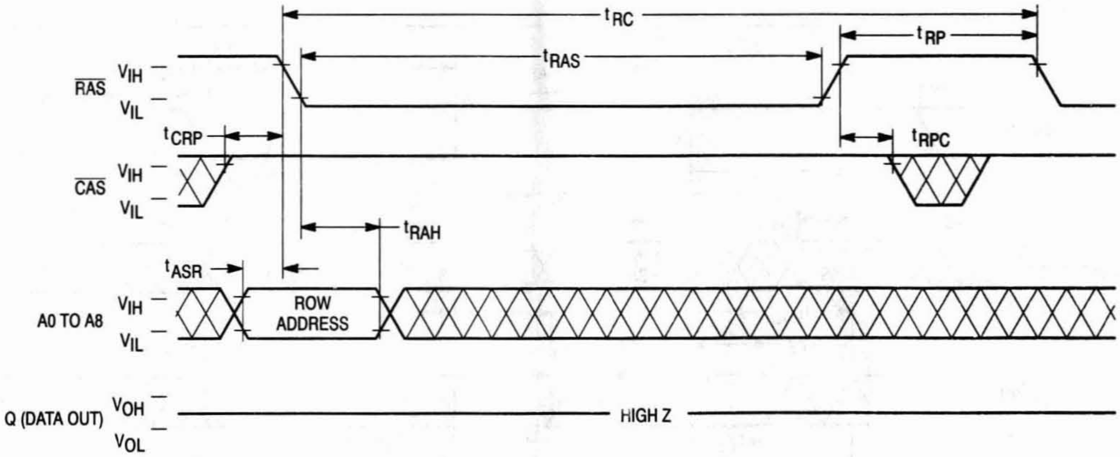

RAS
CAS
ADDRESSES
W
D (DATA IN)
Q (DATA OUT)
VIH
VIL
VOH
VOL
tRASP
tRP
tRCD
tPC
tRSH
tCAS
tCRP
tCP
tAR
tRAL
tASR
tASC
tRAH
tCAH
ROW ADDRESS
COLUMN ADDRESS
tRAD
tWCS
tWCH
tWP
tDS
tDH
VALID DATA
tDHR
HIGH Z

FAST PAGE MODE READ-WRITE CYCLE


RAS
CAS
ADDRESSES
W
D (DATA IN)
Q (DATA OUT)
VIH
VIL
VOH
VOL
tRASP
tRP
tCSH
tPRWC
tRSH
tCP
tCRP
tRCD
tCAS
tRAL
tASR
tASC
tRAH
tCAH
ROW ADDRESS
COLUMN ADDRESS
tRAD
tCWD
tRWL
tRCS
tCWL
tAWD
tCPWD
tDS
tRWD
tWP
tDH
VALID DATA
tCLZ
tCAC
tAA
tRAC
tCPA
tOFF

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

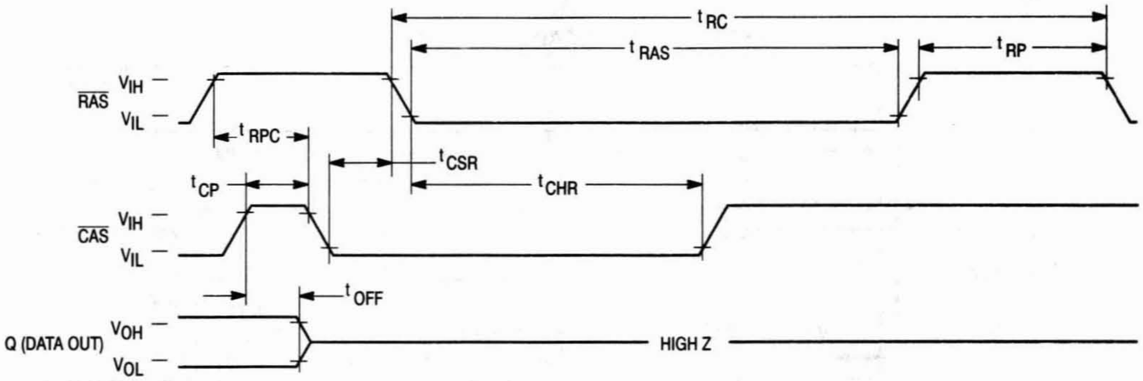
($\overline{\text{W}}$ and A9 are Don't Care)



t RC
t RAS
t RP
RAS
VIH
VIL
t CRP
t RPC
CAS
VIH
VIL
t RAH
t ASR
A0 TO A8
VIH
VIL
ROW ADDRESS
Q (DATA OUT)
VOH
VOL
HIGH Z

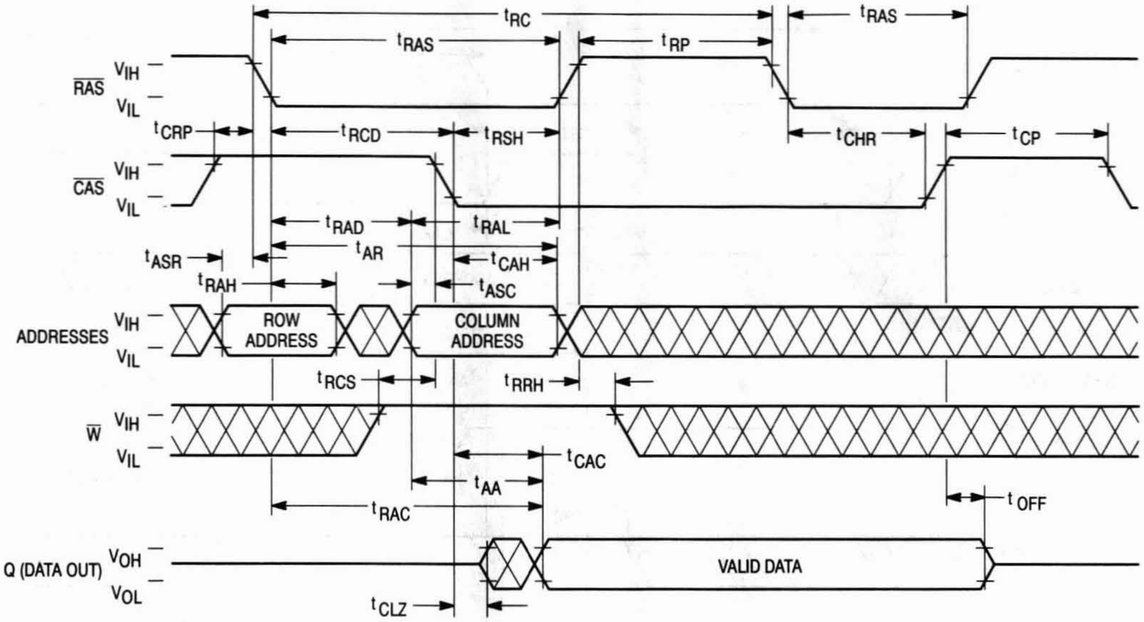
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{W}}$ and A0 – A9 are Don't Care)

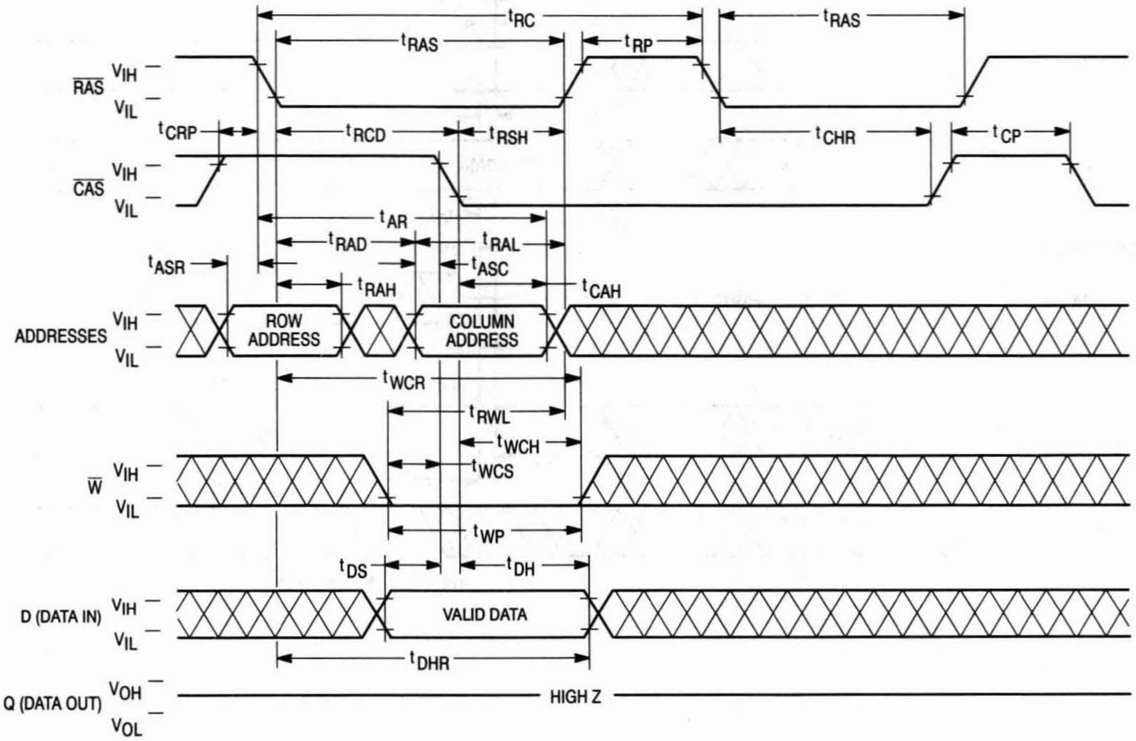


t RC
t RAS
t RP
RAS
VIH
VIL
t RPC
t CSR
t CHR
t CP
CAS
VIH
VIL
t OFF
Q (DATA OUT)
VOH
VOL
HIGH Z

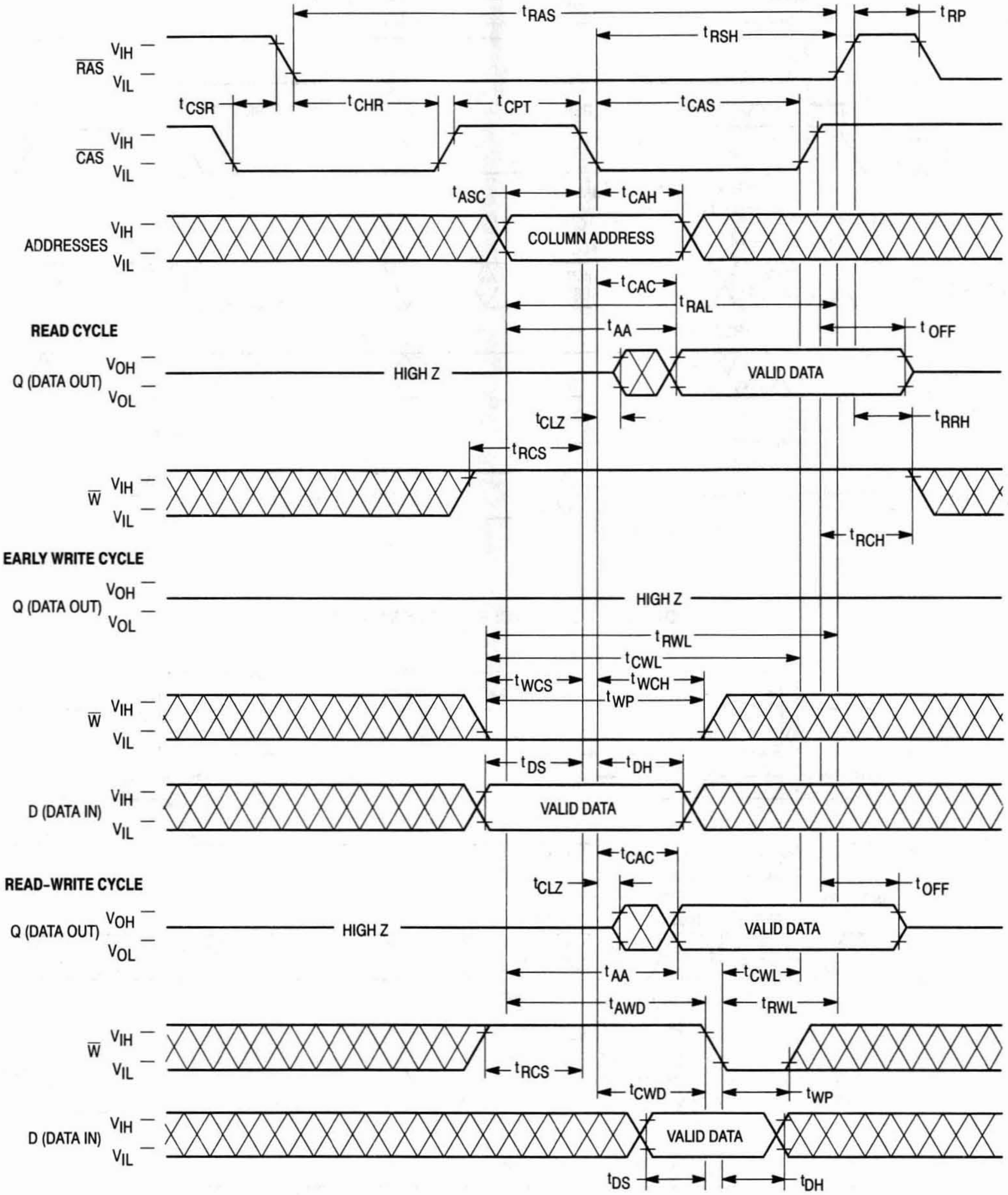
HIDDEN REFRESH CYCLE (READ)


t_{RC}
t_{RAS}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CP}
$\overline{CAS}$
t_{RAD}
t_{RAL}
t_{AR}
t_{ASR}
t_{CAH}
t_{RAH}
t_{ASC}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{RCS}
t_{RRH}
$\overline{W}$
t_{CAC}
t_{AA}
t_{RAC}
t_{OFF}
Q (DATA OUT)
V_{OH}
V_{OL}
VALID DATA
t_{CLZ}

HIDDEN REFRESH CYCLE (EARLY WRITE)


t_{RC}
t_{RAS}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CP}
$\overline{CAS}$
t_{AR}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{WCR}
t_{RWL}
t_{WCH}
t_{WCS}
$\overline{W}$
t_{WP}
t_{DS}
t_{DH}
D (DATA IN)
VALID DATA
t_{DHR}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



tRAS
tRP
tRSH
RAS VIH VIL
tCSR
tCHR
tCPT
tCAS
CAS VIH VIL
tASC
tCAH
ADDRESSES VIH VIL
COLUMN ADDRESS
tCAC
tRAL
tAA
tOFF
READ CYCLE
Q (DATA OUT) VOH VOL
HIGH Z
VALID DATA
tCLZ
tRRH
tRCS
W VIH VIL
tRCH
EARLY WRITE CYCLE
Q (DATA OUT) VOH VOL
HIGH Z
tRWL
tCWL
tWCS
tWCH
tWP
W VIH VIL
tDS
tDH
D (DATA IN) VIH VIL
VALID DATA
READ-WRITE CYCLE
tCAC
tCLZ
tOFF
Q (DATA OUT) VOH VOL
HIGH Z
VALID DATA
tAA
tCWL
tAWD
tRWL
W VIH VIL
tRCS
tCWD
tWP
D (DATA IN) VIH VIL
VALID DATA
tDS
tDH

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are two other variations in addressing the 1M RAM: **$\overline{\text{RAS}}$-only refresh cycle** and **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. However, $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ clock active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \le t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but Q may be indeterminate — see note 16 of AC Operating Conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the 1M dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum of t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM511000B require refresh every 8 milliseconds while refresh time for the MCM51L1000B is 64 milliseconds..

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM511000B and 124.8 microseconds for the MCM51L1000B. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM511000B and 64 milliseconds on the MCM51L1000B.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other mehtods of refresh, **RAS-only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order actives an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1).

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **eight CAS before RAS** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 512 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

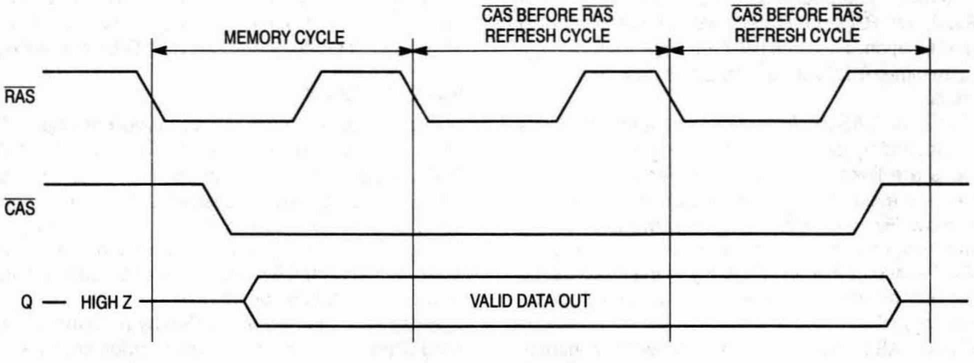


Figure 1. Hidden Refresh Cycle

TEST MODE

Internal organization of this device (256K x 4) allows it to be tested as if it were a 256K x 1 DRAM. Only nine of the ten addresses (A0 – A8) are used in test mode; A9 is internally disabled. A test mode write cycle writes data, D (data in), to a bit in each of the four 256K x 1 blocks (B0 – B3), in parallel. A test mode cycle reads a bit in each of the four blocks. If data is the same in all four bits, Q (data out) is the same as the data in each bit. If data is not the same in all four bits, Q is high Z. See truth table and test mode block diagram.

Test mode can be used in any timing cycle, including page mode cycles. The test mode function is enabled by holding the "TF" pin on "super voltage" for the specified period (t_{TES}, t_{TEHR}, t_{TEHC}; see **TEST MODE CYCLE**).

"Super voltage" = V_{CC} + 4.5 V

where

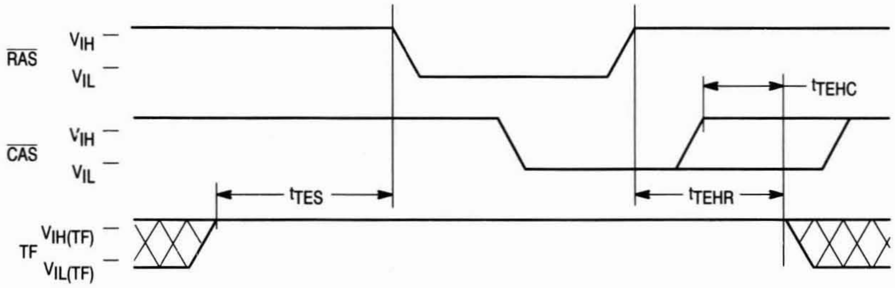
4.5 V < V_{CC} < 5.5 V and maximum voltage = 10.5 V.

A9 is ignored in test mode. In normal operation, the "TF" pin must either be connected to V_{IL}, or left open.

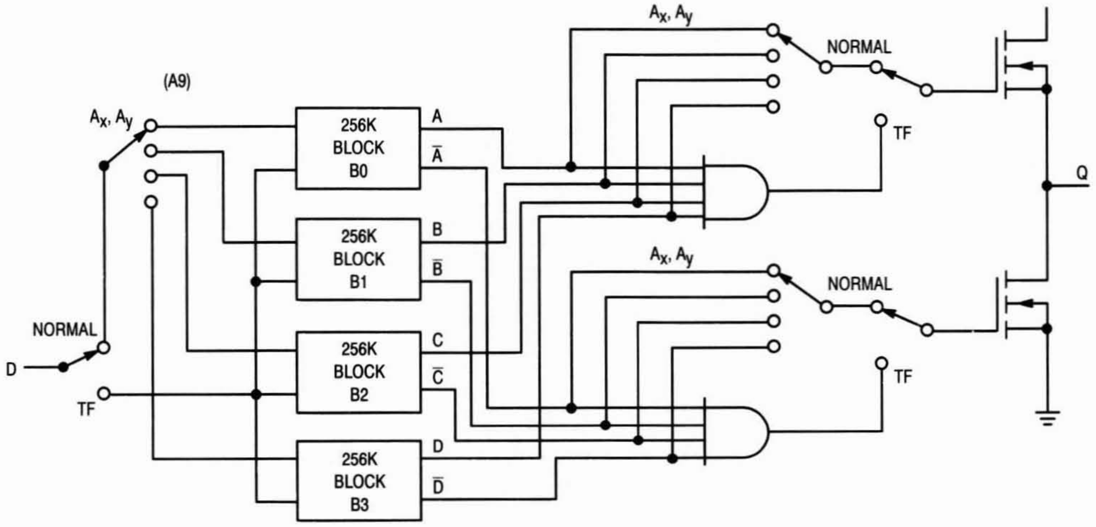
TEST MODE TRUTH TABLE

D	B0	B1	B2	B3	Q
0	0	0	0	0	0
1	1	1	1	1	1
—	Any Other				High-Z

TEST MODE BLOCK DIAGRAM


RAS
V_{IH}
V_{IL}
t_{TEHC}
CAS
V_{IH}
V_{IL}
t_{TES}
t_{TEHR}
TF
$V_{IH(TF)}$
$V_{IL(TF)}$

TEST MODE BLOCK DIAGRAM


A_x, A_y
NORMAL
(A9)
A_x, A_y
256K BLOCK B0
A
$\overline{A}$
TF
Q
256K BLOCK B1
B
$\overline{B}$
A_x, A_y
NORMAL
NORMAL
D
256K BLOCK B2
C
$\overline{C}$
TF
TF
256K BLOCK B3
D
$\overline{D}$

ORDERING INFORMATION
(Order by Full Part Number)

MCM 511000B or 51L1000B X X XX XX

Motorola Memory Prefix — MCM
Part Number — 511000B or 51L1000B
Package (J = 300 mil SOJ, Z = Plastic ZIP)
Temperature (Blank = 0 to 70°C)
Speed (60 = 60 ns)
Shipping Method (R2 = Tape and Reel, Blank = Rails)

Commercial Temperature Range 0 to 70°C

Full Part Numbers— MCM511000BJ60 MCM511000BJ60R2 MCM511000BZ60
MCM51L1000BJ60 MCM51L1000BJ60R2 MCM51L1000BZ60

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM511001A

1M × 1 CMOS Dynamic RAM

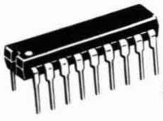
Nibble Mode

The MCM511001A is a 1.0μ CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The fast nibble mode feature allows high-speed serial access of up to 4 bits of data.

The MCM511001A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line plastic package (DIP), a 300-mil SOJ plastic package, and a 100-mil zig-zag in-line plastic package (ZIP).

- Three-State Data Output
- Common I/O with Early Write
- Fast Nibble Mode
- Test Mode
- TTL-Compatible Inputs and Output
- $\overline{\text{RAS}}$ Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM511001A-70 = 70 ns (Maximum)
  MCM511001A-80 = 80 ns (Maximum)
  MCM511001A-10 = 100 ns (Maximum)
- Low Active Power Dissipation: MCM511001A-70 = 440 mW (Maximum)
  MCM511001A-80 = 385 mW (Maximum)
  MCM511001A-10 = 330 mW (Maximum)
- Low Standby Power Dissipation: 11 mW (Maximum, TTL Levels)
  5.5 mW (Maximum, CMOS Levels)

NOT RECOMMENDED FOR NEW DESIGNS



P PACKAGE
300 MIL PLASTIC
CASE 707A

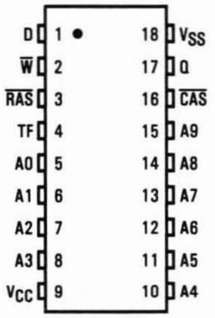
J PACKAGE
300 MIL SOJ
CASE 822

Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

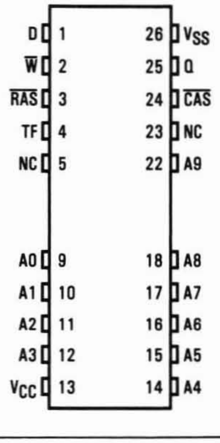
PIN NAMES	
A0-A9	Address Input
D	Data Input
Q	Data Output
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
TF	Test Function Enable
NC	No Connection

PIN ASSIGNMENT

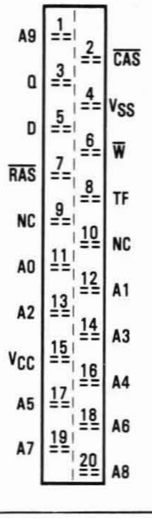
DUAL-IN-LINE


D 1
W̄ 2
RAS̄ 3
TF 4
A0 5
A1 6
A2 7
A3 8
VCC 9
18 VSS
17 Q
16 CAS̄
15 A9
14 A8
13 A7
12 A6
11 A5
10 A4

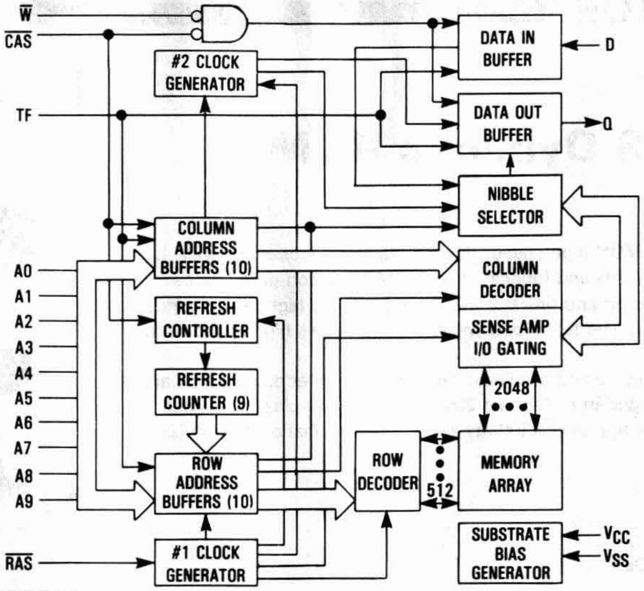
SMALL OUTLINE


D 1
W̄ 2
RAS̄ 3
TF 4
NC 5
A0 9
A1 10
A2 11
A3 12
VCC 13
26 VSS
25 Q
24 CAS̄
23 NC
22 A9
18 A8
17 A7
16 A6
15 A5
14 A4

ZIG-ZAG IN-LINE


A9 1
2 CAS̄
Q 3
4 VSS
D 5
6 W̄
RAS̄ 7
8 TF
NC 9
10 NC
A0 11
12 A1
A2 13
14 A3
VCC 15
16 A4
A5 17
18 A6
A7 19
20 A8

BLOCK DIAGRAM


$\overline{W}$
$\overline{CAS}$
TF
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
$\overline{RAS}$
#2 CLOCK GENERATOR
DATA IN BUFFER
D
DATA OUT BUFFER
Q
NIBBLE SELECTOR
COLUMN ADDRESS BUFFERS (10)
COLUMN DECODER
REFRESH CONTROLLER
SENSE AMP I/O GATING
REFRESH COUNTER (9)
2048
ROW ADDRESS BUFFERS (10)
ROW DECODER
512
MEMORY ARRAY
#1 CLOCK GENERATOR
SUBSTRATE BIAS GENERATOR
V_{CC}
V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Test Function Input Voltage	$V_{in(TF)}$	−1 to +10.5	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}=5.0$ V ±10%, $T_A=0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1
Test Function Input High Voltage	$V_{IH\ (TF)}$	$V_{CC}+4.5$	–	10.5	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM511001A-70, $t_{RC}=130$ ns		–	80		
MCM511001A-80, $t_{RC}=150$ ns		–	70		
MCM511001A-10, $t_{RC}=180$ ns		–	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}=\overline{CAS}=V_{IH}$)	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS}=V_{IH}$)	I_{CC3}			mA	2
MCM511001A-70, $t_{RC}=130$ ns		–	80		
MCM511001A-80, $t_{RC}=150$ ns		–	70		
MCM511001A-10, $t_{RC}=180$ ns		–	60		
V_{CC} Power Supply Current During Nibble Mode Cycle ($\overline{RAS}=V_{IL}$)	I_{CC4}			mA	2
MCM511001A-70, $t_{NC}=35$ ns		–	60		
MCM511001A-80, $t_{NC}=35$ ns		–	50		
MCM511001A-10, $t_{NC}=40$ ns		–	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}=\overline{CAS}=V_{CC}-0.2$ V)	I_{CC5}	–	1.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM511001A-70, $t_{RC}=130$ ns		–	80		
MCM511001A-80, $t_{RC}=150$ ns		–	70		
MCM511001A-10, $t_{RC}=180$ ns		–	60		
Input Leakage Current (Except TF) (0 V $\le V_{in} \le$ 6.5 V)	$I_{lkg(I)}$	−10	10	µA	
Input Leakage Current (TF) (0 V $\le V_{in(TF)} \le V_{CC}+0.5$ V)	$I_{lkg(I)}$	−10	10	µA	
Output Leakage Current ($\overline{CAS}=V_{IH}$, 0 V $\le V_{out} \le$ 5.5 V)	$I_{lkg(O)}$	−10	10	µA	
Test Function Input Current ($V_{CC}+4.5$ V $\le V_{in(TF)} \le$ 10.5 V)	$I_{in(TF)}$	–	1	mA	
Output High Voltage ($I_{OH}=-5$ mA)	V_{OH}	2.4	–	V	
Output Low Voltage ($I_{OL}=4.2$ mA)	V_{OL}	–	0.4	V	

CAPACITANCE ($f=1.0$ MHz, $T_A=25$°C, $V_{CC}=5$ V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9, D	C_{in}	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, TF		7	pF	3
Output Capacitance ($\overline{CAS}=V_{IH}$ to Disable Output)	Q	C_{out}	7	pF	3

NOTES:

1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C=I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}=5.0$ V ±10%, $T_A=0$ to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511001A-70		MCM511001A-80		MCM511001A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	180	—	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	155	—	175	—	210	—	ns	6
Nibble Mode Cycle Time	t_{CEHCEH}	t_{NC}	35	—	35	—	40	—	ns	
Nibble Mode Read-Write Cycle Time	t_{CEHCEH}	t_{NRMW}	55	—	55	—	65	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	70	—	80	—	100	ns	7, 8
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	25	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	50	ns	7, 10
Nibble Mode Access Time	t_{CELQV}	t_{NCAC}	—	15	—	15	—	20	ns	7
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	13
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	—	60	—	75	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	50	—	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements $t_T=5.0$ ns.
5. The TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at $V_{OH}=2.0$ V and $V_{OL}=0.8$ V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

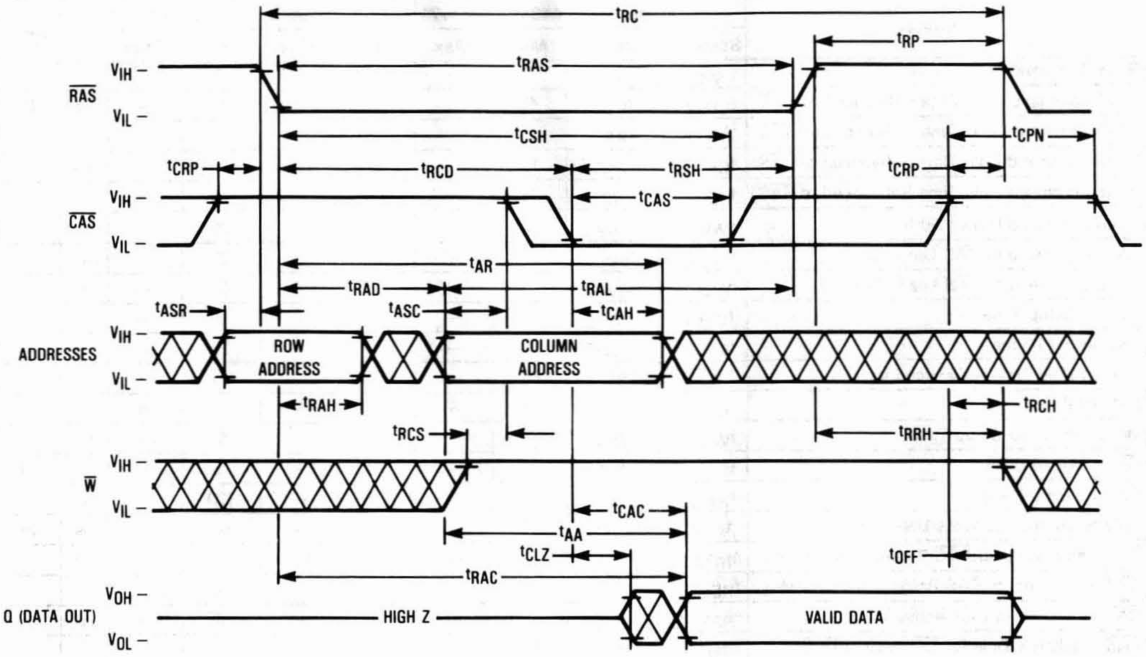
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM511001A-70		MCM511001A-80		MCM511001A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	14
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	14
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELWH}	t_{WCR}	55	—	60	—	75	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	15
Data In Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	20	—	ns	15
Data In Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	55	—	60	—	75	—	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	—	8	—	8	—	8	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	16
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	20	—	20	—	25	—	ns	16
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	70	—	80	—	100	—	ns	16
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	35	—	40	—	50	—	ns	16
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	30	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	50	—	ns	
Nibble Mode Pulse Width	t_{CELCEH}	t_{NCAS}	15	—	15	—	20	—	ns	
Nibble Mode $\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{NCP}	10	—	10	—	10	—	ns	
Nibble Mode $\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{NRSH}	15	—	15	—	20	—	ns	
Nibble Mode $\overline{\text{CAS}}$ to Write Delay Time	t_{CELWL}	t_{NCWD}	15	—	15	—	20	—	ns	
Nibble Mode Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{NRWL}	15	—	15	—	20	—	ns	
Nibble Mode Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{NCWL}	15	—	15	—	20	—	ns	
Test Mode Enable Setup Time Referenced to $\overline{\text{RAS}}$	t_{TEHREL}	t_{TES}	0	—	0	—	0	—	ns	
Test Mode Enable Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHTEL}	t_{TEHR}	0	—	0	—	0	—	ns	
Test Mode Enable Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHTEL}	t_{TEHC}	0	—	0	—	0	—	ns	

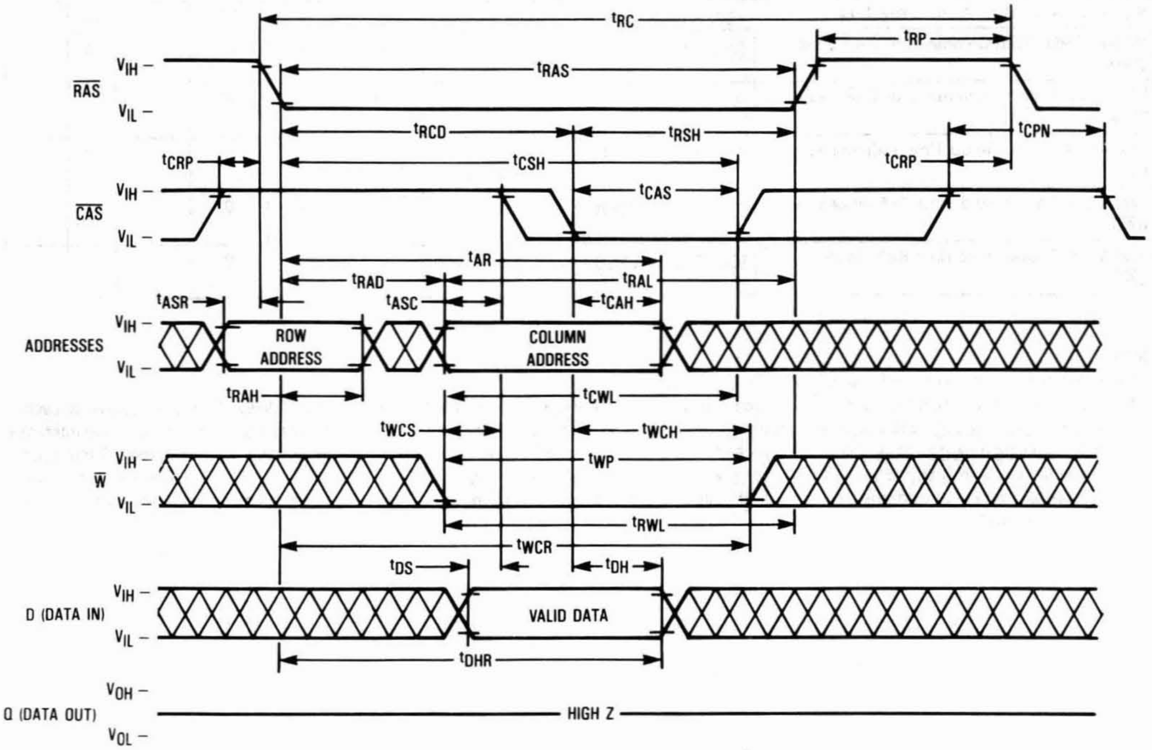
NOTES:

14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles and to $\overline{\text{W}}$ leading edge in delayed write or read-write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

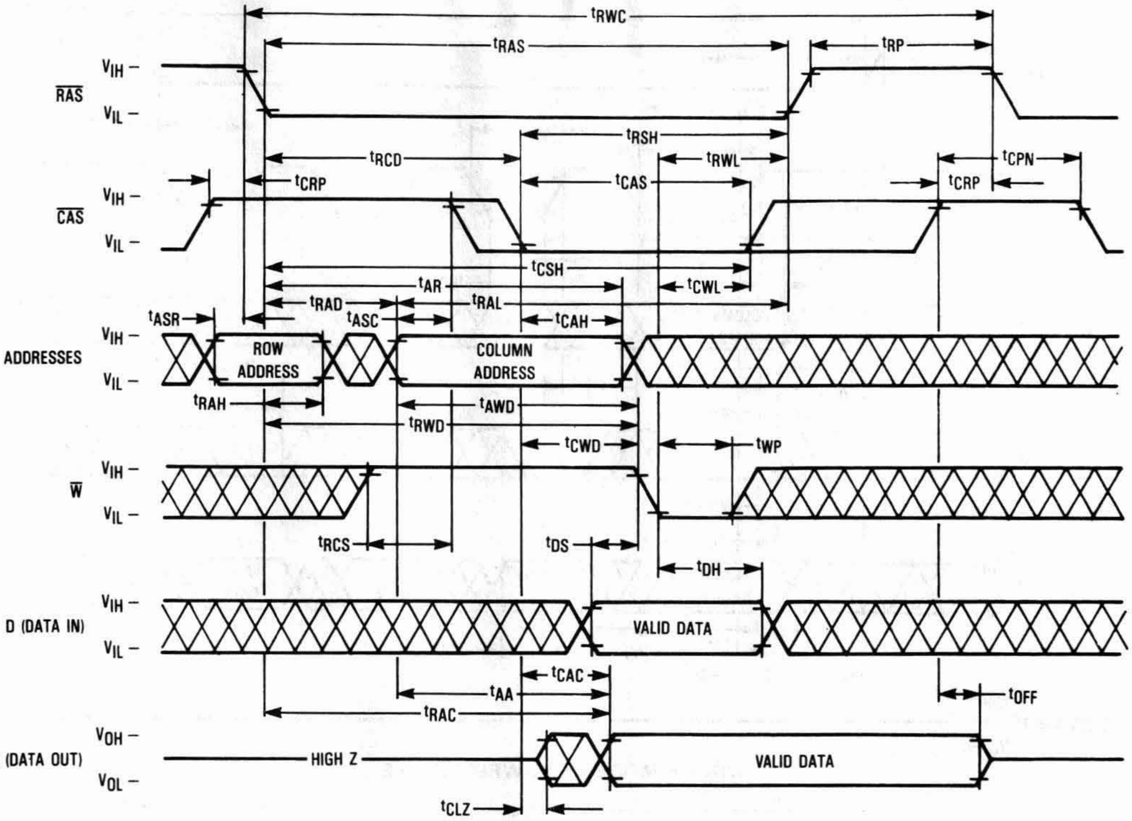
READ CYCLE


tRC
tRP
tRAS
RAS
VIH –
VIL –
tCSH
tCPN
tCRP
tRCD
tRSH
tCRP
CAS
VIH –
VIL –
tCAS
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W
VIH –
VIL –
tCAC
tAA
tCLZ
tOFF
tRAC
Q (DATA OUT)
VOH –
VOL –
HIGH Z
VALID DATA

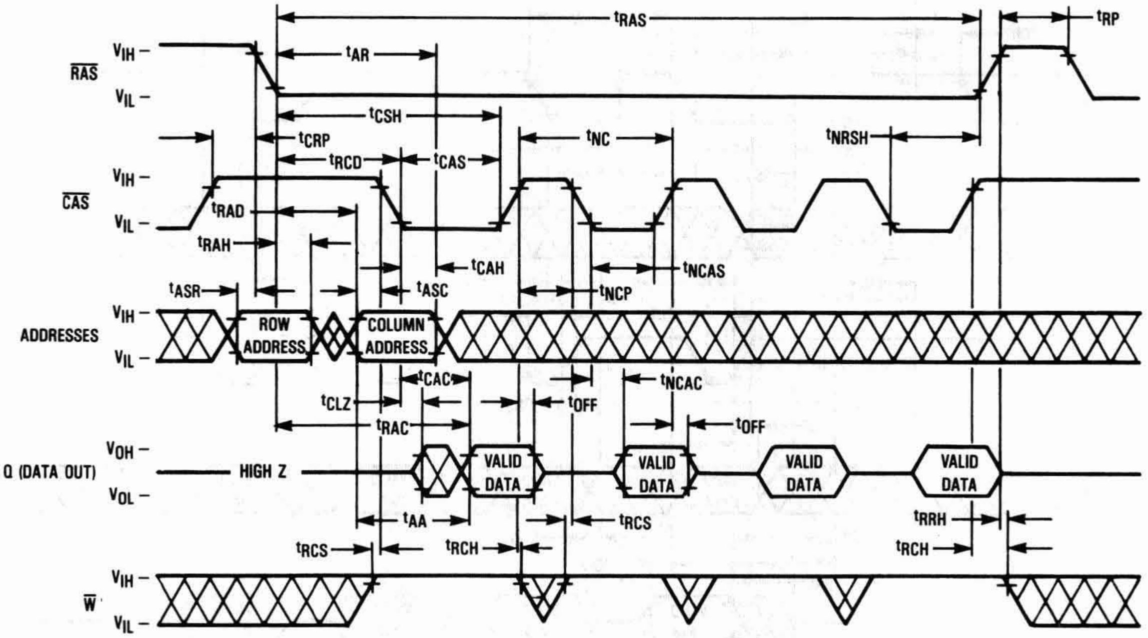
EARLY WRITE CYCLE


tRC
tRP
tRAS
RAS
VIH –
VIL –
tRCD
tRSH
tCPN
tCRP
tCSH
tCRP
CAS
VIH –
VIL –
tCAS
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
W
VIH –
VIL –
tWP
tRWL
tWCR
tDS
tDH
D (DATA IN)
VIH –
VIL –
VALID DATA
tDHR
Q (DATA OUT)
VOH –
VOL –
HIGH Z

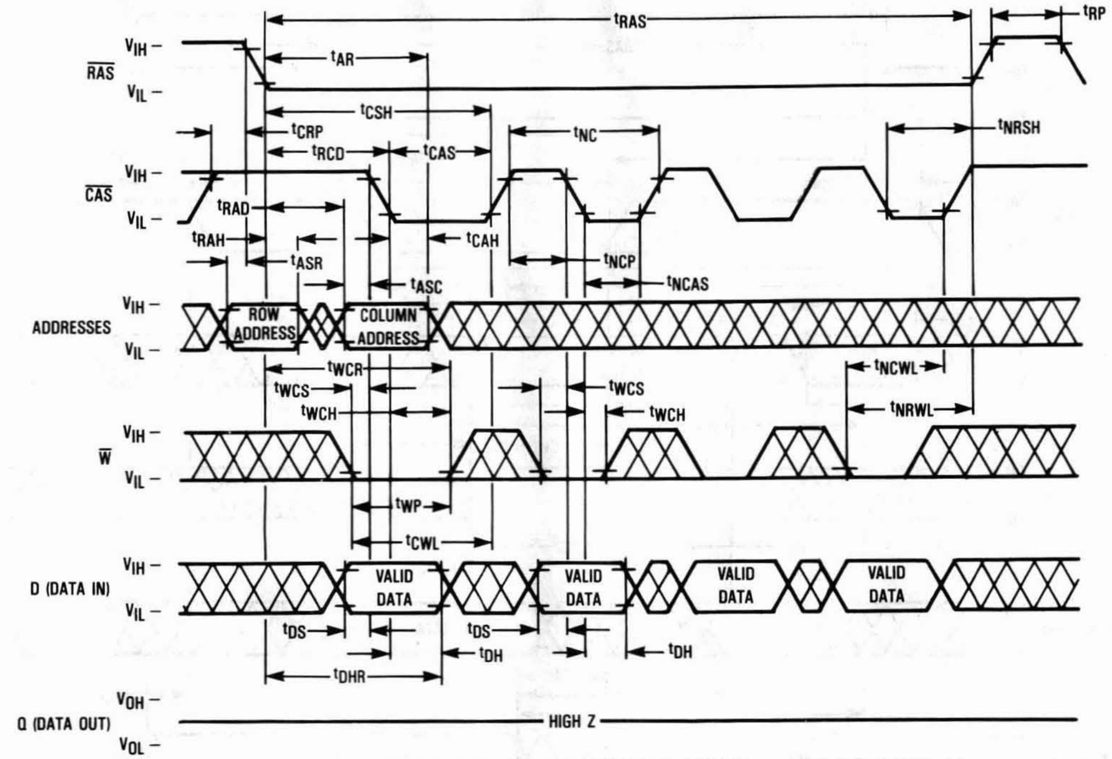
READ-WRITE CYCLE


tRWC
tRAS
tRP
VIH
RAS
VIL
tRSH
tRCD
tRWL
tCPN
tCRP
tCAS
tCRP
CAS
tCSH
tAR
tCWL
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tRAH
tAWD
tRWD
tCWD
tWP
W
tRCS
tDS
tDH
D (DATA IN)
VALID DATA
tCAC
tAA
tOFF
tRAC
VOH
Q (DATA OUT)
HIGH Z
VALID DATA
VOL
tCLZ

NIBBLE MODE READ CYCLE

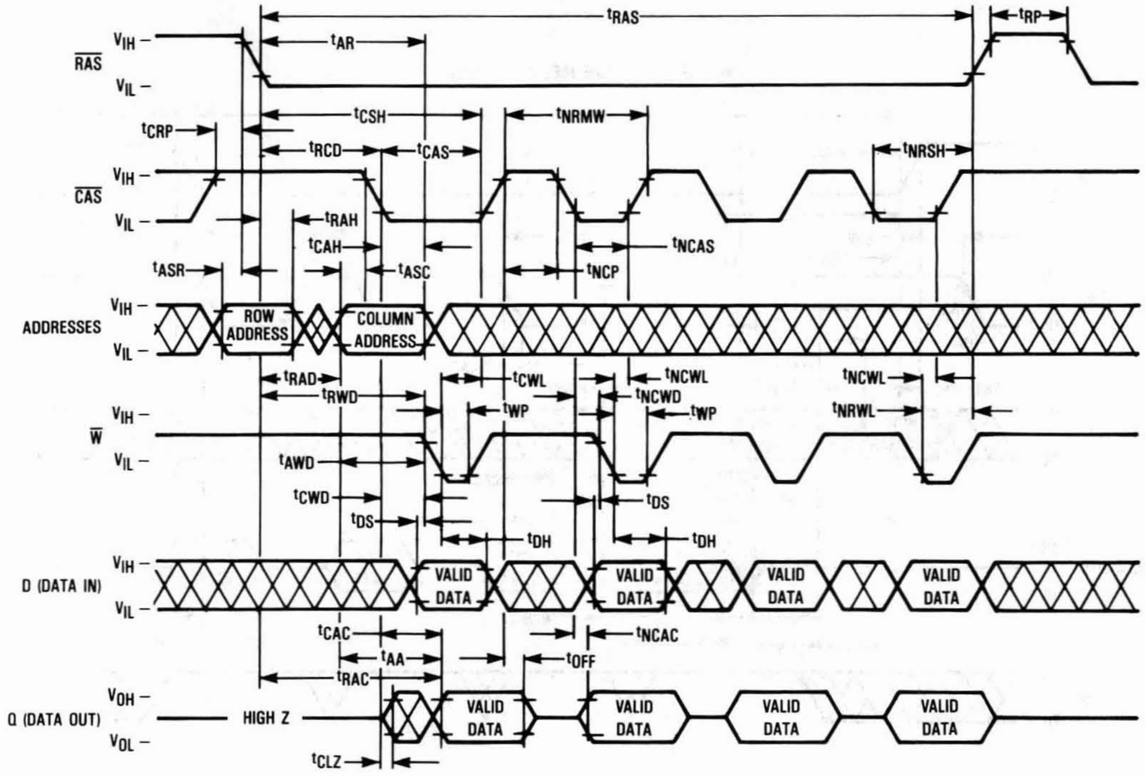

tRAS
tRP
VIH
RAS
VIL
tAR
tCSH
tCRP
tNC
tNRSH
tRCD
tCAS
CAS
tRAD
tRAH
tCAH
tNCAS
tASR
tASC
tNCP
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tCAC
tNCAC
tCLZ
tOFF
tRAC
tOFF
VOH
Q (DATA OUT)
HIGH Z
VALID DATA
VALID DATA
VALID DATA
VALID DATA
VOL
tAA
tRCS
tRRH
tRCS
tRCH
tRCH
W

NIBBLE MODE EARLY WRITE CYCLE



RAS
CAS
ADDRESSES
W
D (DATA IN)
Q (DATA OUT)
VIH –
VIL –
VOH –
VOL –
tRAS
tRP
tAR
tCSH
tCRP
tRCD
tCAS
tNC
tNRSH
tRAD
tRAH
tASR
tCAH
tNCP
tASC
tNCAS
ROW ADDRESS
COLUMN ADDRESS
tWCR
tWCS
tWCH
tNCWL
tNRWL
tWP
tCWL
VALID DATA
tDS
tDH
tDHR
HIGH Z

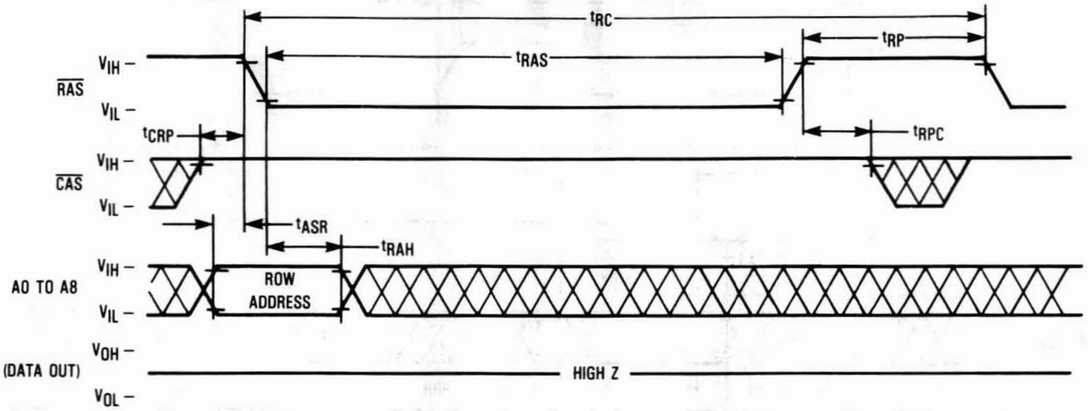
NIBBLE MODE READ-WRITE CYCLE



RAS
CAS
ADDRESSES
W
D (DATA IN)
Q (DATA OUT)
VIH –
VIL –
VOH –
VOL –
tRAS
tRP
tAR
tCSH
tNRMW
tCRP
tRCD
tCAS
tNRSH
tRAH
tCAH
tNCAS
tASR
tASC
tNCP
ROW ADDRESS
COLUMN ADDRESS
tRAD
tCWL
tNCWL
tRWD
tWP
tNCWD
tNRWL
tAWD
tCWD
tDS
tDH
VALID DATA
tCAC
tNCAC
tAA
tOFF
tRAC
HIGH Z
tCLZ

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

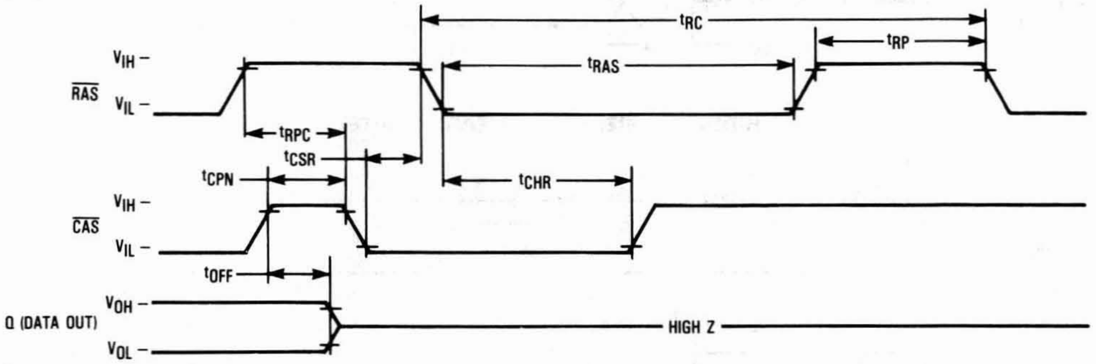
($\overline{\text{W}}$ and A9 are Don't Care)



t_{RC}
t_{RP}
t_{RAS}
V_{IH} –
$\overline{RAS}$
V_{IL} –
t_{CRP}
t_{RPC}
V_{IH} –
$\overline{CAS}$
V_{IL} –
t_{ASR}
t_{RAH}
V_{IH} –
A0 TO A8
ROW ADDRESS
V_{IL} –
V_{OH} –
Q (DATA OUT)
HIGH Z
V_{OL} –

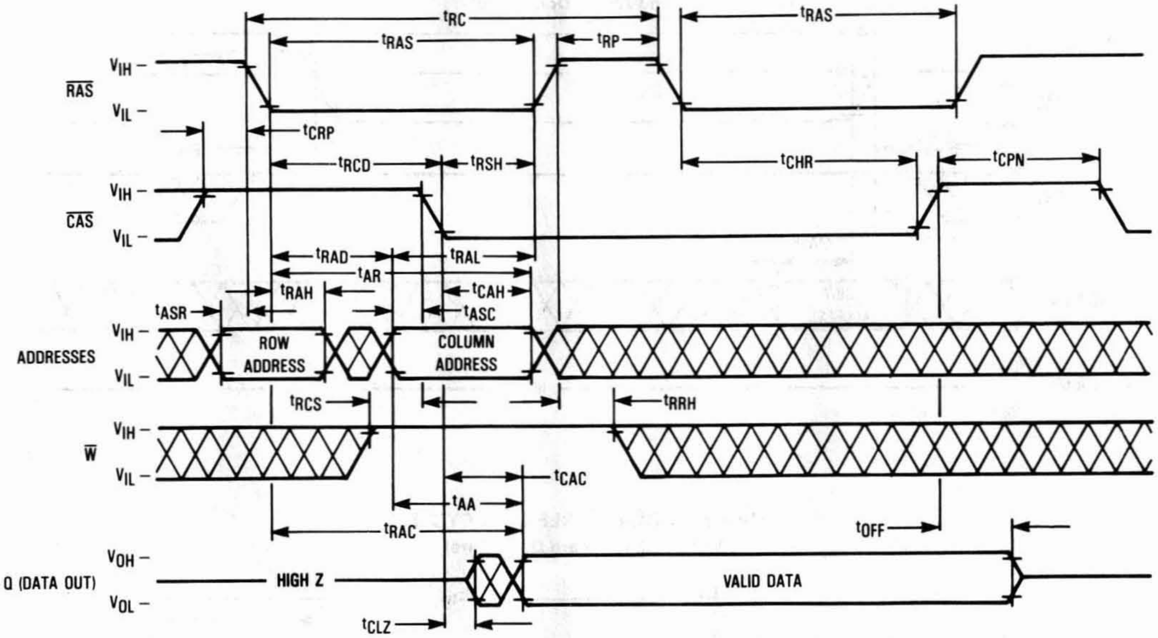
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{W}}$ and A0 to A9 are Don't Care)

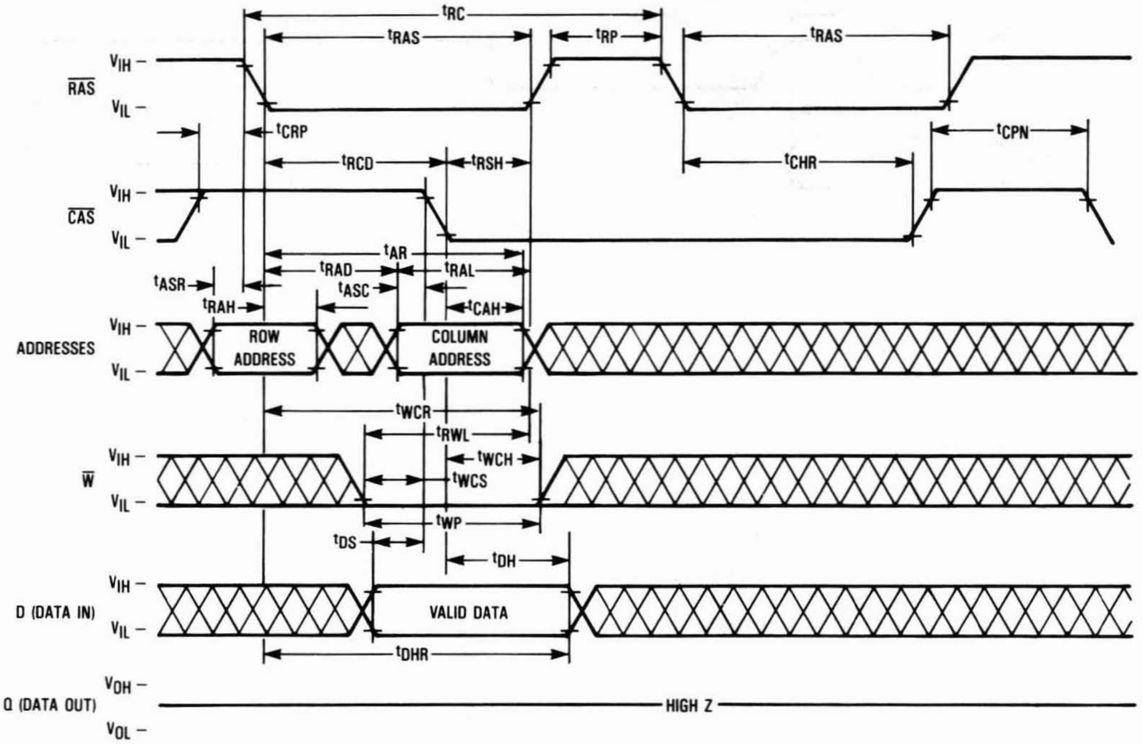


t_{RC}
t_{RP}
V_{IH} –
t_{RAS}
$\overline{RAS}$
V_{IL} –
t_{RPC}
t_{CSR}
t_{CPN}
t_{CHR}
V_{IH} –
$\overline{CAS}$
V_{IL} –
t_{OFF}
V_{OH} –
Q (DATA OUT)
HIGH Z
V_{OL} –

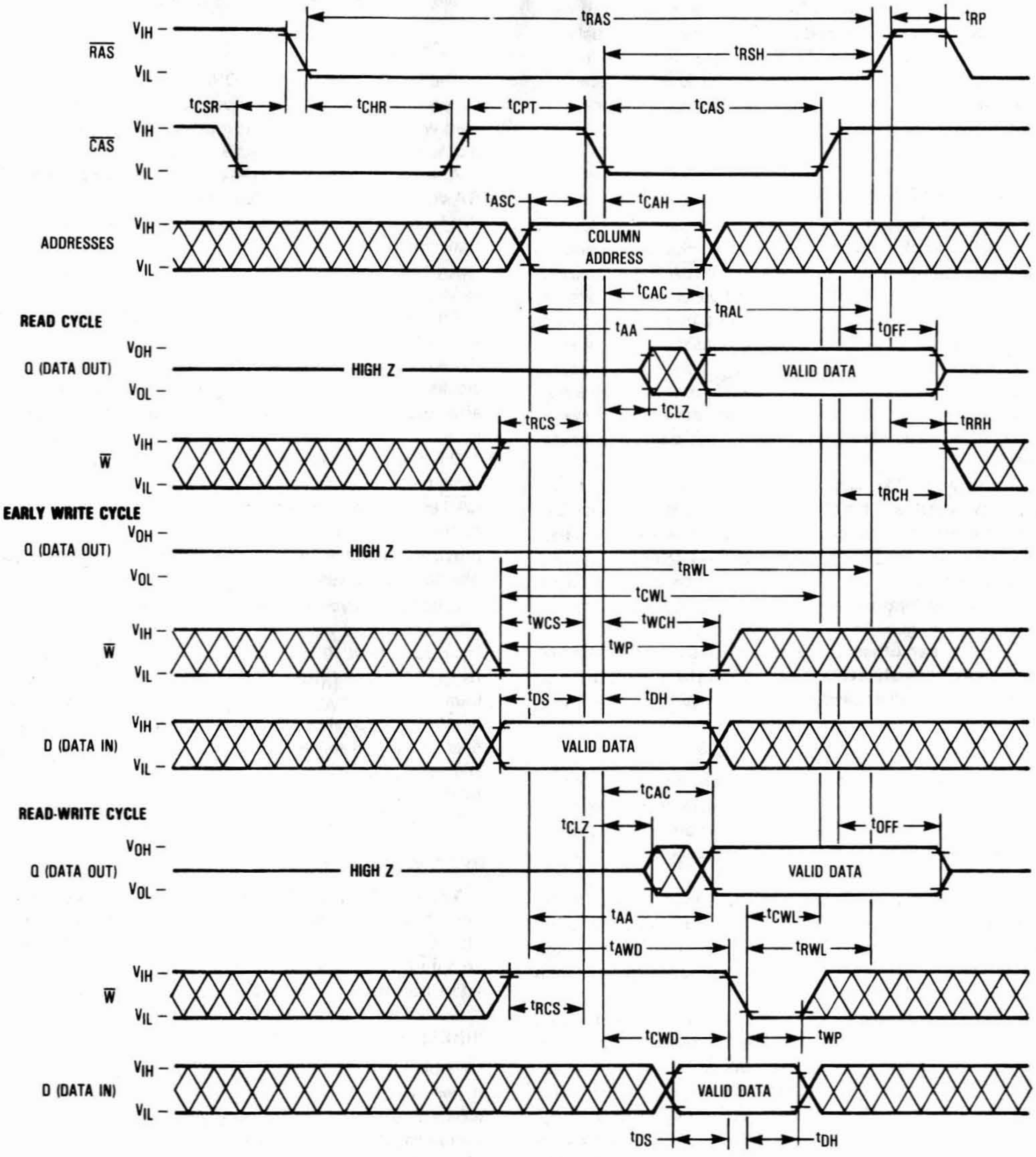
HIDDEN REFRESH CYCLE (READ)


tRC
tRAS
tRP
tRAS
RAS
VIH –
VIL –
tCRP
tRCD
tRSH
tCHR
tCPN
CAS
VIH –
VIL –
tRAD
tRAL
tAR
tRAH
tCAH
tASR
tASC
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
tRCS
tRRH
W
VIH –
VIL –
tCAC
tAA
tRAC
tOFF
Q (DATA OUT)
VOH –
VOL –
HIGH Z
VALID DATA
tCLZ

HIDDEN REFRESH CYCLE (EARLY WRITE)


tRC
tRAS
tRP
tRAS
RAS
VIH –
VIL –
tCRP
tRCD
tRSH
tCHR
tCPN
CAS
VIH –
VIL –
tAR
tRAD
tRAL
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
tWCR
tRWL
tWCH
tWCS
W
VIH –
VIL –
tWP
tDS
tDH
D (DATA IN)
VIH –
VIL –
VALID DATA
tDHR
Q (DATA OUT)
VOH –
VOL –
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
ADDRESSES
READ CYCLE
Q (DATA OUT)
$\overline{\text{W}}$
EARLY WRITE CYCLE
Q (DATA OUT)
$\overline{\text{W}}$
D (DATA IN)
READ-WRITE CYCLE
Q (DATA OUT)
$\overline{\text{W}}$
D (DATA IN)
V_{IH}
V_{IL}
V_{OH}
V_{OL}
t_{RAS}
t_{RP}
t_{RSH}
t_{CSR}
t_{CHR}
t_{CPT}
t_{CAS}
t_{ASC}
t_{CAH}
COLUMN ADDRESS
t_{CAC}
t_{RAL}
t_{AA}
t_{OFF}
HIGH Z
VALID DATA
t_{CLZ}
t_{RCS}
t_{RRH}
t_{RCH}
t_{RWL}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
t_{DS}
t_{DH}
t_{AWD}
t_{CWD}

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active $= V_{IL}$, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are two other variations in addressing the 1M RAM: **$\overline{\text{RAS}}$ only refresh cycle** and **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, nibble mode read cycle, read-write cycle, and nibble mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. However, $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ clock active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, nibble mode early write, and nibble mode read-write. Early and late write modes are discussed here, while nibble mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active times t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, $(t_{RCD}+t_{CWD}+t_{RWL}+2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL} and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but Q may be indeterminate—see note 16 of AC operating conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

NIBBLE MODE CYCLES

Nibble mode allows fast successive serial data operations at two, three, or four bits of the 1M dynamic RAM. Read access time in nibble mode (t_{NCAC}) is considerably faster than the regular $\overline{\text{RAS}}$ clock access time t_{RAC}. Nibble mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The address of the first nibble bit is latched by $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions. Each subsequent $\overline{\text{CAS}}$ active transition increments the row and column addresses internally to access the next bit in binary fashion. After the fourth bit is accessed, the nibble pattern repeats itself: (0,0) (0,1) (1,0) (1,1) (0,0) (0,1) (1,0) (1,1) . . . . The A10 address determines the starting point of the 4-bit nibble, with row address A10 the least significant of the (column, row) ordered pair. External addresses are ignored after the first nibble bit is selected.

A nibble mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum of t_{NCP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first nibble mode cycle (t_{NC} or t_{NRMW}). Either a read, write, or read-write operation can be performed in a nibble mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive nibble mode cycles and performed in any order. The maximum number of consecutive nibble mode cycles is limited by t_{RAS}. Nibble mode operation ends when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following a $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM511001A require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM511001A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh**, **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh**, and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

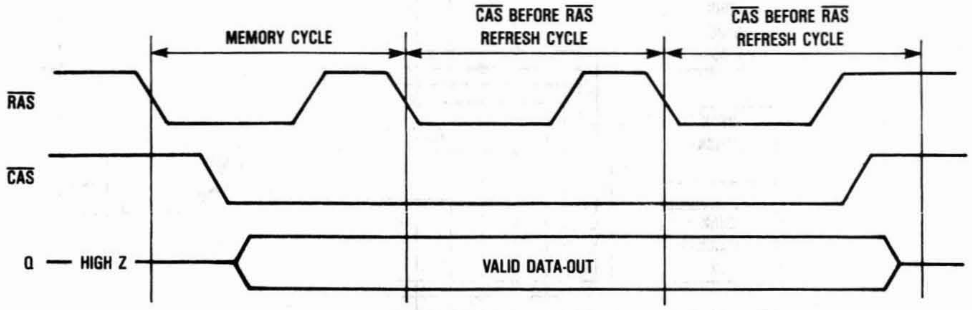

MEMORY CYCLE
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
Q — HIGH Z
VALID DATA-OUT

Figure 1. Hidden Refresh Cycle

TEST MODE

Internal organization of this device (256K × 4) allows it to be tested as if it were a 256K × 1 DRAM. Only nine of the ten addresses (A0–A8) are used in test mode; A9 is internally disabled. A test mode write cycle writes data, D (data in), to a bit in each of the four 256K × 1 blocks (B0–B3), in parallel. A test mode read cycle reads a bit in each of the four blocks. If data is the same in all four bits, Q (data out) is the same as the data in each bit. If data is not the same in all four bits, Q is high Z. See truth table and block diagram.

Test mode can be used in any timing cycle except nibble mode cycles. The test mode function is enabled by holding the "TF" pin on "super voltage" for the specified period (t_{TES}, t_{TEHR}, t_{TEHC}; see TEST MODE CYCLE).

"Super voltage" = V_{CC} + 4.5 V

where

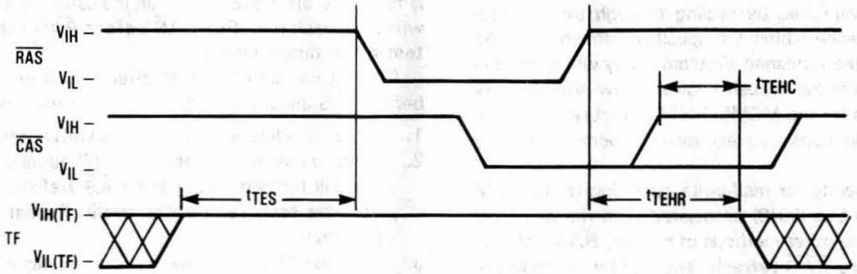
$4.5\ V < V_{CC} < 5.5\ V$ and maximum voltage = 10.5 V.

A9 is ignored in test mode. In normal operation, the "TF" pin must either be connected to V_{IL}, or left open.

Test Mode Truth Table

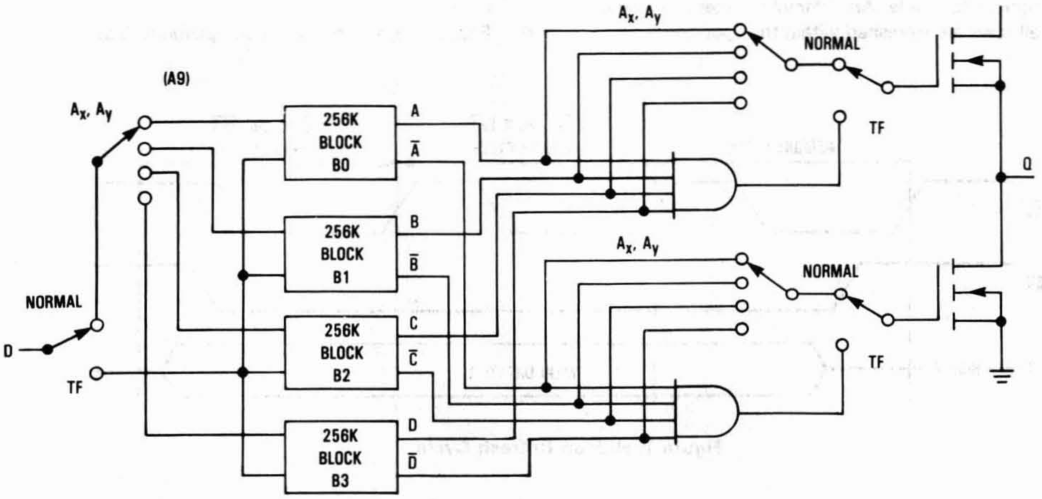
D	B0	B1	B2	B3	Q
0	0	0	0	0	0
1	1	1	1	1	1
—	Any Other				High-Z

TEST MODE CYCLE



V_IH –
RAS
V_IL –
V_IH –
CAS
V_IL –
tTEHC
tTES
tTEHR
V_IH(TF) –
TF
V_IL(TF) –

TEST FUNCTION BLOCK DIAGRAM



Ax, Ay
(A9)
Ax, Ay
256K BLOCK B0
A
Ā
256K BLOCK B1
B
B̄
256K BLOCK B2
C
C̄
256K BLOCK B3
D
D̄
NORMAL
D
TF
Ax, Ay
NORMAL
TF
Q
Ax, Ay
NORMAL
TF

ORDERING INFORMATION
(Order by Full Part Number)

MCM 511001A X XX XX

Motorola Memory Prefix — MCM
Part Number — 511001A
Package (P = 300 mil Plastic DIP, J = 300 mil SOJ, Z = Plastic ZIP) — X
Speed (70 = 70 ns, 80 = 80 ns, 10 = 100 ns) — XX
Shipping Method (R2 = Tape & Reel, Blank = Rails) — XX

Full Part Numbers — MCM511001AP70 MCM511001AJ70 MCM511001AJ70R2 MCM511001AZ70
MCM511001AP80 MCM511001AJ80 MCM511001AJ80R2 MCM511001AZ80
MCM511001AP10 MCM511001AJ10 MCM511001AJ10R2 MCM511001AZ10

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM511002A

1M × 1 CMOS Dynamic RAM

Static Column

The MCM511002A is a 1.0μ CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The static column mode feature allows column data to be accessed upon the column address transition when $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ are held low, similar to static RAM operation.

The MCM511002A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line plastic package (DIP), a 300-mil SOJ plastic package, and a 100-mil zig-zag in-line plastic package (ZIP).

- Three-State Data Output
- Common I/O with Early Write
- Static Column Mode
- Test Mode
- TTL-Compatible Inputs and Output
- $\overline{\text{RAS}}$ Only Refresh
- $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM511002A-70 = 70 ns (Maximum)
  MCM511002A-80 = 80 ns (Maximum)
  MCM511002A-10 = 100 ns (Maximum)
- Low Active Power Dissipation: MCM511002A-70 = 440 mW (Maximum)
  MCM511002A-80 = 385 mW (Maximum)
  MCM511002A-10 = 330 mW (Maximum)
- Low Standby Power Dissipation: 11 mW (Maximum, TTL Levels)
  5.5 mW (Maximum, CMOS Levels)

NOT RECOMMENDED FOR NEW DESIGNS

P PACKAGE
300 MIL PLASTIC
CASE 707A

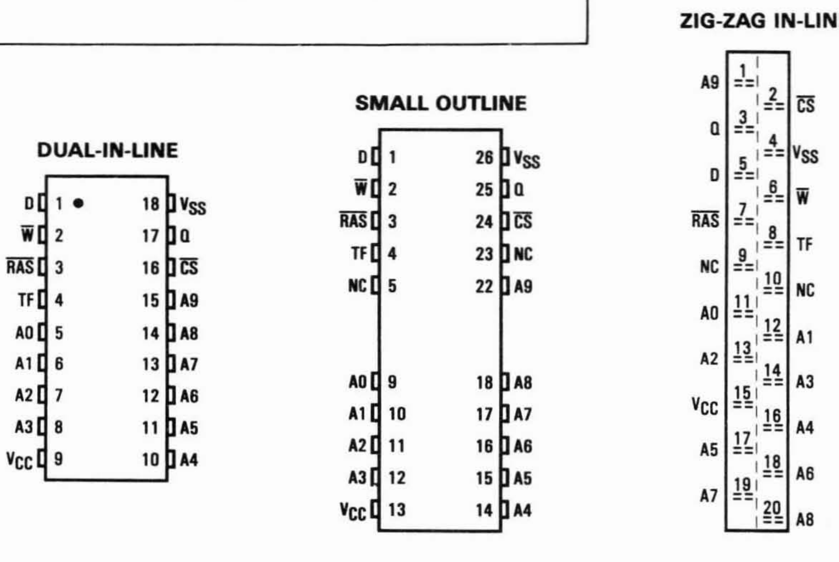
J PACKAGE
300 MIL SOJ
CASE 822

Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

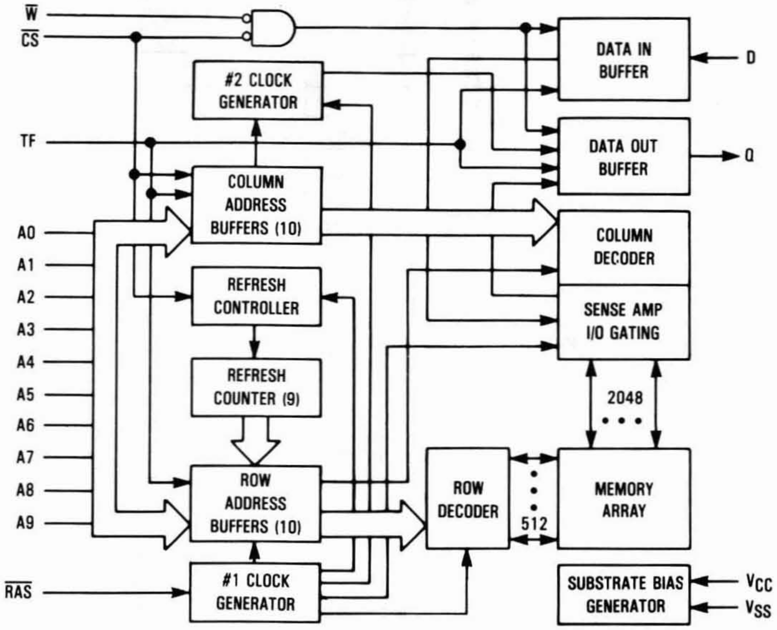
PIN NAMES

A0-A9	Address Input
D	Data Input
Q	Data Output
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CS}}$	Chip Select
V_{CC}	Power (+5 V)
V_{SS}	Ground
TF	Test Function Enable
NC	No Connection

PIN ASSIGNMENT


DUAL-IN-LINE
D 1
W 2
RAS 3
TF 4
A0 5
A1 6
A2 7
A3 8
VCC 9
18 VSS
17 Q
16 CS
15 A9
14 A8
13 A7
12 A6
11 A5
10 A4
SMALL OUTLINE
D 1
W 2
RAS 3
TF 4
NC 5
A0 9
A1 10
A2 11
A3 12
VCC 13
26 VSS
25 Q
24 CS
23 NC
22 A9
18 A8
17 A7
16 A6
15 A5
14 A4
ZIG-ZAG IN-LINE
A9 1
2 CS
Q 3
4 VSS
D 5
6 W
RAS 7
8 TF
NC 9
10 NC
A0 11
12 A1
A2 13
14 A3
VCC 15
16 A4
A5 17
18 A6
A7 19
20 A8

BLOCK DIAGRAM


W
CS
TF
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
RAS
#2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (10)
REFRESH CONTROLLER
REFRESH COUNTER (9)
ROW ADDRESS BUFFERS (10)
#1 CLOCK GENERATOR
ROW DECODER
512
DATA IN BUFFER
D
DATA OUT BUFFER
Q
COLUMN DECODER
SENSE AMP I/O GATING
2048
MEMORY ARRAY
SUBSTRATE BIAS GENERATOR
VCC
VSS

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Test Function Input Voltage	$V_{in(TF)}$	−1 to +10.5	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	—	0.8	V	1
Test Function Input High Voltage	$V_{IH\,(TF)}$	$V_{CC}+4.5$	—	10.5	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM511002A-70, t_{RC} = 130 ns		—	80		
MCM511002A-80, t_{RC} = 150 ns		—	70		
MCM511002A-10, t_{RC} = 180 ns		—	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}=\overline{CS}=V_{IH}$)	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CS}=V_{IH}$)	I_{CC3}			mA	2
MCM511002A-70, t_{RC} = 130 ns		—	80		
MCM511002A-80, t_{RC} = 150 ns		—	70		
MCM511002A-10, t_{RC} = 180 ns		—	60		
V_{CC} Power Supply Current During Static Column Mode Cycle ($\overline{RAS}=\overline{CS}=V_{IL}$)	I_{CC4}			mA	2, 3
MCM511002A-70, t_{SC} = 40 ns		—	60		
MCM511002A-80, t_{SC} = 45 ns		—	50		
MCM511002A-10, t_{SC} = 50 ns		—	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}=\overline{CS}=V_{CC}-0.2$ V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM511002A-70, t_{RC} = 130 ns		—	80		
MCM511002A-80, t_{RC} = 150 ns		—	70		
MCM511002A-10, t_{RC} = 180 ns		—	60		
Input Leakage Current (Except TF) (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	µA	
Input Leakage Current (TF) (0 V ≤ $V_{in(TF)}$ ≤ V_{CC} + 0.5 V)	$I_{lkg(I)}$	−10	10	µA	
Output Leakage Current ($\overline{CS}=V_{IH}$, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	µA	
Test Function Input Current (V_{CC} + 4.5 V ≤ $V_{in(TF)}$ ≤ 10.5 V)	$I_{in(TF)}$	—	1	mA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9, D	C_{in}	5	pF	4
	$\overline{RAS}$, $\overline{CS}$, $\overline{W}$, TF		7	pF	4
Output Capacitance ($\overline{CS}=V_{IH}$ to Disable Output)	Q	C_{out}	7	pF	4

NOTES:

1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Measured with one address transition per static column mode cycle.
4. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511002A-70		MCM511002A-80		MCM511002A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	180	—	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	155	—	155	—	210	—	ns	6
Static Column Mode Cycle Time	t_{AVAV}	t_{SC}	40	—	45	—	50	—	ns	
Static Column Mode Read-Write Cycle Time	t_{AVAV}	t_{SRWC}	70	—	80	—	100	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	70	—	80	—	100	ns	7, 8
Access Time from $\overline{CS}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	25	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	50	ns	7, 10
Access Time from Last Write	t_{WLQV}	t_{ALW}	—	65	—	75	—	95	ns	7, 11
$\overline{CS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	12
Data Out Hold from Address Change	t_{AXQX}	t_{AOH}	5	—	5	—	5	—	ns	
Data Out Enable from Write	t_{WHQV}	t_{OW}	—	20	—	20	—	25	ns	
Data Out Hold from Write	t_{WHQX}	t_{WOH}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Static Column Mode)	t_{RELREH}	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CS}$ Pulse Width	t_{CELCEH}	t_{CS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CS}$ Pulse Width (Static Column Mode)	t_{CELCEH}	t_{CSC}	20	100,000	20	100,000	25	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	13
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	14
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{CS}$ Precharge Time (Static Column Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max), and/or $t_{LWAD} \geq t_{LWAD}$ (max).
11. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max).
12. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

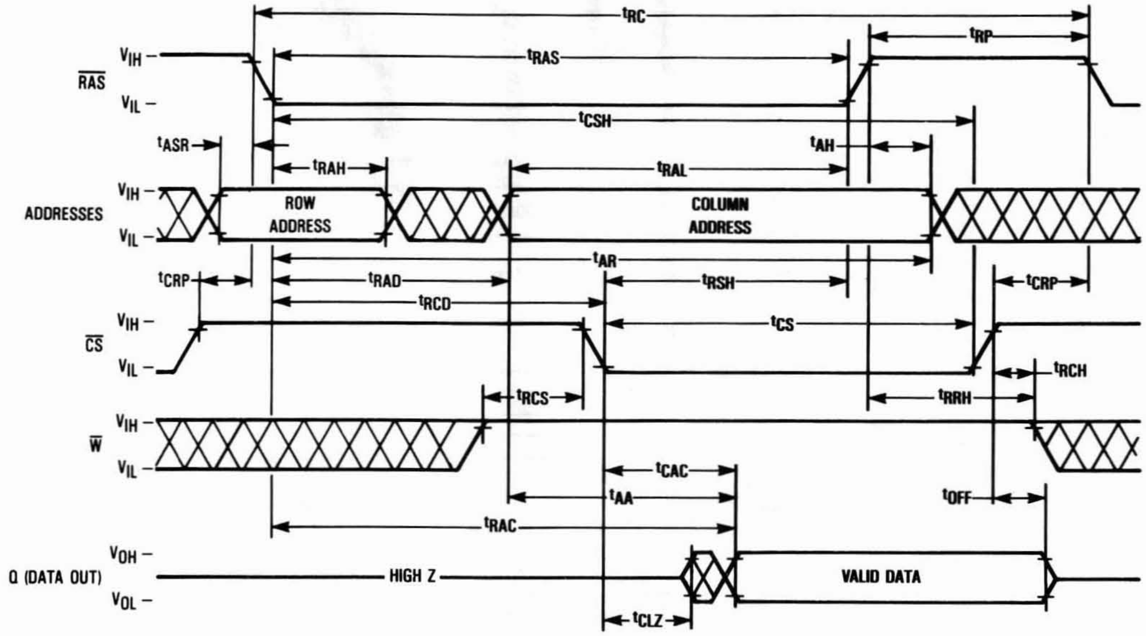
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM511002A-70		MCM511002A-80		MCM511002A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	ns	
Write Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELAX}	t_{AWR}	55	—	60	—	75	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELAX}	t_{AR}	80	—	90	—	115	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	50	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$ High	t_{REHAX}	t_{AH}	5	—	5	—	10	—	ns	15
Write Command to $\overline{\text{CS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	ns	
Last Write to Column Address Delay Time	t_{WLAV}	t_{LWAD}	20	30	20	35	25	45	ns	16
Last Write to Column Address Hold Time	t_{WLAX}	t_{AHLW}	65	—	75	—	95	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	17
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	17
Write Command Hold Time	t_{CELWX}	t_{WCH}	15	—	15	—	20	—	ns	18
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELWH}	t_{WCR}	55	—	60	—	75	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	
Write Command Inactive Time	t_{WHWL}	t_{WI}	10	—	10	—	10	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	19
Data In Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	20	—	ns	19
Data In Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	55	—	60	—	75	—	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	—	8	—	8	—	8	ms	
Write Command Setup Time (Output Data Disable)	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	18
$\overline{\text{CS}}$ to Write Delay	t_{CELWL}	t_{CWD}	20	—	20	—	25	—	ns	18
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	70	—	80	—	100	—	ns	18
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	35	—	40	—	50	—	ns	18
$\overline{\text{CS}}$ Setup Time for $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{\text{CS}}$ Hold Time for $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	30	—	ns	
$\overline{\text{CS}}$ Precharge to $\overline{\text{CS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CS}}$ Precharge Time for $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	50	—	ns	
$\overline{\text{CS}}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	15	—	ns	
Test Mode Enable Setup Time Referenced to $\overline{\text{RAS}}$	t_{TEHREL}	t_{TES}	0	—	0	—	0	—	ns	
Test Mode Enable Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHTEL}	t_{TEHR}	0	—	0	—	0	—	ns	
Test Mode Enable Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHTEL}	t_{TEHC}	0	—	0	—	0	—	ns	

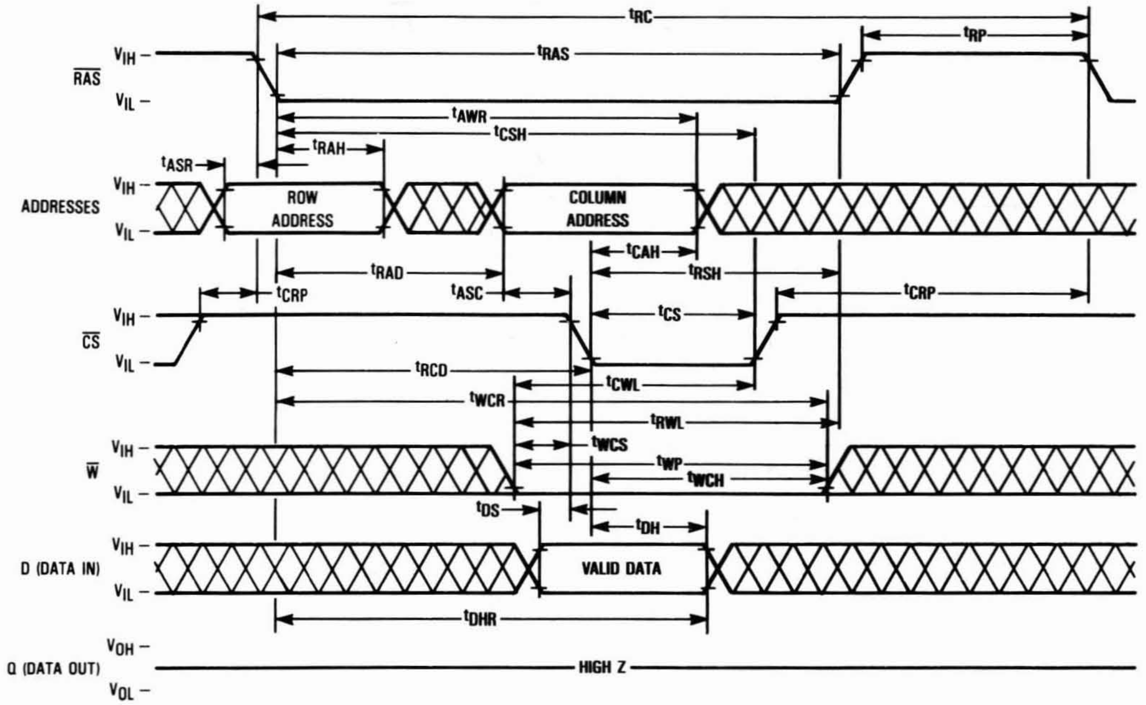
NOTES:

15. t_{AH} must be met for a read cycle.
16. Operation within the t_{LWAD} limit ensures that t_{ALW} can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
17. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
18. t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min) and $t_{WCH} \geq t_{WCH}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
19. These parameters are referenced to $\overline{\text{CS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in late write or read-write cycles.

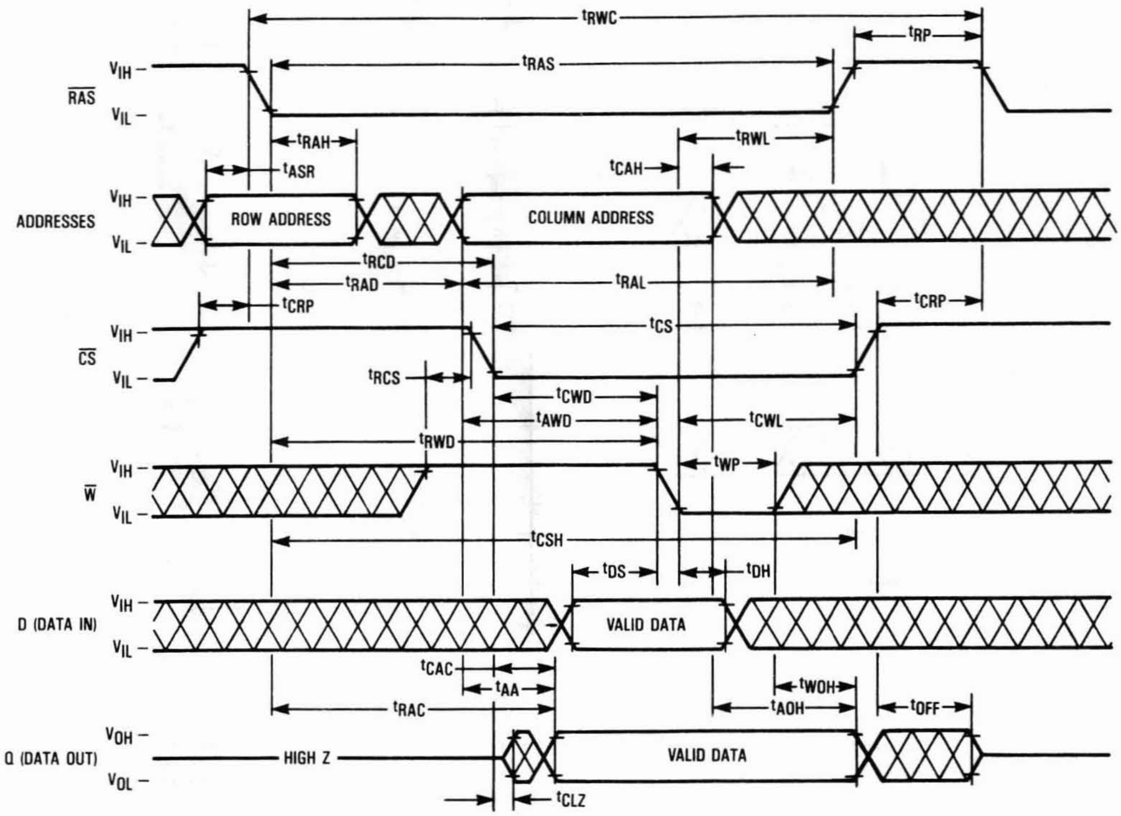
READ CYCLE


t_{RC}
t_{RP}
t_{RAS}
V_{IH} –
$\overline{RAS}$
V_{IL} –
t_{CSH}
t_{ASR}
t_{AH}
t_{RAH}
t_{RAL}
V_{IH} –
ADDRESSES
V_{IL} –
ROW ADDRESS
COLUMN ADDRESS
t_{AR}
t_{CRP}
t_{RAD}
t_{RSH}
t_{CRP}
t_{RCD}
V_{IH} –
$\overline{CS}$
V_{IL} –
t_{CS}
t_{RCH}
t_{RCS}
t_{RRH}
V_{IH} –
$\overline{W}$
V_{IL} –
t_{CAC}
t_{AA}
t_{OFF}
t_{RAC}
V_{OH} –
Q (DATA OUT)
V_{OL} –
HIGH Z
VALID DATA
t_{CLZ}

EARLY WRITE CYCLE

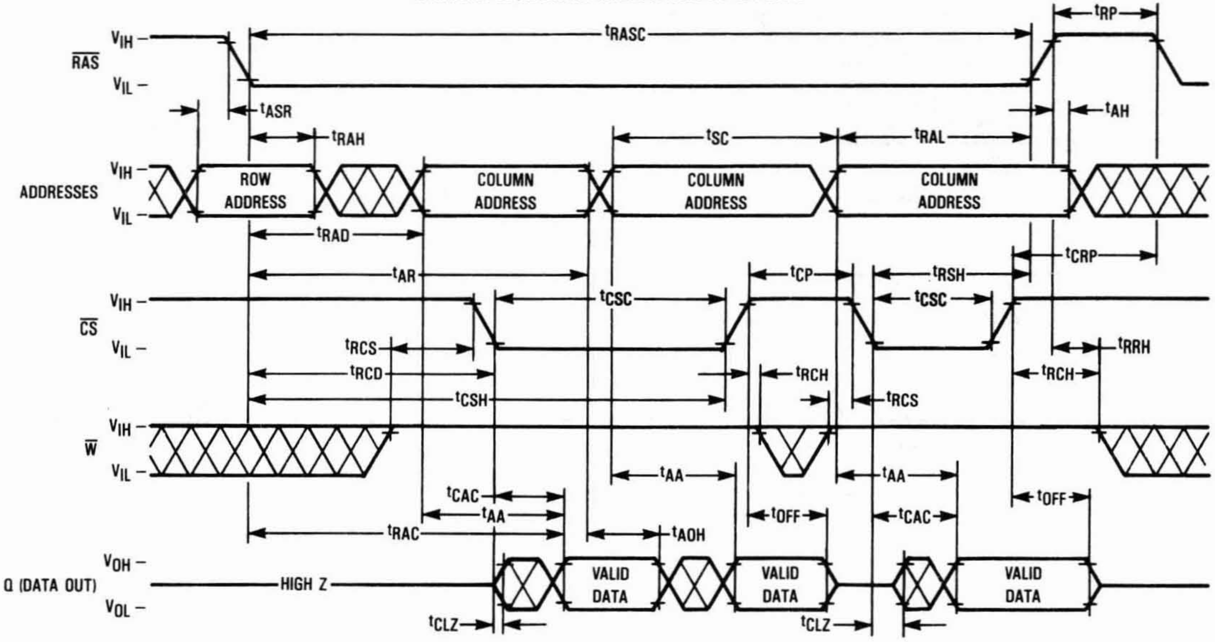

t_{RC}
t_{RP}
V_{IH} –
$\overline{RAS}$
V_{IL} –
t_{RAS}
t_{AWR}
t_{CSH}
t_{RAH}
t_{ASR}
V_{IH} –
ADDRESSES
V_{IL} –
ROW ADDRESS
COLUMN ADDRESS
t_{CAH}
t_{RAD}
t_{RSH}
t_{CRP}
t_{ASC}
t_{CRP}
V_{IH} –
$\overline{CS}$
V_{IL} –
t_{CS}
t_{RCD}
t_{CWL}
t_{WCR}
t_{RWL}
t_{WCS}
V_{IH} –
$\overline{W}$
V_{IL} –
t_{WP}
t_{WCH}
t_{DS}
t_{DH}
V_{IH} –
D (DATA IN)
V_{IL} –
VALID DATA
t_{DHR}
V_{OH} –
Q (DATA OUT)
V_{OL} –
HIGH Z

READ-WRITE CYCLE



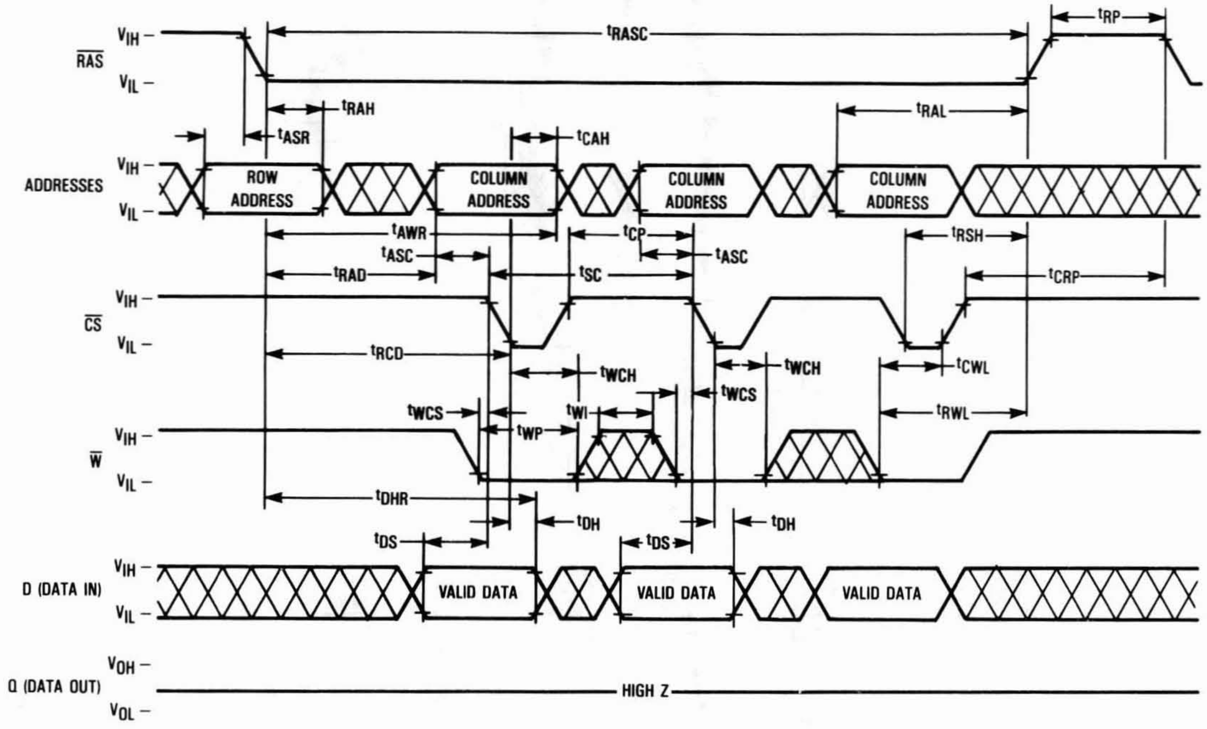
tRWC
tRP
tRAS
VIH
RAS
VIL
tRAH
tASR
tCAH
tRWL
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tRCD
tRAD
tRAL
tCRP
tCS
CS
tRCS
tCWD
tAWD
tCWL
tRWD
tWP
W
tCSH
tDS
tDH
D (DATA IN)
VALID DATA
tCAC
tAA
tRAC
tWOH
tAOH
tOFF
VOH
Q (DATA OUT)
VOL
HIGH Z
tCLZ

STATIC COLUMN MODE READ CYCLE

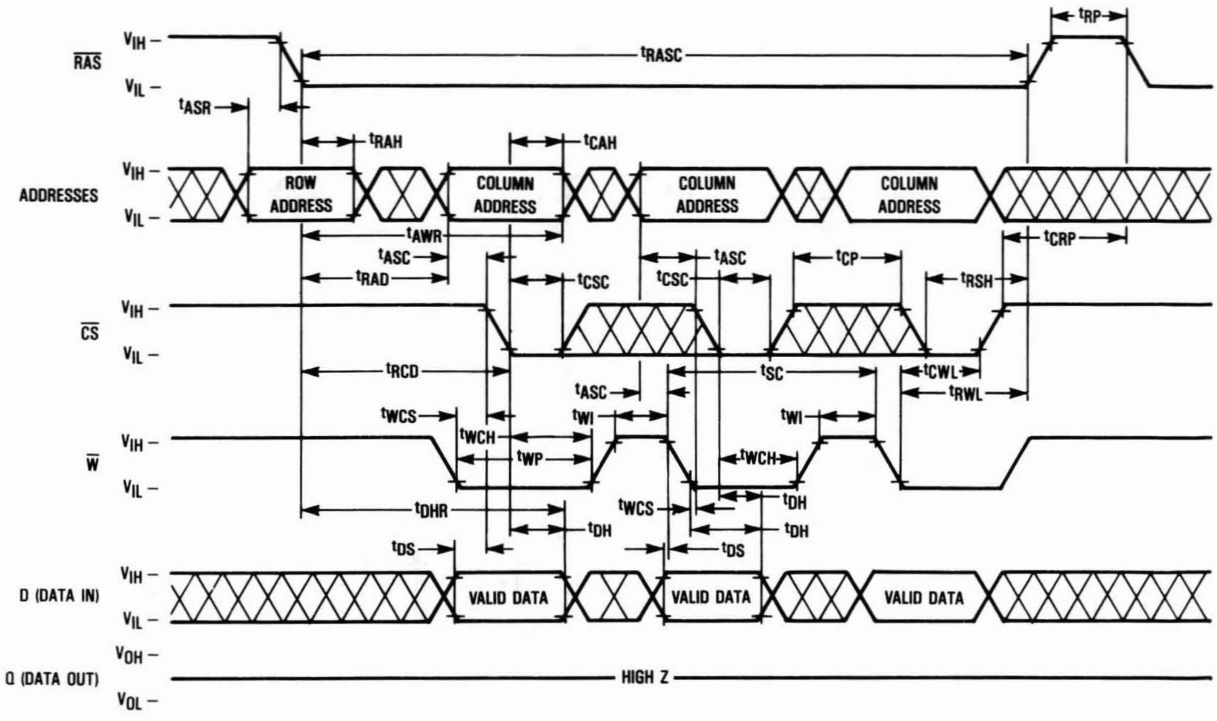


tRP
tRASC
VIH
RAS
VIL
tASR
tAH
tRAH
tSC
tRAL
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tCRP
tAR
tCP
tRSH
tCSC
tCSC
CS
tRRH
tRCS
tRCD
tRCH
tRCH
tCSH
tRCS
W
tAA
tAA
tCAC
tAA
tOFF
tOFF
tAOH
tCAC
tRAC
VOH
Q (DATA OUT)
VOL
HIGH Z
VALID DATA
VALID DATA
VALID DATA
tCLZ
tCLZ

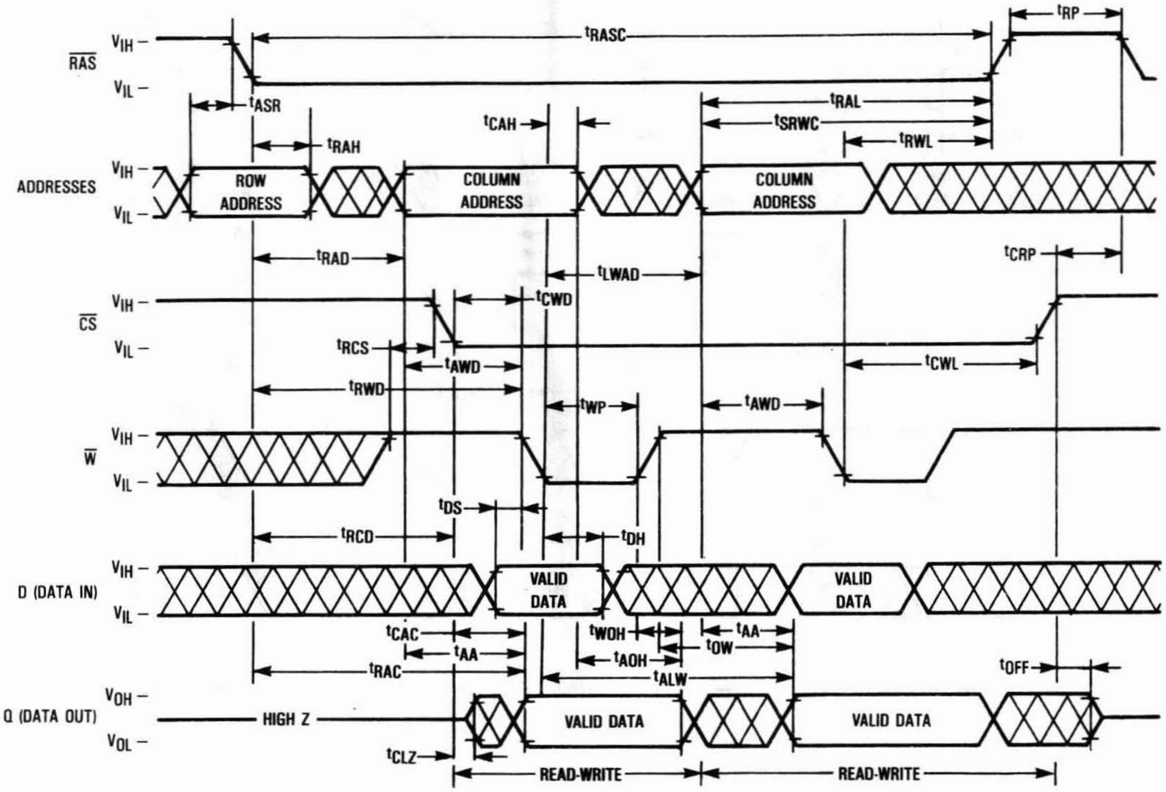
STATIC COLUMN MODE EARLY WRITE CYCLE (A)


RAS
ADDRESSES
CS
W
D (DATA IN)
Q (DATA OUT)
VIH –
VIL –
VOH –
VOL –
tRASC
tRP
tRAH
tASR
tCAH
tRAL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tAWR
tCP
tASC
tASC
tRSH
tRAD
tSC
tCRP
tRCD
tWCH
tWCH
tCWL
tWCS
tWCS
tWI
tRWL
tWP
tDHR
tDH
tDH
tDS
tDS
VALID DATA
VALID DATA
VALID DATA
HIGH Z

STATIC COLUMN MODE EARLY WRITE CYCLE (B)

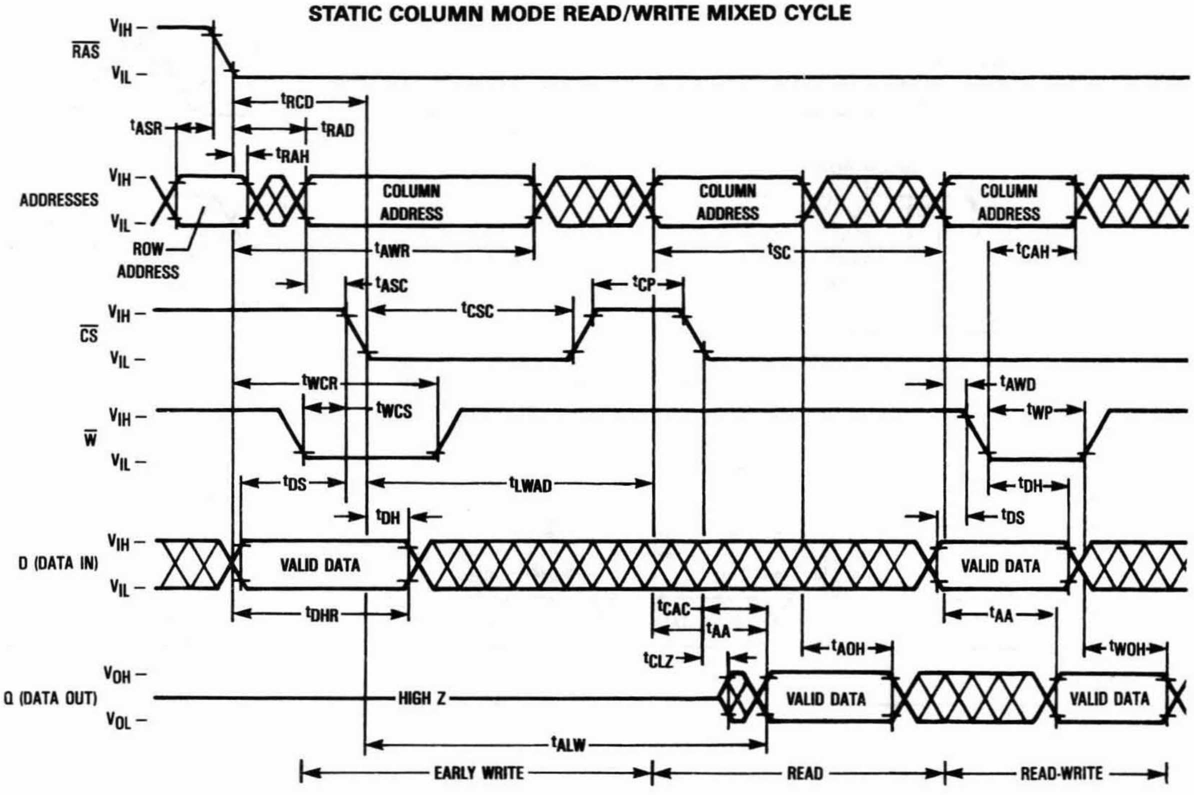

RAS
ADDRESSES
CS
W
D (DATA IN)
Q (DATA OUT)
VIH –
VIL –
VOH –
VOL –
tRP
tRASC
tASR
tRAH
tCAH
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tAWR
tCRP
tASC
tASC
tCP
tRAD
tCSC
tCSC
tRSH
tRCD
tSC
tCWL
tASC
tRWL
tWCS
tWI
tWI
tWCH
tWP
tWCH
tDHR
tWCS
tDH
tDH
tDH
tDS
tDS
VALID DATA
VALID DATA
VALID DATA
HIGH Z

STATIC COLUMN MODE READ-WRITE CYCLE



RAS
VIH
VIL
tRASC
tRP
tASR
tRAH
tCAH
tRAL
tSRWC
tRWL
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tLWAD
tCRP
CS
tCWD
tRCS
tAWD
tCWL
tRWD
tWP
tAWD
W
tDS
tRCD
tDH
D (DATA IN)
VALID DATA
VALID DATA
tCAC
tWOH
tAA
tAA
tOW
tAOH
tRAC
tALW
tOFF
Q (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA
VALID DATA
tCLZ
READ-WRITE
READ-WRITE

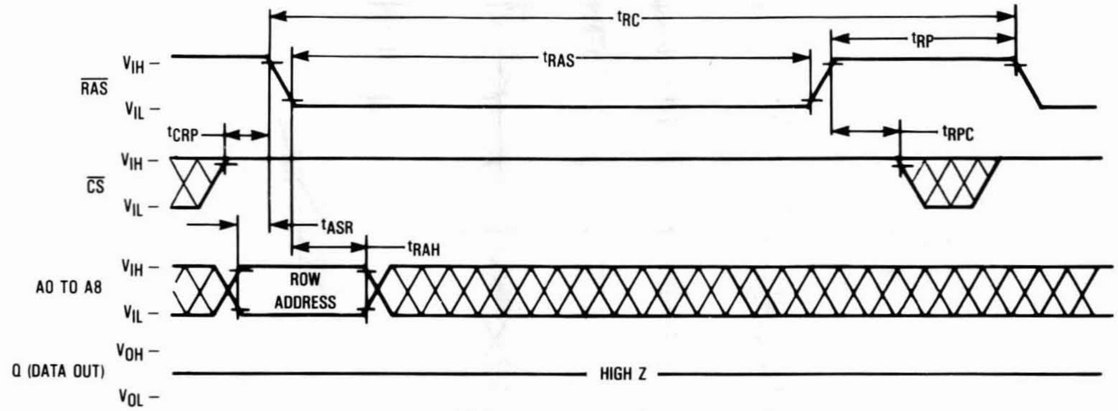
STATIC COLUMN MODE READ/WRITE MIXED CYCLE



RAS
VIH
VIL
tRCD
tASR
tRAD
tRAH
ADDRESSES
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
ROW ADDRESS
tAWR
tSC
tCAH
tASC
tCP
CS
tCSC
tWCR
tAWD
W
tWCS
tWP
tDS
tLWAD
tDH
tDH
tDS
D (DATA IN)
VALID DATA
VALID DATA
tDHR
tCAC
tAA
tAA
tCLZ
tAOH
tWOH
Q (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA
VALID DATA
tALW
EARLY WRITE
READ
READ-WRITE

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

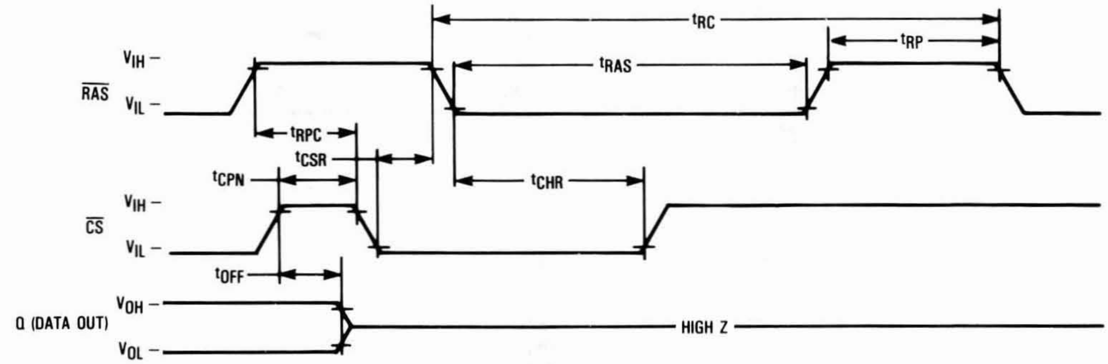
($\overline{\text{W}}$ and A9 are Don't Care)



t_{RC}
t_{RP}
t_{RAS}
V_{IH} –
$\overline{\text{RAS}}$
V_{IL} –
t_{CRP}
t_{RPC}
V_{IH} –
$\overline{\text{CS}}$
V_{IL} –
t_{ASR}
t_{RAH}
V_{IH} –
A0 TO A8
V_{IL} –
ROW ADDRESS
V_{OH} –
Q (DATA OUT)
HIGH Z
V_{OL} –

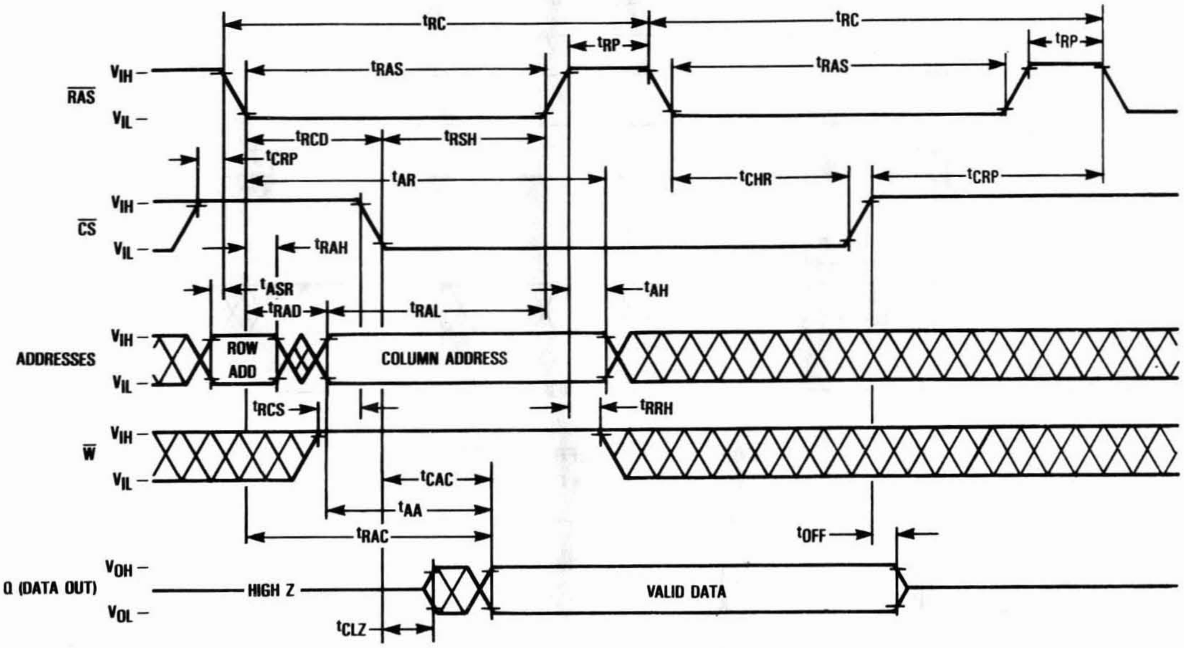
$\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{W}}$ and A0 to A9 are Don't Care)

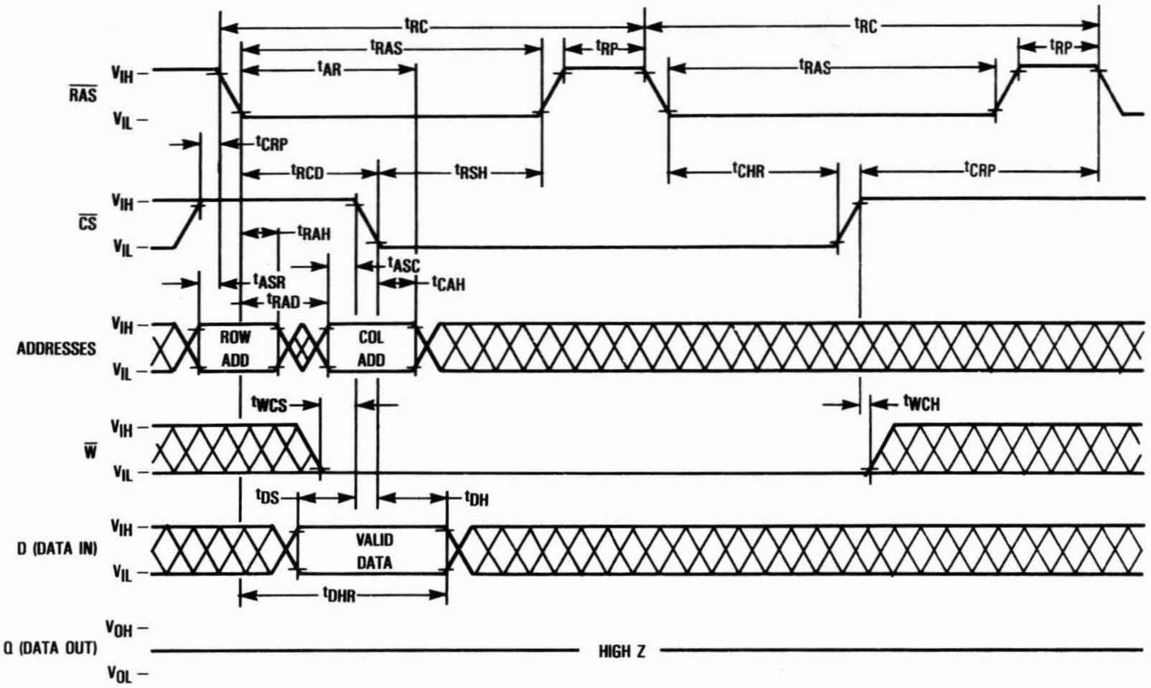


t_{RC}
t_{RP}
t_{RAS}
V_{IH} –
$\overline{\text{RAS}}$
V_{IL} –
t_{RPC}
t_{CSR}
t_{CPN}
t_{CHR}
V_{IH} –
$\overline{\text{CS}}$
V_{IL} –
t_{OFF}
V_{OH} –
Q (DATA OUT)
HIGH Z
V_{OL} –

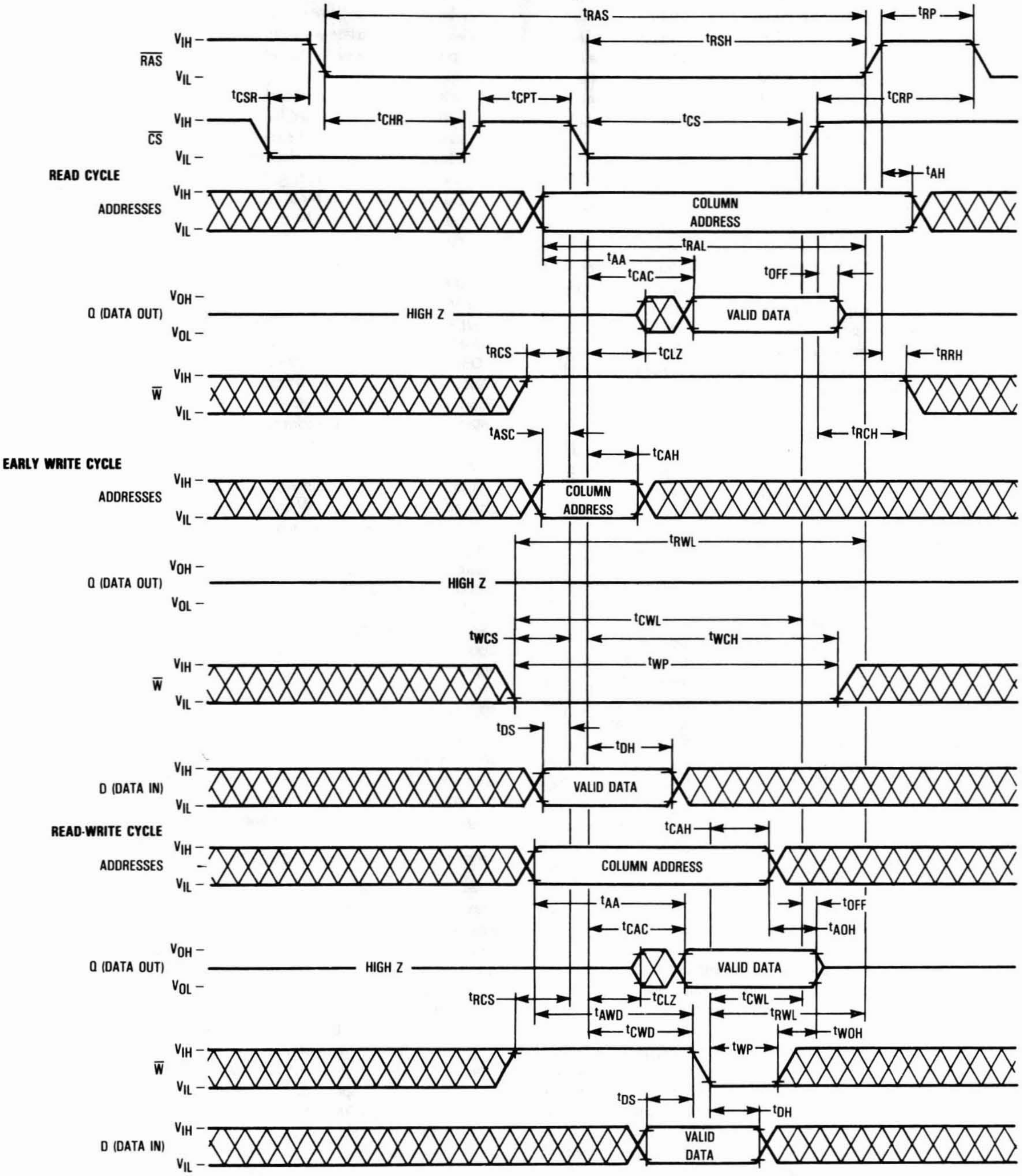
HIDDEN REFRESH CYCLE (READ)


tRC
tRC
tRP
tRP
tRAS
tRAS
RAS
VIH
VIL
tRCD
tRSH
tCRP
tAR
tCHR
tCRP
CS
tRAH
tASR
tAH
tRAD
tRAL
ADDRESSES
ROW ADD
COLUMN ADDRESS
tRCS
tRRH
W
tCAC
tAA
tRAC
tOFF
Q (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA
tCLZ

HIDDEN REFRESH CYCLE (EARLY WRITE)


tRC
tRC
tRAS
tRP
tRP
tAR
tRAS
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCRP
CS
tRAH
tASC
tASR
tCAH
tRAD
ADDRESSES
ROW ADD
COL ADD
tWCS
tWCH
W
tDS
tDH
D (DATA IN)
VALID DATA
tDHR
Q (DATA OUT)
VOH
VOL
HIGH Z

$\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



tRAS
tRP
tRSH
VIH
RAS
VIL
tCSR
tCPT
tCRP
tCHR
tCS
CS
READ CYCLE
tAH
ADDRESSES
COLUMN ADDRESS
tRAL
tAA
tCAC
tOFF
VOH
Q (DATA OUT)
HIGH Z
VALID DATA
VOL
tRCS
tCLZ
tRRH
W
tASC
tRCH
tCAH
EARLY WRITE CYCLE
tRWL
tCWL
tWCS
tWCH
tWP
tDS
tDH
D (DATA IN)
READ-WRITE CYCLE
tAOH
tAWD
tCWD
tWOH
VALID DATA

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by the row address strobe ($\overline{RAS}$) clock, into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{RAS}$ active transition latches the row address field. Column addresses are not latched, hence the "static column" designation of this device. Chip select ($\overline{CS}$) active transition (active = V_{IL}, t_{RCD} minimum) follows $\overline{RAS}$ on all read, write, or read-write cycles, and is independent of column address. The static column feature allows greater flexibility in setting up the external external column addresses into the RAM.

There are other variations in addressing the 1M RAM: **$\overline{RAS}$ only refresh cycle** and **$\overline{CS}$ before $\overline{RAS}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: random read cycle, read-write cycle, and "static column mode" read, and read-write. The random read cycle is outlined here, while the other cycles are discussed in separate sections.

The random read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ active transition latching the desired row. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CS}$ active transition, to enable read mode. A valid column address can be provided at any time (t_{RAD} minimum), independent of the $\overline{CS}$ active transition.

Both the $\overline{RAS}$ and $\overline{CS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. $\overline{CS}$ must be active and column address must be valid by t_{RCD} and t_{RAD} maximums, respectively, to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If either t_{RCD} or t_{RAD} maximum is exceeded, read access time is determined by the $\overline{CS}$ clock active transition (t_{CAC}) and/or valid column address (t_{AA}).

The $\overline{RAS}$ and $\overline{CS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CS}, respectively, to complete the read cycle. The column address must remain valid for t_{AH} after $\overline{RAS}$ inactive transition to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CS}$ clock is active. When the $\overline{CS}$ clock transitions to inactive, the output will switch to High Z.

WRITE CYCLE

The DRAM may be written with any of four cycles: early write, late write and "static column mode" early write, and read-write. Early and late write modes are discussed here, while static column mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL} level). Early and late write modes are distinguished by the active transition of $\overline{W}$ with respect to $\overline{CS}$ leading edge. Minimum active time t_{RAS} and t_{CS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CS}$ active transition. Column address set up and hold times (t_{ASC}, t_{CAH}), and data in (D) set up and hold times (t_{DS}, t_{DH}) are referenced to $\overline{CS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CS}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{W}$ active transition is made after $\overline{CS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. Column address and D timing parameters are referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CS}$ active transition but Q may be indeterminate—see note 18 of AC operating conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

STATIC COLUMN MODE CYCLES

Static column mode refers to multiple successive data operations performed at any or all 1024 column locations on the selected row of the 1M dynamic RAM during one $\overline{RAS}$ cycle. Read access time of multiple operations (t_{AA} or t_{CAC}) is considerably faster than the regular $\overline{RAS}$ clock access time t_{RAC}. Multiple operations can be performed simply by keeping $\overline{RAS}$ active. $\overline{CS}$ may be toggled between active and inactive states at any time within the $\overline{RAS}$ cycle.

Once the timing requirements for the initial read, write, or read-write cycle are met and $\overline{RAS}$ remains low, the device is ready for the next operation. Operations can be intermixed in any order, at any column address, subject to normal operating conditions previously described. Every write operation must be clocked with either $\overline{CS}$ or $\overline{W}$, as indicated in **static column mode early write cycle** timing diagrams **A** and **B**. Column address and D timing parameters are referenced to the signal clocking the write operation. $\overline{\text{CS}}$ must be toggled inactive (t_{CP}) to perform a read operation after an early write operation (to turn output on), as indicated in **static column mode read/write mixed cycle** timing diagram. The maximum number of consecutive operations is limited by t_{RASC}. The cycle ends when $\overline{\text{RAS}}$ transitions to inactive.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM511002A require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM511002A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM511002A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$ only refresh, $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

$\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh counter test.** This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
5. Read "0"s which were written at in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

TEST MODE

Internal organization of this device (256K × 4) allows it to be tested as if it were a 256K × 1 DRAM. Only nine of the ten addresses (A0–A8) are used in test mode; A9 is internally disabled. A test mode write cycle writes data, D (data in), to a bit in each of the four 256K × 1 blocks (B0–B3), in parallel. A test mode read cycle reads a bit in each of the four blocks. If data is the same in all four bits, Q (data out) is the same as the data in each bit. If data is not the same in all four bits, Q is high Z. See truth table and block diagram.

Test mode can be used in any timing cycle, including page mode cycles. The test mode function is enabled by holding the "TF" pin on "super voltage" for the specified period (t_{TES}, t_{TEHR}, t_{TEHC}; see TEST MODE CYCLE).

$$\text{"Super voltage"} = V_{CC} + 4.5\ \text{V}$$

where

$4.5\ \text{V} < V_{CC} < 5.5\ \text{V}$ and maximum voltage = 10.5 V.

A9 is ignored in test mode. In normal operation, the "TF" pin must either be connected to V_{IL}, or left open.

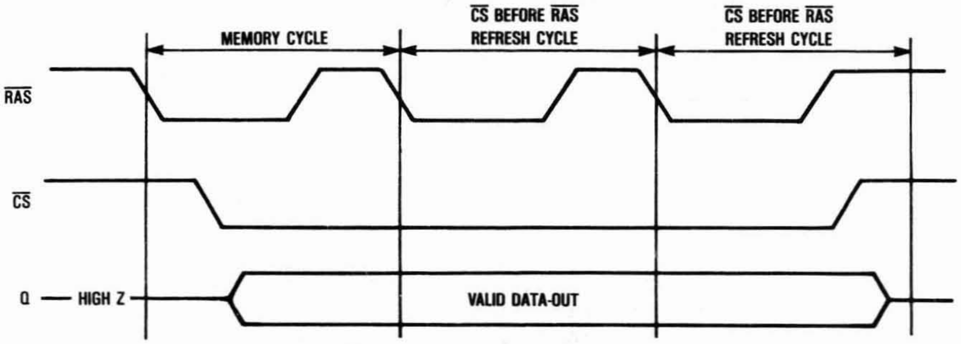
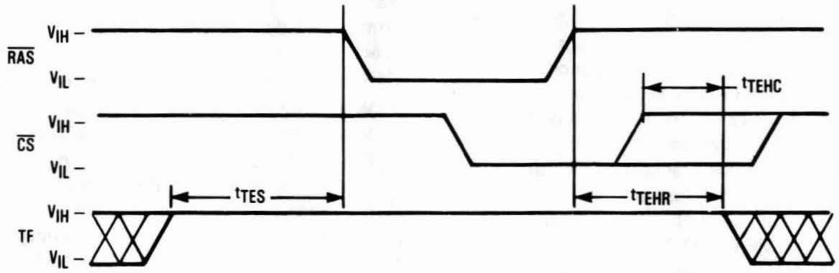


Figure 1. Hidden Refresh Cycle

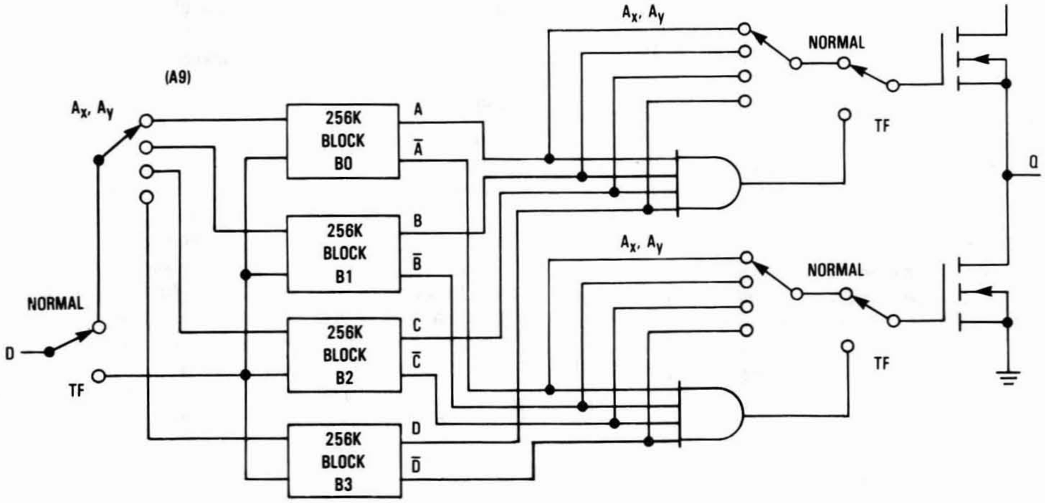
Test Mode Truth Table

D	B0	B1	B2	B3	Q
0	0	0	0	0	0
1	1	1	1	1	1
—	Any Other				High-Z

TEST MODE CYCLE


RAS
CS
TF
VIH –
VIL –
tTES
tTEHR
tTEHC

TEST FUNCTION BLOCK DIAGRAM


(A9)
Ax, Ay
NORMAL
D
TF
256K BLOCK B0
256K BLOCK B1
256K BLOCK B2
256K BLOCK B3
A
Ā
B
B̄
C
C̄
D
D̄
Ax, Ay
NORMAL
TF
Ax, Ay
NORMAL
TF
Q

ORDERING INFORMATION
(Order by Full Part Number)

MCM 511002A X XX XX

Motorola Memory Prefix — MCM

Part Number — 511002A

Package (P = 300 mil Plastic DIP, J = 300 mil SOJ, Z = Plastic ZIP) — X

Speed (70 = 70 ns, 80 = 80 ns, 10 = 100 ns) — XX

Shipping Method (R2 = Tape & Reel, Blank = Rails) — XX

Full Part Numbers—			
MCM511002AP70	MCM511002AJ70	MCM511002AJ70R2	MCM511002AZ70
MCM511002AP80	MCM511002AJ80	MCM511002AJ80R2	MCM511002AZ80
MCM511002AP10	MCM511002AJ10	MCM511002AJ10R2	MCM511002AZ10

NOTE: For mechanical data, please see Chapter 10.

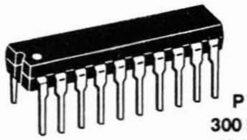
MCM514256A
MCM51L4256A

256K x 4 Bit CMOS Dynamic RAM
Page Mode, Commercial and Industrial Temperature Range

The MCM514256A is a 1.0μ CMOS high-speed dynamic random access memory. It is organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM514256A requires only nine address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil dual-in-line package (DIP), a 300 mil SOJ plastic package, and a 100 mil zig-zag in-line package (ZIP).

- Two Temperature Ranges:
  Commercial: 0°C to 70°C
  Industrial: – 40°C to +85°C
- Three-State Data Output
- Fast Page Mode
- TTL-Compatible Inputs and Output
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM514256A = 8 ms
  MCM51L4256A = 64 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM514256A-70 and MCM51L4256A-70 = 70 ns (Max)
  MCM514256A-80 and MCM51L4256A-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM514256A-70 and MCM51L4256A-70 = 440 mW (Max)
  MCM514256A-80 and MCM51L4256A-80 = 385 mW (Max)
- Low Standby Power Dissipation:
  MCM514256A and MCM51L4256A = 11 mW (Max), TTL Levels
  MCM514256A = 5.5 mW (Max), CMOS Levels
  MCM51L4256A = 1.1 mW (Max), CMOS Levels



P PACKAGE
300 MIL PLASTIC
CASE 738A-01

N PACKAGE
300 MIL SOJ
CASE 822-03

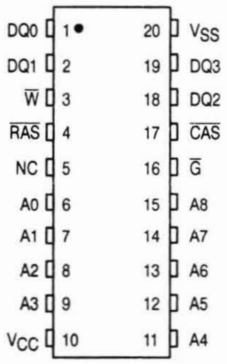
Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836-02

PIN NAMES

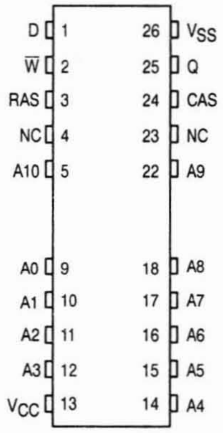
A0 – A8	Address Input
DQ0 – DQ3	Data Input/Output
$\overline{\text{G}}$	Output Enable
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENTS

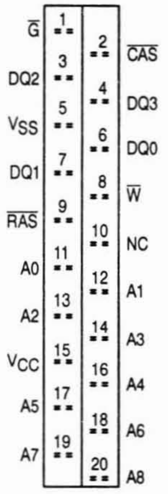
DUAL-IN-LINE


DQ0 1
DQ1 2
W 3
RAS 4
NC 5
A0 6
A1 7
A2 8
A3 9
VCC 10
20 VSS
19 DQ3
18 DQ2
17 CAS
16 G
15 A8
14 A7
13 A6
12 A5
11 A4

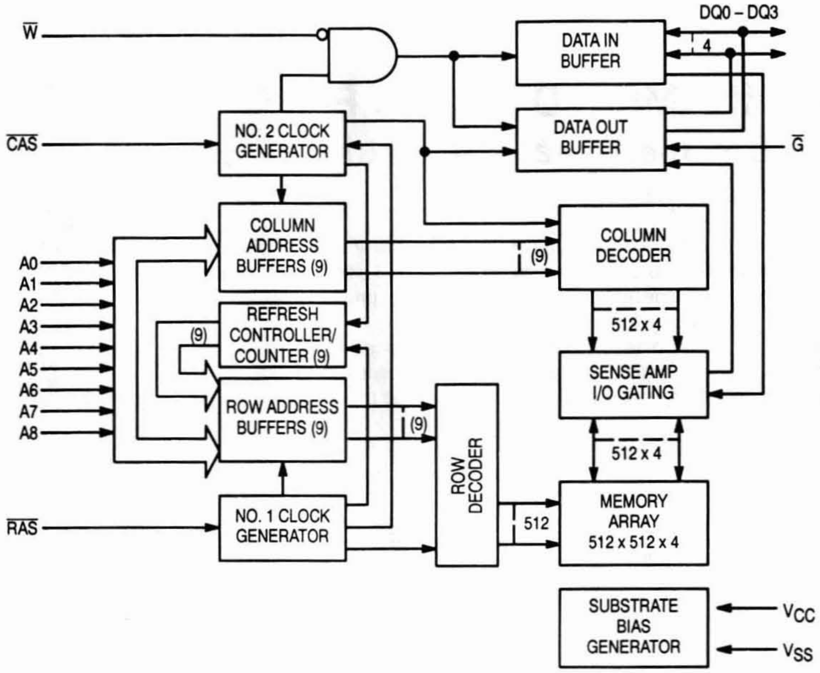
SMALL OUTLINE


D 1
W 2
RAS 3
NC 4
A10 5
A0 9
A1 10
A2 11
A3 12
VCC 13
26 VSS
25 Q
24 CAS
23 NC
22 A9
18 A8
17 A7
16 A6
15 A5
14 A4

ZIG-ZAG IN-LINE


G 1
2 CAS
DQ2 3
4 DQ3
VSS 5
6 DQ0
DQ1 7
8 W
RAS 9
10 NC
A0 11
12 A1
A2 13
14 A3
VCC 15
16 A4
A5 17
18 A6
A7 19
20 A8

BLOCK DIAGRAM


W̄
CAS̄
RAS̄
A0
A1
A2
A3
A4
A5
A6
A7
A8
NO. 2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (9)
REFRESH CONTROLLER/ COUNTER (9)
(9)
ROW ADDRESS BUFFERS (9)
NO. 1 CLOCK GENERATOR
ROW DECODER
(9)
512
DATA IN BUFFER
DATA OUT BUFFER
DQ0 – DQ3
4
Ḡ
COLUMN DECODER
(9)
512 x 4
SENSE AMP I/O GATING
512 x 4
MEMORY ARRAY 512 x 512 x 4
SUBSTRATE BIAS GENERATOR
V_{CC}
V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}		V_{in}, V_{out}	– 1 to + 7	V
Data Output Current		I_{out}	50	mA
Power Dissipation		P_D	600	mW
Operating Temperature Range	Commercial Industrial	T_A	0 to + 70 – 40 to + 85	°C
Storage Temperature Range		T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C and – 40 to + 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM514256A-70 and MCM51L4256A-70, t_{RC} = 130 ns, T_A = 0 to 70°C MCM514256A-80 and MCM51L4256A-80, t_{RC} = 150 ns, T_A = 0 to 70°C MCM514256A-C70 and MCM51L4256A-C70, t_{RC} = 130 ns, T_A = – 40 to + 85°C MCM514256A-C80 and MCM51L4256A-C80, t_{RC} = 150 ns, T_A = – 40 to + 85°C	I_{CC1}	 — — — —	 80 70 85 75	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) MCM514256A and MCM51L4256A, T_A = 0 to 70°C MCM514256A-C and MCM51L4256A-C, T_A = – 40 to + 85°C	I_{CC2}	 — —	 2 3	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles ($\overline{CAS}$ = V_{IH}) MCM514256A-70 and MCM51L4256A-70, t_{RC} = 130 ns, T_A = 0 to 70°C MCM514256A-80 and MCM51L4256A-80, t_{RC} = 150 ns, T_A = 0 to 70°C MCM514256A-C70 and MCM51L4256A-C70, t_{RC} = 130 ns, T_A = – 40 to + 85°C MCM514256A-C80 and MCM51L4256A-C80, t_{RC} = 150 ns, T_A = – 40 to + 85°C	I_{CC3}	 — — — —	 80 70 85 75	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL}) MCM514256A-70 and MCM51L4256A-70, t_{PC} = 40 ns, T_A = 0 to 70°C MCM514256A-80 and MCM51L4256A-80, t_{PC} = 45 ns, T_A = 0 to 70°C MCM514256A-C70 and MCM51L4256A-C70, t_{PC} = 40 ns, T_A = – 40 to + 85°C MCM514256A-C80 and MCM51L4256A-C80, t_{PC} = 45 ns, T_A = – 40 to + 85°C	I_{CC4}	 — — — —	 60 50 65 55	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM514256A, T_A = 0 to 70°C and MCM514256A-C, T_A = – 40 to + 85°C MCM51L4256A, T_A = 0 to 70°C MCM51L4256A-C, T_A = – 40 to + 85°C	I_{CC5}	 — — —	 1.0 200 400	 mA µA µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM514256A-70 and MCM51L4256A-70, t_{RC} = 130 ns, T_A = 0 to 70°C MCM514256A-80 and MCM51L4256A-80, t_{RC} = 150 ns, T_A = 0 to 70°C MCM514256A-C70 and MCM51L4256A-C70, t_{RC} = 130 ns, T_A = – 40 to + 85°C MCM514256A-C80 and MCM51L4256A-C80, t_{RC} = 150 ns, T_A = – 40 to + 85°C	I_{CC6}	 — — — —	 80 70 85 75	mA	1
V_{CC} Power Supply Current, Battery Backup Mode (t_{RC} = 125 µs, t_{RAS} = 1 µs, $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V, A0 – A9, $\overline{W}$, D = V_{CC} – 0.2 V or 0.2 V) MCM51L4256A, T_A = 0 to 70°C MCM51L4256A-C, T_A = – 40 to + 85°C	I_{CC5}	 — —	 300 500	µA	1
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	–10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V, Output Disable)	$I_{lkg(O)}$	–10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A8	C_{in}	5	pF
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0 – DQ3	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C and – 40 to + 85°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514256A-70 MCM51L4256A-70		MCM514256A-80 MCM51L4256A-80			
	Std	Alt	Min	Max	Min	Max	Unit	Notes
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RMW}	185	—	205	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRMW}	95	—	100	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	70	—	80	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	6, 9
Access Time from $\overline{CAS}$ Precharge	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Page Mode Cycle Only)	t_{CELREH}	t_{RHCP}	35	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C and – 40 to + 85°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) and/or t_{GZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

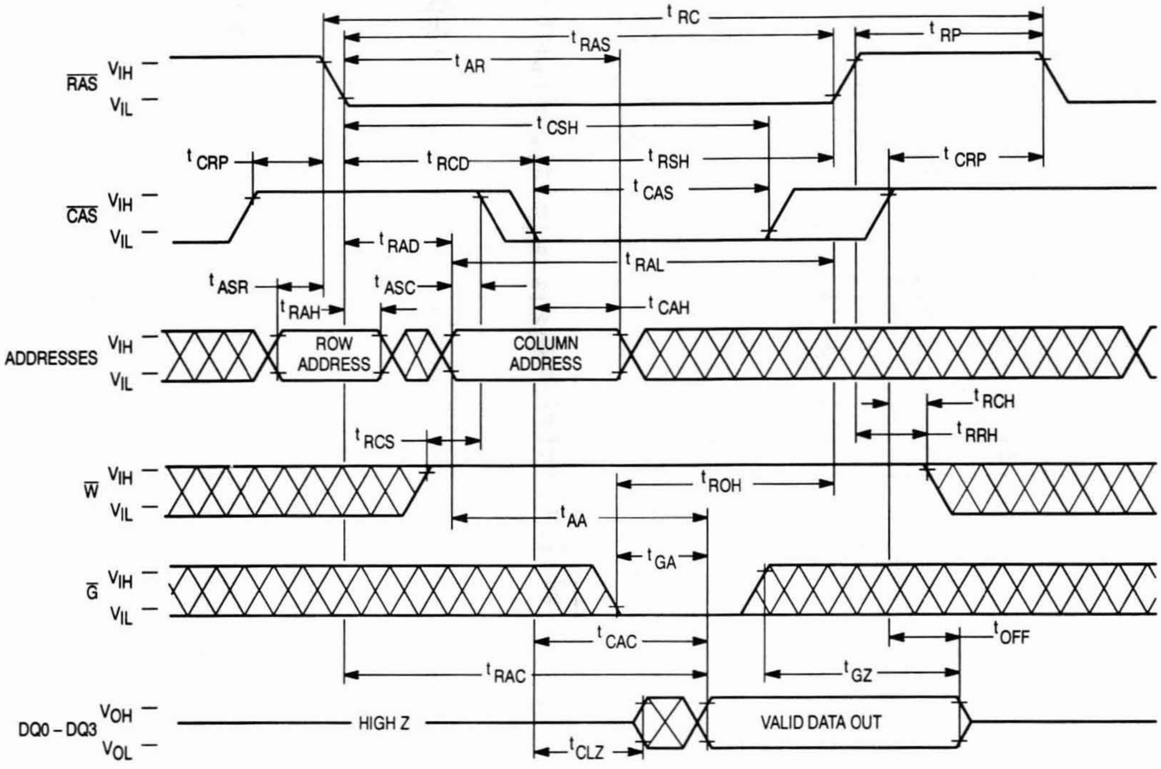
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM514256A-70 MCM51L4256A-70		MCM514256A-80 MCM51L4256A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELAX}	t_{AR}	55	—	60	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	15	—	15	—	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELWH}	t_{WCR}	55	—	60	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	55	—	60	—	ns	
Refresh Period MCM514256A MCM51L4256A	t_{RVRV}	t_{RFSH}	— —	8 64	— —	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	ns	15
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	100	—	110	—	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	65	—	70	—	ns	15
$\overline{\text{CAS}}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	65	—	70	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	ns	
$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{G}}$	t_{GLREH}	t_{ROH}	10	—	10	—	ns	
$\overline{\text{G}}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	20	ns	
$\overline{\text{G}}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{\text{G}}$	t_{GHQZ}	t_{GZ}	0	20	0	20	ns	10
$\overline{\text{G}}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	ns	

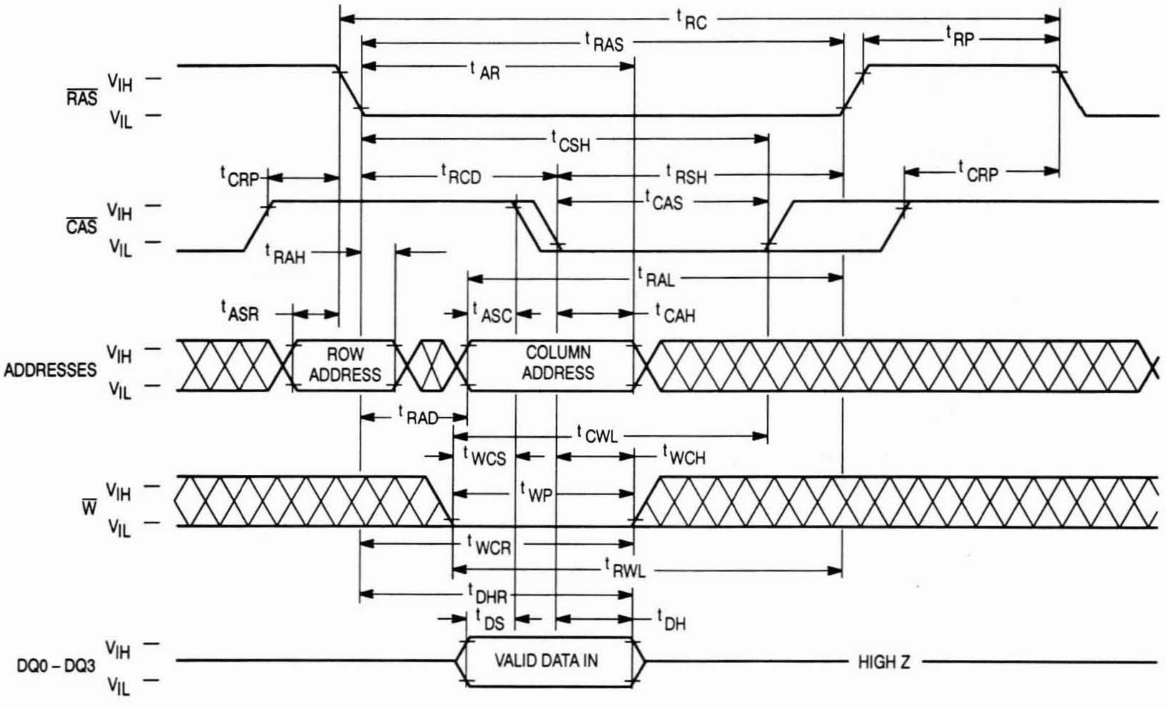
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in delayed write or read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

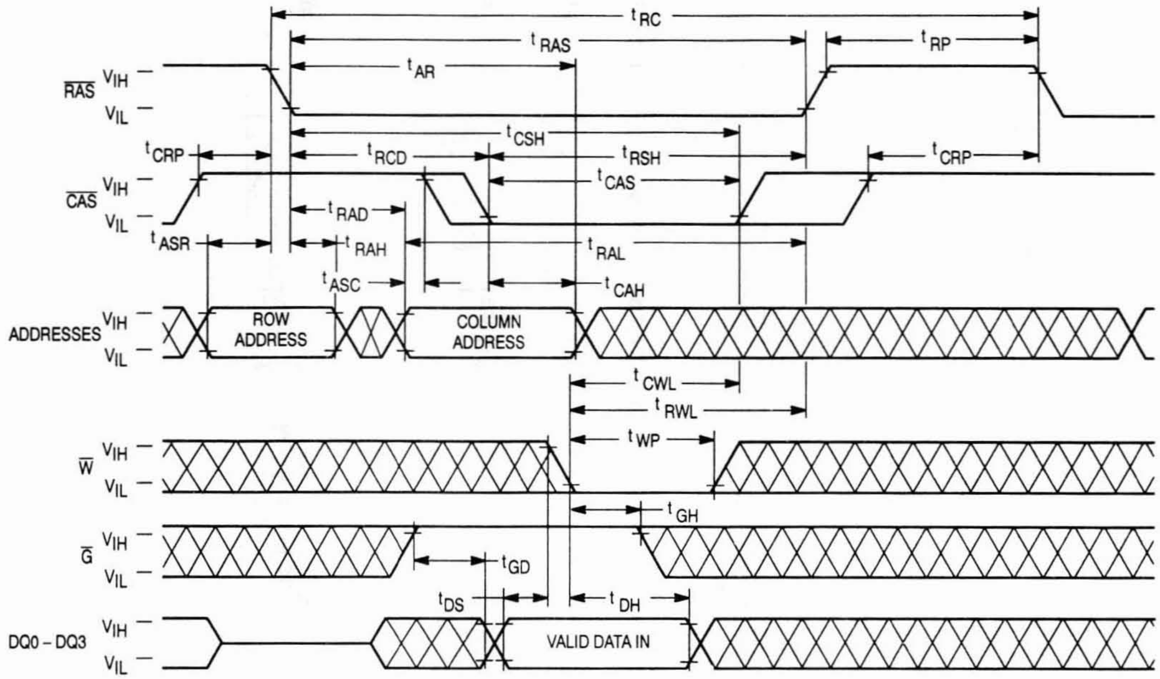
READ CYCLE


t_{RC}
t_{RAS}
t_{RP}
t_{AR}
$\overline{RAS}$ V_{IH} V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$ V_{IH} V_{IL}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES V_{IH} V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RCH}
t_{RCS}
t_{RRH}
$\overline{W}$ V_{IH} V_{IL}
t_{ROH}
t_{AA}
t_{GA}
$\overline{G}$ V_{IH} V_{IL}
t_{CAC}
t_{OFF}
t_{RAC}
t_{GZ}
DQ0 – DQ3 V_{OH} V_{OL}
HIGH Z
VALID DATA OUT
t_{CLZ}

EARLY WRITE CYCLE


t_{RC}
t_{RAS}
t_{RP}
t_{AR}
$\overline{RAS}$ V_{IH} V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$ V_{IH} V_{IL}
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
ADDRESSES V_{IH} V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RAD}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{W}$ V_{IH} V_{IL}
t_{WCR}
t_{RWL}
t_{DHR}
t_{DS}
t_{DH}
DQ0 – DQ3 V_{IH} V_{IL}
VALID DATA IN
HIGH Z

$\overline{\text{G}}$ CONTROLLED LATE WRITE CYCLE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t AR
RAS VIH
VIL
t CSH
t CRP
t RCD
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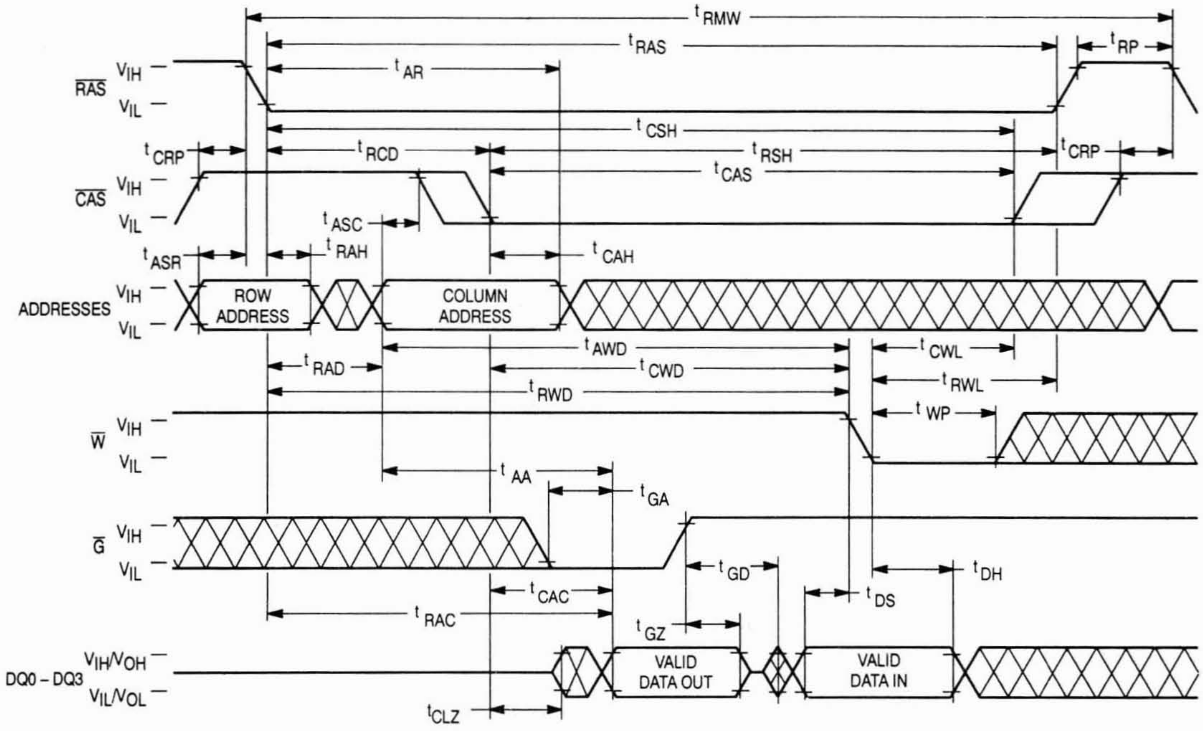
t CRP
t CAS
CAS VIH
VIL
t RAD
t ASR
t RAH
t RAL
t ASC
t CAH
ADDRESSES VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
t CWL
t RWL
t WP
W VIH
VIL
t GH
G VIH
VIL
t GD
t DS
t DH
DQ0 – DQ3 VIH
VIL
VALID DATA IN

READ-WRITE CYCLE


t RMW
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t AR
RAS VIH
VIL
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t CRP
t RCD
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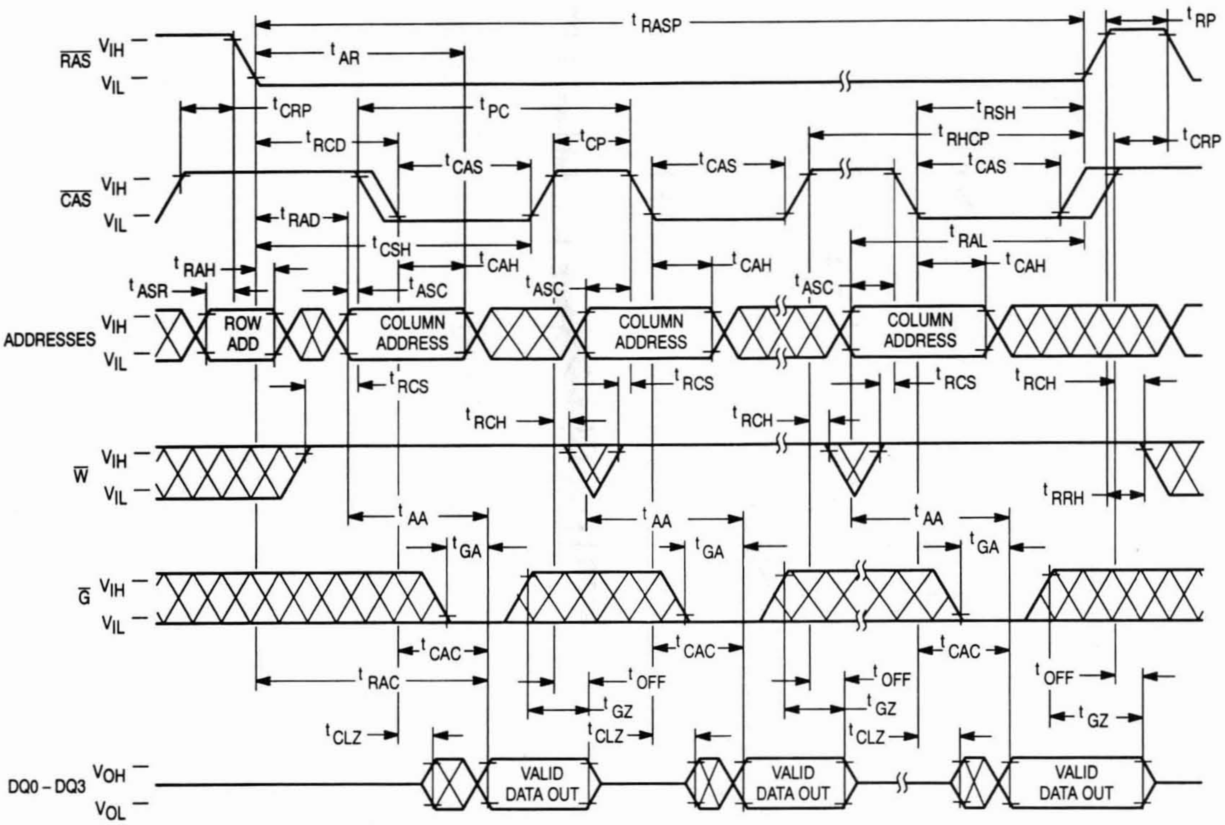
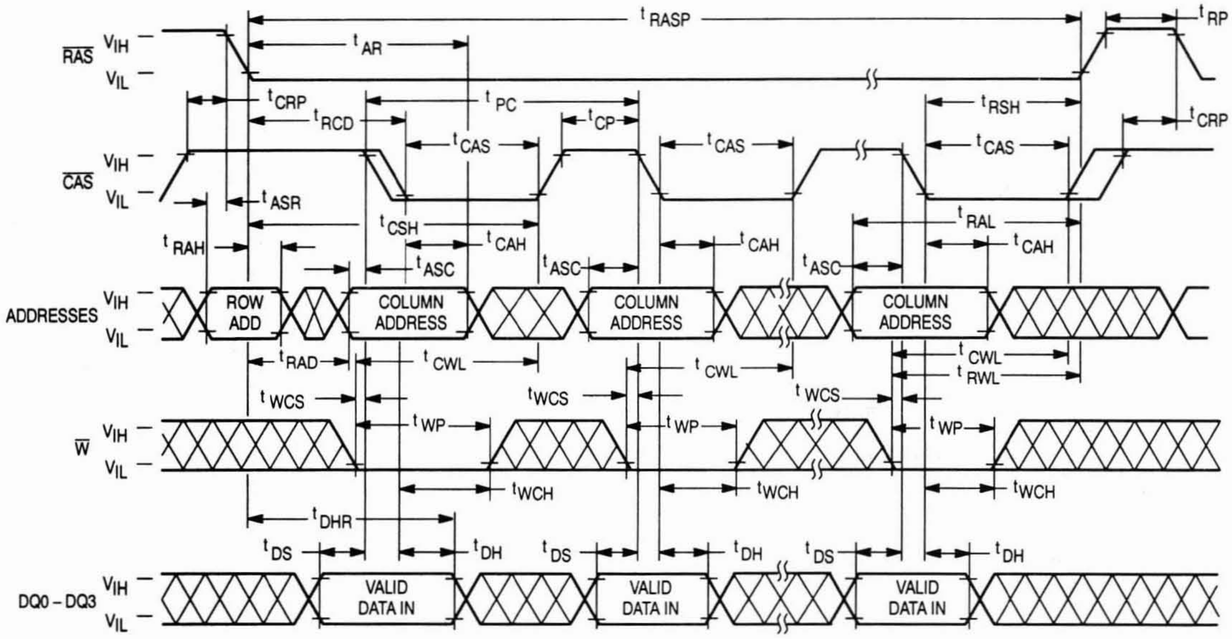
t CRP
t CAS
CAS VIH
VIL
t ASC
t ASR
t RAH
t CAH
ADDRESSES VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
t AWD
t CWL
t RAD
t CWD
t RWL
t RWD
t WP
W VIH
VIL
t AA
t GA
G VIH
VIL
t GD
t DH
t CAC
t DS
t RAC
t GZ
DQ0 – DQ3 VIH/VOH
VIL/VOL
VALID DATA OUT
VALID DATA IN
t CLZ

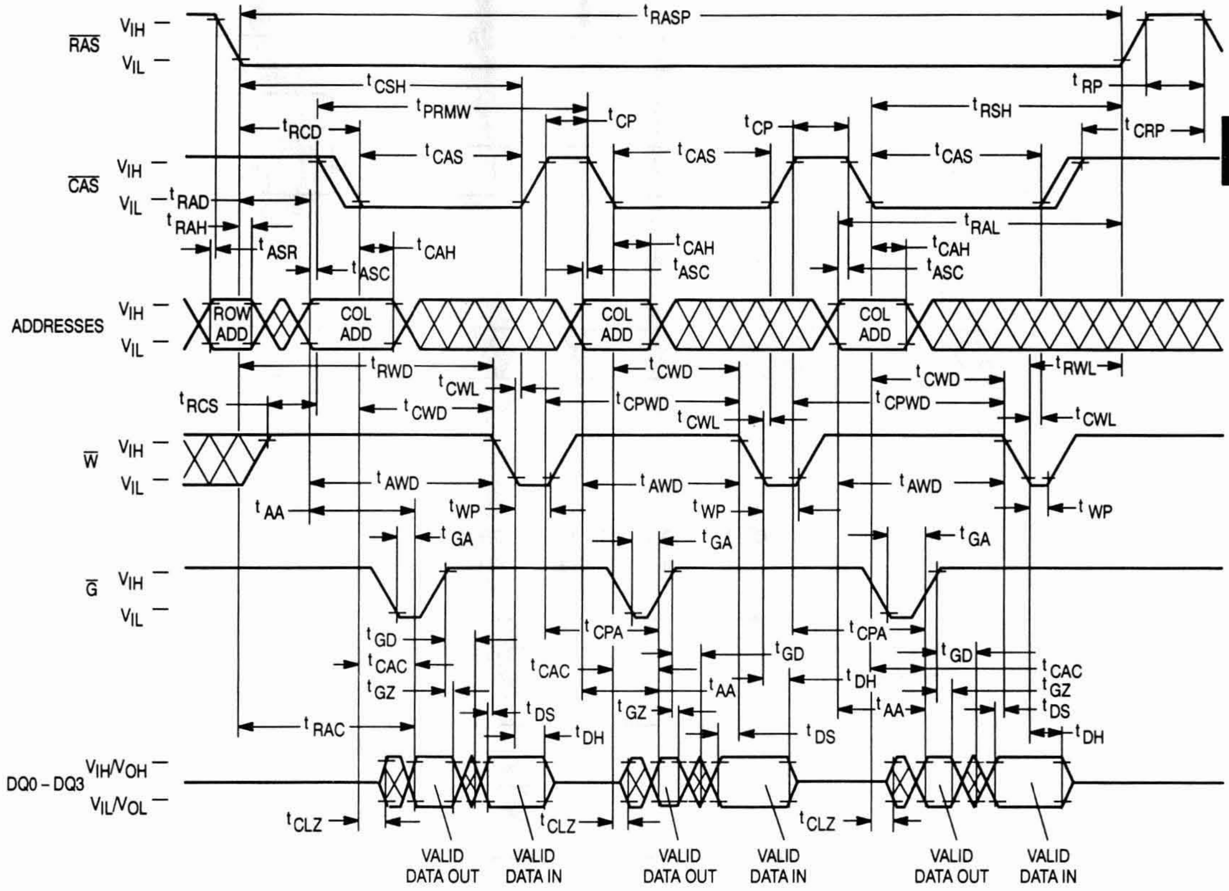
FAST PAGE MODE READ CYCLE


RAS
VIH
VIL
tRASP
tRP
tAR
tCRP
tPC
tRSH
tRCD
tRHCP
tCP
tCAS
tCRP
CAS
VIH
VIL
tRAD
tRAL
tCSH
tCAH
tRAH
tASR
tASC
ADDRESSES
ROW ADD
COLUMN ADDRESS
tRCS
tRCH
W
tRRH
tAA
tGA
G
tCAC
tRAC
tOFF
tGZ
tCLZ
DQ0 – DQ3
VOH
VOL
VALID DATA OUT

FAST PAGE MODE EARLY-WRITE CYCLE

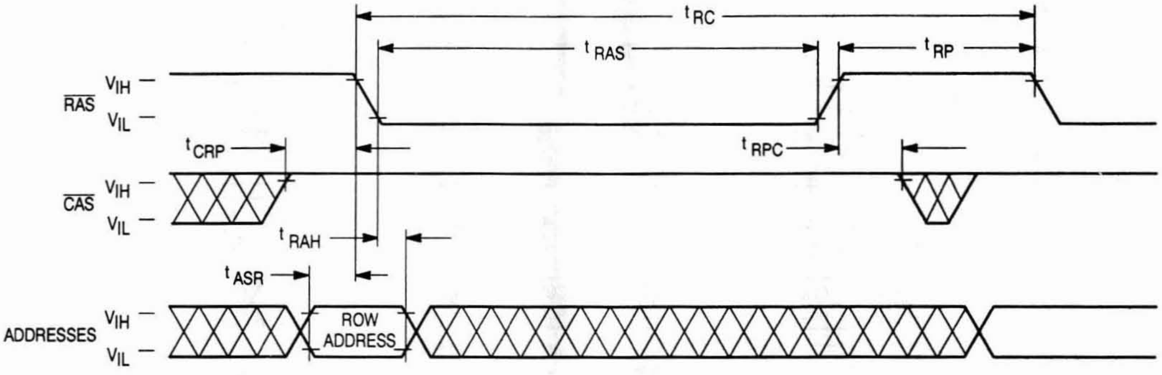

RAS
VIH
VIL
tRASP
tRP
tAR
tCRP
tPC
tRCD
tCP
tRSH
tCAS
tCRP
CAS
VIH
VIL
tASR
tCSH
tRAL
tRAH
tCAH
tASC
ADDRESSES
ROW ADD
COLUMN ADDRESS
tRAD
tCWL
tRWL
tWCS
tWP
W
tWCH
tDHR
tDS
tDH
DQ0 – DQ3
VALID DATA IN

FAST PAGE MODE READ-WRITE CYCLE


RAS
VIH
VIL
CAS
ADDRESSES
W
G
DQ0 – DQ3
VIH/VOH
VIL/VOL
tRASP
tCSH
tPRMW
tRCD
tCP
tRSH
tRP
tCRP
tCAS
tRAD
tRAH
tASR
tCAH
tASC
tRAL
ROW ADD
COL ADD
tRWD
tCWL
tCWD
tCPWD
tRCS
tRWL
tAWD
tAA
tWP
tGA
tGD
tCAC
tGZ
tCPA
tDH
tDS
tRAC
tCLZ
VALID DATA OUT
VALID DATA IN

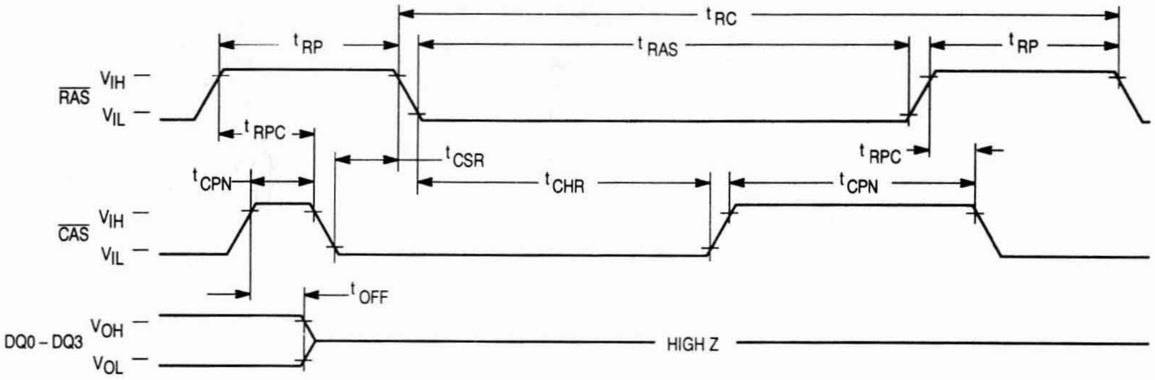
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

($\overline{\text{W}}$ and $\overline{\text{G}}$ are Don't Care)

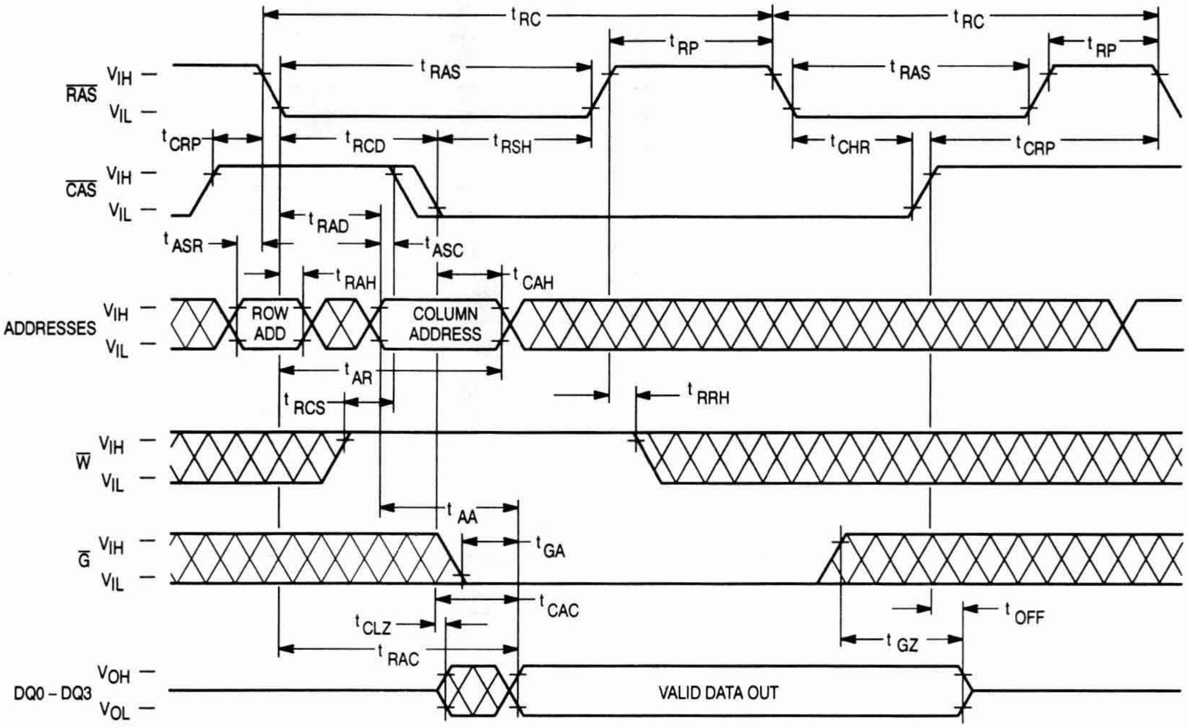

t RC
t RAS
t RP
RAS
VIH
VIL
t CRP
t RPC
CAS
VIH
VIL
t RAH
t ASR
ADDRESSES
VIH
VIL
ROW
ADDRESS

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{W}}$, $\overline{\text{G}}$, and A0 – A8 are Don't Care)


t RC
t RP
t RAS
t RP
RAS
VIH
VIL
t RPC
t CSR
t RPC
t CPN
t CHR
t CPN
CAS
VIH
VIL
t OFF
DQ0 – DQ3
VOH
VOL
HIGH Z

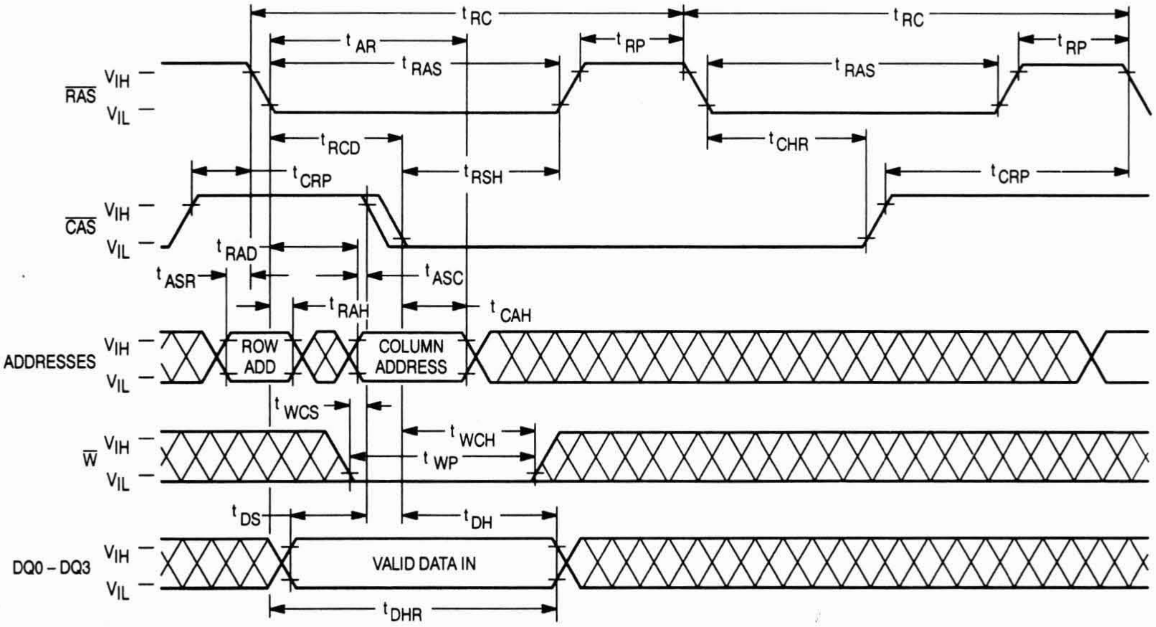
HIDDEN REFRESH CYCLE (READ)



t_{RC}
t_{RC}
t_{RP}
t_{RP}
$\overline{RAS}$ V_{IH} –
V_{IL} –
t_{RAS}
t_{RAS}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CRP}
$\overline{CAS}$ V_{IH} –
V_{IL} –
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES V_{IH} –
V_{IL} –
ROW ADD
COLUMN ADDRESS
t_{AR}
t_{RCS}
t_{RRH}
$\overline{W}$ V_{IH} –
V_{IL} –
t_{AA}
$\overline{G}$ V_{IH} –
V_{IL} –
t_{GA}
t_{CAC}
t_{CLZ}
t_{OFF}
t_{GZ}
t_{RAC}
DQ0 – DQ3 V_{OH} –
V_{OL} –
VALID DATA OUT

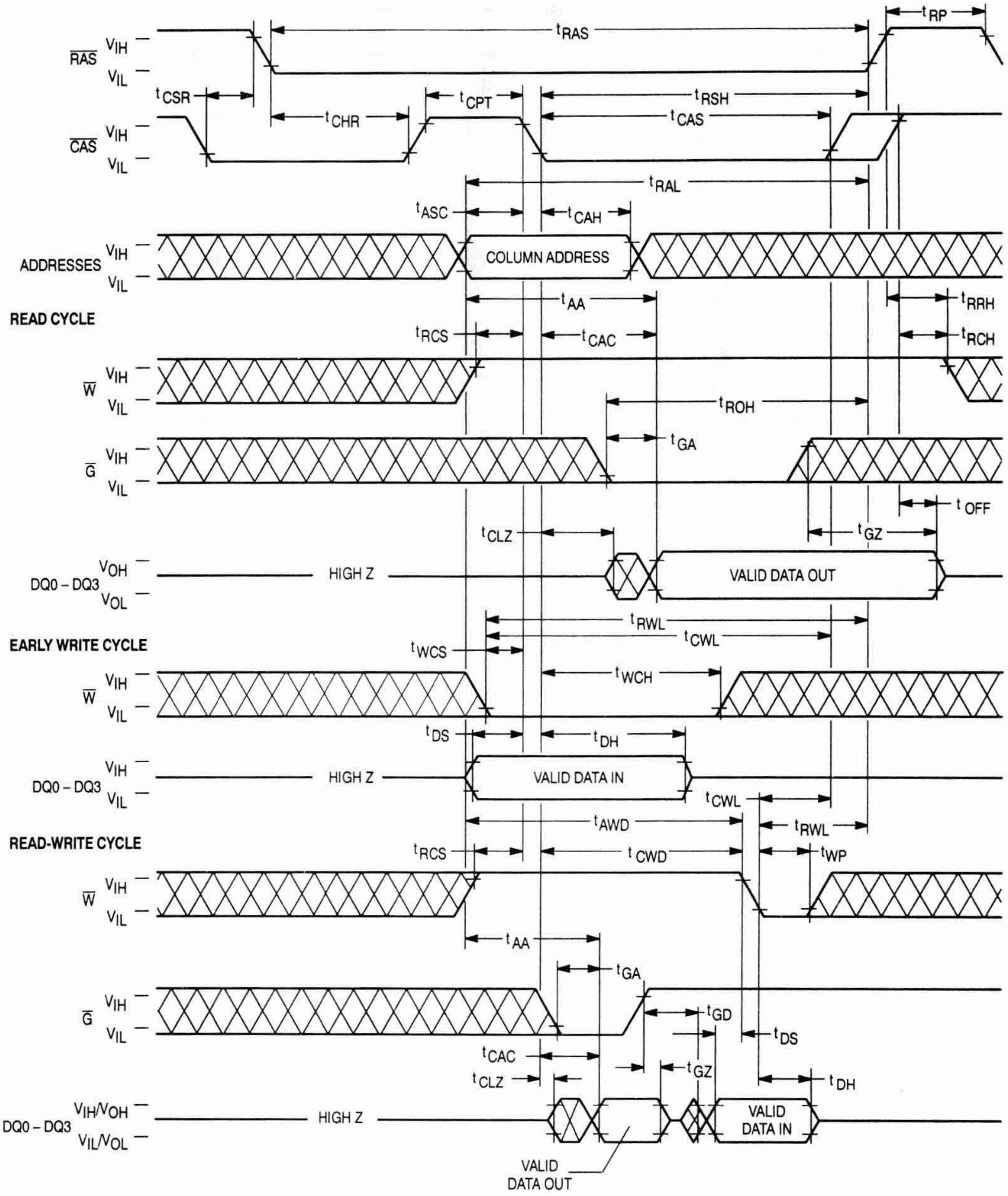
2

HIDDEN REFRESH CYCLE (EARLY WRITE)



t_{RC}
t_{RC}
t_{AR}
t_{RP}
t_{RP}
t_{RAS}
t_{RAS}
$\overline{RAS}$ V_{IH} –
V_{IL} –
t_{RCD}
t_{CHR}
t_{CRP}
t_{RSH}
t_{CRP}
$\overline{CAS}$ V_{IH} –
V_{IL} –
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES V_{IH} –
V_{IL} –
ROW ADD
COLUMN ADDRESS
t_{WCS}
t_{WCH}
t_{WP}
$\overline{W}$ V_{IH} –
V_{IL} –
t_{DS}
t_{DH}
DQ0 – DQ3 V_{IH} –
V_{IL} –
VALID DATA IN
t_{DHR}

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE


$\overline{\text{RAS}}$ V_{IH} V_{IL}
t_{RAS}
t_{RP}
t_{CSR}
t_{CHR}
t_{CPT}
t_{RSH}
t_{CAS}
$\overline{\text{CAS}}$ V_{IH} V_{IL}
t_{RAL}
t_{ASC}
t_{CAH}
ADDRESSES V_{IH} V_{IL}
COLUMN ADDRESS
t_{AA}
t_{RRH}
READ CYCLE
t_{RCS}
t_{CAC}
t_{RCH}
$\overline{\text{W}}$ V_{IH} V_{IL}
t_{ROH}
t_{GA}
$\overline{\text{G}}$ V_{IH} V_{IL}
t_{OFF}
t_{CLZ}
t_{GZ}
DQ0 – DQ3 V_{OH} V_{OL}
HIGH Z
VALID DATA OUT
t_{RWL}
t_{CWL}
EARLY WRITE CYCLE
t_{WCS}
t_{WCH}
$\overline{\text{W}}$ V_{IH} V_{IL}
t_{DS}
t_{DH}
DQ0 – DQ3 V_{IH} V_{IL}
HIGH Z
VALID DATA IN
t_{CWL}
t_{AWD}
t_{RWL}
READ-WRITE CYCLE
t_{RCS}
t_{CWD}
t_{WP}
$\overline{\text{W}}$ V_{IH} V_{IL}
t_{AA}
t_{GA}
$\overline{\text{G}}$ V_{IH} V_{IL}
t_{GD}
t_{DS}
t_{CAC}
t_{CLZ}
t_{GZ}
t_{DH}
DQ0 – DQ3 V_{IH}/V_{OH} V_{IL}/V_{OL}
HIGH Z
VALID DATA IN
VALID DATA OUT

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 bit locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gate feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are two other variations in addressing the 256K x 4 RAM: **$\overline{RAS}$-only refresh cycle** and **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: normal random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{CAS}$ and output enable ($\overline{G}$) control read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum and $\overline{G}$ must be active t_{RAC}-t_{GA} (both minimum) after $\overline{RAS}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{G}$ active transition does not occur in time, read access time is determined by either the $\overline{CAS}$ or $\overline{G}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CAS}$ and $\overline{G}$ clocks are active. When either the $\overline{CAS}$ or $\overline{G}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The DRAM may be written with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data In (D) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data out buffers disabled, effectively disabling $\overline{G}$.

A late write cycle (referred to as $\overline{G}$ controlled write) occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + t_T) \le t_{RAS}$, if timing minimums ($t_{RCD}$, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition but Q may be indeterminate — see note 15 of AC Operating Conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} minimum after the $\overline{CAS}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 512 column locations on a selected row of the 256K x 4 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically refreshed (recharged) to maintain the correct bit state. Bits in the MCM514256A require refresh every 8 milliseconds while refresh time for the MCM51L4256A is 64 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM514256A and 124.8 microseconds for the MCM51L4256A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM514256A and 64 milliseconds on the MCM51L4256A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other mehtods of refresh, **RAS-only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1).

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **eight CAS before RAS** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 512 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

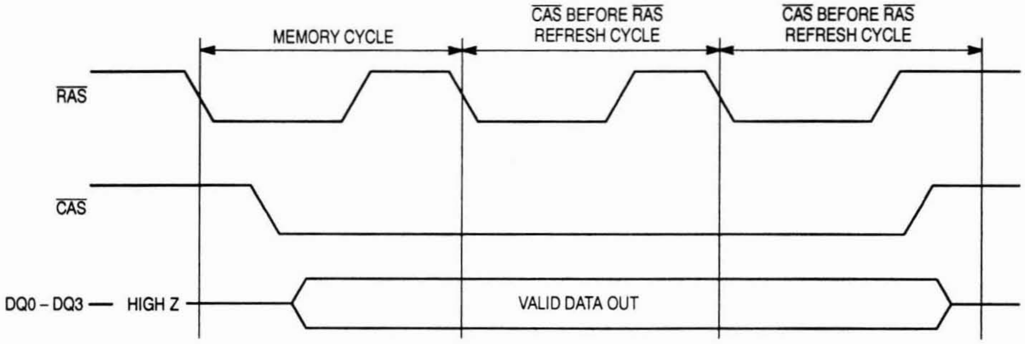


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 514256A or 51L4256A X X XX XX

Motorola Memory Prefix — MCM

Part Number — 514256A or 51L4256A

Shipping Method (R2 = Tape and Reel, Blank = Rails)

Speed (70 = 70 ns, 80 = 80 ns)

Temperature (Blank = 0 to 70°C, C = – 40 to 85°C)

Package (P = 300 mil Plastic DIP, J = 300 mil SOJ, Z = Plastic ZIP)

Commercial Temperature Range 0 to 70°C

Full Part Numbers —	MCM514256AP70	MCM514256AJ70	MCM514256AJ70R2	MCM514256AZ70
	MCM514256AP80	MCM514256AJ80	MCM514256AJ80R2	MCM514256AZ80
	MCM51L4256AP70	MCM51L4256AJ70	MCM51L4256AJ70R2	MCM51L4256AZ70
	MCM51L4256AP80	MCM51L4256AJ80	MCM51L4256AJ80R2	MCM51L4256AZ80

Industrial Temperature Range – 40 to + 85°C

MCM514256APC70	MCM514256AJC70	MCM514256AJC70R2	MCM514256AZC70
MCM514256APC80	MCM514256AJC80	MCM514256AJC80R2	MCM514256AZC80
MCM51L4256APC70	MCM51L426AJC70	MCM51L426AJC70R2	MCM51L4256AZC70
MCM51L4256APC80	MCM51L426AJC80	MCM51L426AJC80R2	MCM51L4256AZC80

NOTE: Low Power Industrial Temperature SOJ device part numbers are one character shorter than corresponding PDIP or ZIP part numbers.

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM514256B
MCM51L4256B

256K x 4 Bit CMOS Dynamic RAM
Page Mode

The MCM514256B is a 0.8µ CMOS high-speed dynamic random access memory. It is organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM514256B requires only nine address lines; row and column address inputs are multiplexed. The device is packaged in a 300 mil SOJ plastic package, and a 100 mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Fast Page Mode
- TTL-Compatible Inputs and Output
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM514256B = 8 ms
  MCM51L4256B = 64 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM514256B-60 and MCM51L4256B-60 = 60 ns (Max)
- Low Active Power Dissipation:
  MCM514256B-60 and MCM51L4256B-60 = 495 mW (Max)
- Low Standby Power Dissipation:
  MCM514256B and MCM51L4256B = 11 mW (Max), TTL Levels
  MCM514256B = 5.5 mW (Max), CMOS Levels
  MCM51L4256B = 1.1 mW (Max), CMOS Levels

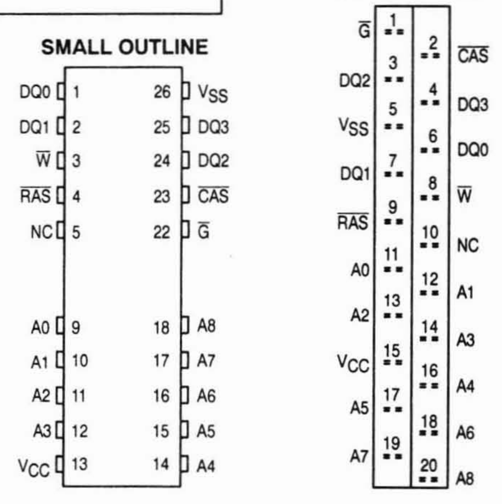
J PACKAGE
300 MIL SOJ
CASE 822-03

Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836-02

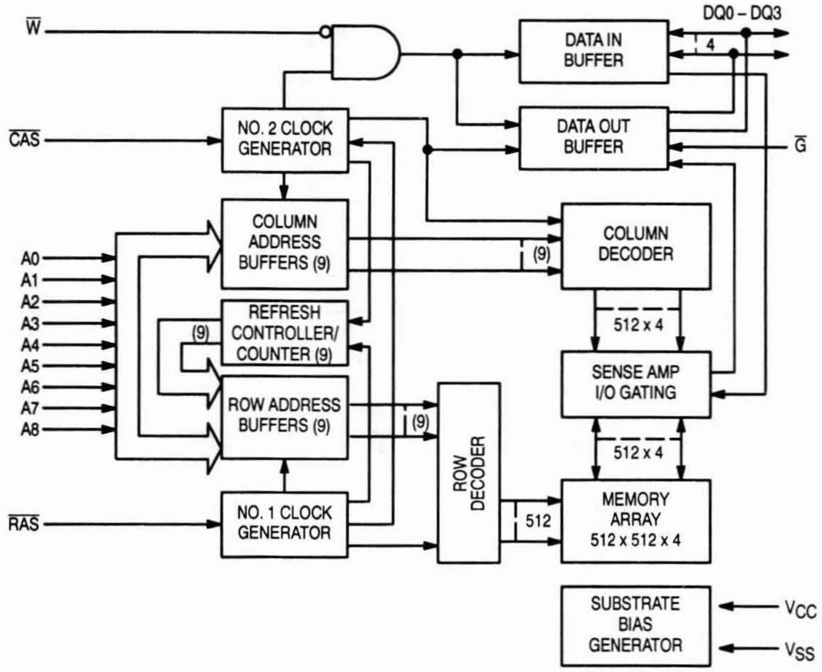
PIN NAMES

A0 – A8	Address Input
DQ0 – DQ3	Data Input/Output
$\overline{\text{G}}$	Output Enable
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENTS


SMALL OUTLINE
ZIG-ZAG IN-LINE
DQ0 1
DQ1 2
W 3
RAS 4
NC 5
A0 9
A1 10
A2 11
A3 12
VCC 13
26 VSS
25 DQ3
24 DQ2
23 CAS
22 G
18 A8
17 A7
16 A6
15 A5
14 A4
G 1
2 CAS
DQ2 3
4 DQ3
VSS 5
6 DQ0
DQ1 7
8 W
RAS 9
10 NC
A0 11
12 A1
A2 13
14 A3
VCC 15
16 A4
A5 17
18 A6
A7 19
20 A8

BLOCK DIAGRAM


W̄
CAS̄
RAS̄
A0
A1
A2
A3
A4
A5
A6
A7
A8
DQ0 – DQ3
4
G̅
NO. 2 CLOCK GENERATOR
DATA IN BUFFER
DATA OUT BUFFER
COLUMN ADDRESS BUFFERS (9)
REFRESH CONTROLLER/ COUNTER (9)
(9)
ROW ADDRESS BUFFERS (9)
NO. 1 CLOCK GENERATOR
(9)
ROW DECODER
COLUMN DECODER
(9)
512 x 4
SENSE AMP I/O GATING
512 x 4
MEMORY ARRAY 512 x 512 x 4
512
SUBSTRATE BIAS GENERATOR
VCC
VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM514256B-60 and MCM51L4256B-60, t_{RC} = 110 ns	I_{CC1}	—	90	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) MCM514256B and MCM51L4256B	I_{CC2}	—	2	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles ($\overline{CAS}$ = V_{IH}) MCM514256B-60 and MCM51L4256B-60, t_{RC} = 110 ns	I_{CC3}	—	90	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL}) MCM514256B-60 and MCM51L4256B-60, t_{PC} = 40 ns	I_{CC4}	—	60	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM514256B MCM51L4256B	I_{CC5}	— —	1.0 200	mA µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM514256B-60 and MCM51L4256B-60, t_{RC} = 110 ns	I_{CC6}	—	90	mA	1
V_{CC} Power Supply Current, Battery Backup Mode (t_{RC} = 125 µs, t_{RAS} = 1 µs, $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V, A0 – A8, $\overline{W}$, D = V_{CC} – 0.2 V or 0.2 V) MCM51L4256B	I_{CC5}	—	300	µA	1
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	–10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V, Output Disable)	$I_{lkg(O)}$	–10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A8	C_{in}	5	pF
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0 – DQ3	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514256B-60 MCM51L4256B-60		Unit	Notes
	Std	Alt	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RMW}	165	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRMW}	95	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	ns	6, 9
Access Time from $\overline{CAS}$ Precharge	t_{CEHQV}	t_{CPA}	—	35	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Page Mode Cycle Only)	t_{CELREH}	t_{RHCP}	35	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	50	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) and/or t_{GZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

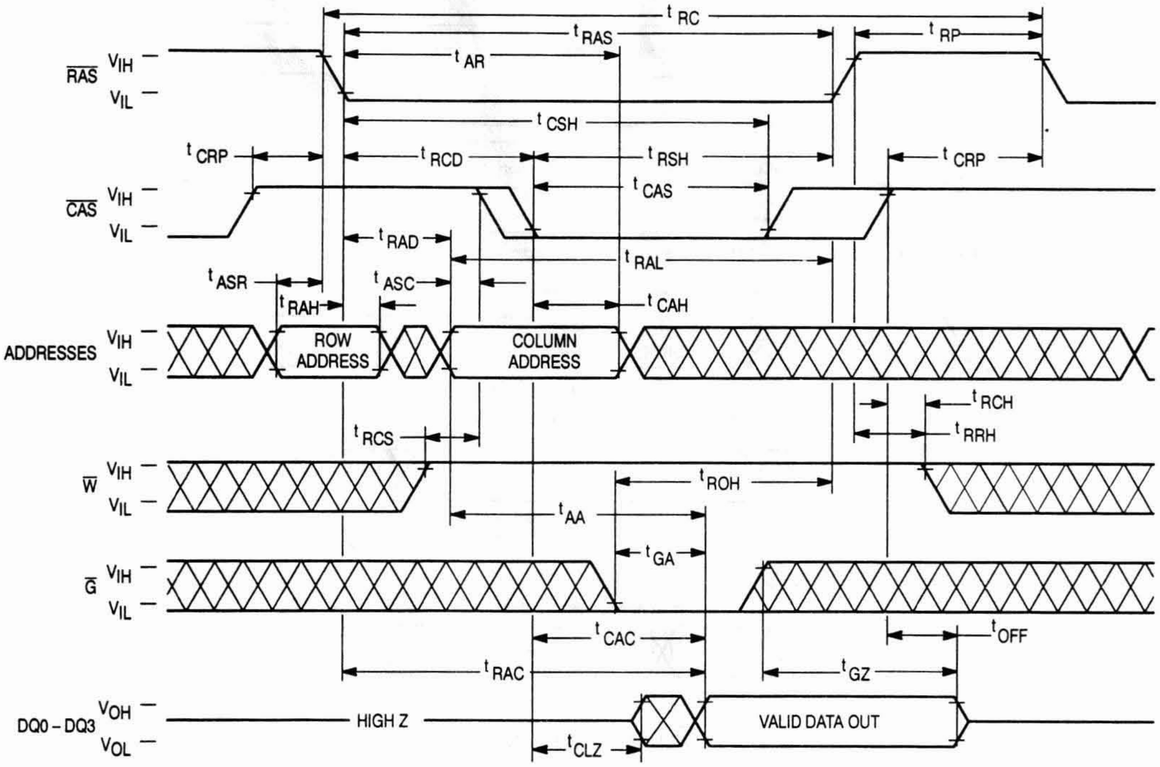
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter		Symbol		MCM514256B-60 MCM51L4256B-60		Unit	Notes
		Std	Alt	Min	Max		
Column Address Hold Time		t_{CELAX}	t_{CAH}	15	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$		t_{RELAX}	t_{AR}	50	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time		t_{AVREH}	t_{RAL}	30	—	ns	
Read Command Setup Time		t_{WHCEL}	t_{RCS}	0	—	ns	
Read Command Hold Time		t_{CEHWX}	t_{RCH}	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$		t_{REHWX}	t_{RRH}	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$		t_{CELWH}	t_{WCH}	10	—	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$		t_{RELWH}	t_{WCR}	45	—	ns	
Write Command Pulse Width		t_{WLWH}	t_{WP}	10	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time		t_{WLREH}	t_{RWL}	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time		t_{WLCEH}	t_{CWL}	20	—	ns	
Data in Setup Time		t_{DVCEL}	t_{DS}	0	—	ns	14
Data in Hold Time		t_{CELDX}	t_{DH}	15	—	ns	14
Data in Hold Time Referenced to $\overline{\text{RAS}}$		t_{RELDX}	t_{DHR}	50	—	ns	
Refresh Period	MCM514256B MCM51L4256B	t_{RVRV}	t_{RFSH}	— —	8 64	ms	
Write Command Setup Time		t_{WLCEL}	t_{WCS}	0	—	ns	15
$\overline{\text{CAS}}$ to Write Delay		t_{CELWL}	t_{CWD}	50	—	ns	15
$\overline{\text{RAS}}$ to Write Delay		t_{RELWL}	t_{RWD}	90	—	ns	15
Column Address to Write Delay Time		t_{AVWL}	t_{AWD}	60	—	ns	15
$\overline{\text{CAS}}$ Precharge to Write Delay		t_{CEHWL}	t_{CPWD}	65	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh		t_{RELCEL}	t_{CSR}	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh		t_{RELCEH}	t_{CHR}	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time		t_{REHCEL}	t_{RPC}	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test		t_{CEHCEL}	t_{CPT}	30	—	ns	
$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{G}}$		t_{GLREH}	t_{ROH}	10	—	ns	
$\overline{\text{G}}$ Access Time		t_{GLQV}	t_{GA}	—	20	ns	
$\overline{\text{G}}$ to Data Delay		t_{GLHDX}	t_{GD}	20	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{\text{G}}$		t_{GHQZ}	t_{GZ}	0	20	ns	10
$\overline{\text{G}}$ Command Hold Time		t_{WLGL}	t_{GH}	20	—	ns	
Output Disable Setup Time		t_{GHCEL}	t_{GS}	0	—	ns	

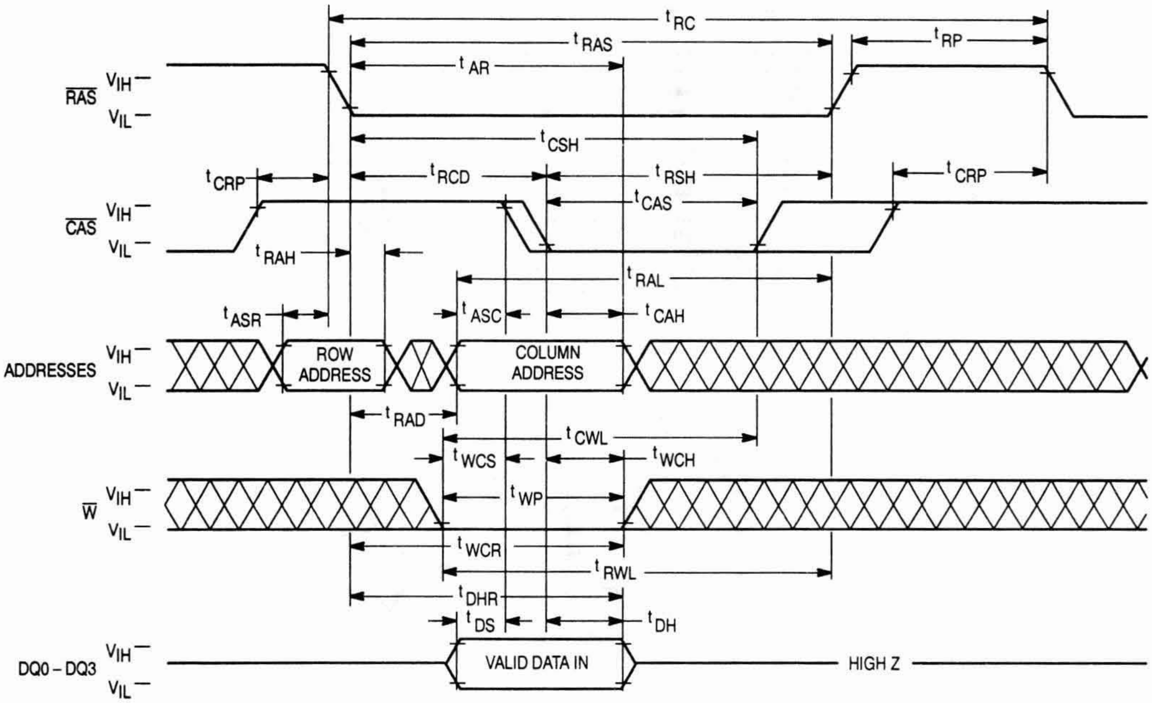
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in delayed write or read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \ge t_{CWD}$ (min), $t_{RWD} \ge t_{RWD}$ (min), $t_{CPWD} \ge t_{CPWD}$ (min), and $t_{AWD} \ge t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

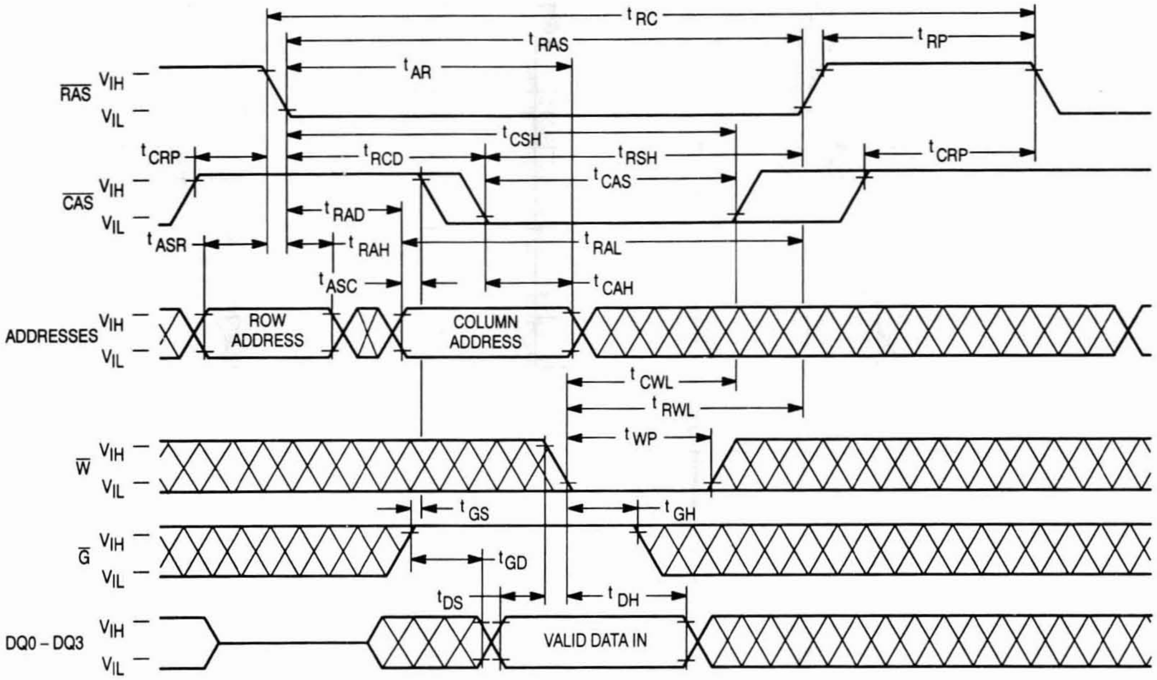
READ CYCLE


t_{RC}
t_{RAS}
t_{RP}
t_{AR}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RCH}
t_{RRH}
t_{RCS}
$\overline{W}$
V_{IH}
V_{IL}
t_{ROH}
t_{AA}
t_{GA}
$\overline{G}$
V_{IH}
V_{IL}
t_{CAC}
t_{OFF}
t_{RAC}
t_{GZ}
DQ0 – DQ3
V_{OH}
V_{OL}
HIGH Z
VALID DATA OUT
t_{CLZ}

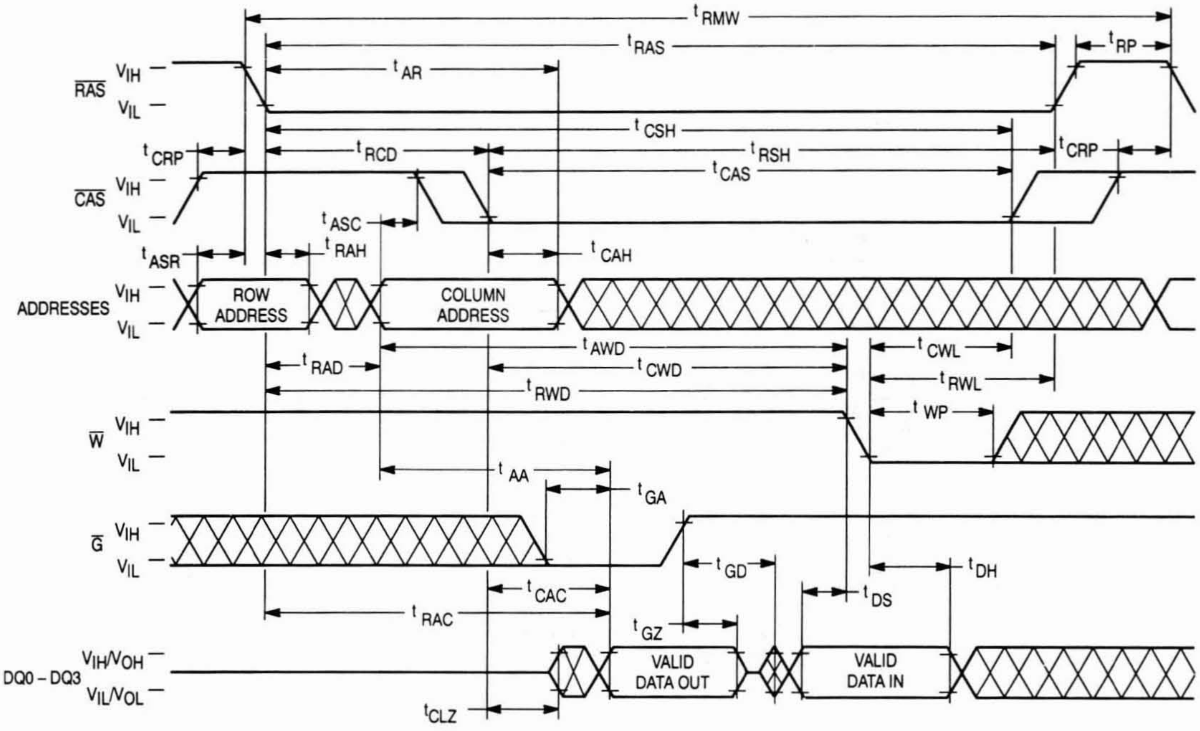
EARLY WRITE CYCLE


t_{RC}
t_{RAS}
t_{RP}
t_{AR}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RAD}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{W}$
V_{IH}
V_{IL}
t_{WCR}
t_{RWL}
t_{DHR}
t_{DS}
t_{DH}
DQ0 – DQ3
V_{IH}
V_{IL}
VALID DATA IN
HIGH Z

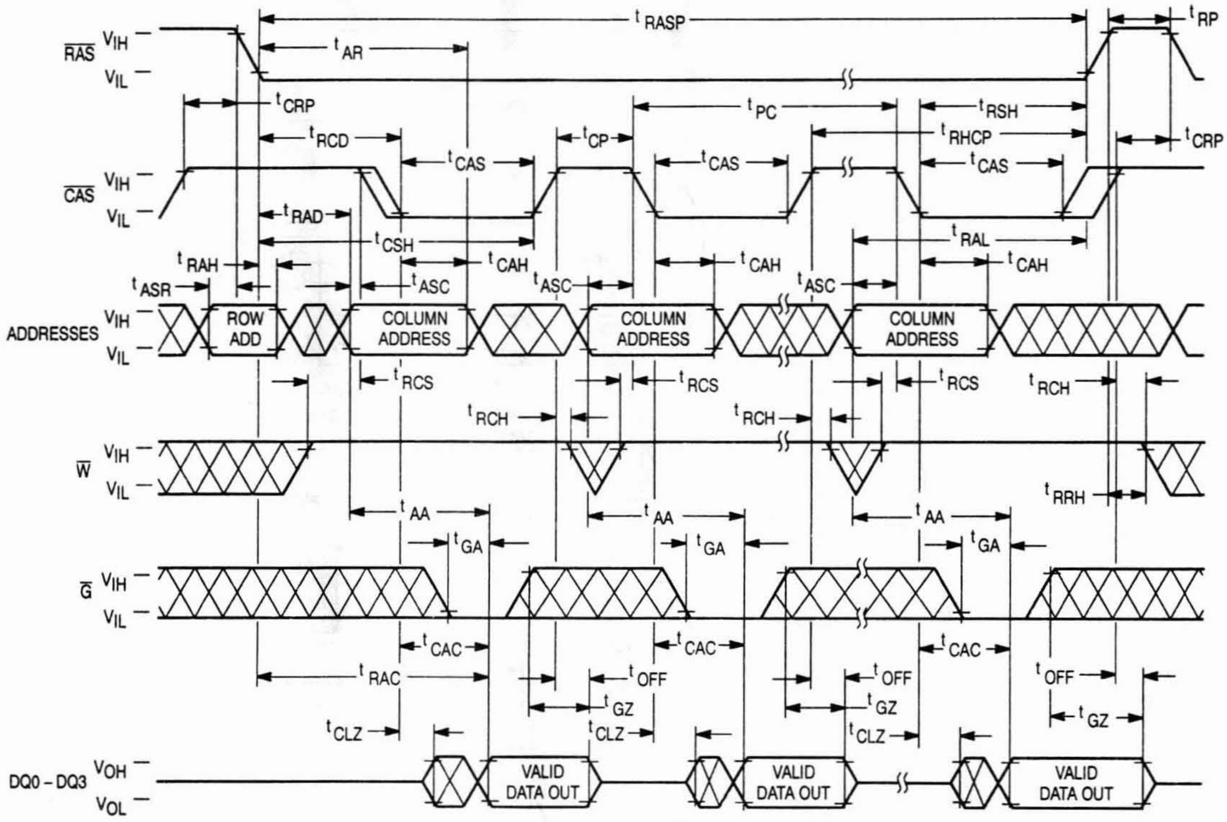
G̅ CONTROLLED LATE WRITE CYCLE


t RC
t RAS
t RP
t AR
RAS̅ VIH
VIL
t CSH
t CRP
t RCD
t RSH
t CRP
t CAS
CAS̅ VIH
VIL
t RAD
t ASR
t RAH
t RAL
t ASC
t CAH
ADDRESSES VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
t CWL
t RWL
t WP
W̅ VIH
VIL
t GS
t GH
G̅ VIH
VIL
t GD
t DS
t DH
DQ0 – DQ3 VIH
VIL
VALID DATA IN

READ-WRITE CYCLE


t RMW
t RAS
t RP
t AR
RAS̅ VIH
VIL
t CSH
t CRP
t RCD
t RSH
t CRP
t CAS
CAS̅ VIH
VIL
t ASC
t RAH
t ASR
t CAH
ADDRESSES VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
t AWD
t CWL
t RAD
t CWD
t RWL
t RWD
t WP
W̅ VIH
VIL
t AA
t GA
G̅ VIH
VIL
t GD
t DH
t CAC
t DS
t RAC
t GZ
DQ0 – DQ3 VIH/VOH
VIL/VOL
VALID DATA OUT
VALID DATA IN
t CLZ

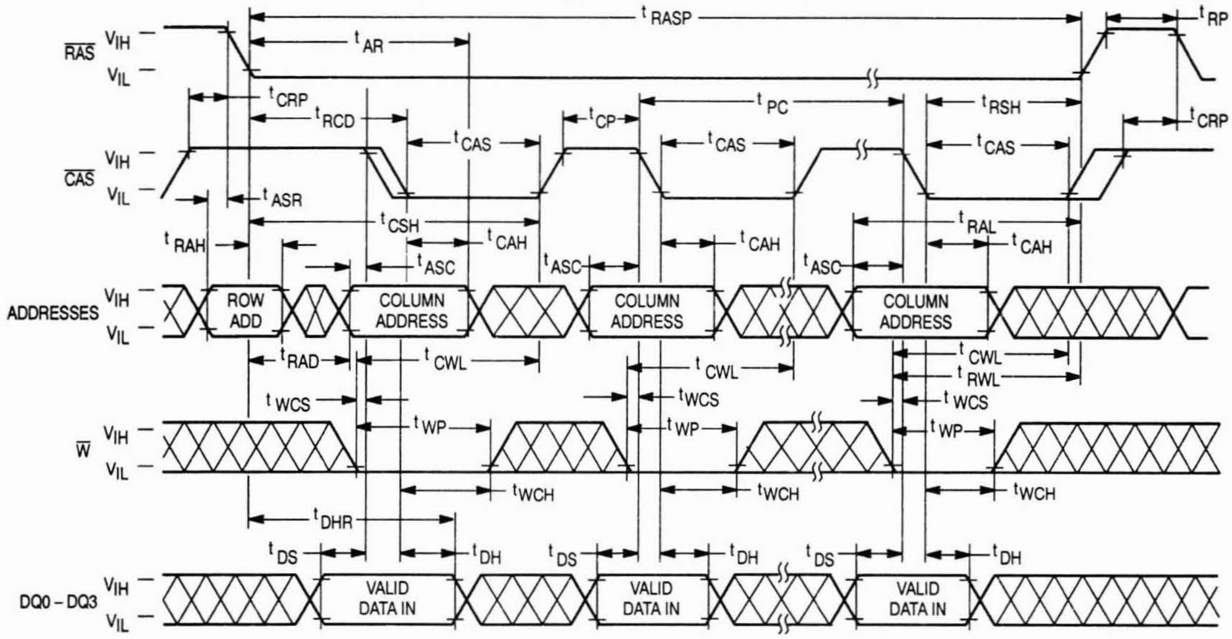
FAST PAGE MODE READ CYCLE



RAS
VIH
VIL
CAS
ADDRESSES
W
G
DQ0 – DQ3
VOH
VOL
tRASP
tRP
tAR
tCRP
tPC
tRSH
tRCD
tCP
tRHCP
tCAS
tRAD
tCSH
tRAL
tRAH
tCAH
tASR
tASC
ROW ADD
COLUMN ADDRESS
tRCS
tRCH
tRRH
tAA
tGA
tCAC
tRAC
tOFF
tGZ
tCLZ
VALID DATA OUT

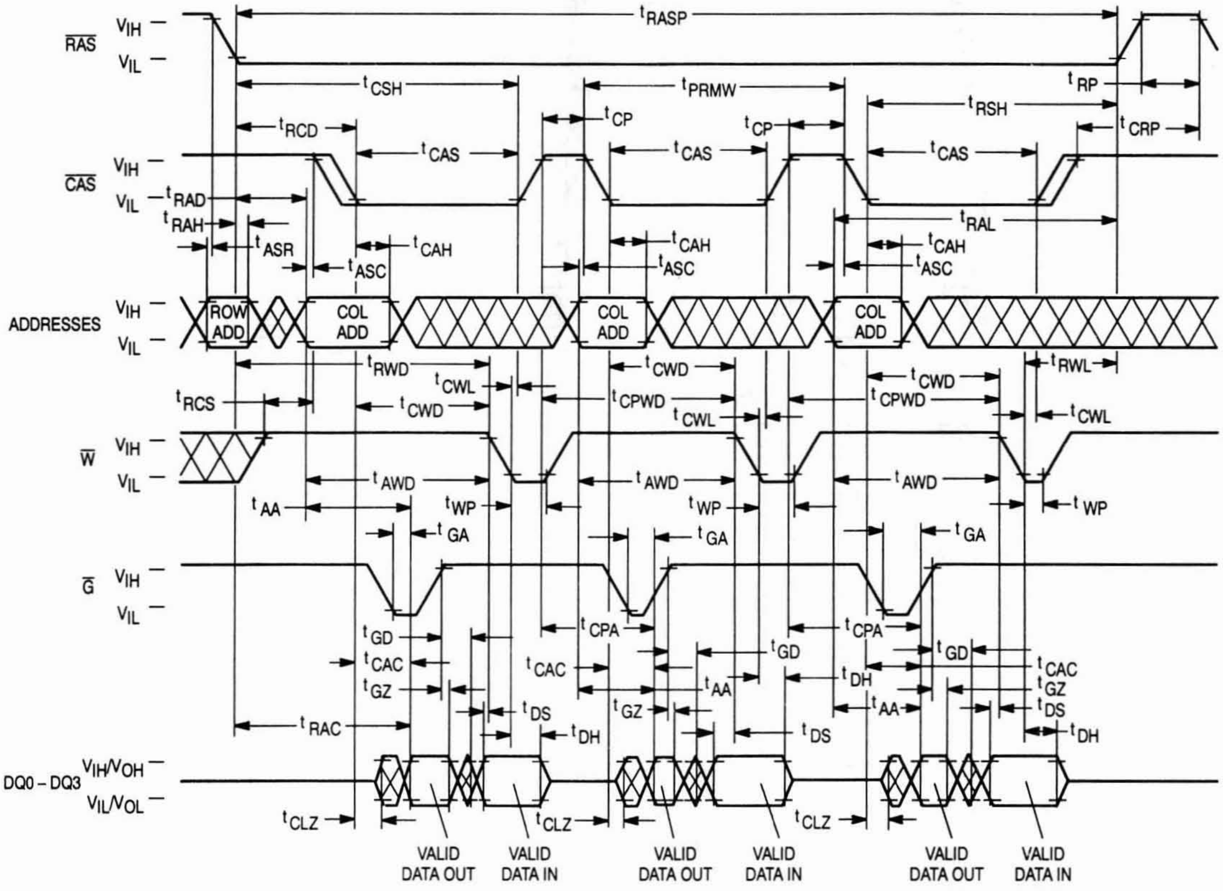
2

FAST PAGE MODE EARLY-WRITE CYCLE



RAS
VIH
VIL
CAS
ADDRESSES
W
DQ0 – DQ3
tRASP
tRP
tAR
tCRP
tPC
tRSH
tRCD
tCP
tCAS
tASR
tCSH
tRAL
tRAH
tCAH
tASC
ROW ADD
COLUMN ADDRESS
tRAD
tCWL
tRWL
tWCS
tWP
tWCH
tDHR
tDS
tDH
VALID DATA IN

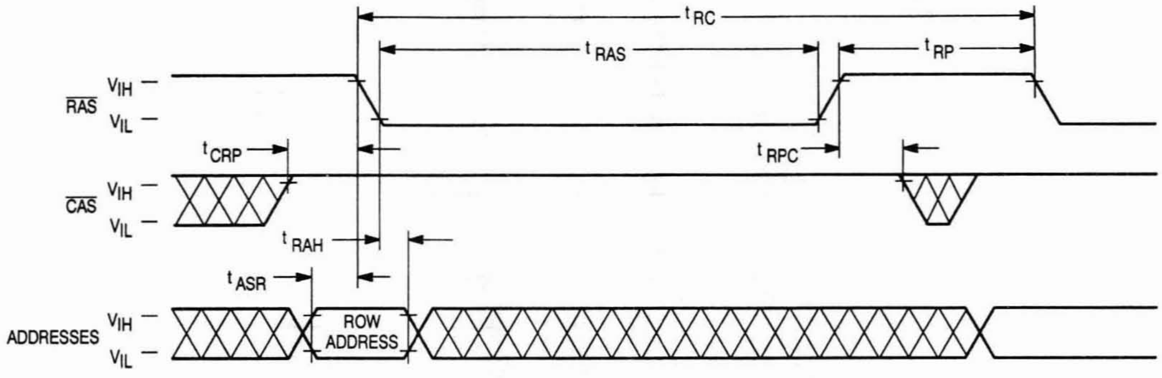
FAST PAGE MODE READ-WRITE CYCLE



RAS
CAS
ADDRESSES
W
G
DQ0 – DQ3
VIH
VIL
VIH/VOH
VIL/VOL
tRASP
tCSH
tPRMW
tRSH
tRP
tCRP
tRCD
tCP
tCAS
tRAD
tRAH
tASR
tASC
tCAH
tRAL
ROW ADD
COL ADD
tRWD
tCWL
tCWD
tCPWD
tRWL
tRCS
tAWD
tAA
tWP
tGA
tGD
tCAC
tGZ
tCPA
tRAC
tDS
tDH
tCLZ
VALID DATA OUT
VALID DATA IN

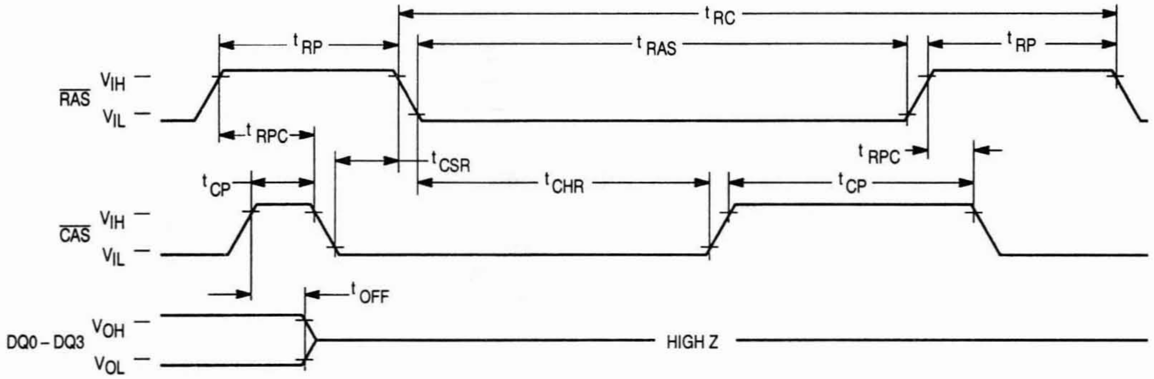
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

($\overline{\text{W}}$ and $\overline{\text{G}}$ are Don't Care)

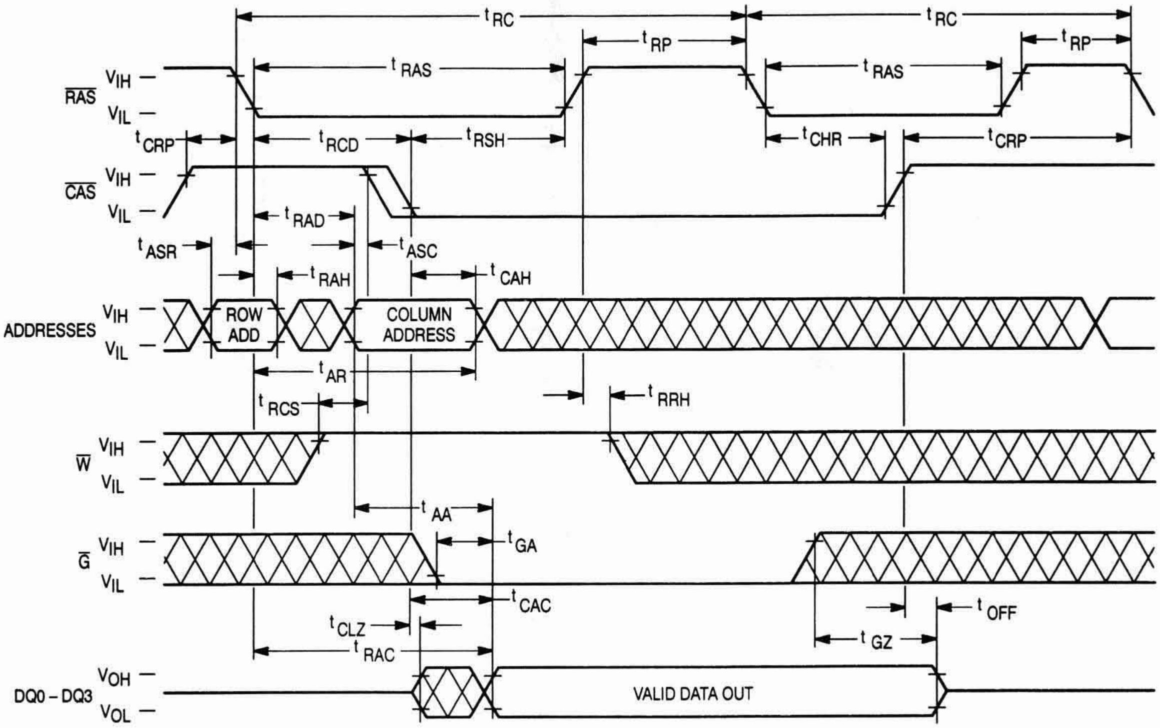

t RC
t RAS
t RP
$\overline{\text{RAS}}$
V IH
V IL
t CRP
t RPC
$\overline{\text{CAS}}$
V IH
V IL
t RAH
t ASR
ADDRESSES
V IH
V IL
ROW ADDRESS

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{W}}$, $\overline{\text{G}}$, and A0 – A8 are Don't Care)

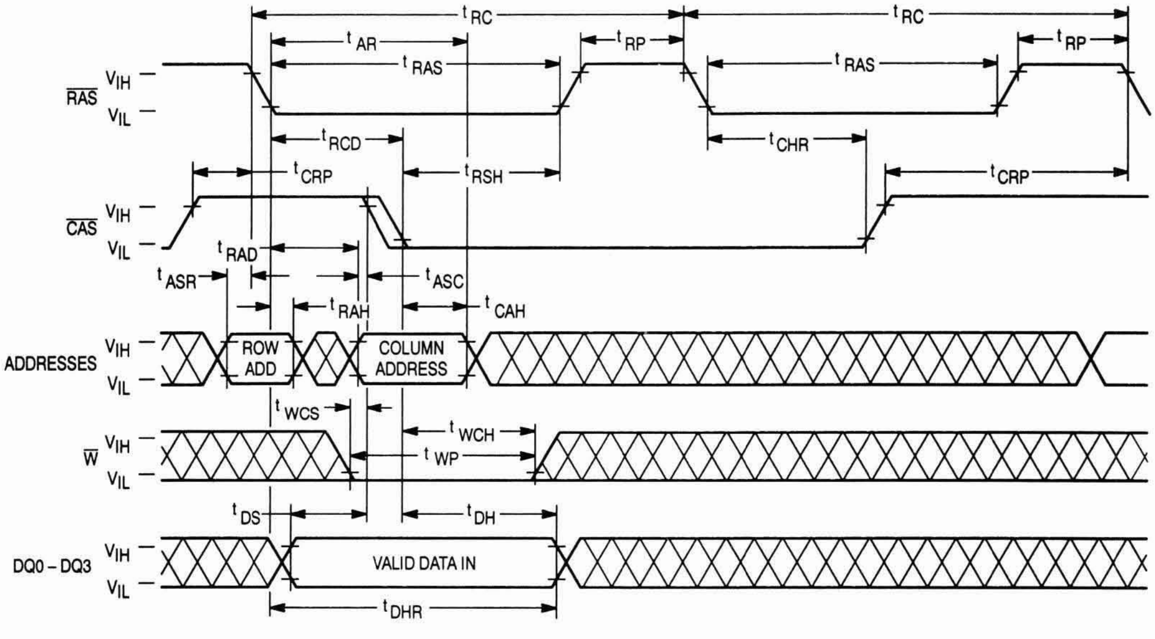

t RC
t RP
t RAS
t RP
$\overline{\text{RAS}}$
V IH
V IL
t RPC
t CSR
t RPC
t CP
t CHR
t CP
$\overline{\text{CAS}}$
V IH
V IL
t OFF
DQ0 – DQ3
V OH
V OL
HIGH Z

HIDDEN REFRESH CYCLE (READ)



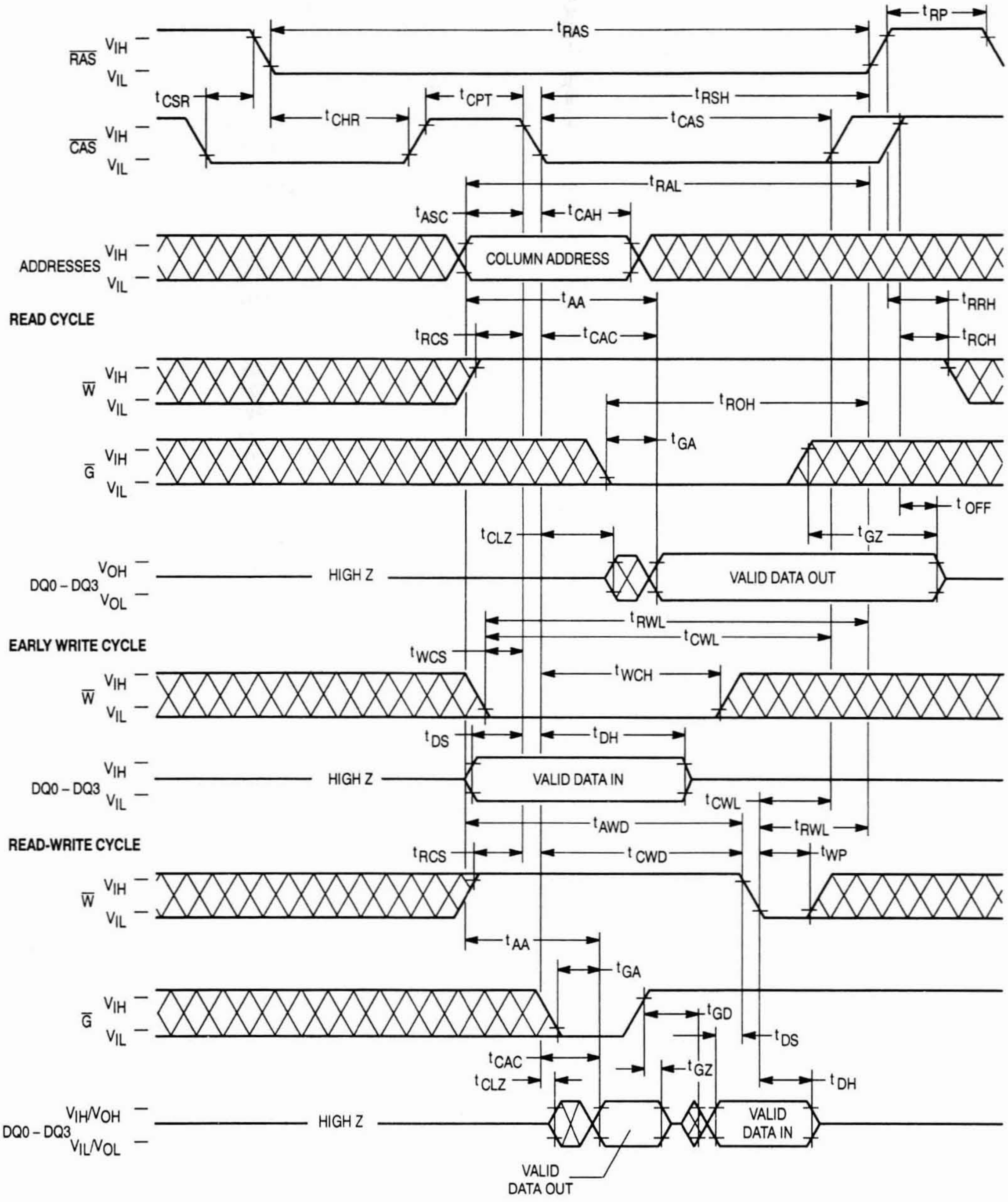
RAS
CAS
ADDRESSES
W
G
DQ0 – DQ3
V_{IH}
V_{IL}
V_{OH}
V_{OL}
t_{RC}
t_{RP}
t_{RAS}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ROW ADD
COLUMN ADDRESS
t_{AR}
t_{RCS}
t_{RRH}
t_{AA}
t_{GA}
t_{CAC}
t_{CLZ}
t_{RAC}
t_{OFF}
t_{GZ}
VALID DATA OUT

HIDDEN REFRESH CYCLE (EARLY WRITE)



RAS
CAS
ADDRESSES
W
DQ0 – DQ3
V_{IH}
V_{IL}
t_{RC}
t_{AR}
t_{RP}
t_{RAS}
t_{RCD}
t_{CHR}
t_{CRP}
t_{RSH}
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ROW ADD
COLUMN ADDRESS
t_{WCS}
t_{WCH}
t_{WP}
t_{DS}
t_{DH}
VALID DATA IN
t_{DHR}

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE


$\overline{\text{RAS}}$
VIH
VIL
tRAS
tRP
tCSR
tCHR
tCPT
tRSH
tCAS
$\overline{\text{CAS}}$
tRAL
tASC
tCAH
ADDRESSES
COLUMN ADDRESS
READ CYCLE
tAA
tRRH
tRCS
tCAC
tRCH
$\overline{\text{W}}$
tROH
tGA
$\overline{\text{G}}$
tOFF
tCLZ
tGZ
VOH
VOL
DQ0 – DQ3
HIGH Z
VALID DATA OUT
tRWL
tCWL
EARLY WRITE CYCLE
tWCS
tWCH
tDS
tDH
VALID DATA IN
tAWD
READ-WRITE CYCLE
tCWD
tWP
tGD
VIH/VOH
VIL/VOL
VALID DATA IN
VALID DATA OUT

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 bit locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This gate feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are two other variations in addressing the 256K x 4 RAM: **$\overline{\text{RAS}}$-only refresh cycle** and **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: normal random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{\text{CAS}}$ and output enable ($\overline{\text{G}}$) control read access time: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum and $\overline{\text{G}}$ must be active t_{RAC}-t_{GA} (both minimum) after $\overline{\text{RAS}}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{\text{G}}$ active transition does not occur in time, read access time is determined by either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ and $\overline{\text{G}}$ clocks are active. When either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The DRAM may be written with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data In (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data out buffers disabled, effectively disabling $\overline{\text{G}}$.

A late write cycle (referred to as $\overline{\text{G}}$ controlled write) occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, $(t_{RCD} + t_{CWD} + t_{RWL} + t_{T}) \le t_{RAS}$, if timing minimums ($t_{RCD}$, t_{RWL}, and t_{T}) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but Q may be indeterminate — see note 15 of AC Operating Conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 512 column locations on a selected row of the 256K x 4 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically refreshed (recharged) to maintain the correct bit state. Bits in the MCM514256B require refresh every 8 milliseconds while refresh time for the MCM51L4256B is 64 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM514256B and 124.8 microseconds for the MCM51L4256B. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM514256B and 64 milliseconds on the MCM51L4256B.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other mehtods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

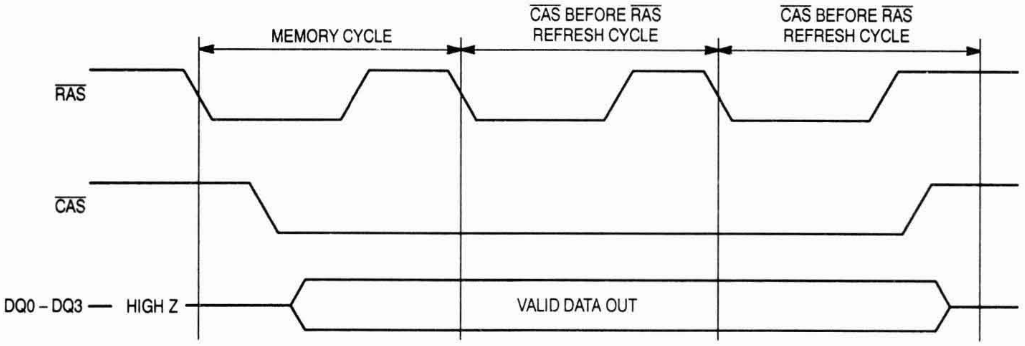


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 514256B or 51L4256B X XX XX

Motorola Memory Prefix — MCM
Part Number — 514256B or 51L4256B
Shipping Method (R2 = Tape and Reel, Blank = Rails)
Speed (60 = 60 ns)
Package (J = 300 mil SOJ, Z = Plastic ZIP)

Full Part Numbers — MCM514256BJ60 MCM514256BJ60R2 MCM514256BZ60
MCM51L4256BJ60 MCM51L4256BJ60R2 MCM51L4256BZ60

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM514258A

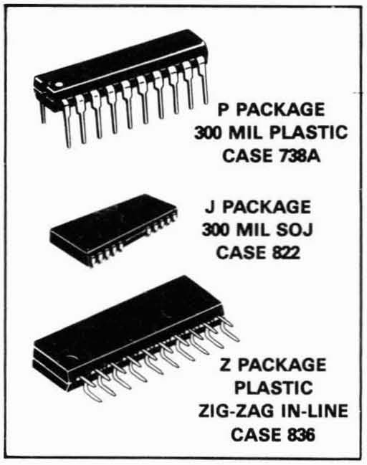
256K × 4 CMOS Dynamic RAM
Static Column

The MCM514258A is a 1.0μ CMOS high-speed, dynamic random access memory. It is organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

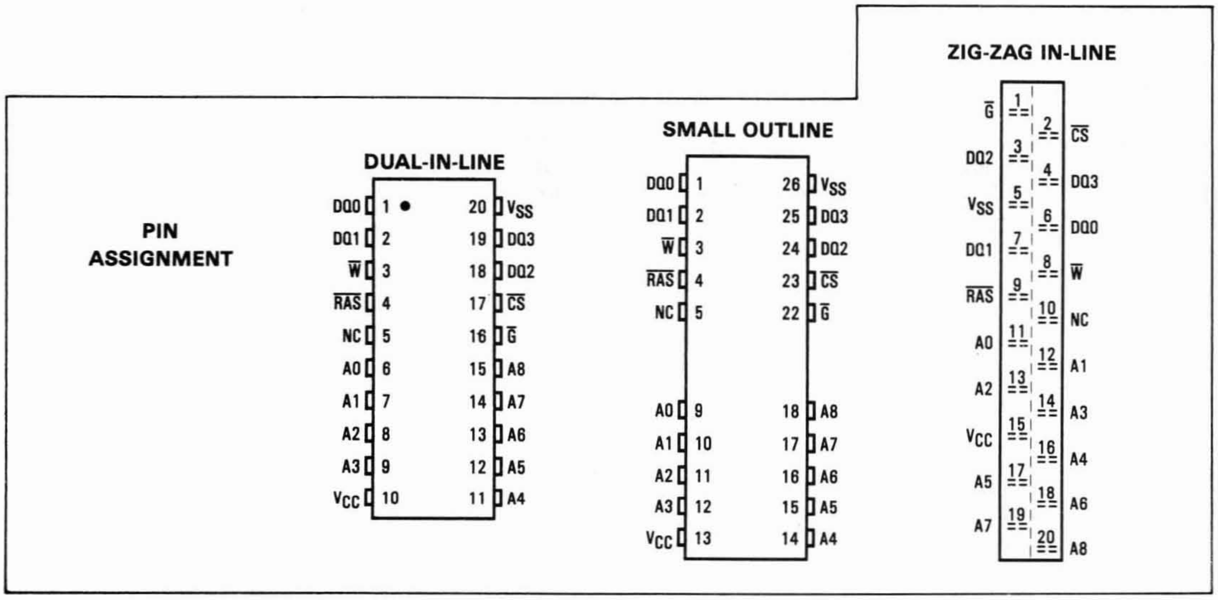
The MCM514258A requires only nine address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line plastic package (DIP), a 300-mil SOJ plastic package, and a 100-mil zig-zag in-line plastic package (ZIP).

- Three-State Data Output
- Static Column Mode
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM514258A-70 = 70 ns (Max)
  - MCM514258A-80 = 80 ns (Max)
  - MCM514258A-10 = 100 ns (Max)
- Low Active Power Dissipation:
  - MCM514258A-70 = 440 mW (Max)
  - MCM514258A-80 = 385 mW (Max)
  - MCM514258A-10 = 330 mW (Max)
- Low Standby Power Dissipation:
  - 11 mW (Max), TTL Levels
  - 5.5 mW (Max), CMOS Levels

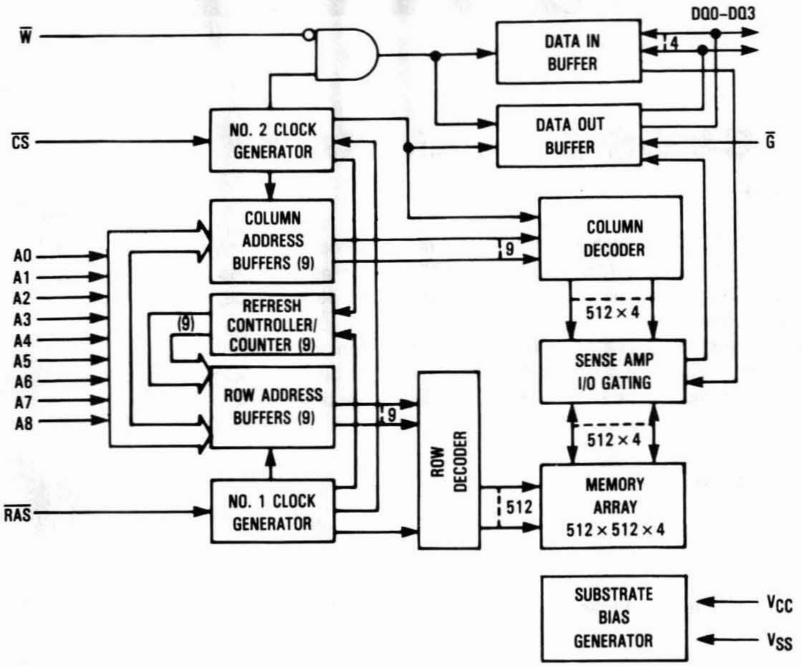
NOT RECOMMENDED FOR NEW DESIGNS


P PACKAGE
300 MIL PLASTIC
CASE 738A
J PACKAGE
300 MIL SOJ
CASE 822
Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

PIN NAMES	
A0-A8	Address Input
DQ0-DQ3	Data Input/Output
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection


PIN ASSIGNMENT
DUAL-IN-LINE
DQ0 1
DQ1 2
W 3
RAS 4
NC 5
A0 6
A1 7
A2 8
A3 9
VCC 10
20 VSS
19 DQ3
18 DQ2
17 CS
16 G
15 A8
14 A7
13 A6
12 A5
11 A4
SMALL OUTLINE
DQ0 1
DQ1 2
W 3
RAS 4
NC 5
A0 9
A1 10
A2 11
A3 12
VCC 13
26 VSS
25 DQ3
24 DQ2
23 CS
22 G
18 A8
17 A7
16 A6
15 A5
14 A4
ZIG-ZAG IN-LINE
G 1
2 CS
DQ2 3
4 DQ3
VSS 5
6 DQ0
DQ1 7
8 W
RAS 9
10 NC
A0 11
12 A1
A2 13
14 A3
VCC 15
16 A4
A5 17
18 A6
A7 19
20 A8

BLOCK DIAGRAM



W̄
CS̄
A0
A1
A2
A3
A4
A5
A6
A7
A8
RAS̄
NO. 2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (9)
REFRESH CONTROLLER/ COUNTER (9)
(9)
ROW ADDRESS BUFFERS (9)
NO. 1 CLOCK GENERATOR
9
ROW DECODER
512
DATA IN BUFFER
DATA OUT BUFFER
DQ0–DQ3
4
Ḡ
9
COLUMN DECODER
512 × 4
SENSE AMP I/O GATING
512 × 4
MEMORY ARRAY 512 × 512 × 4
SUBSTRATE BIAS GENERATOR
VCC
VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM514258A-70, t_{RC}=130 ns		—	80		
MCM514258A-80, t_{RC}=150 ns		—	70		
MCM514258A-10, t_{RC}=180 ns		—	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}=\overline{CS}=V_{IH}$)	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CS}=V_{IH}$)	I_{CC3}			mA	2
MCM514258A-70, t_{RC}=130 ns		—	80		
MCM514258A-80, t_{RC}=150 ns		—	70		
MCM514258A-10, t_{RC}=180 ns		—	60		
V_{CC} Power Supply Current During Static Column Mode Cycle ($\overline{RAS}=\overline{CS}=V_{IL}$)	I_{CC4}			mA	2, 4
MCM514258A-70, t_{SC}=40 ns		—	60		
MCM514258A-80, t_{SC}=45 ns		—	50		
MCM514258A-10, t_{SC}=50 ns		—	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}=\overline{CS}=V_{CC}-0.2$ V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM514258A-70, t_{RC}=130 ns		—	80		
MCM514258A-80, t_{RC}=150 ns		—	70		
MCM514258A-10, t_{RC}=180 ns		—	60		
Input Leakage Current (0 V≤V_{in}≤6.5 V)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CS}=V_{IH}$, 0 V≤V_{out}≤5.5 V)	$I_{lkg(O)}$	−10	10	μA	
Output High Voltage (I_{OH}=−5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL}=4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f=1.0 MHz, T_A=25°C, V_{CC}=5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A8	C_{in}	5	pF	3
	$\overline{G}$, $\overline{RAS}$, $\overline{CS}$, $\overline{W}$		7	pF	3
Output Capacitance ($\overline{CS}=V_{IH}$ to Disable Output)	DQ0-DQ3	C_{out}	7	pF	3

NOTES:

1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.
4. Measured with one address transition per static column mode cycle.

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}=5.0$ V ±10%, $T_A=0$ to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514258A-70		MCM514258A-80		MCM514258A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	180	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RMW}	185	—	205	—	245	—	ns	5
Static Column Mode Cycle Time	t_{AVAV}	t_{SC}	40	—	45	—	55	—	ns	
Static Column Mode Read-Write Cycle Time	t_{AVAV}	t_{SRMW}	100	—	110	—	135	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access Time from $\overline{\text{CS}}$	t_{CELQV}	t_{CAC}	—	25	—	25	—	30	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	50	ns	6, 9
Access Time from Last Write	t_{WLQV}	t_{ALW}	—	65	—	75	—	95	ns	6, 10
$\overline{\text{CS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	30	ns	11
Output Data Hold Time from Column Address	t_{AXQX}	t_{AOH}	5	—	5	—	5	—	ns	
Output Data Enable Time from Write	t_{WHQV}	t_{OW}	—	20	—	20	—	30	ns	
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	70	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Static Column Mode)	t_{RELREH}	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{\text{CS}}$ to $\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{\text{CS}}$ Pulse Width	t_{CELCEH}	t_{CS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{\text{CS}}$ Pulse Width (Static Column Mode)	t_{CELCEH}	t_{CSC}	25	100,000	25	100,000	30	100,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	45	20	55	25	70	ns	12
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	13
$\overline{\text{CS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{CS}}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	15	—	ns	
$\overline{\text{CS}}$ Precharge Time (Static Column Mode)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	ns	
Write Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELAX}	t_{AWR}	55	—	60	—	75	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELAX}	t_{AR}	85	—	95	—	115	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	50	—	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements $t_T=5.0$ ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
6. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at $V_{OH}=2.0$ V and $V_{OL}=0.8$ V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max).
11. t_{OFF} (max) and/or t_{GZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

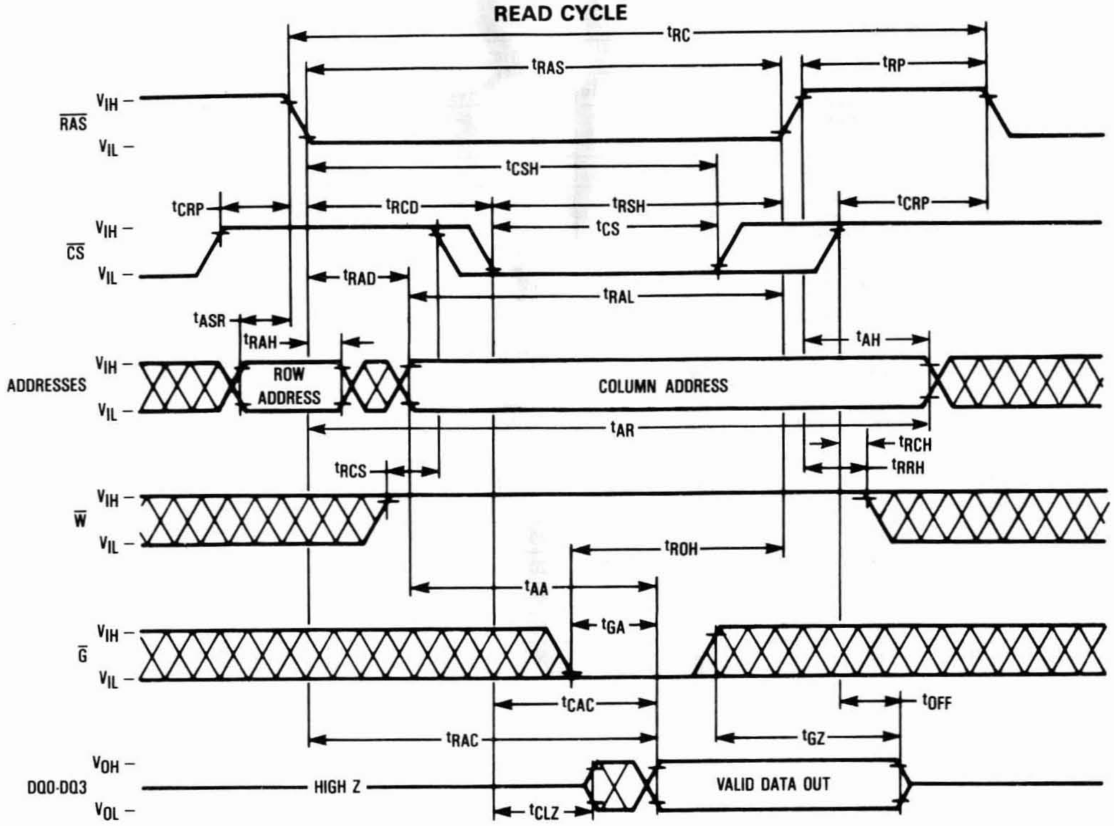
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM514258A-70		MCM514258A-80		MCM514258A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Column Address Hold Time Referenced to $\overline{RAS}$	t_{REHAX}	t_{AH}	10	—	10	—	10	—	ns	14
Last Write to Column Address Delay Time	t_{WLAV}	t_{LWAD}	20	30	20	35	25	45	ns	15
Last Write to Column Address Hold Time	t_{WLAX}	t_{AHLW}	65	—	75	—	95	—	ns	
Read Command Setup Time Referenced to $\overline{CS}$	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	16
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	16
Write Command Hold Time (Output Data Disable)	t_{CEHWH}	t_{WCH}	15	—	15	—	20	—	ns	17
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	—	60	—	75	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	
Write Inactive Time	t_{WHWL}	t_{WI}	10	—	10	—	10	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	18
Data In Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	20	—	ns	18
Data In Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	—	60	—	75	—	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	—	8	—	8	—	8	ms	
Write Command Setup Time (Output Data Disable)	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	17
$\overline{CS}$ to Write Delay (RW Cycle)	t_{CELWL}	t_{CWD}	55	—	55	—	65	—	ns	17
$\overline{RAS}$ to Write Delay (RW Cycle)	t_{RELWL}	t_{RWD}	100	—	110	—	135	—	ns	17
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	65	—	70	—	85	—	ns	17
$\overline{CS}$ Setup Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{CELREL}	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CS}$ Hold Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{CS}$ Precharge Time for $\overline{CS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	50	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	—	10	—	20	—	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	—	25	—	25	—	25	ns	
$\overline{G}$ to Data Delay	t_{GHDX}	t_{GD}	20	—	20	—	25	—	ns	
Output Buffer Turn-off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	25	ns	11
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	25	—	ns	

NOTES:

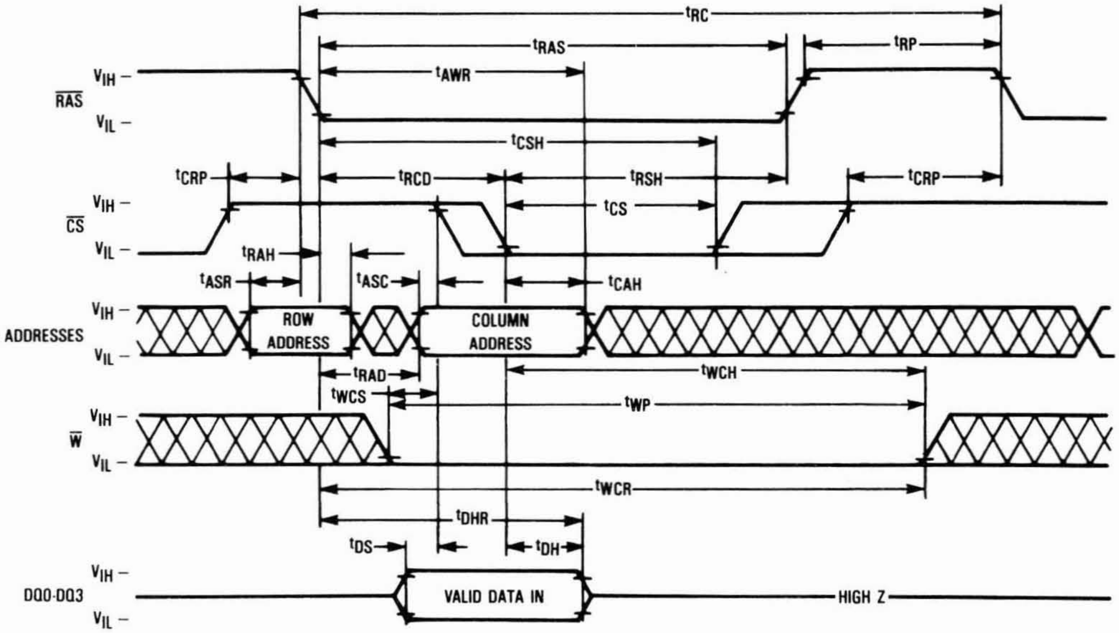
14. t_{AH} must be met for a read cycle.
15. Operation within the t_{LWAD} (max) limit ensures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
17. t_{WCH}, t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min) and $t_{WCH} \geq t_{WCH}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
18. These parameters are referenced to $\overline{CS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in late write or read-write cycles.

READ CYCLE

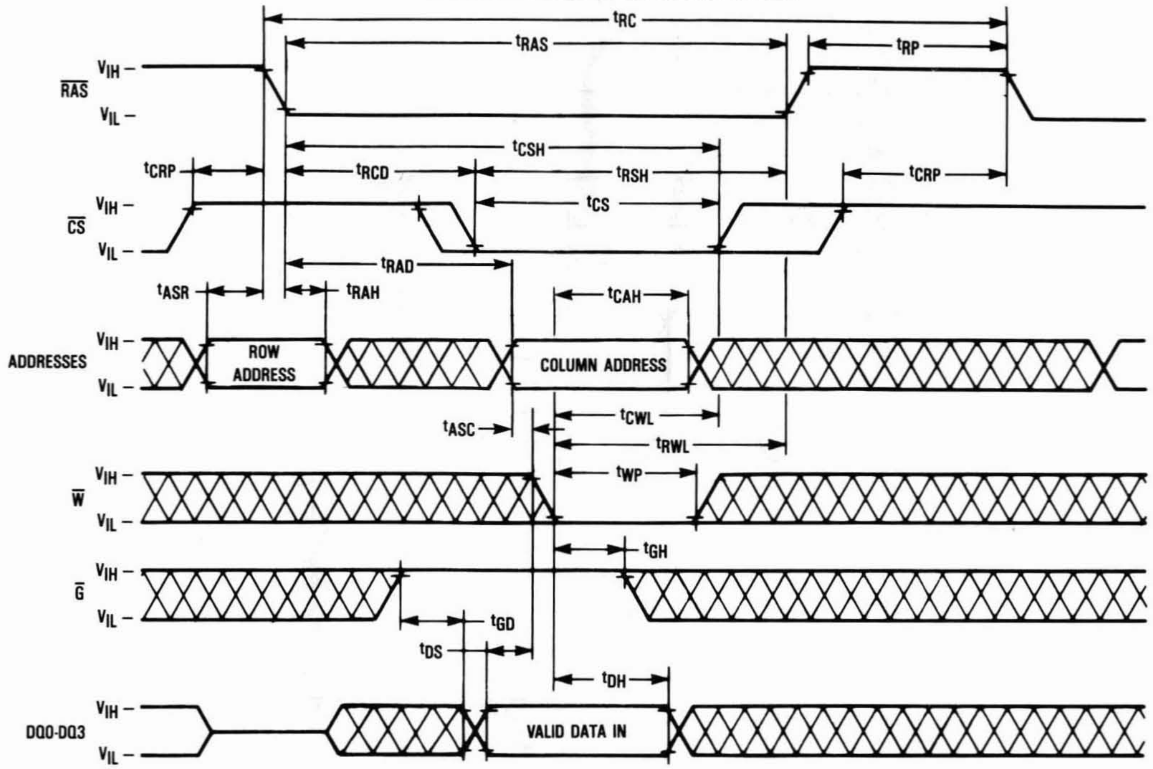

tRC
tRAS
tRP
VIH
VIL
RAS
tCSH
tCRP
tRCD
tRSH
tCS
tCRP
CS
tRAD
tRAL
tASR
tRAH
tAH
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tAR
tRCH
tRRH
tRCS
W
tROH
tAA
tGA
G
tCAC
tOFF
tRAC
tGZ
VOH
VOL
DQ0-DQ3
HIGH Z
VALID DATA OUT
tCLZ

EARLY WRITE CYCLE

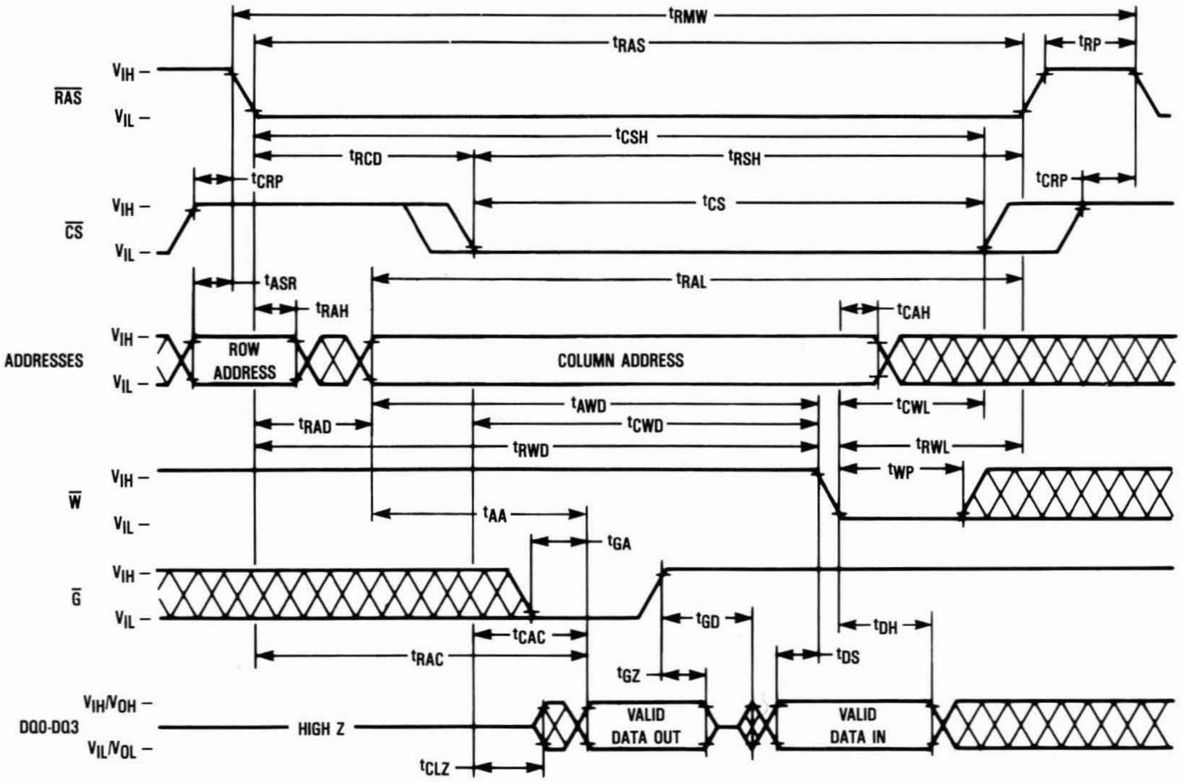
($\overline{G}$ is Don't Care)


tRC
tRAS
tRP
tAWR
VIH
VIL
RAS
tCSH
tCRP
tRCD
tRSH
tCRP
tCS
CS
tRAH
tASR
tASC
tCAH
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tRAD
tWCH
tWCS
tWP
W
tWCR
tDHR
tDS
tDH
DQ0-DQ3
VALID DATA IN
HIGH Z

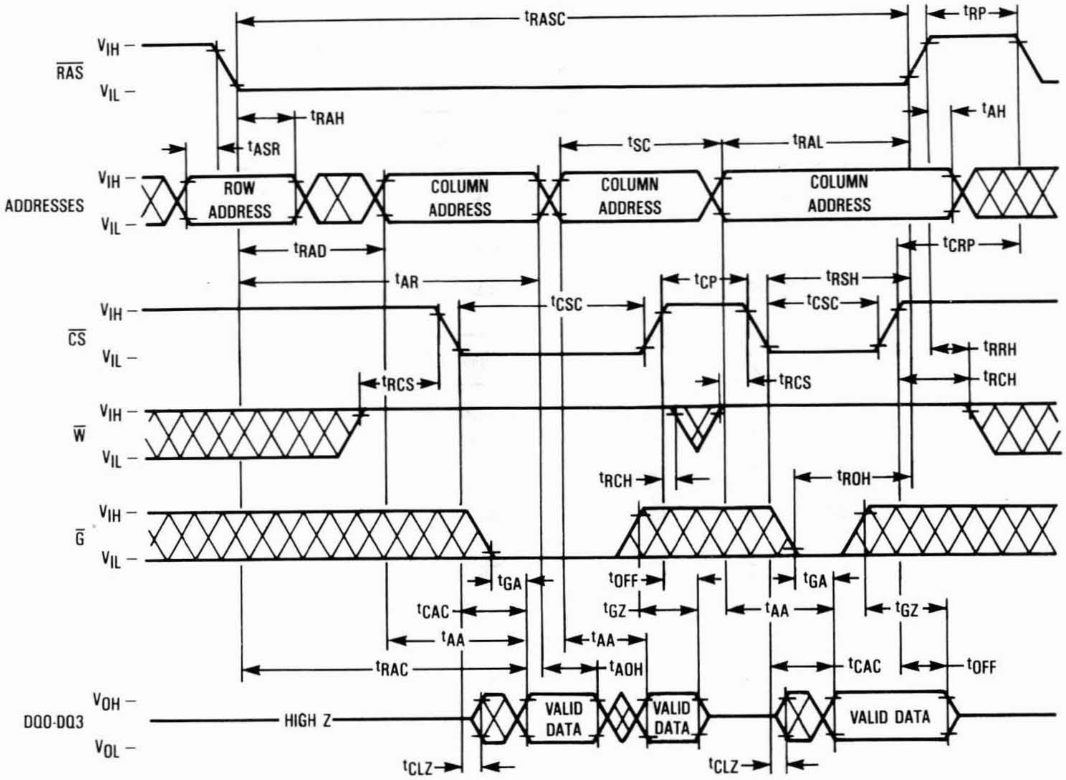
G̅ CONTROLLED LATE WRITE CYCLE


tRC
tRAS
tRP
RAS̅
VIH –
VIL –
tCSH
tCRP
tRCD
tRSH
tCRP
tCS
CS̅
VIH –
VIL –
tRAD
tASR
tRAH
tCAH
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
tASC
tCWL
tRWL
tWP
W̅
VIH –
VIL –
tGH
G̅
VIH –
VIL –
tGD
tDS
tDH
DQ0-DQ3
VIH –
VIL –
VALID DATA IN

READ-WRITE CYCLE

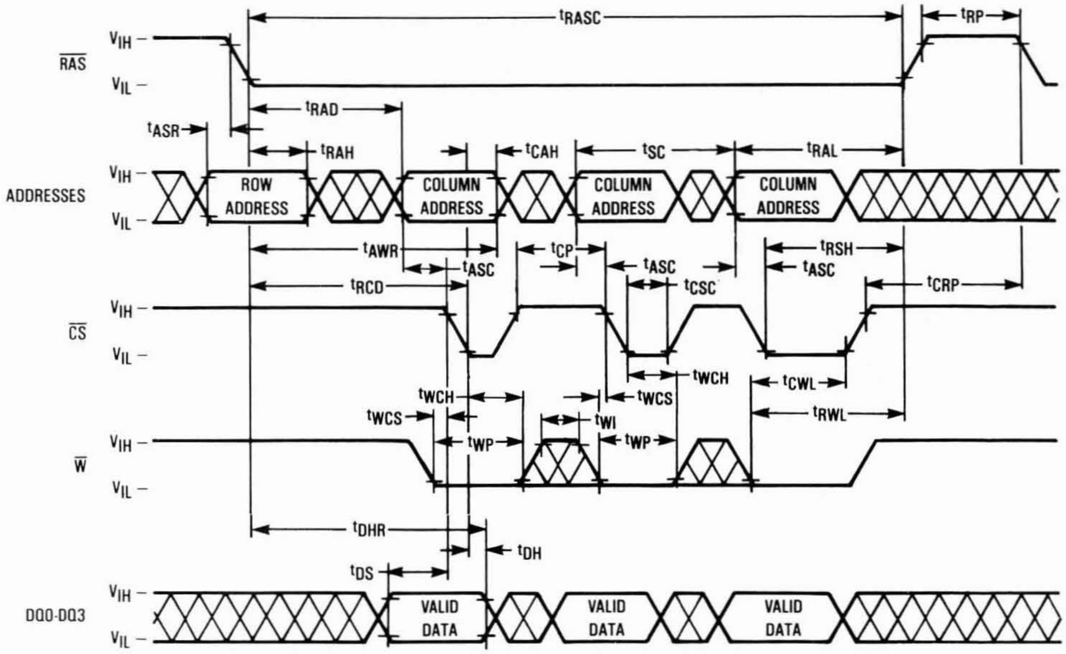

tRMW
tRAS
tRP
RAS̅
VIH –
VIL –
tCSH
tRCD
tRSH
tCRP
tCRP
tCS
CS̅
VIH –
VIL –
tASR
tRAL
tRAH
tCAH
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
tAWD
tRAD
tCWD
tCWL
tRWD
tRWL
tWP
W̅
VIH –
VIL –
tAA
tGA
G̅
VIH –
VIL –
tGD
tDH
tCAC
tRAC
tDS
tGZ
DQ0-DQ3
VIH/VOH –
VIL/VOL –
HIGH Z
VALID DATA OUT
VALID DATA IN
tCLZ

STATIC COLUMN MODE READ CYCLE


t_{RASC}
t_{RP}
V_{IH}
V_{IL}
$\overline{\text{RAS}}$
t_{RAH}
t_{ASR}
t_{AH}
t_{SC}
t_{RAL}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
t_{RAD}
t_{CRP}
t_{AR}
t_{CP}
t_{RSH}
t_{CSC}
t_{CSC}
$\overline{\text{CS}}$
t_{RRH}
t_{RCS}
t_{RCS}
t_{RCH}
$\overline{\text{W}}$
t_{RCH}
t_{ROH}
$\overline{\text{G}}$
t_{GA}
t_{OFF}
t_{GA}
t_{CAC}
t_{GZ}
t_{AA}
t_{GZ}
t_{AA}
t_{AA}
t_{RAC}
t_{AOH}
t_{CAC}
t_{OFF}
V_{OH}
DQ0-DQ3
HIGH Z
VALID DATA
VALID DATA
VALID DATA
V_{OL}
t_{CLZ}
t_{CLZ}

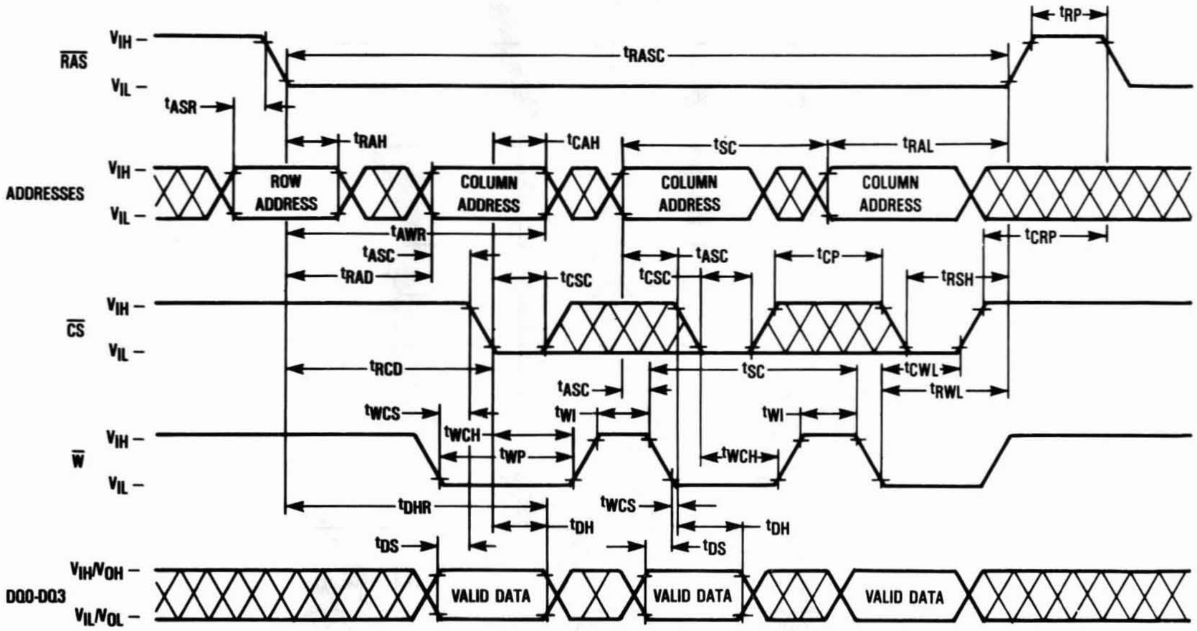
STATIC COLUMN MODE EARLY WRITE CYCLE (A)

($\overline{\text{G}}$ is Don't Care)

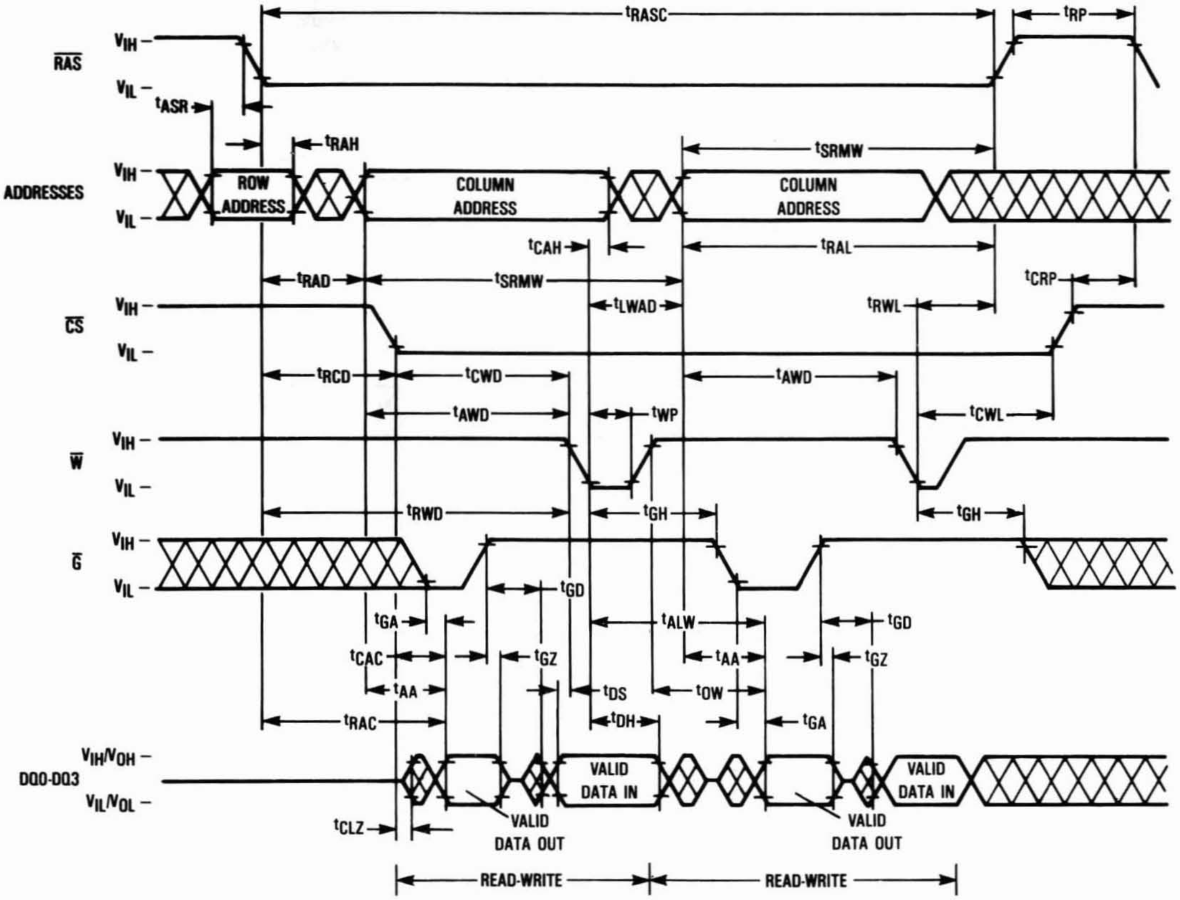

t_{RASC}
t_{RP}
V_{IH}
V_{IL}
$\overline{\text{RAS}}$
t_{RAD}
t_{ASR}
t_{RAH}
t_{CAH}
t_{SC}
t_{RAL}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
t_{AWR}
t_{CP}
t_{ASC}
t_{RSH}
t_{ASC}
t_{ASC}
t_{RCD}
t_{CSC}
t_{CRP}
$\overline{\text{CS}}$
t_{WCH}
t_{WCH}
t_{CWL}
t_{WCS}
t_{WCS}
t_{WI}
t_{RWL}
t_{WP}
t_{WP}
$\overline{\text{W}}$
t_{DHR}
t_{DH}
t_{DS}
DQ0-DQ3
VALID DATA
VALID DATA
VALID DATA

STATIC COLUMN MODE EARLY WRITE CYCLE (B)

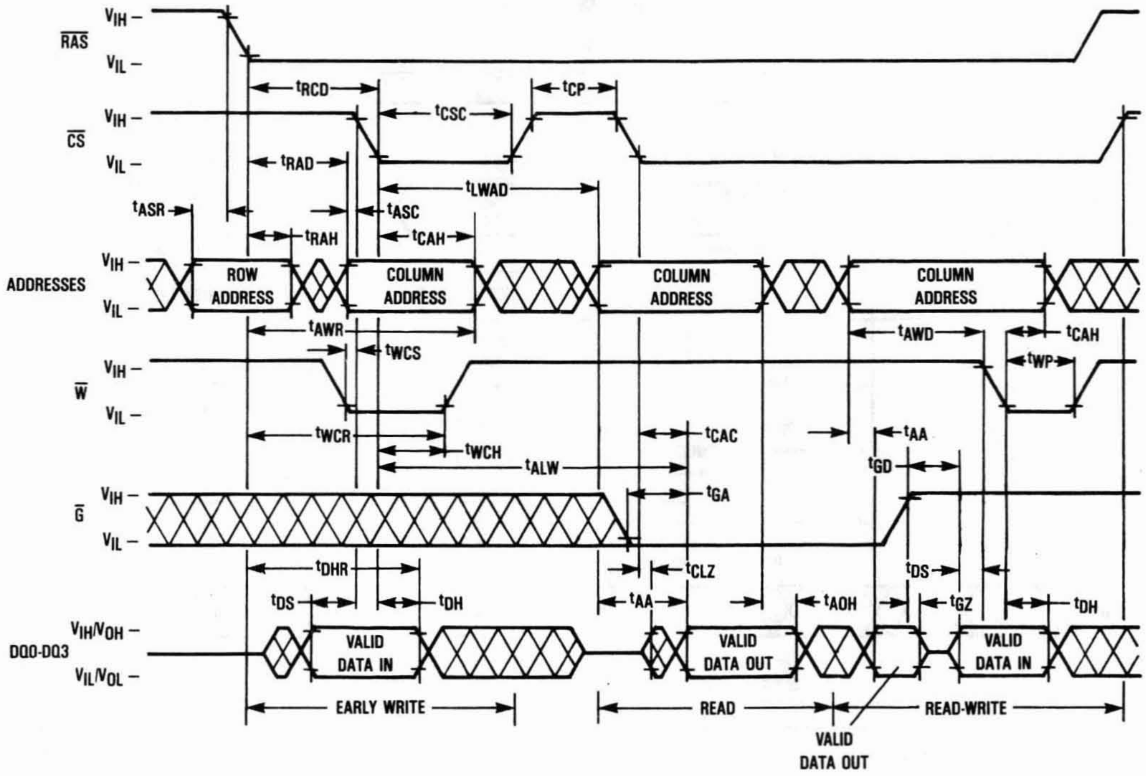
(G̅ is Don't Care)


RAS
VIH
VIL
ADDRESSES
CS
W
DQ0-DQ3
VIH/VOH
VIL/VOL
tRASC
tRP
tASR
tRAH
tCAH
tSC
tRAL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tAWR
tCRP
tASC
tASC
tCP
tRAD
tCSC
tCSC
tRSH
tRCD
tSC
tCWL
tASC
tRWL
tWCS
tWI
tWI
tWCH
tWCH
tWP
tDHR
tWCS
tDH
tDH
tDS
tDS
VALID DATA
VALID DATA
VALID DATA

STATIC COLUMN MODE READ-WRITE CYCLE

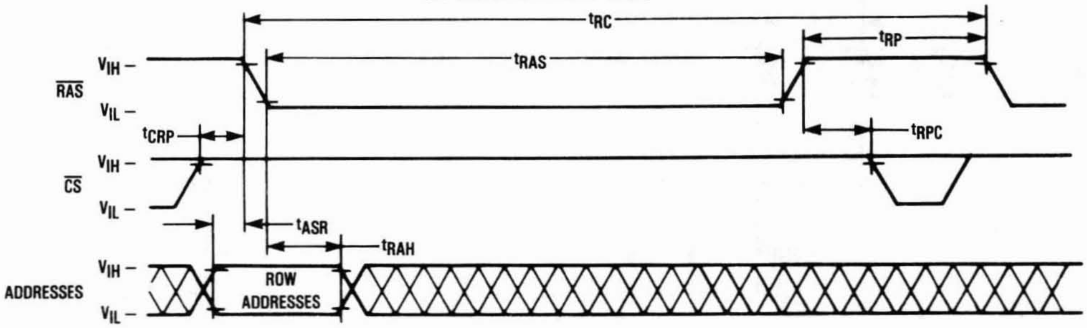

RAS
VIH
VIL
ADDRESSES
CS
W
G
DQ0-DQ3
VIH/VOH
VIL/VOL
tRASC
tRP
tASR
tRAH
tSRMW
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tCAH
tRAL
tRAD
tSRMW
tCRP
tLWAD
tRWL
tRCD
tCWD
tAWD
tAWD
tWP
tCWL
tRWD
tGH
tGH
tGD
tGA
tALW
tGD
tCAC
tGZ
tAA
tGZ
tAA
tDS
tOW
tRAC
tDH
tGA
VALID DATA IN
VALID DATA IN
VALID DATA OUT
VALID DATA OUT
tCLZ
READ-WRITE
READ-WRITE

STATIC COLUMN MODE READ/WRITE MIXED CYCLE


$\overline{RAS}$
$\overline{CS}$
ADDRESSES
$\overline{W}$
$\overline{G}$
DQ0-DQ3
V_{IH}
V_{IL}
V_{IH}/V_{OH}
V_{IL}/V_{OL}
t_{RCD}
t_{CP}
t_{CSC}
t_{RAD}
t_{LWAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
t_{AWR}
t_{WCS}
t_{AWD}
t_{CAH}
t_{WP}
t_{WCR}
t_{WCH}
t_{ALW}
t_{CAC}
t_{AA}
t_{GD}
t_{GA}
t_{DHR}
t_{CLZ}
t_{DS}
t_{DS}
t_{DH}
t_{AA}
t_{AOH}
t_{GZ}
t_{DH}
VALID DATA IN
VALID DATA OUT
VALID DATA IN
EARLY WRITE
READ
READ-WRITE
VALID DATA OUT

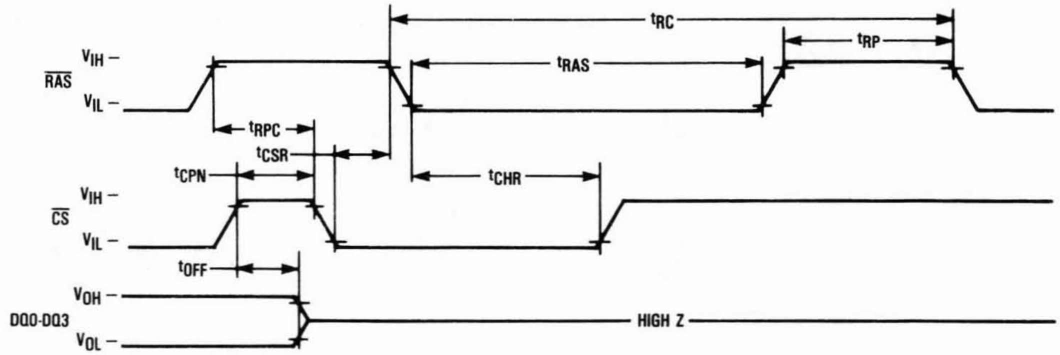
$\overline{RAS}$ ONLY REFRESH CYCLE

($\overline{W}$ and $\overline{G}$ are Don't Care)

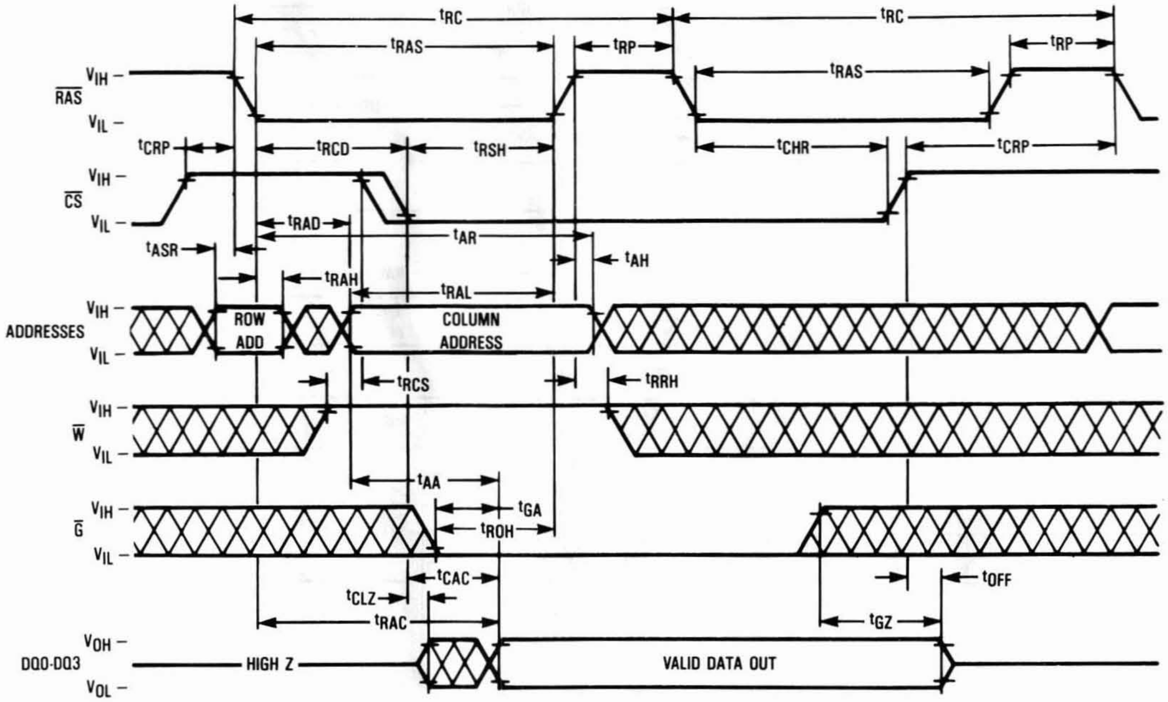

t_{RC}
t_{RP}
t_{RAS}
$\overline{RAS}$
$\overline{CS}$
ADDRESSES
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
t_{ASR}
t_{RAH}
ROW ADDRESSES

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

($\overline{W}$, $\overline{G}$, and A0 to A8 are Don't Care)

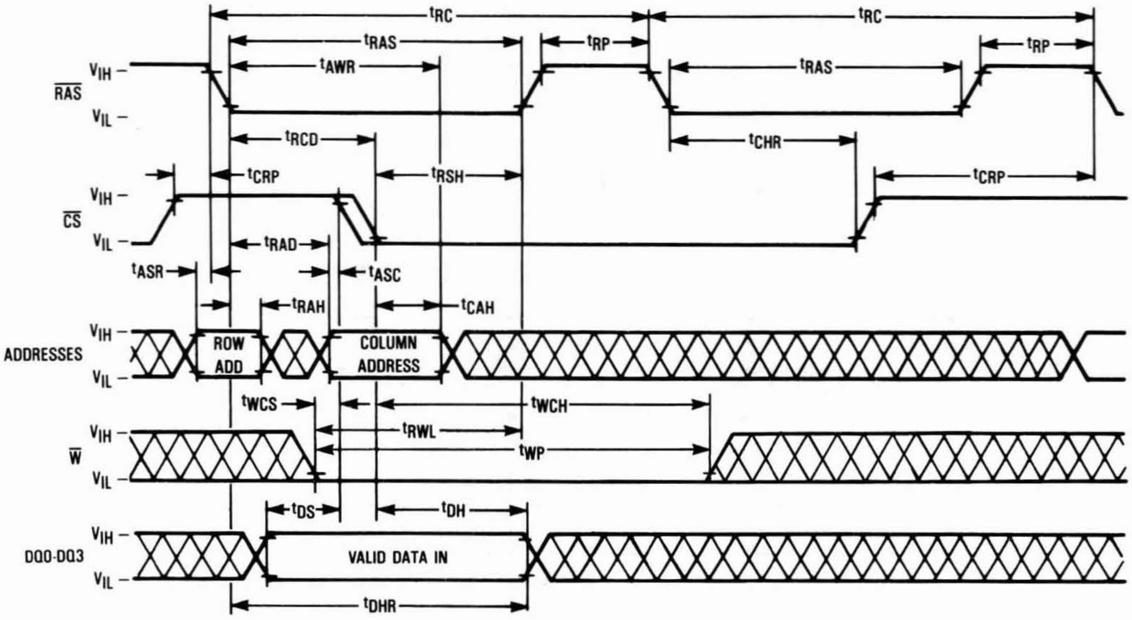

t_{RC}
t_{RP}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RPC}
t_{CSR}
t_{CPN}
t_{CHR}
$\overline{CS}$
t_{OFF}
V_{OH}
V_{OL}
DQ0-DQ3
HIGH Z

HIDDEN REFRESH CYCLE (READ)

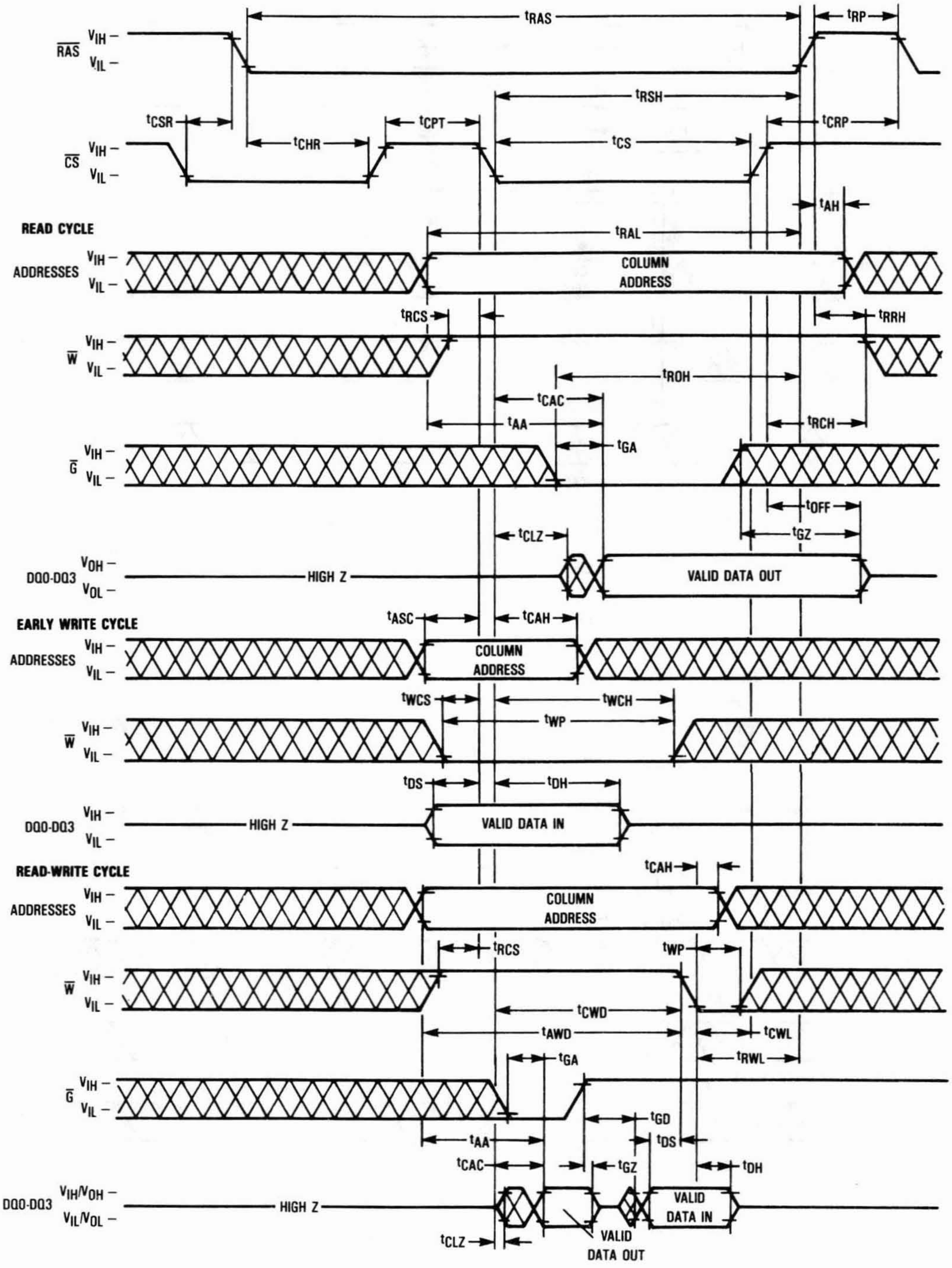

tRC
tRC
tRAS
tRP
tRAS
tRP
VIH
RAS
VIL
tCRP
tRCD
tRSH
tCHR
tCRP
VIH
CS
VIL
tRAD
tAR
tASR
tAH
tRAH
tRAL
VIH
ADDRESSES
VIL
ROW ADD
COLUMN ADDRESS
tRCS
tRRH
VIH
W
VIL
tAA
VIH
G
VIL
tGA
tROH
tCAC
tOFF
tCLZ
tRAC
tGZ
VOH
DQ0-DQ3
VOL
HIGH Z
VALID DATA OUT

HIDDEN REFRESH CYCLE (EARLY WRITE)

($\overline{G}$ is Don't Care)


tRC
tRC
tRAS
tRP
tAWR
tRAS
tRP
VIH
RAS
VIL
tRCD
tCHR
tCRP
tRSH
tCRP
VIH
CS
VIL
tRAD
tASR
tASC
tRAH
tCAH
VIH
ADDRESSES
VIL
ROW ADD
COLUMN ADDRESS
tWCS
tWCH
tRWL
tWP
VIH
W
VIL
tDS
tDH
VIH
DQ0-DQ3
VIL
VALID DATA IN
tDHR

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



$\overline{RAS}$
V_{IH} –
V_{IL} –
t_{RAS}
t_{RP}
t_{RSH}
t_{CSR}
t_{CPT}
t_{CRP}
t_{CHR}
t_{CS}
$\overline{CS}$
t_{AH}
READ CYCLE
t_{RAL}
ADDRESSES
COLUMN ADDRESS
t_{RCS}
t_{RRH}
$\overline{W}$
t_{ROH}
t_{CAC}
t_{AA}
t_{RCH}
t_{GA}
$\overline{G}$
t_{OFF}
t_{CLZ}
t_{GZ}
DQ0-DQ3
V_{OH} –
V_{OL} –
HIGH Z
VALID DATA OUT
EARLY WRITE CYCLE
t_{ASC}
t_{CAH}
COLUMN ADDRESS
t_{WCS}
t_{WCH}
t_{WP}
t_{DS}
t_{DH}
VALID DATA IN
READ-WRITE CYCLE
t_{CAH}
COLUMN ADDRESS
t_{RCS}
t_{WP}
t_{CWD}
t_{AWD}
t_{CWL}
t_{RWL}
t_{GA}
t_{GD}
t_{AA}
t_{DS}
t_{CAC}
t_{GZ}
t_{DH}
V_{IH}/V_{OH} –
V_{IL}/V_{OL} –
VALID DATA IN
VALID DATA OUT
t_{CLZ}

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by the row address strobe ($\overline{RAS}$) clock, into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 bit locations in the device. $\overline{RAS}$ active transition latches the row address field. Column addresses are not latched, hence the "static column" designation of this device. Chip select ($\overline{CS}$) active transition (active $= V_{IL}$, t_{RCD} minimum) follows $\overline{RAS}$ on all read, write, or read-write cycles, and is independent of column address. The static column feature allows greater flexibility in setting up the external external column addresses into the RAM.

There are two other variations in addressing the 256K × 4 RAM: **$\overline{RAS}$ only refresh cycle** and **$\overline{CS}$ before $\overline{RAS}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: random read cycle, read-write cycle, and "static column mode" read, and read-write. The random read cycle is outlined here, while the other cycles are discussed in separate sections.

The random read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ active transition latching the desired row. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CS}$ active transition, to enable read mode. A valid column address can be provided at any time (t_{RAD} minimum), independent of the $\overline{CS}$ active transition.

Both the $\overline{RAS}$ and $\overline{CS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{CS}$ and output enable ($\overline{G}$) control read access time: $\overline{CS}$ and $\overline{G}$ must be active (and column address must be valid) by t_{RCD} maximum, and t_{RAC}-t_{GA} minimum, respectively, to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If either t_{RCD} maximum is exceeded or $\overline{G}$ active transition does not occur in time, read access time is determined by the $\overline{CS}$ and/or $\overline{G}$ clock active transition (t_{CAC}, t_{GA}).

The $\overline{RAS}$ and $\overline{CS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CS}, respectively, to complete the read cycle. The column address must remain valid for t_{AH} after $\overline{RAS}$ inactive transition to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CS}$ and $\overline{G}$ clocks are active. When either the $\overline{CS}$ or $\overline{G}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} or t_{GZ} after inactive transition.

WRITE CYCLE

The DRAM may be written with any of four cycles: early write, late write and "static column mode" early write, and read-write. Early and late write modes are discussed here, while static column mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL} level). Early and late write modes are distinguished by the active transition of $\overline{W}$ with respect to $\overline{CS}$ leading edge. Minimum active time t_{RAS} and t_{CS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CS}$ active transition. Column address set up and hold times (t_{ASC}, t_{CAH}), and data in (D) set up and hold times (t_{DS}, t_{DH}) are referenced to $\overline{CS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CS}$ active transition, keeping data-out buffers disabled effectively disabling $\overline{G}$.

A late write cycle (referred to as $\overline{G}$ controlled write) occurs when $\overline{W}$ active transition is made after $\overline{CS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CS}$ active transition, ($t_{RAD} + t_{ASC} + t_{RWL} + 2t_T \leq t_{RAS}$, if other timing minimums (t_{ASC}, t_{RWL}, and t_T) are maintained. Column address and D timing parameters are referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CS}$ active transition but Q may be indeterminate—see note 17 of AC operating conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

STATIC COLUMN MODE CYCLES

Static column mode refers to multiple successive data operations performed at any or all 512 column locations on the selected row of the 256 × 4 dynamic RAM during one $\overline{RAS}$ cycle. Read access time of multiple operations (t_{AA} or t_{CAC}) is considerably faster than the regular $\overline{RAS}$ clock access time t_{RAC}. Multiple operations can be performed simply by keeping $\overline{RAS}$ active. $\overline{CS}$ may be toggled between active and inactive states at any time within the $\overline{RAS}$ cycle.

Once the timing requirements for the initial read, write, or read-write cycle are met and $\overline{RAS}$ remains low, the device is ready for the next operation. Operations can be intermixed in any order, at any column address, subject to normal operating conditions previously described. Every write operation must be clocked with either $\overline{CS}$ or $\overline{W}$, as indicated in **static column**

mode early write cycle timing diagrams **A** and **B**. Column address and D timing parameters are referenced to the signal clocking the write operation. $\overline{\text{CS}}$ must be toggled inactive (t_{CP}) to perform a read operation after an early write operation (to turn output on), as indicated in **static column mode read/write mixed cycle** timing diagram. The maximum number of consecutive operations is limited by t_{RASC}. The cycle ends when $\overline{\text{RAS}}$ transitions to inactive.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM514258A require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM514258A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM514258A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$ only refresh, $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

$\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
5. Read "0"s which were written at in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

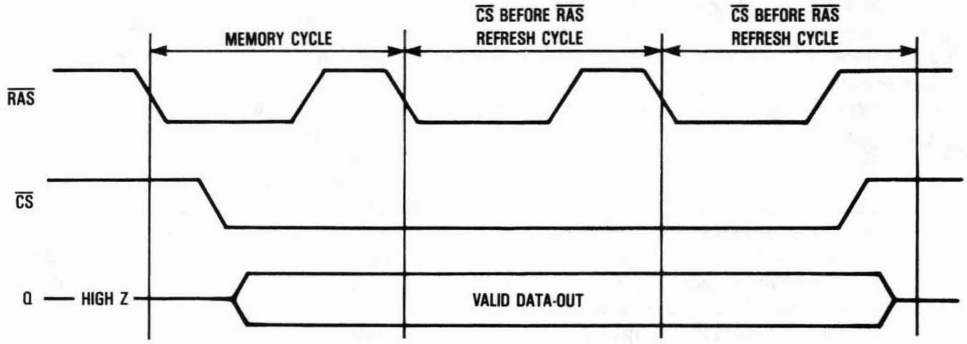

MEMORY CYCLE
$\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{RAS}}$
$\overline{\text{CS}}$
Q — HIGH Z
VALID DATA-OUT

Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 514258A X XX XX

Motorola Memory Prefix — MCM

Part Number — 514258A

Package (P = Plastic DIP, J = Plastic SO with J leads, Z = Plastic ZIP) — X

Speed (70 = 70 ns, 80 = 80 ns, 10 = 100 ns) — XX

Shipping Method (R2 = Tape & Reel, Blank = Rails) — XX

Full Part Numbers—
MCM514258AP70
MCM514257AP80
MCM514258AP10
MCM514258AJ70
MCM514258AJ80
MCM514258AJ10
MCM514258AJ70R2
MCM514258AJ80R2
MCM514258AJ10R2
MCM514258AZ70
MCM514258AZ80
MCM514258AZ10

NOTE: For mechanical data, please see Chapter 10.

CMOS 4M Dynamic RAMs

MCM44100 3-3
MCM44400 3-20
MCM54100A 3-38
MCM54100A-C 3-57
MCM54101A 3-75
MCM54102A 3-92
MCM54170B 3-114
MCM54190B 3-149
MCM54260B 3-184
MCM54280B 3-213
MCM54400A 3-241
MCM54400A-C 3-261
MCM54402A 3-281
MCM54800A 3-303

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM44100
MCM4L4100

Advance Information

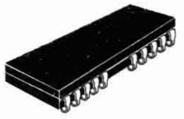
4M x 1 CMOS Dynamic RAM

Fast Page Mode

The MCM44100 is a 0.8μ CMOS high-speed dynamic random access memory. It is organized as 4,194,304 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM44100 requires only 11 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil J-lead small outline package, and a 100 mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Fast Page Mode
- Test Mode
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  MCM44100 = 16 ms
  MCM4L4100 = 128 ms
- Fast Access Time (t_{RAC}):
  MCM44100-60 and MCM4L4100-60 = 60 ns (Max)
  MCM44100-70 and MCM4L4100-70 = 70 ns (Max)
  MCM44100-80 and MCM4L4100-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM44100-60 and MCM4L4100-60 = 605 mW (Max)
  MCM44100-70 and MCM4L4100-70 = 550 mW (Max)
  MCM44100-80 and MCM4L4100-80 = 495 mW (Max)
- Low Standby Power Dissipation:
  MCM44100 and MCM4L4100 = 11 mW (Max, TTL Levels)
  MCM44100 = 5.5 mW (Max, CMOS Levels)
  MCM4L4100 = 1.1 mW (Max, CMOS Levels)



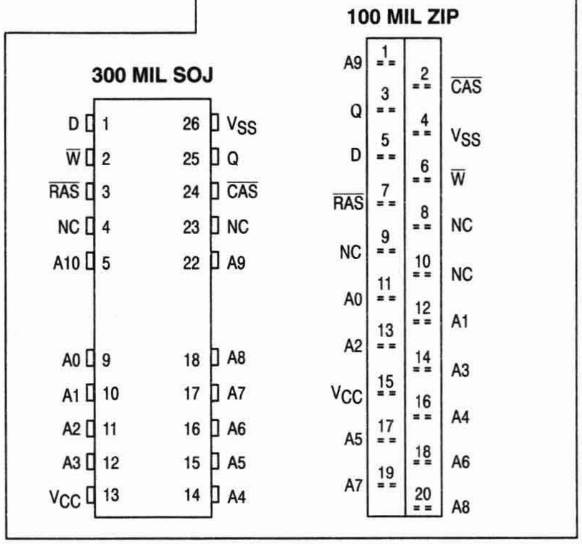
J PACKAGE
300 MIL SOJ
CASE 822B-01

Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836A-01

PIN NAMES

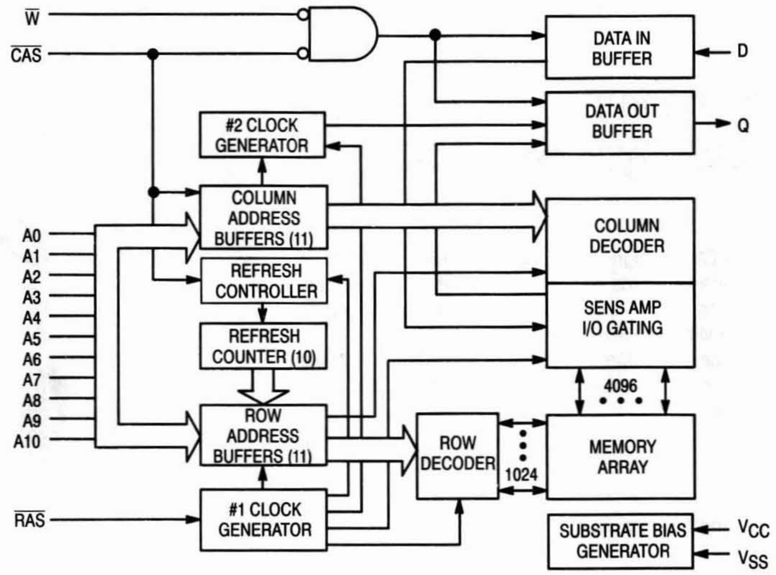
A0 – A10	Address Inputs
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENTS


100 MIL ZIP
300 MIL SOJ
D 1
W 2
RAS 3
NC 4
A10 5
A0 9
A1 10
A2 11
A3 12
VCC 13
26 VSS
25 Q
24 CAS
23 NC
22 A9
18 A8
17 A7
16 A6
15 A5
14 A4
A9 1
2 CAS
Q 3
4 VSS
D 5
6 W
RAS 7
8 NC
NC 9
10 NC
A0 11
12 A1
A2 13
14 A3
VCC 15
16 A4
A5 17
18 A6
A7 19
20 A8

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM


W
CAS
DATA IN BUFFER
D
DATA OUT BUFFER
Q
#2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (11)
COLUMN DECODER
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
REFRESH CONTROLLER
SENS AMP I/O GATING
REFRESH COUNTER (10)
4096
ROW ADDRESS BUFFERS (11)
ROW DECODER
1024
MEMORY ARRAY
RAS
#1 CLOCK GENERATOR
SUBSTRATE BIAS GENERATOR
VCC
VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	1, 2
MCM44100-60 and MCM4L4100-60, t_{RC} = 110 ns		—	110		
MCM44100-70 and MCM4L4100-70, t_{RC} = 130 ns		—	100		
MCM44100-80 and MCM4L4100-80, t_{RC} = 150 ns		—	90		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	1, 2
MCM44100-60 and MCM4L4100-60, t_{RC} = 110 ns		—	110		
MCM44100-70 and MCM4L4100-70, t_{RC} = 130 ns		—	100		
MCM44100-80 and MCM4L4100-80, t_{RC} = 150 ns		—	90		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	1, 3
MCM44100-60 and MCM4L4100-60, t_{PC} = 45 ns		—	110		
MCM44100-70 and MCM4L4100-70, t_{PC} = 45 ns		—	100		
MCM44100-80 and MCM4L4100-80, t_{PC} = 50 ns		—	90		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} – 0.2 V)	I_{CC5}				
MCM44100		—	1.0	mA	
MCM4L4100		—	200	µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	1
MCM44100-60 and MCM4L4100-60, t_{RC} = 110 ns		—	110		
MCM44100-70 and MCM4L4100-70, t_{RC} = 130 ns		—	100		
MCM44100-80 and MCM4L4100-80, t_{RC} = 150 ns		—	90		
V_{CC} Power Supply Current, Battery Backup Mode — MCM4L4100 Only (t_{RC} = 125 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$ = V_{CC} – 0.2 V; D_{in} = V_{CC} – 0.2 V or 0.2 V or OPEN; A0 – A10 = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}			µA	1, 4
t_{RAS} = 300 ns to 1 µs		—	400		
t_{RAS} = Min to 300 ns		—	300		
Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Q = Enable	I_{CC8}	—	5	mA	1
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	V_{CC}	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	0	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Column address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. t_{RAS} (max) = 1 µs is only applied to refresh of battery-back up. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A10, D	C_{in}	5	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM44100-60 MCM4L4100-60		MCM44100-70 MCM4L4100-70		MCM44100-80 MCM4L4100-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	130	—	155	—	175	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	50	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	60	—	70	—	75	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6,7,8
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	15	—	20	—	20	ns	6,8,9,10
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6,8,10,11
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	35	—	40	—	45	ns	6,8,10
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	20	0	20	ns	12
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	1
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	45	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	—	100 k	—	100 k	—	100 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	15	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	35	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	15	10 k	20	10 k	20	10 k	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	45	20	50	20	60	ns	13
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	14
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	

NOTES:

(continued)

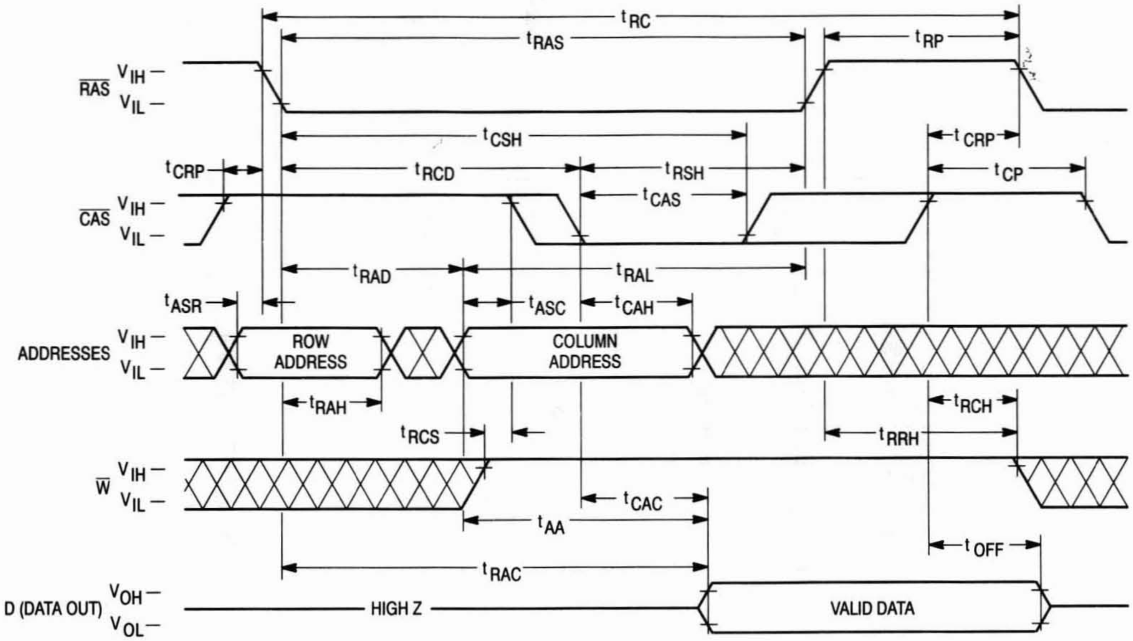
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100 µs is required after power-up followed by 8 initialization cycles ($\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements assume t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
8. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC}, and t_{CPA} is delayed for 2 ns to 5 ns for the specified value. These parameters should be in the test mode cycles by adding the above value to the specified value in the data sheet.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
10. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
11. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
12. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

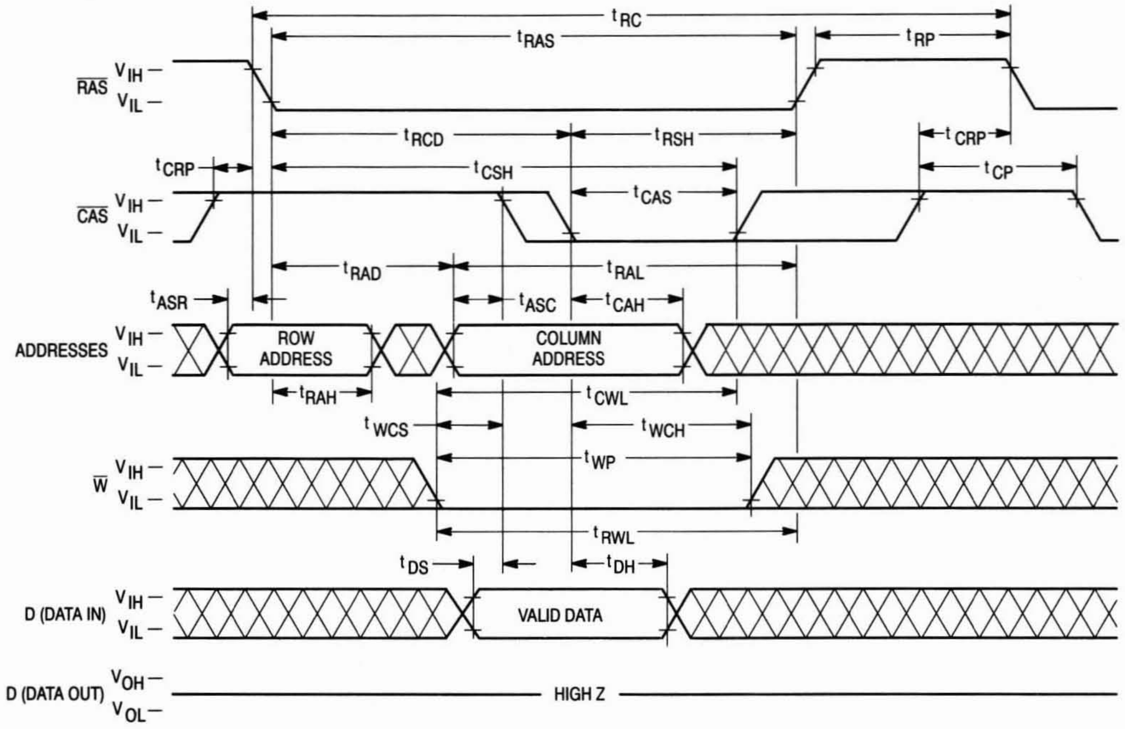
Parameter	Symbol		MCM44100-60 MCM4L4100-60		MCM44100-70 MCM4L4100-70		MCM44100-80 MCM4L4100-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	15
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	15
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	—	10	—	10	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	15	—	20	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	15	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	16
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	16
Refresh Period MCM44100 MCM4L4100	t_{RVRV}	t_{RFSH}	 — —	 16 128	 — —	 16 128	 — —	 16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	17
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	15	—	20	—	20	—	ns	17
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	60	—	70	—	80	—	ns	17
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	30	—	35	—	40	—	ns	17
$\overline{CAS}$ Precharge to Write Delay Time (Page Mode)	t_{CEHWL}	t_{CPWD}	35	—	40	—	45	—	ns	17
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	5	—	5	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Time	t_{CEHCEL}	t_{CPT}	40	—	40	—	40	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	0	—	0	—	0	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	ns	
Write to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{WHREL}	t_{WRP}	0	—	0	—	0	—	ns	
Write to $\overline{RAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	

15. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
16. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in read-write cycles.
17. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

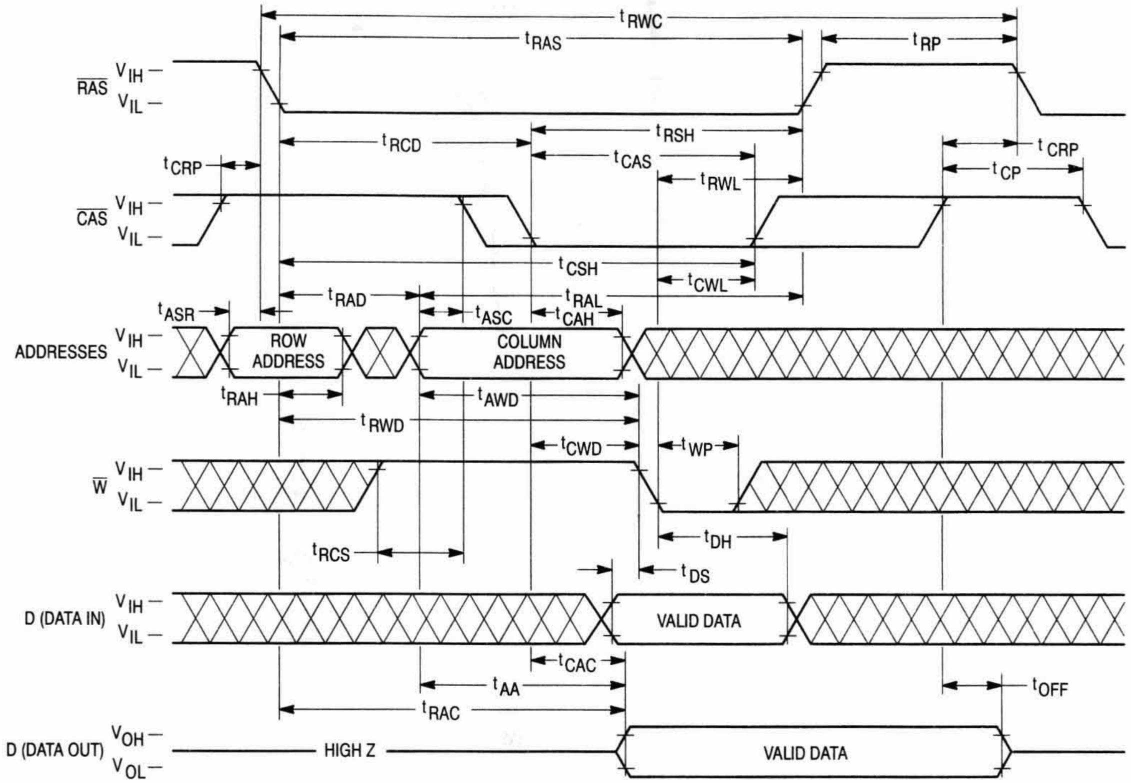
READ CYCLE


t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH} –
V_{IL} –
t_{CSH}
t_{CRP}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CP}
t_{CAS}
$\overline{CAS}$
V_{IH} –
V_{IL} –
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
ADDRESSES
V_{IH} –
V_{IL} –
ROW ADDRESS
COLUMN ADDRESS
t_{RAH}
t_{RCH}
t_{RCS}
t_{RRH}
$\overline{W}$
V_{IH} –
V_{IL} –
t_{CAC}
t_{AA}
t_{OFF}
t_{RAC}
D (DATA OUT)
V_{OH} –
V_{OL} –
HIGH Z
VALID DATA

EARLY WRITE CYCLE

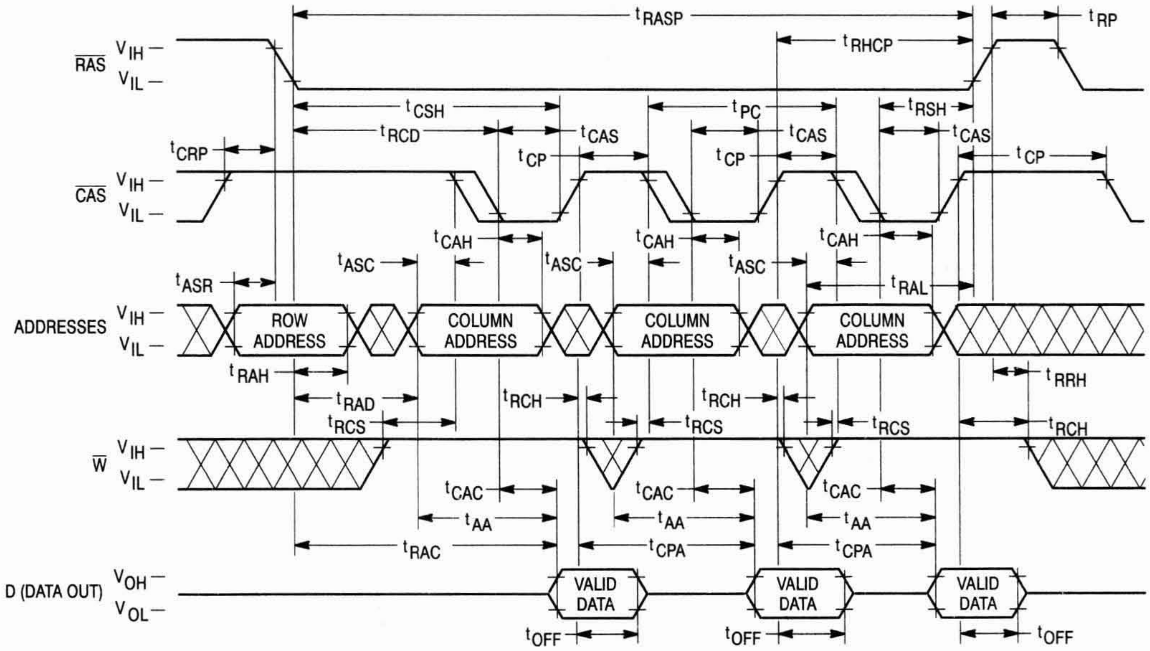

t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH} –
V_{IL} –
t_{RCD}
t_{RSH}
t_{CRP}
t_{CRP}
t_{CSH}
t_{CP}
t_{CAS}
$\overline{CAS}$
V_{IH} –
V_{IL} –
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
ADDRESSES
V_{IH} –
V_{IL} –
ROW ADDRESS
COLUMN ADDRESS
t_{RAH}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{W}$
V_{IH} –
V_{IL} –
t_{RWL}
t_{DS}
t_{DH}
D (DATA IN)
V_{IH} –
V_{IL} –
VALID DATA
D (DATA OUT)
V_{OH} –
V_{OL} –
HIGH Z

READ-WRITE CYCLE



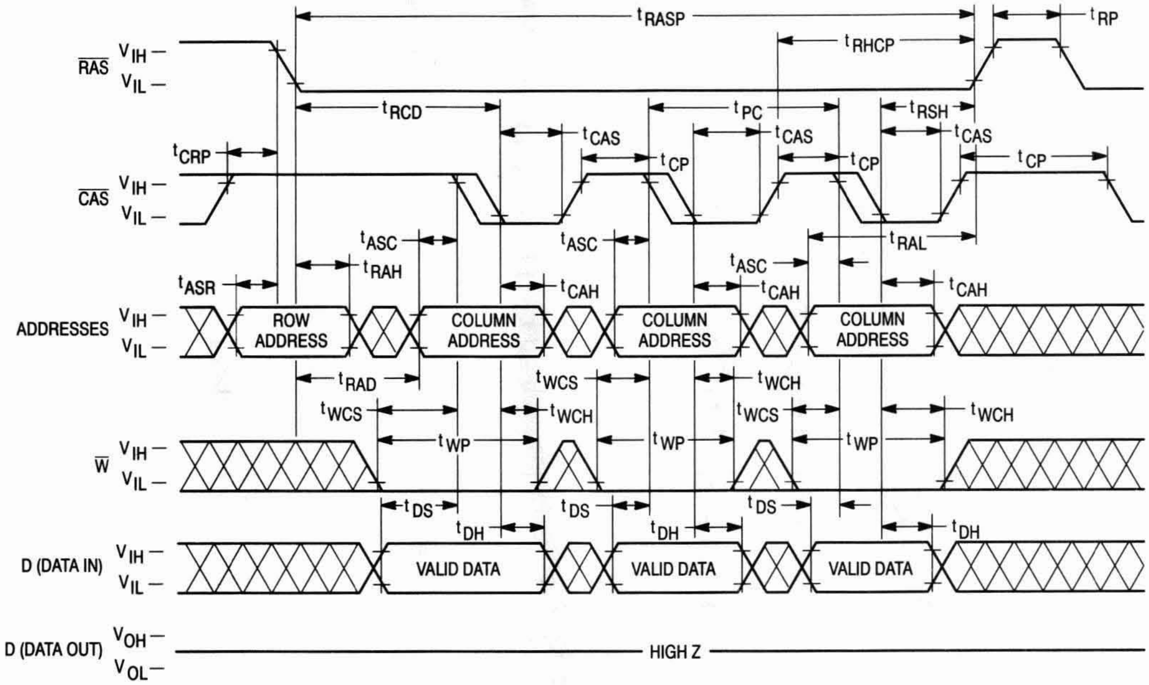
tRWC
tRAS
tRP
RAS
VIH –
VIL –
tRCD
tRSH
tCRP
tCAS
tCRP
tCP
tRWL
CAS
VIH –
VIL –
tCSH
tCWL
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
tRAH
tAWD
tRWD
tCWD
tWP
W
VIH –
VIL –
tDH
tRCS
tDS
D (DATA IN)
VIH –
VIL –
VALID DATA
tCAC
tAA
tOFF
tRAC
D (DATA OUT)
VOH –
VOL –
HIGH Z
VALID DATA

FAST PAGE MODE READ CYCLE

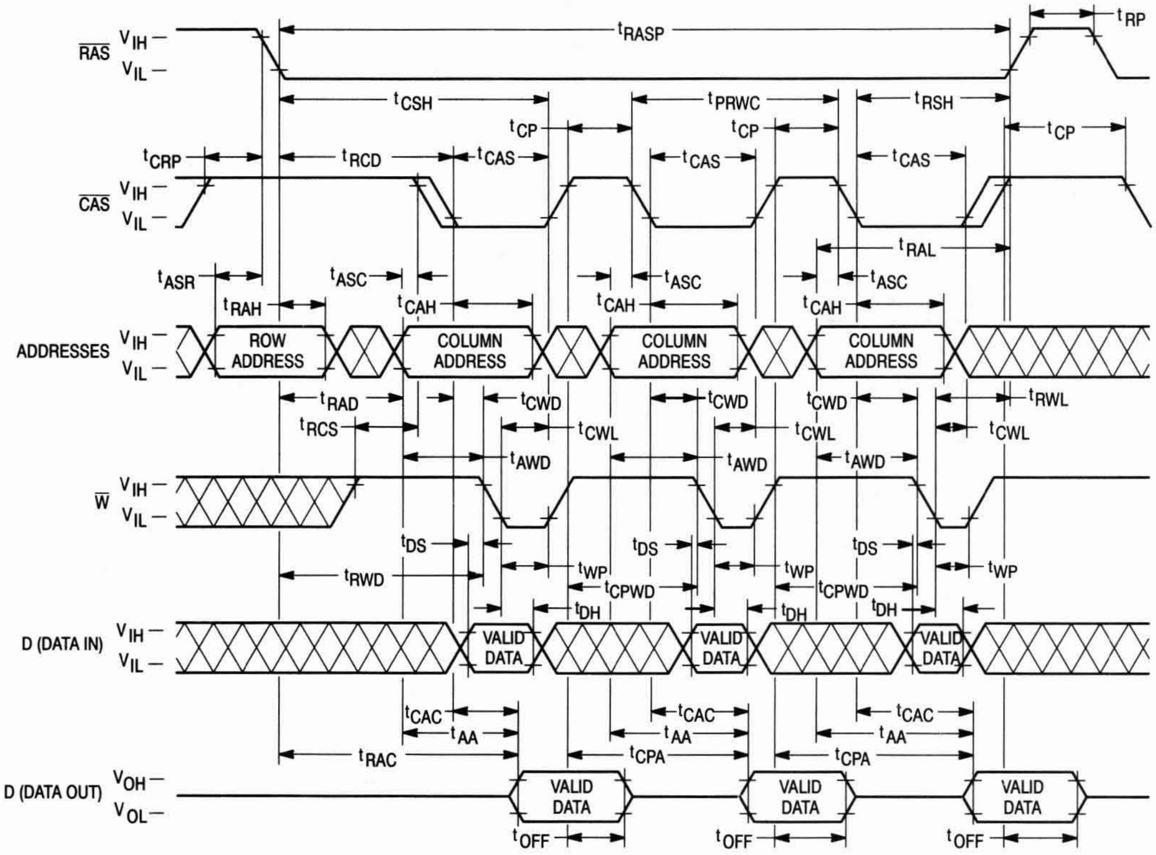


tRASP
tRP
tRHCP
RAS
VIH –
VIL –
tCSH
tPC
tRSH
tRCD
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCP
CAS
VIH –
VIL –
tCAH
tCAH
tCAH
tASC
tASC
tASC
tRAL
tASR
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAH
tRRH
tRCH
tRCH
tRAD
tRCS
tRCS
tRCS
tRCH
W
VIH –
VIL –
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
D (DATA OUT)
VOH –
VOL –
VALID DATA
VALID DATA
VALID DATA
tOFF
tOFF
tOFF

FAST PAGE MODE EARLY WRITE CYCLE

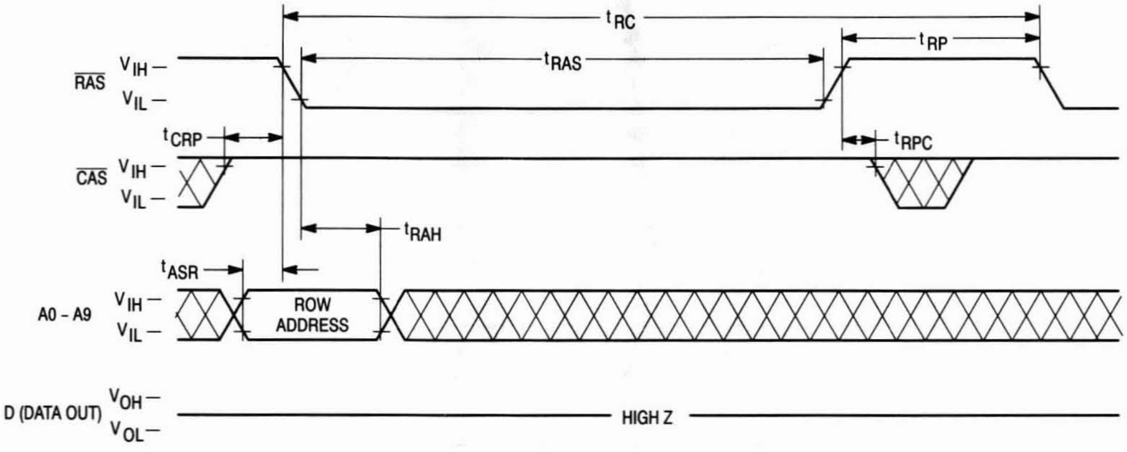

tRASP
tRP
tRHCP
RAS VIH VIL
tRCD
tPC
tRSH
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCP
CAS VIH VIL
tASC
tASC
tASC
tRAL
tASR
tRAH
tCAH
tCAH
tCAH
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tWCS
tWCH
tWCS
tWCH
tWCS
tWCH
tWP
tWP
tWP
W VIH VIL
tDS
tDS
tDS
tDH
tDH
tDH
D (DATA IN) VIH VIL
VALID DATA
VALID DATA
VALID DATA
D (DATA OUT) VOH VOL
HIGH Z

FAST PAGE MODE READ-WRITE CYCLE


tRASP
tRP
RAS VIH VIL
tCSH
tPRWC
tRSH
tCP
tCP
tCP
tCRP
tRCD
tCAS
tCAS
tCAS
CAS VIH VIL
tRAL
tASR
tASC
tASC
tASC
tRAH
tCAH
tCAH
tCAH
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tCWD
tCWD
tCWD
tRWL
tRCS
tCWL
tCWL
tCWL
tAWD
tAWD
tAWD
W VIH VIL
tDS
tDS
tDS
tRWD
tWP
tWP
tWP
tCPWD
tCPWD
tDH
tDH
tDH
D (DATA IN) VIH VIL
VALID DATA
VALID DATA
VALID DATA
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
D (DATA OUT) VOH VOL
VALID DATA
VALID DATA
VALID DATA
tOFF
tOFF
tOFF

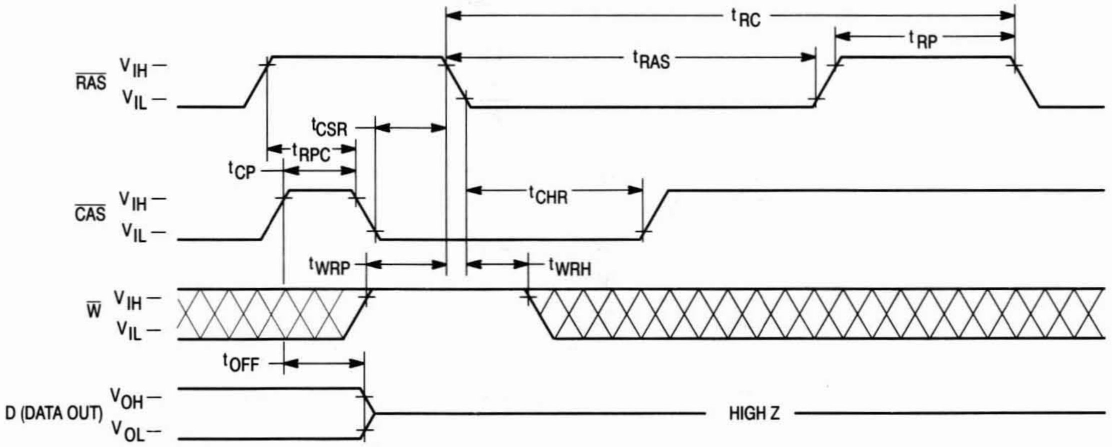
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

($\overline{\text{W}}$ and A10 are Don't Care)

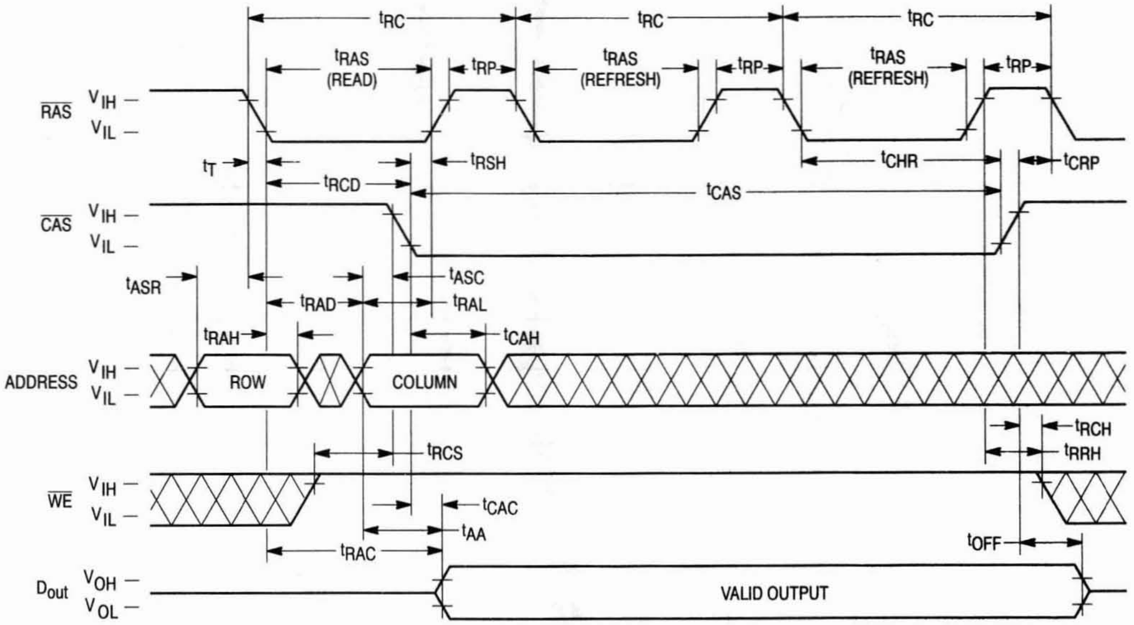

t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH} –
V_{IL} –
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$
V_{IH} –
V_{IL} –
t_{RAH}
t_{ASR}
A0 - A9
V_{IH} –
V_{IL} –
ROW ADDRESS
D (DATA OUT)
V_{OH} –
V_{OL} –
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

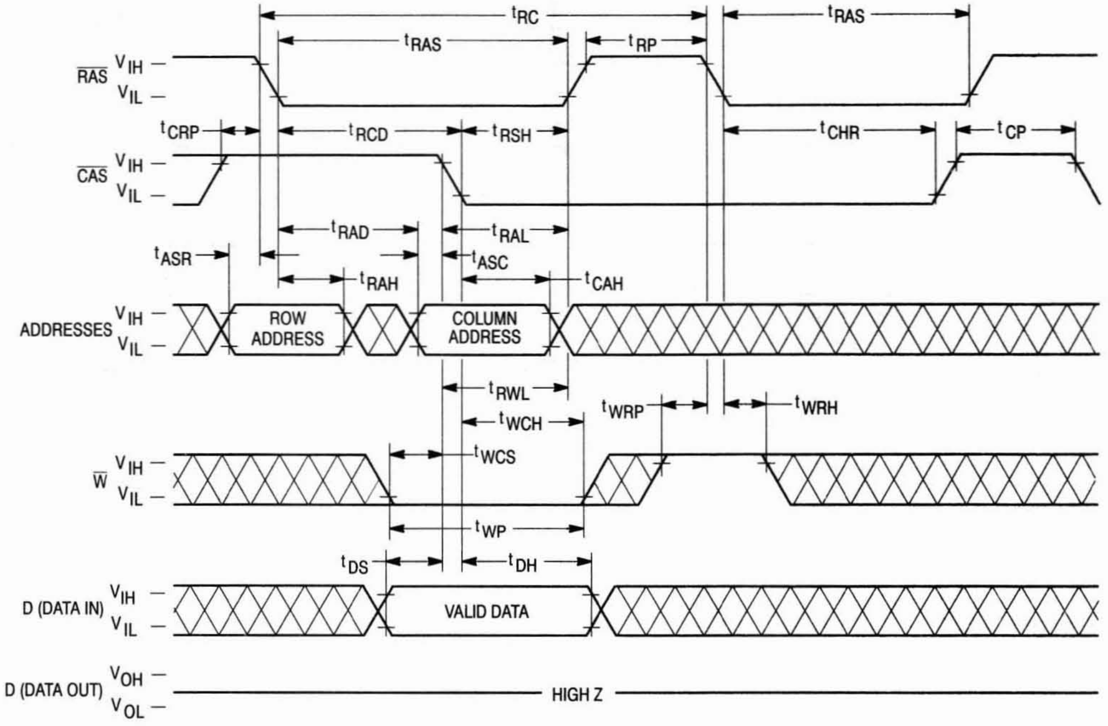
(A0 – A10 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH} –
V_{IL} –
t_{CSR}
t_{RPC}
t_{CP}
t_{CHR}
$\overline{\text{CAS}}$
V_{IH} –
V_{IL} –
t_{WRP}
t_{WRH}
$\overline{\text{W}}$
V_{IH} –
V_{IL} –
t_{OFF}
D (DATA OUT)
V_{OH} –
V_{OL} –
HIGH Z

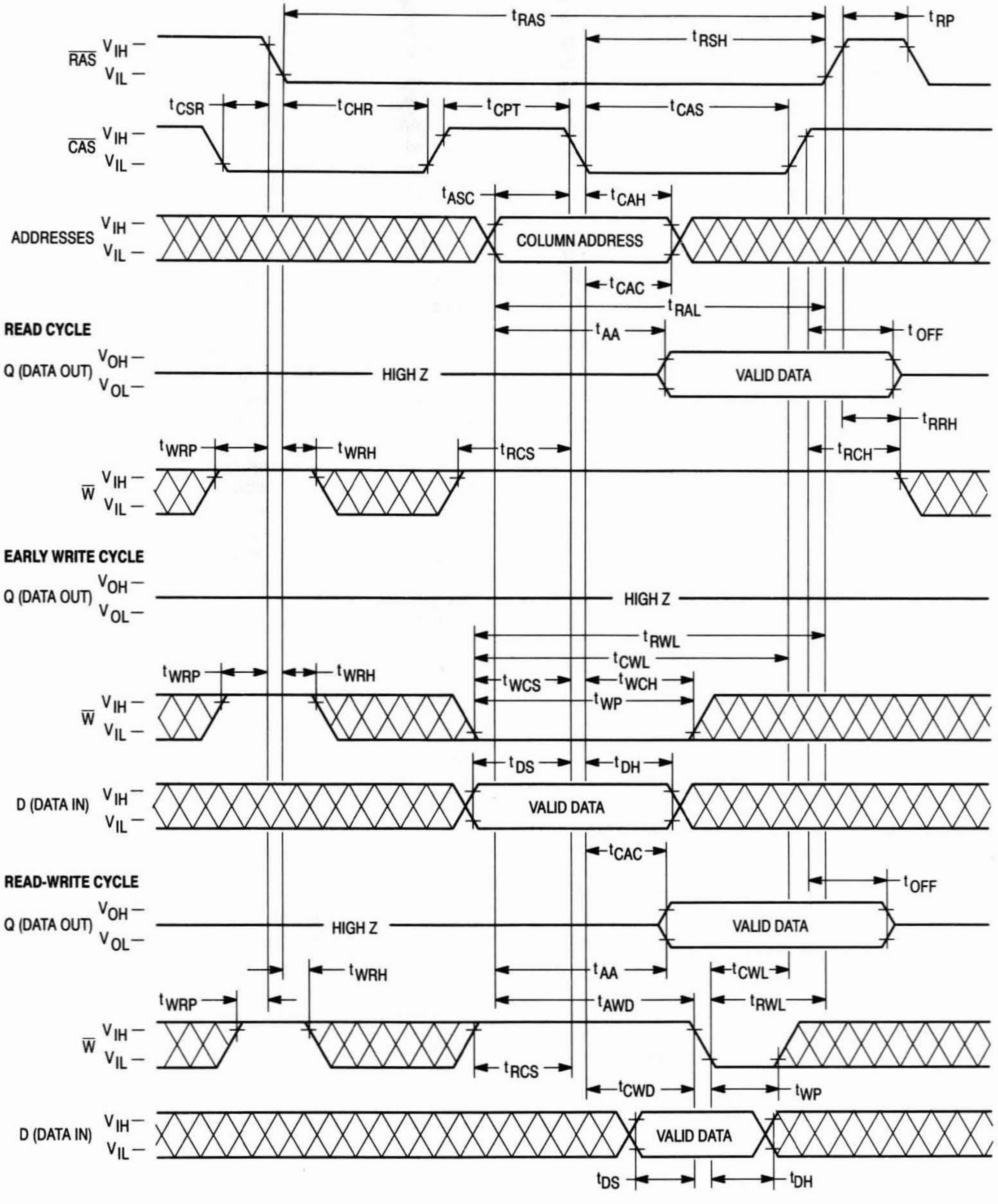
HIDDEN REFRESH CYCLE


tRC
tRC
tRC
tRAS (READ)
tRP
tRAS (REFRESH)
tRP
tRAS (REFRESH)
tRP
RAS
VIH
VIL
tT
tRSH
tCHR
tCRP
tRCD
tCAS
CAS
VIH
VIL
tASR
tASC
tRAD
tRAL
tRAH
tCAH
ADDRESS
VIH
VIL
ROW
COLUMN
tRCH
tRCS
tRRH
WE
VIH
VIL
tCAC
tAA
tRAC
tOFF
Dout
VOH
VOL
VALID OUTPUT

HIDDEN REFRESH CYCLE (EARLY WRITE)


tRC
tRAS
tRAS
tRP
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCP
CAS
VIH
VIL
tRAD
tRAL
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRWL
tWRP
tWRH
tWCH
tWCS
W
VIH
VIL
tWP
tDS
tDH
D (DATA IN)
VIH
VIL
VALID DATA
D (DATA OUT)
VOH
VOL
HIGH Z

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



t_{RAS}
t_{RP}
t_{RSH}
$\overline{RAS}$
V_{IH} –
V_{IL} –
t_{CSR}
t_{CHR}
t_{CPT}
t_{CAS}
$\overline{CAS}$
V_{IH} –
V_{IL} –
t_{ASC}
t_{CAH}
ADDRESSES
V_{IH} –
V_{IL} –
COLUMN ADDRESS
t_{CAC}
t_{RAL}
READ CYCLE
t_{AA}
t_{OFF}
Q (DATA OUT)
V_{OH} –
V_{OL} –
HIGH Z
VALID DATA
t_{RRH}
t_{WRP}
t_{WRH}
t_{RCS}
t_{RCH}
$\overline{W}$
V_{IH} –
V_{IL} –
EARLY WRITE CYCLE
Q (DATA OUT)
V_{OH} –
V_{OL} –
HIGH Z
t_{RWL}
t_{CWL}
t_{WRP}
t_{WRH}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{W}$
V_{IH} –
V_{IL} –
t_{DS}
t_{DH}
D (DATA IN)
V_{IH} –
V_{IL} –
VALID DATA
t_{CAC}
READ-WRITE CYCLE
t_{OFF}
Q (DATA OUT)
V_{OH} –
V_{OL} –
HIGH Z
VALID DATA
t_{WRH}
t_{AA}
t_{CWL}
t_{WRP}
t_{AWD}
t_{RWL}
$\overline{W}$
V_{IH} –
V_{IL} –
t_{RCS}
t_{CWD}
t_{WP}
D (DATA IN)
V_{IH} –
V_{IL} –
VALID DATA
t_{DS}
t_{DH}

DEVICE INITIALIZATION

On power-up, an initial pause of 100 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds or 128 milliseconds in case of low power device, with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 11-bit address fields. A total of twenty-two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 bit locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the 4M RAM: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window; however, $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ clock active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered elsewhere.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, $(t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \le t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but Q may be indeterminate (see note 17 of the AC Operating Conditions table). $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the 4M dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum of t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM44100 require refresh every 16 milliseconds, while refresh time for the MCM4L4100 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM44100, and 124.8 microseconds for the MCM4L4100. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM44100 and 128 milliseconds on the MCM4L4100.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{\text{RAS}}$ active transition to prevent switching the device into **test mode**.

Hidden Refresh

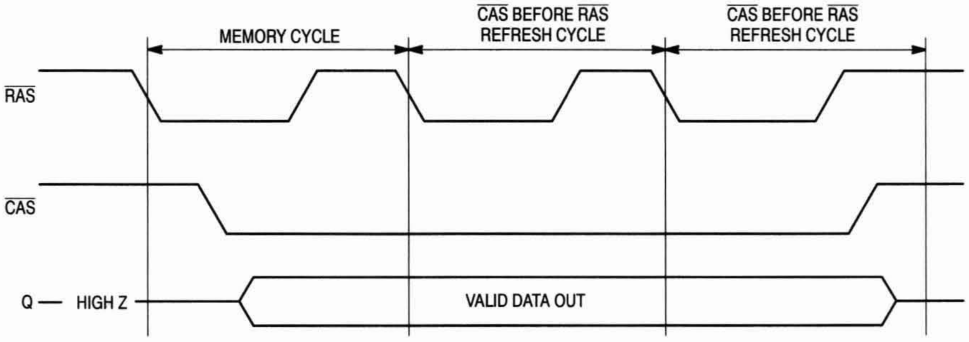
Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode entry) as in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of 8 **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.



MEMORY CYCLE
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
Q — HIGH Z
VALID DATA OUT

Figure 1. Hidden Refresh Cycle

TEST MODE

The internal organization of this device (512K x 8) allows it to be tested as if it were a 512K x 1 DRAM. Nineteen of the twenty two addresses are used when operating the device in test mode. Row address A0, and column addresses A0 and A10 are ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0 – B7) in parallel. External data out is determined by the internal test mode logic of the device. See the following truth table and test mode block diagram.

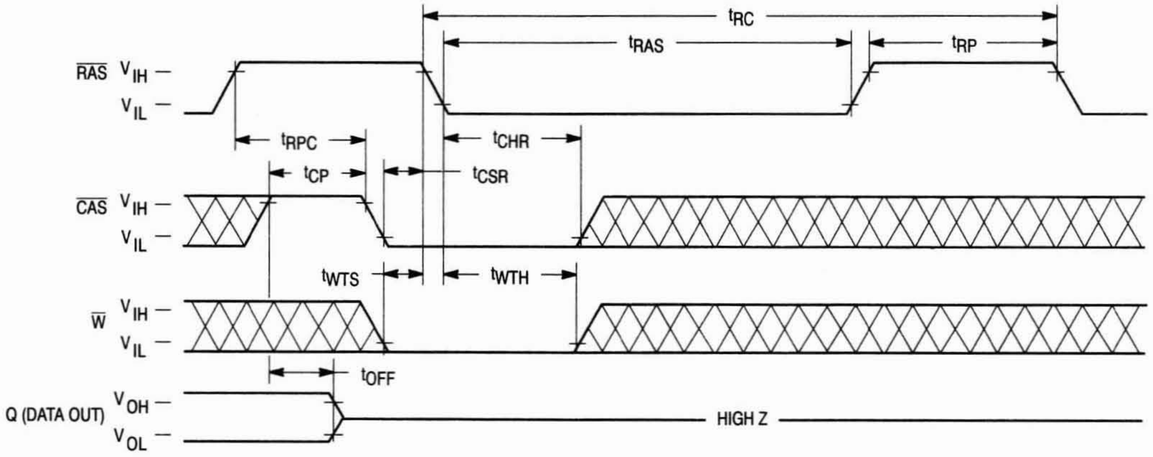
$\overline{\text{W}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ timing puts the device in **Test Mode** as shown in the test mode timing diagram. A **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** or a **$\overline{\text{RAS}}$-only refresh cycle** puts the device back into normal mode. Refresh is performed in test mode by using a **$\overline{\text{W}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle** which uses internal refresh address counter.

TEST MODE TRUTH TABLE

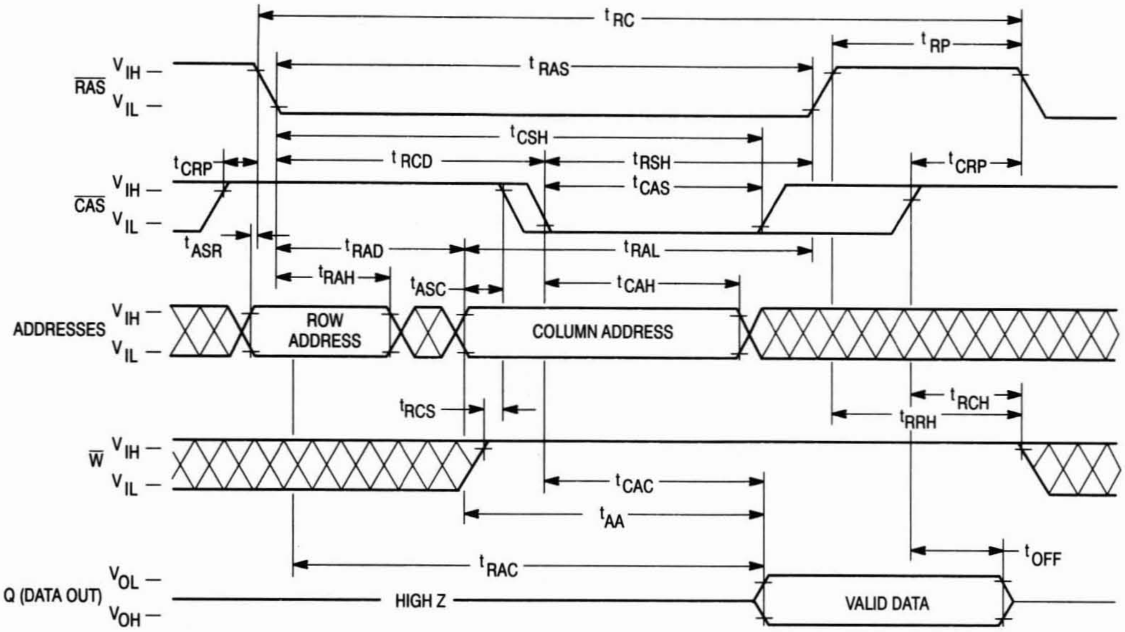
D	B0	B1	B2	B3	B4	B5	B6	B7	Q
0	0	0	0	0	0	0	0	0	1
1	1	1	1	1	1	1	1	1	1
—	Any Other								0

$\overline{\text{W}}$, $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE (TEST MODE ENTRY)

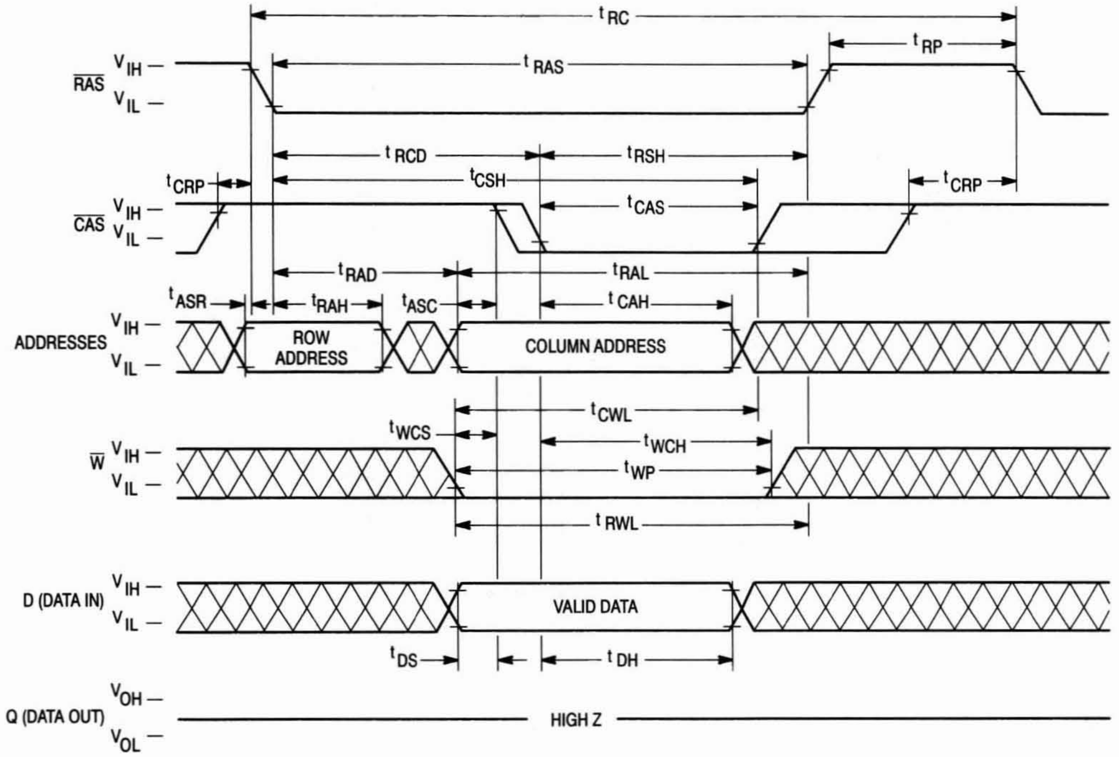
(D and A0 – A10 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH} –
V_{IL} –
t_{RPC}
t_{CHR}
t_{CP}
t_{CSR}
$\overline{\text{CAS}}$
V_{IH} –
V_{IL} –
t_{WTS}
t_{WTH}
$\overline{\text{W}}$
V_{IH} –
V_{IL} –
t_{OFF}
Q (DATA OUT)
V_{OH} –
V_{OL} –
HIGH Z

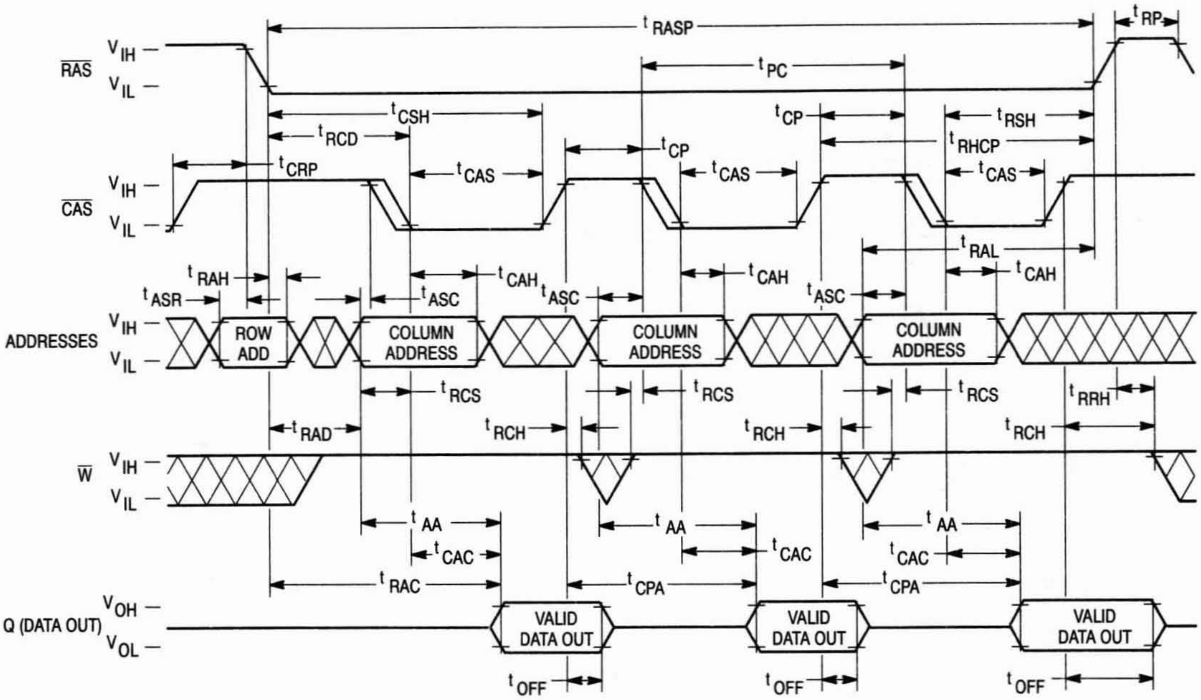
TEST MODE – READ CYCLE


t RC
t RP
t RAS
RAS
V IH –
V IL –
t CSH
t CRP
t RCD
t RSH
t CAS
t CRP
CAS
V IH –
V IL –
t ASR
t RAD
t RAL
t RAH
t ASC
t CAH
ADDRESSES
V IH –
V IL –
ROW ADDRESS
COLUMN ADDRESS
t RCS
t RCH
t RRH
W
V IH –
V IL –
t CAC
t AA
t RAC
t OFF
Q (DATA OUT)
V OL –
V OH –
HIGH Z
VALID DATA

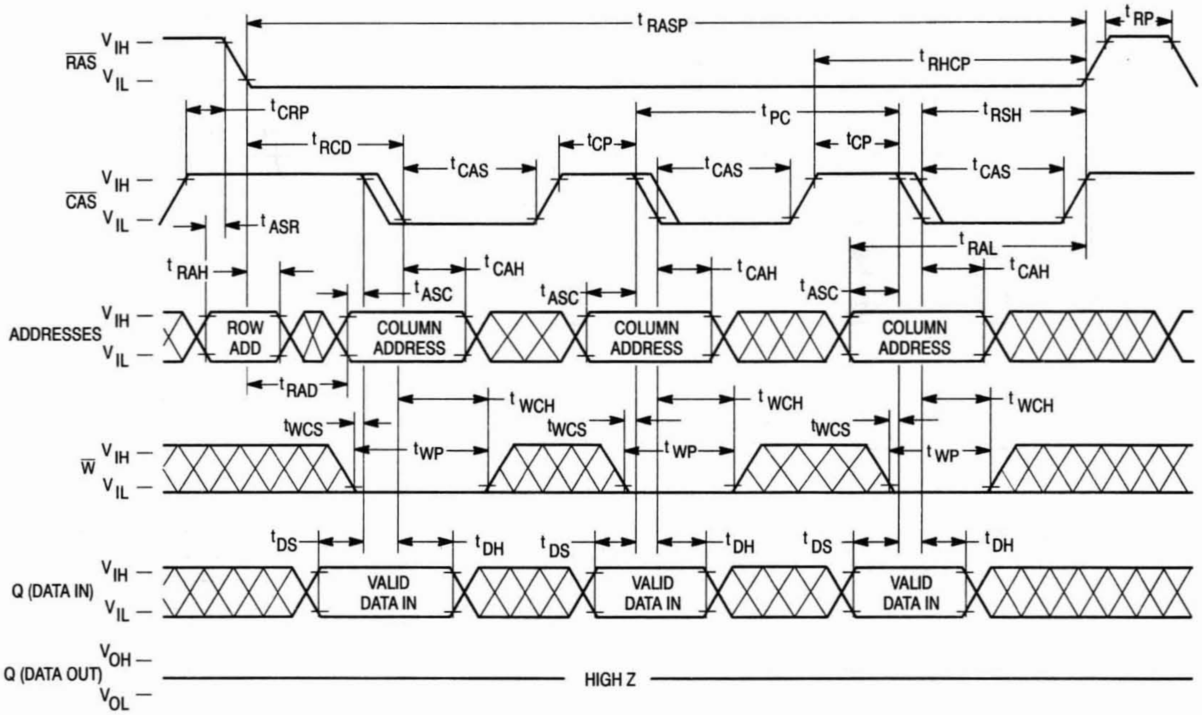
TEST MODE – EARLY WRITE CYCLE


t RC
t RP
t RAS
RAS
V IH –
V IL –
t RCD
t RSH
t CRP
t CSH
t CRP
t CAS
CAS
V IH –
V IL –
t RAD
t RAL
t ASR
t RAH
t ASC
t CAH
ADDRESSES
V IH –
V IL –
ROW ADDRESS
COLUMN ADDRESS
t CWL
t WCS
t WCH
t WP
W
V IH –
V IL –
t RWL
D (DATA IN)
V IH –
V IL –
VALID DATA
t DS
t DH
Q (DATA OUT)
V OH –
V OL –
HIGH Z

TEST MODE – FAST PAGE MODE READ CYCLE


RAS
CAS
ADDRESSES
W
Q (DATA OUT)
V_{IH}
V_{IL}
V_{OH}
V_{OL}
t_{RASP}
t_{RP}
t_{PC}
t_{CSH}
t_{RCD}
t_{CRP}
t_{CAS}
t_{CP}
t_{RSH}
t_{RHCP}
t_{RAL}
t_{RAH}
t_{ASR}
t_{CAH}
t_{ASC}
ROW ADD
COLUMN ADDRESS
t_{RCS}
t_{RRH}
t_{RAD}
t_{RCH}
t_{AA}
t_{CAC}
t_{RAC}
t_{CPA}
VALID DATA OUT
t_{OFF}

TEST MODE – FAST PAGE MODE EARLY WRITE CYCLE


RAS
CAS
ADDRESSES
W
Q (DATA IN)
Q (DATA OUT)
V_{IH}
V_{IL}
V_{OH}
V_{OL}
t_{RASP}
t_{RP}
t_{RHCP}
t_{CRP}
t_{PC}
t_{RSH}
t_{RCD}
t_{CP}
t_{CAS}
t_{ASR}
t_{RAL}
t_{RAH}
t_{CAH}
t_{ASC}
ROW ADD
COLUMN ADDRESS
t_{RAD}
t_{WCH}
t_{WCS}
t_{WP}
t_{DS}
t_{DH}
VALID DATA IN
HIGH Z

ORDERING INFORMATION

(Order by Full Part Number)

MCM 44100 or 4L4100 X XX XX

Motorola Memory Prefix — MCM

Part Number — 44100 or 4L4100

Package (N = 300 mil SOJ, Z = 100 mil Plastic ZIP) — X

Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Shipping Method (R2 = Tape and Reel, Blank = Rails) — XX

Full Part Numbers —

MCM44100N60	MCM44100N60R2	MCM44100Z60
MCM44100N70	MCM44100N70R2	MCM44100Z70
MCM44100N80	MCM44100N80R2	MCM44100Z80
MCM4L4100N60	MCM4L4100N60R2	MCM4L4100Z60
MCM4L4100N70	MCM4L4100N70R2	MCM4L4100Z70
MCM4L4100N80	MCM4L4100N80R2	MCM4L4100Z80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM44400
MCM4L4400

Advance Information

1M x 4 CMOS Dynamic RAM

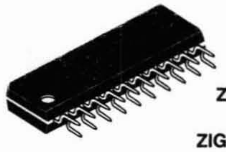
Fast Page Mode

The MCM44400 is a 0.8μ CMOS high-speed dynamic random access memory. It is organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM44400 requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil J-lead small outline package, and a 100 mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Fast Page Mode
- Test Mode
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  - MCM44400 = 16 ms
  - MCM4L4400 = 128 ms
- Fast Access Time (t_{RAC}):
  - MCM44400-60 and MCM4L4400-60 = 60 ns (Max)
  - MCM44400-70 and MCM4L4400-70 = 70 ns (Max)
  - MCM44400-80 and MCM4L4400-80 = 80 ns (Max)
- Low Active Power Dissipation:
  - MCM44400-60 and MCM4L4400-60 = 605 mW (Max)
  - MCM44400-70 and MCM4L4400-70 = 550 mW (Max)
  - MCM44400-80 and MCM4L4400-80 = 495 mW (Max)
- Low Standby Power Dissipation:
  - MCM44400 and MCM4L4400 = 11 mW (Max, TTL Levels)
  - MCM44400 = 5.5 mW (Max, CMOS Levels)
  - MCM4L4400 = 1.1 mW (Max, CMOS Levels)

N PACKAGE
300 MIL SOJ
CASE 822B-01

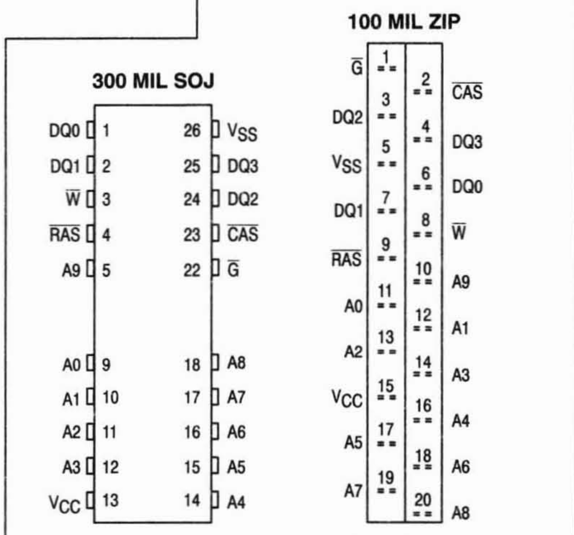


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836A-01

PIN NAMES

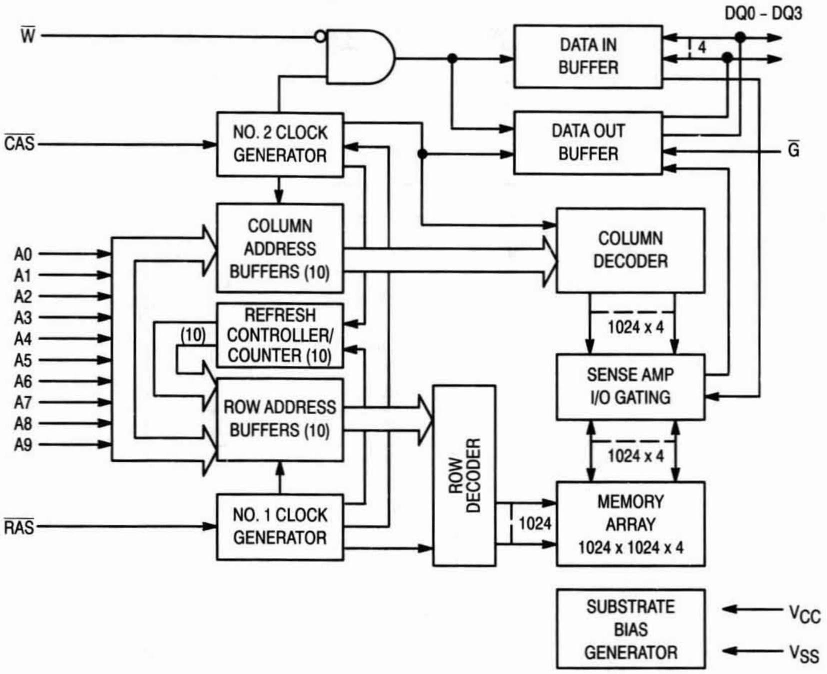
A0 – A9	Address Inputs
DQ0 – DQ3	Data Input/Output
$\overline{\text{G}}$	Output Enable
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

PIN ASSIGNMENTS


100 MIL ZIP
300 MIL SOJ
DQ0 1
DQ1 2
$\overline{\text{W}}$ 3
$\overline{\text{RAS}}$ 4
A9 5
A0 9
A1 10
A2 11
A3 12
V_{CC} 13
26 V_{SS}
25 DQ3
24 DQ2
23 $\overline{\text{CAS}}$
22 $\overline{\text{G}}$
18 A8
17 A7
16 A6
15 A5
14 A4
$\overline{\text{G}}$ 1
2 $\overline{\text{CAS}}$
DQ2 3
4 DQ3
V_{SS} 5
6 DQ0
DQ1 7
8 $\overline{\text{W}}$
$\overline{\text{RAS}}$ 9
10 A9
A0 11
12 A1
A2 13
14 A3
V_{CC} 15
16 A4
A5 17
18 A6
A7 19
20 A8

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM


W̄
CAS̄
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
RAS̄
NO. 2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (10)
REFRESH CONTROLLER/ COUNTER (10)
(10)
ROW ADDRESS BUFFERS (10)
NO. 1 CLOCK GENERATOR
ROW DECODER
DATA IN BUFFER
DATA OUT BUFFER
DQ0 - DQ3
4
Ḡ
COLUMN DECODER
1024 x 4
SENSE AMP I/O GATING
1024 x 4
MEMORY ARRAY 1024 x 1024 x 4
1024
SUBSTRATE BIAS GENERATOR
VCC
VSS

3

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	1, 2
MCM44400-60 and MCM4L4400-60, t_{RC} = 110 ns		—	110		
MCM44400-70 and MCM4L4400-70, t_{RC} = 130 ns		—	100		
MCM44400-80 and MCM4L4400-80, t_{RC} = 150 ns		—	90		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	1, 2
MCM44400-60 and MCM4L4400-60, t_{RC} = 110 ns		—	110		
MCM44400-70 and MCM4L4400-70, t_{RC} = 130 ns		—	100		
MCM44400-80 and MCM4L4400-80, t_{RC} = 150 ns		—	90		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	1, 3
MCM44400-60 and MCM4L4400-60, t_{PC} = 45 ns		—	110		
MCM44400-70 and MCM4L4400-70, t_{PC} = 45 ns		—	100		
MCM44400-80 and MCM4L4400-80, t_{PC} = 50 ns		—	90		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}				
MCM44400		—	1.0	mA	
MCM4L4400		—	200	µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	1
MCM44400-60 and MCM4L4400-60, t_{RC} = 110 ns		—	110		
MCM44400-70 and MCM4L4400-70, t_{RC} = 130 ns		—	100		
MCM44400-80 and MCM4L4400-80, t_{RC} = 150 ns		—	90		
V_{CC} Power Supply Current, Battery Backup Mode — MCM4L4400 Only (t_{RC} = 125 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2 V; $\overline{G}$, $\overline{W}$ = V_{CC} – 0.2 V; A0 – A9 = V_{CC} – 0.2 V or 0.2 V; DQ0 – DQ3 = V_{CC} – 0.2 V or 0.2 V or OPEN; t_{RAS} = Min to 1 µs)	I_{CC7}	—	300	µA	1, 4
Standby Current — $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Q = Enable	I_{CC8}	—	5	mA	1
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	V_{CC}	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	0	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Column address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. t_{RAS} (max) = 1 µs is only applied to refresh of battery-back up. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A9	C_{in}	5	pF
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0 – DQ3	$C_{I/O}$	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM44400-60 MCM4L4400-60		MCM44400-70 MCM4L4400-70		MCM44400-80 MCM4L4400-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	150	—	180	—	200	—	ns	6
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	50	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	80	—	95	—	100	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	7,8,9
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	15	—	20	—	20	ns	7,9,10,11
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	7,9,11,12
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	—	40	—	45	ns	7,9,11
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	20	0	20	ns	13
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	1
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	—	100 k	—	100 k	—	100 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	15	—	20	—	20	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	t_{CEHREH}	t_{RHCP}	35	—	40	—	45	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	15	10 k	20	10 k	20	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	45	20	50	20	60	ns	14
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	15
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	

NOTES:

(continued)

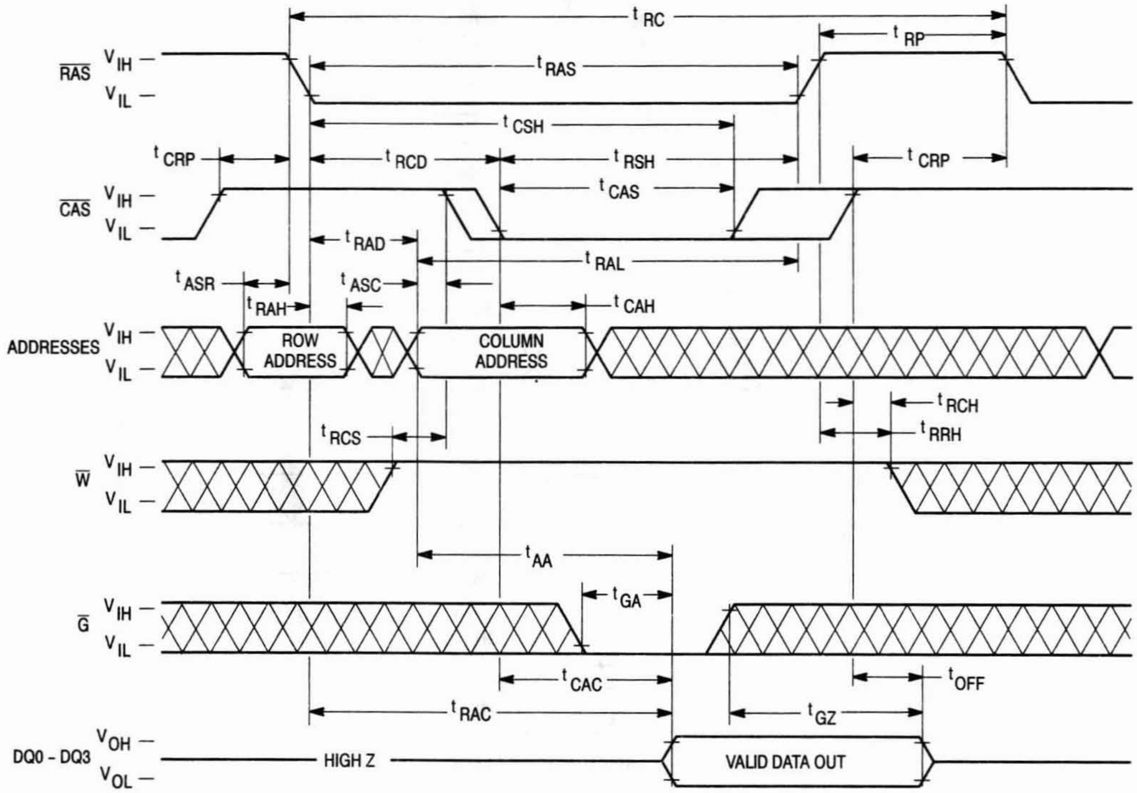
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100 μs is required after power-up followed by 8 initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements assume t_T = 5.0 ns.
5. In delayed write or read modify write cycles, must disable output buffer prior to applying data to the device.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
7. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \le t_{RCD}$ (max) and $t_{RAD} \le t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC}, and t_{CPA} is delayed for 2 ns to 5 ns for the specified value. These parameters should be in the test mode cycles by adding the above value to the specified value in the data sheet.
10. Assumes that $t_{RCD} \ge t_{RCD}$ (max) and $t_{RAD} \le t_{RAD}$ (max).
11. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
12. Assumes that $t_{RCD} \le t_{RCD}$ (max) and $t_{RAD} \ge t_{RAD}$ (max).
13. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM44400-60 MCM4L4400-60		MCM44400-70 MCM4L4400-70		MCM44400-80 MCM4L4400-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	16
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	16
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	10	—	10	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	15	—	20	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	15	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	17
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	17
Refresh Period MCM44400 MCM4L4400	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	18
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	35	—	45	—	45	—	ns	18
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	80	—	95	—	105	—	ns	18
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	50	—	60	—	65	—	ns	18
$\overline{CAS}$ Precharge to Write Delay Time (Page Mode)	t_{CEHWL}	t_{CPWD}	55	—	65	—	70	—	ns	18
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Time	t_{CEHCEL}	t_{CPT}	40	—	40	—	40	—	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	—	15	—	20	—	20	ns	7
$\overline{G}$ to Data Delay	t_{GLHDX}	t_{GD}	15	—	20	—	20	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	15	0	20	0	20	ns	13
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	15	—	20	—	20	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	0	—	0	—	0	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	ns	
Write to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{WHREL}	t_{WRP}	0	—	0	—	0	—	ns	
Write to $\overline{RAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	

16. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
17. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in read-write cycles.
18. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE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RAS
VIH
VIL
tCSH
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CAS
VIH
VIL
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tRAD
tRAL
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRCH
tRCS
tRRH
W
VIH
VIL
tAA
G
VIH
VIL
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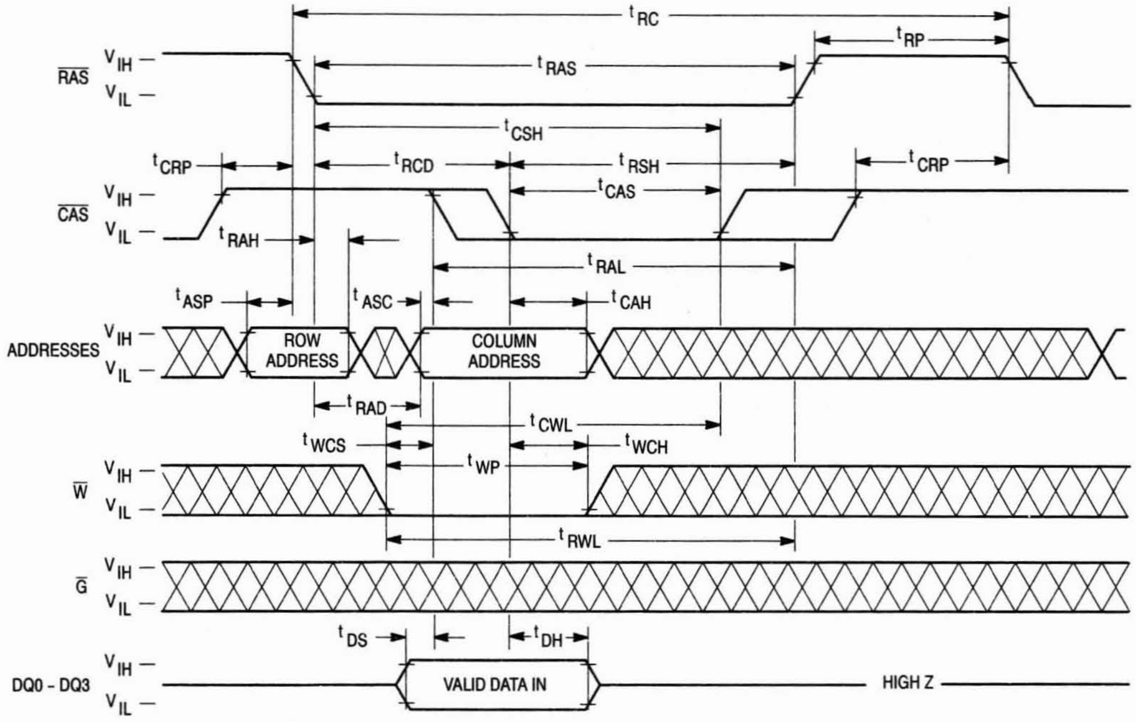
tOFF
tRAC
tGZ
DQ0 - DQ3
VOH
VOL
HIGH Z
VALID DATA OUT

EARLY WRITE CYCLE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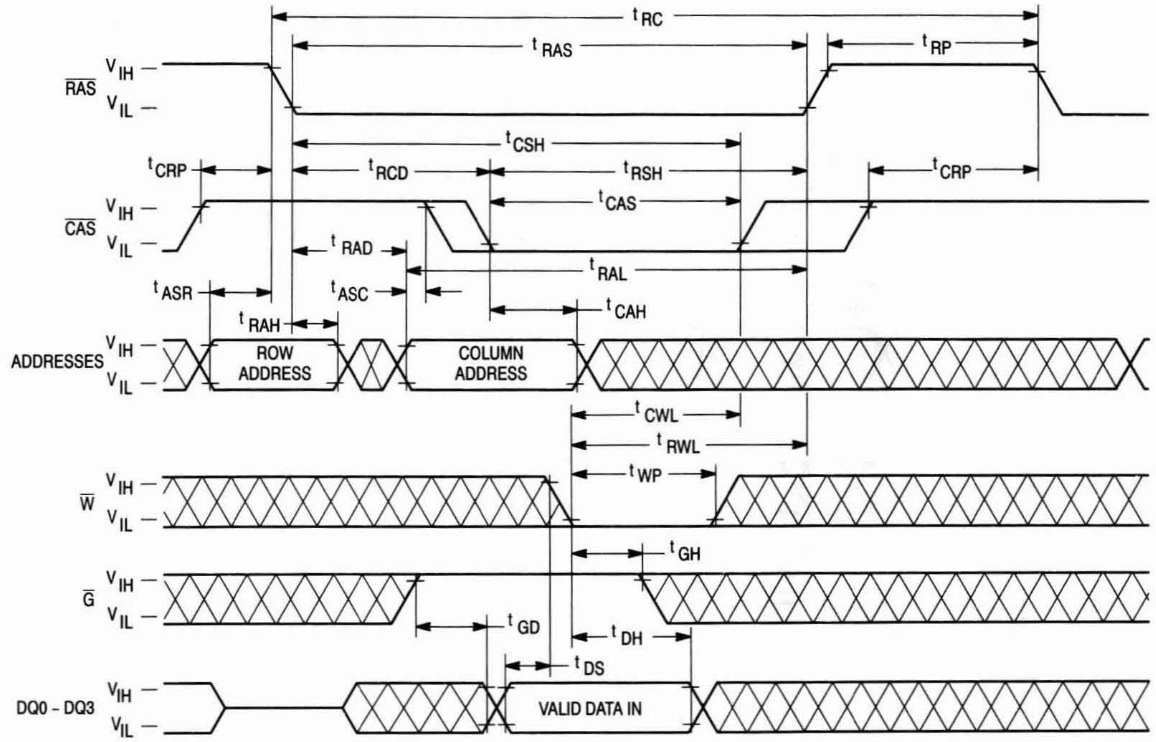
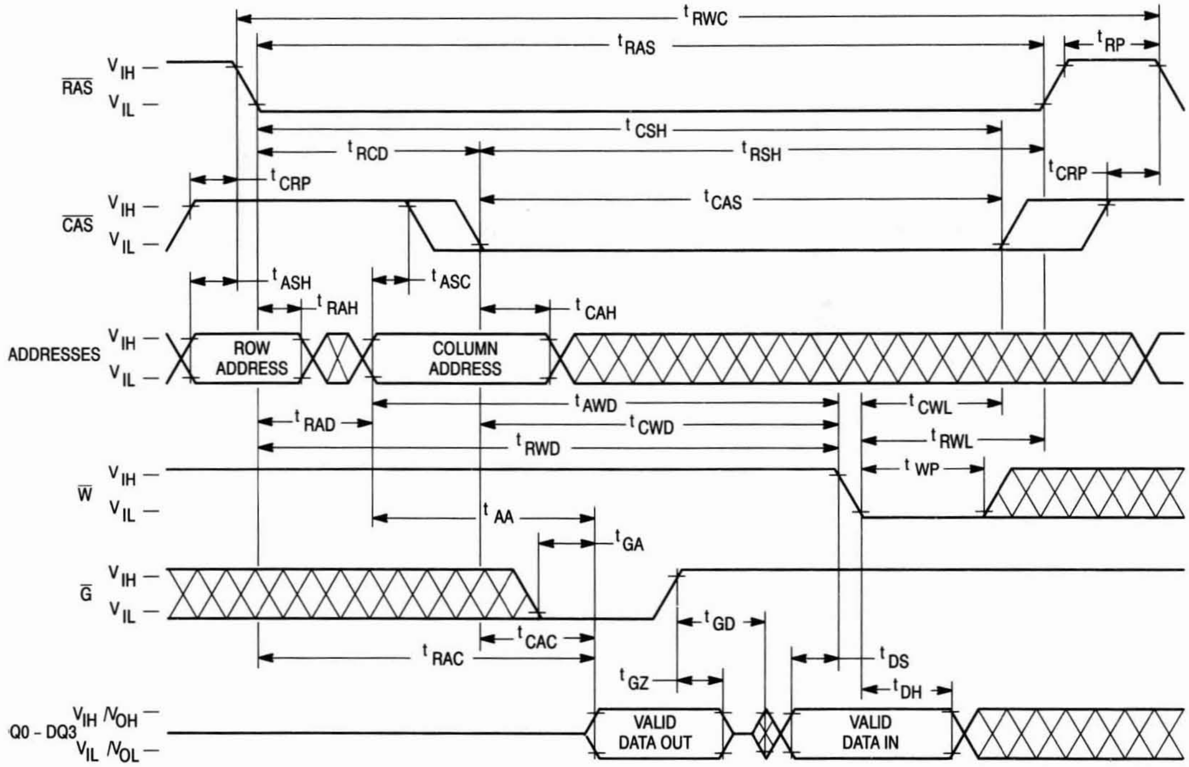
CAS
VIH
VIL
tCAS
tRAH
tRAL
tASP
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAD
tCWL
tWCS
tWCH
tWP
W
VIH
VIL
tRWL
G
VIH
VIL
tDS
tDH
DQ0 - DQ3
VIH
VIL
VALID DATA IN
HIGH Z

$\overline{G}$ CONTROLLED WRITE CYCLE



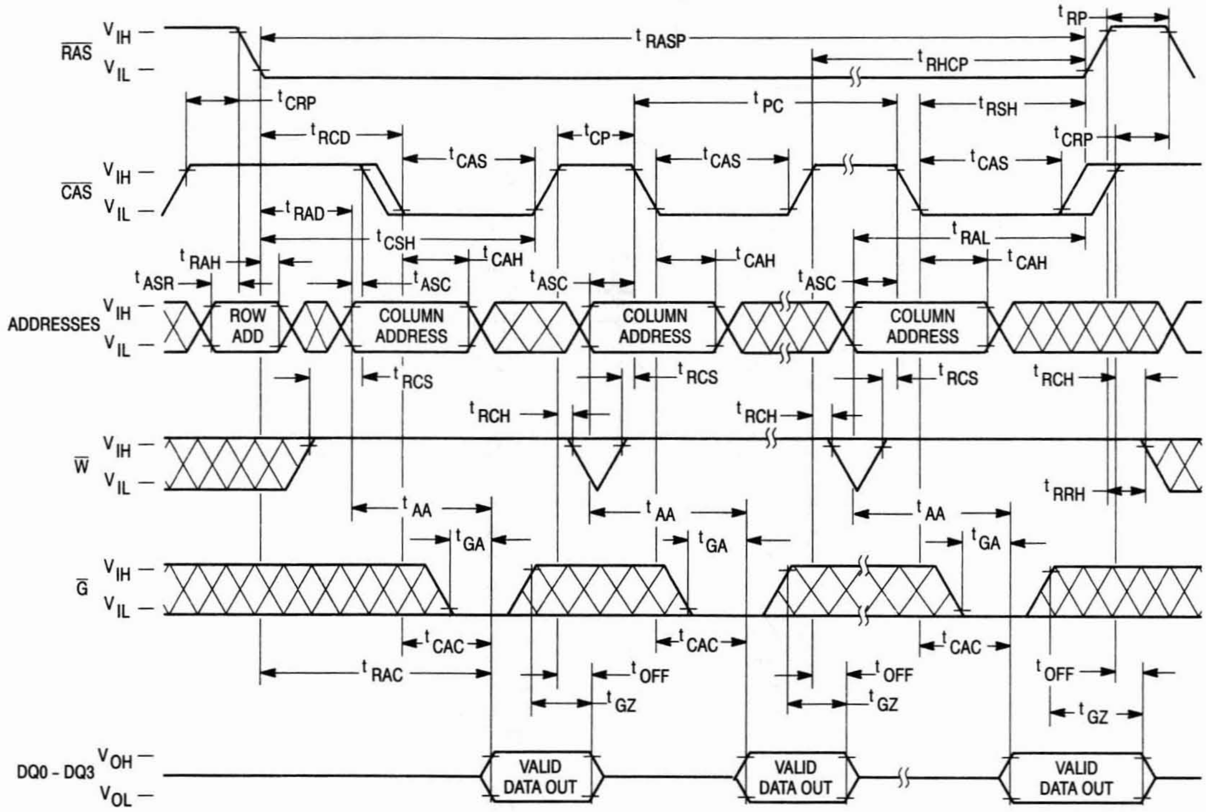
tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
tRAD
tRAL
tASR
tASC
tCAH
tRAH
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tCWL
tRWL
tWP
W
tGH
G
tGD
tDH
tDS
DQ0 – DQ3
VALID DATA IN

READ-WRITE CYCLE

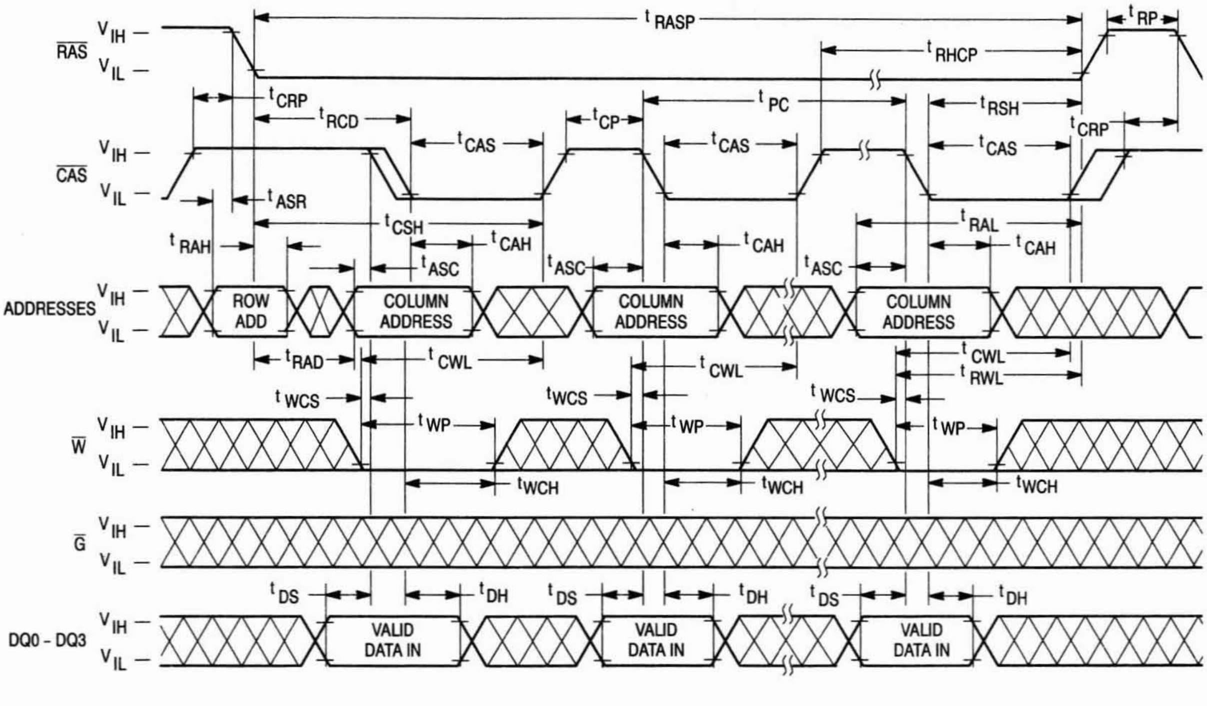


tRWC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
tCRP
tCAS
CAS
tASH
tASC
tRAH
tCAH
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tAWD
tCWL
tRAD
tCWD
tRWD
tRWL
tWP
W
tAA
tGA
G
tGD
tCAC
tRAC
tDS
tGZ
tDH
Q0 – DQ3
VIH/VOH
VIL/VOL
VALID DATA OUT
VALID DATA IN

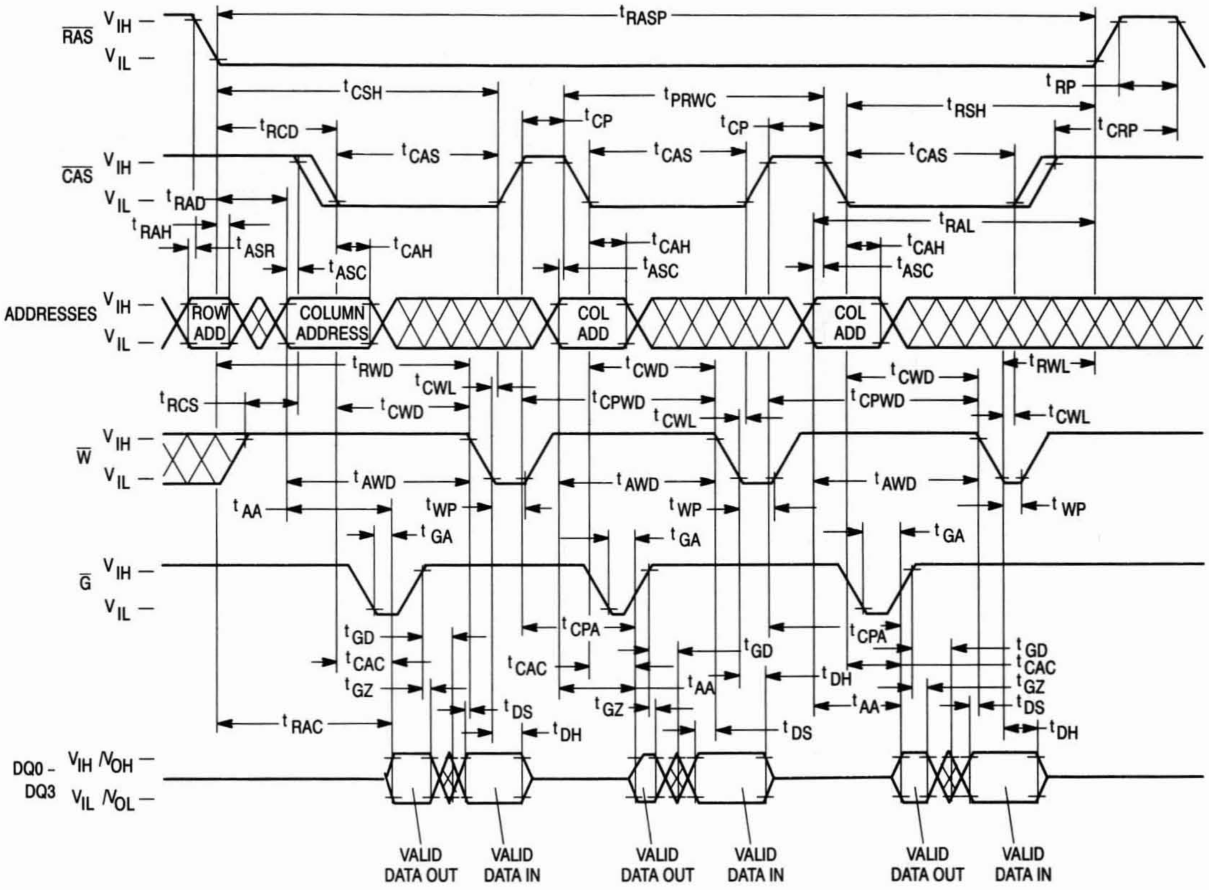
FAST PAGE MODE READ CYCLE


RAS
CAS
ADDRESSES
W
G
DQ0 - DQ3
V_{IH}
V_{IL}
V_{OH}
V_{OL}
t_{RP}
t_{RASP}
t_{RHCP}
t_{CRP}
t_{PC}
t_{RSH}
t_{RCD}
t_{CAS}
t_{CP}
t_{RAD}
t_{CSH}
t_{RAL}
t_{RAH}
t_{CAH}
t_{ASR}
t_{ASC}
ROW ADD
COLUMN ADDRESS
t_{RCS}
t_{RCH}
t_{RRH}
t_{AA}
t_{GA}
t_{CAC}
t_{RAC}
t_{OFF}
t_{GZ}
VALID DATA OUT

FAST PAGE MODE EARLY WRITE CYCLE

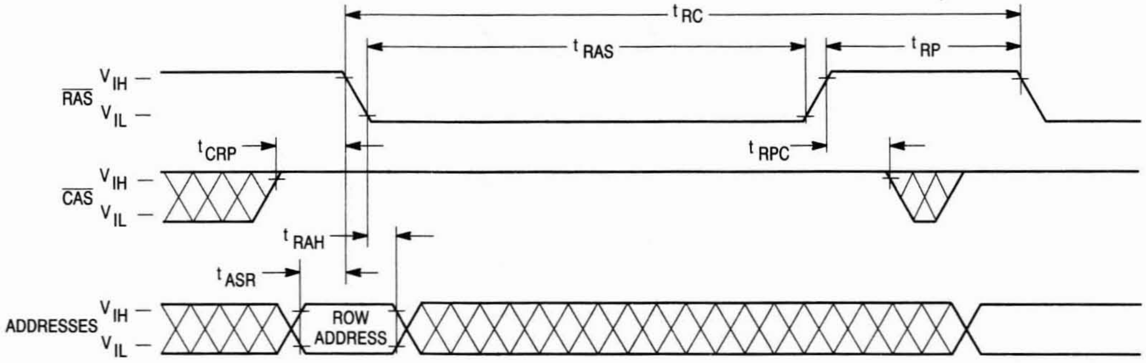

RAS
CAS
ADDRESSES
W
G
DQ0 - DQ3
V_{IH}
V_{IL}
t_{RASP}
t_{RP}
t_{RHCP}
t_{CRP}
t_{PC}
t_{RSH}
t_{RCD}
t_{CP}
t_{CAS}
t_{ASR}
t_{CSH}
t_{RAL}
t_{RAH}
t_{CAH}
t_{ASC}
ROW ADD
COLUMN ADDRESS
t_{RAD}
t_{CWL}
t_{RWL}
t_{WCS}
t_{WP}
t_{WCH}
t_{DS}
t_{DH}
VALID DATA IN

FAST PAGE MODE READ-WRITE CYCLE


RAS
VIH
VIL
tRASP
tRP
tCSH
tPRWC
tRSH
tCRP
tRCD
tCP
tCAS
CAS
tRAD
tRAH
tASR
tCAH
tASC
tRAL
ADDRESSES
ROW ADD
COLUMN ADDRESS
COL ADD
tRWD
tCWL
tCWD
tCPWD
tRWL
tRCS
W
tAWD
tAA
tWP
tGA
G
tGD
tCAC
tGZ
tCPA
tDS
tDH
tRAC
DQ0 - DQ3
VOH
VOL
VALID DATA OUT
VALID DATA IN

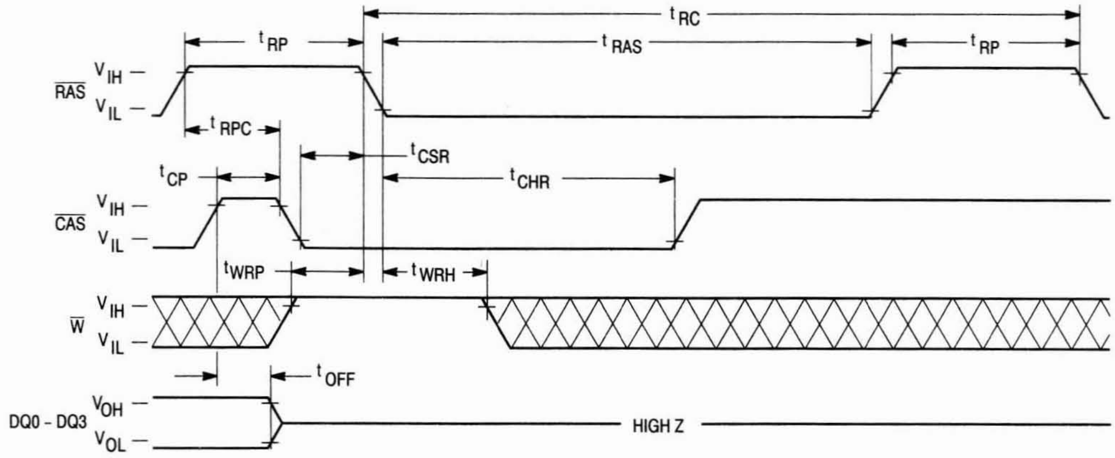
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

($\overline{\text{W}}$ and $\overline{\text{G}}$ are Don't Care)

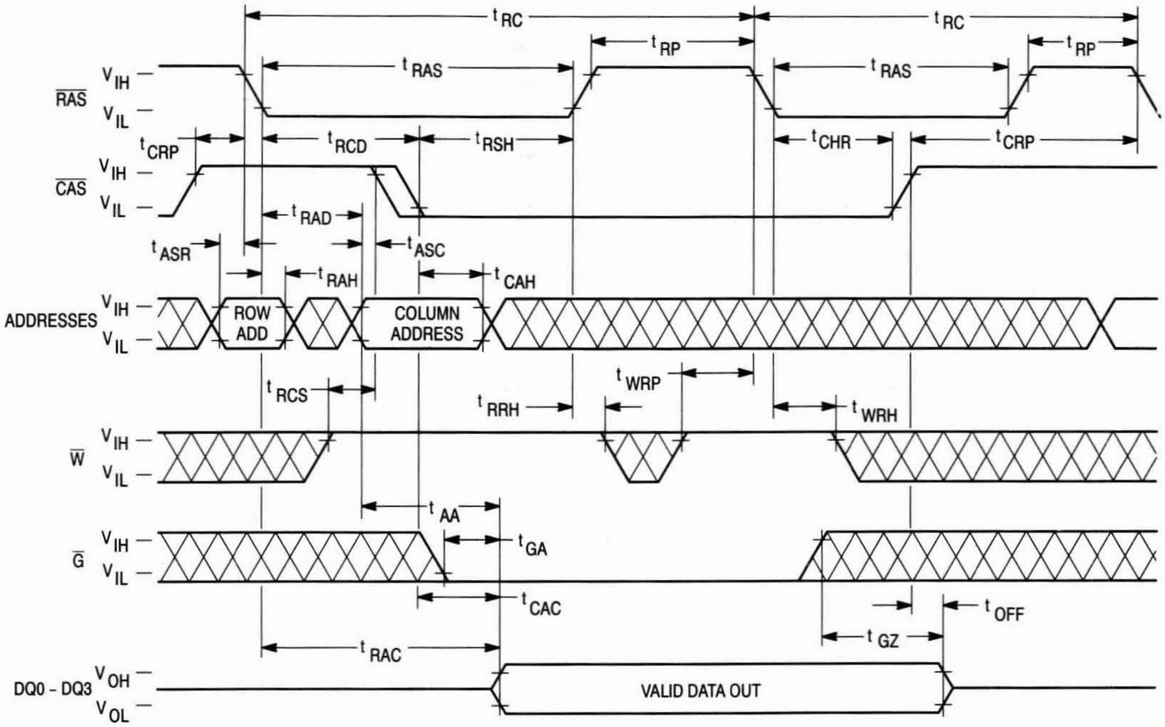

t RC
t RAS
t RP
RAS
V IH
V IL
t CRP
t RPC
CAS
V IH
V IL
t RAH
t ASR
ADDRESSES
V IH
V IL
ROW ADDRESS

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

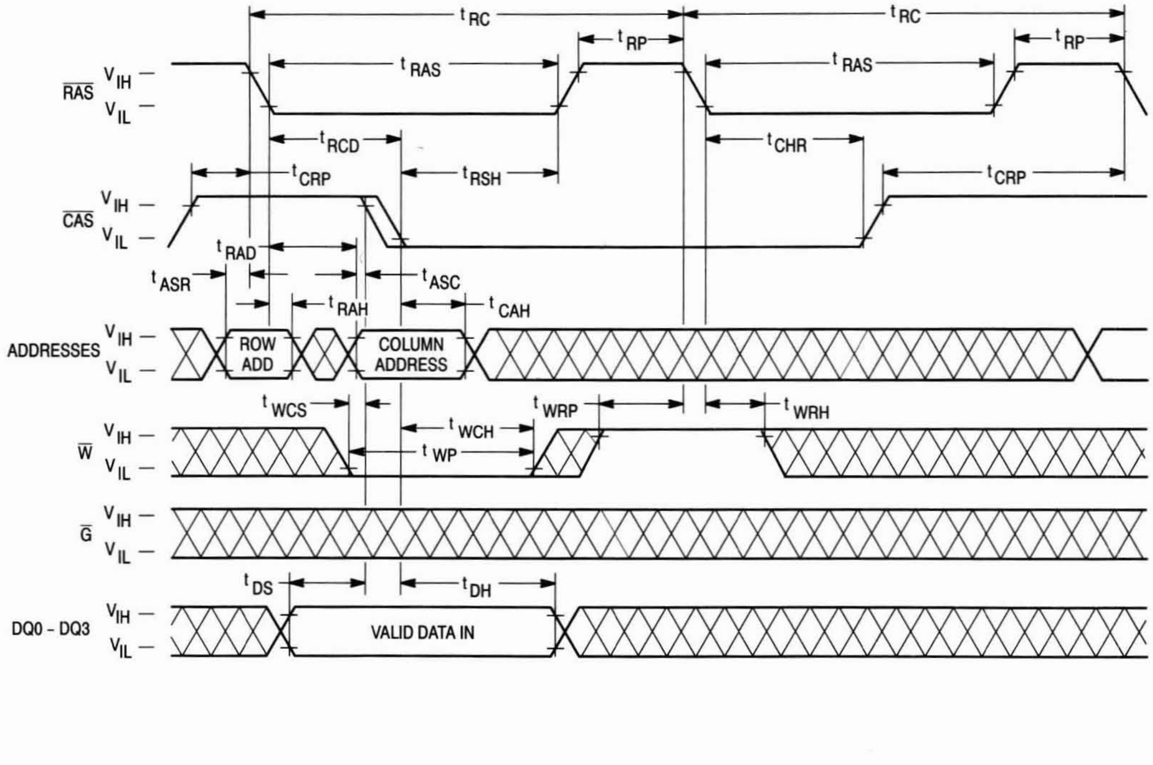
($\overline{\text{G}}$ and A0 – A9 are Don't Care)


t RC
t RP
t RAS
t RP
RAS
V IH
V IL
t RPC
t CSR
t CP
t CHR
CAS
V IH
V IL
t WRP
t WRH
W
V IH
V IL
t OFF
DQ0 - DQ3
V OH
V OL
HIGH Z

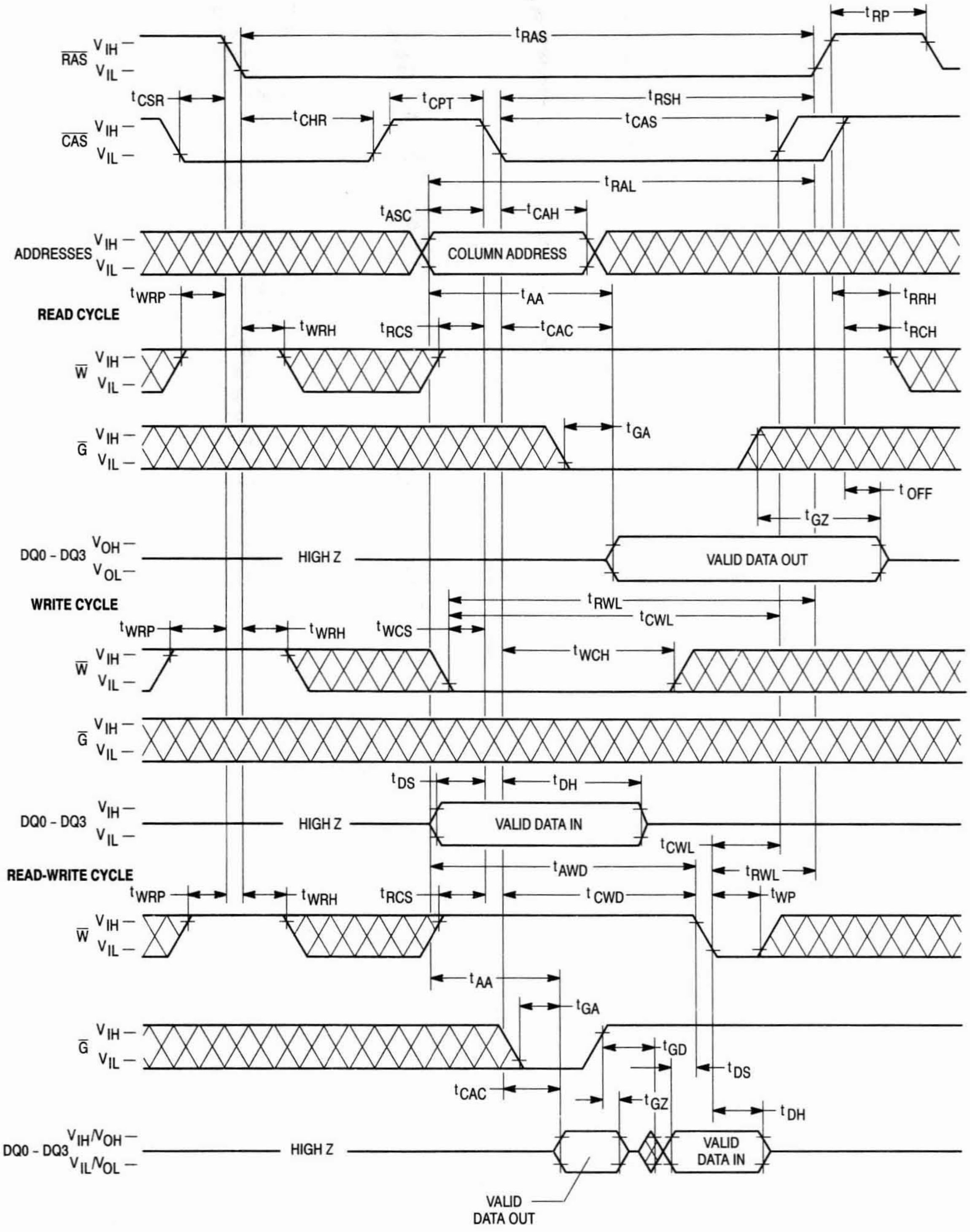
HIDDEN REFRESH CYCLE (READ)


RAS
CAS
ADDRESSES
W
G
DQ0 – DQ3
V IH
V IL
V OH
V OL
t RC
t RP
t RAS
t CRP
t RCD
t RSH
t CHR
t RAD
t ASR
t ASC
t RAH
t CAH
ROW ADD
COLUMN ADDRESS
t RCS
t WRP
t RRH
t WRH
t AA
t GA
t CAC
t OFF
t GZ
t RAC
VALID DATA OUT

HIDDEN REFRESH CYCLE (EARLY WRITE)


RAS
CAS
ADDRESSES
W
G
DQ0 – DQ3
V IH
V IL
t RC
t RP
t RAS
t RCD
t CHR
t CRP
t RSH
t RAD
t ASR
t ASC
t RAH
t CAH
ROW ADD
COLUMN ADDRESS
t WCS
t WRP
t WRH
t WCH
t WP
t DS
t DH
VALID DATA IN

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



RAS
CAS
ADDRESSES
COLUMN ADDRESS
READ CYCLE
W
G
DQ0 - DQ3
HIGH Z
VALID DATA OUT
WRITE CYCLE
VALID DATA IN
READ-WRITE CYCLE
VALID DATA OUT
VALID DATA IN
V_{IH}
V_{IL}
V_{OH}
V_{OL}
V_{IH}/V_{OH}
V_{IL}/V_{OL}
t_{RAS}
t_{RP}
t_{CSR}
t_{CHR}
t_{CPT}
t_{RSH}
t_{CAS}
t_{RAL}
t_{ASC}
t_{CAH}
t_{WRP}
t_{WRH}
t_{RCS}
t_{AA}
t_{CAC}
t_{RRH}
t_{RCH}
t_{GA}
t_{OFF}
t_{GZ}
t_{RWL}
t_{CWL}
t_{WCS}
t_{WCH}
t_{DS}
t_{DH}
t_{AWD}
t_{CWD}
t_{WP}
t_{GD}

DEVICE INITIALIZATION

On power-up, an initial pause of 100 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds or 128 milliseconds in case of low power device with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the 1M x 4 RAM: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{\text{CAS}}$ and output enable ($\overline{\text{G}}$) control read access time: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum and $\overline{\text{G}}$ must be active $t_{RAC} - t_{GA}$ (both minimum) after $\overline{\text{RAS}}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{\text{G}}$ active transition does not occur in time, read access time is determined by either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ and $\overline{\text{G}}$ clocks are active. When either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers and $\overline{\text{G}}$ disabled.

A late write cycle (referred to as $\overline{\text{G}}$-controlled write) occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but outputs are switched off by $\overline{\text{G}}$ inactive transition, which is required to write to the device. Q may be indeterminate (see note 18 of the AC Operating Conditions table). $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle. $\overline{\text{G}}$ must remain inactive for t_{GH} after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the 1M x 4 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM44400 require refresh every 16 milliseconds, while refresh time for the MCM4L4400 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM44400, and 124.8 microseconds for the MCM4L4400. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM44400 and 128 milliseconds on the MCM4L4400.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decodes. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{\text{RAS}}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode entry) as in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

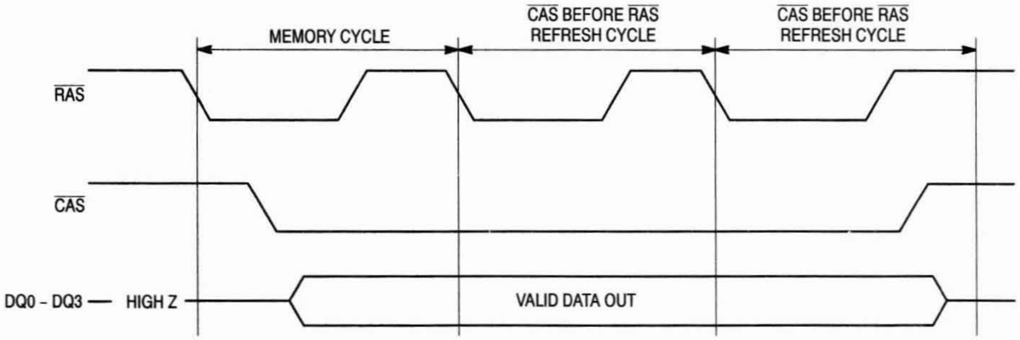


Figure 1. Hidden Refresh Cycle

TEST MODE

The internal organization of this device (512K x 8) allows it to be tested as if it were a 512K x 4 DRAM. Nineteen of the twenty addresses are used when operating the device in test mode. Column address A0 is ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0 – B7) in parallel. External data out is determined by the internal test mode logic of the device. See following truth table and test mode block diagram.

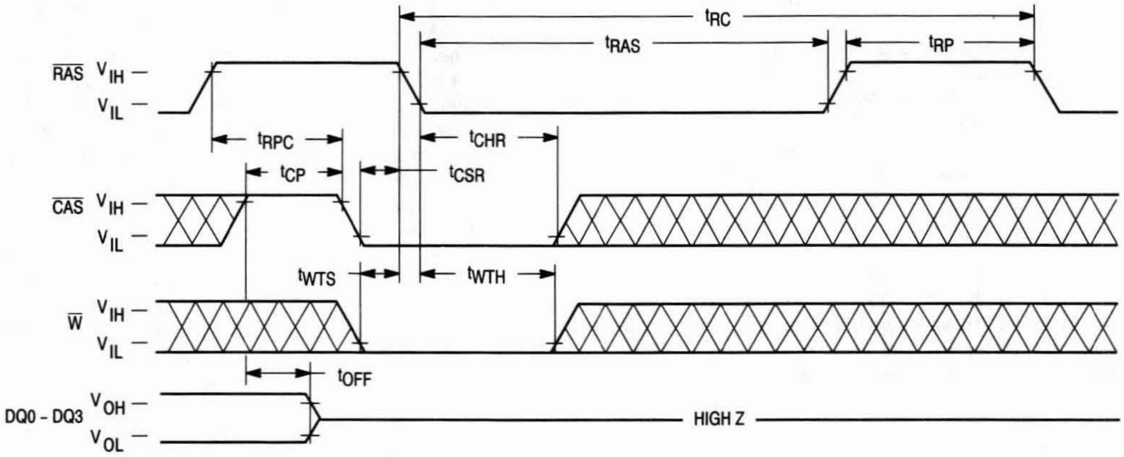
$\overline{W}$, $\overline{CAS}$ before $\overline{RAS}$ timing puts the device in **Test Mode** as shown in the test mode timing diagram. A **$\overline{CAS}$ before $\overline{RAS}$** or a **$\overline{RAS}$-only refresh cycle** puts the device back into normal mode. Refresh is performed in test mode by using a **$\overline{W}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle** which uses internal refresh address counter.

TEST MODE TRUTH TABLE

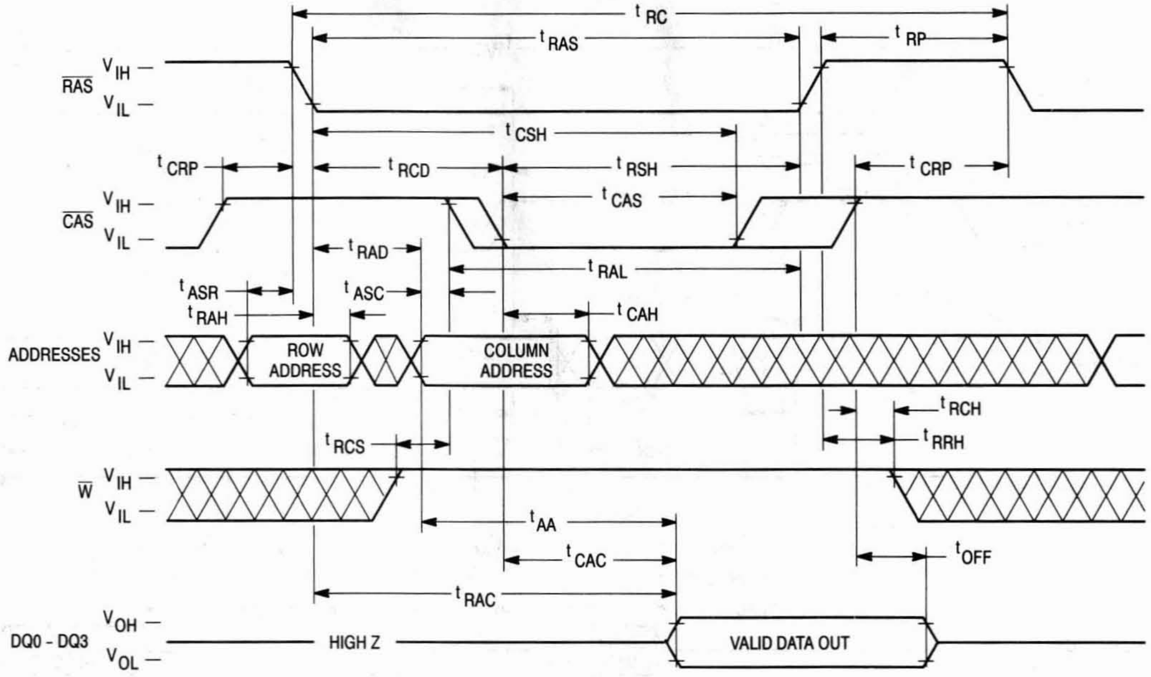
D	B0, B1	B2, B3	B4, B5	B6, B7	Q
0	0	0	0	0	1
1	1	1	1	1	1
—	Any Other				0

$\overline{W}$, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE (TEST MODE ENTRY)

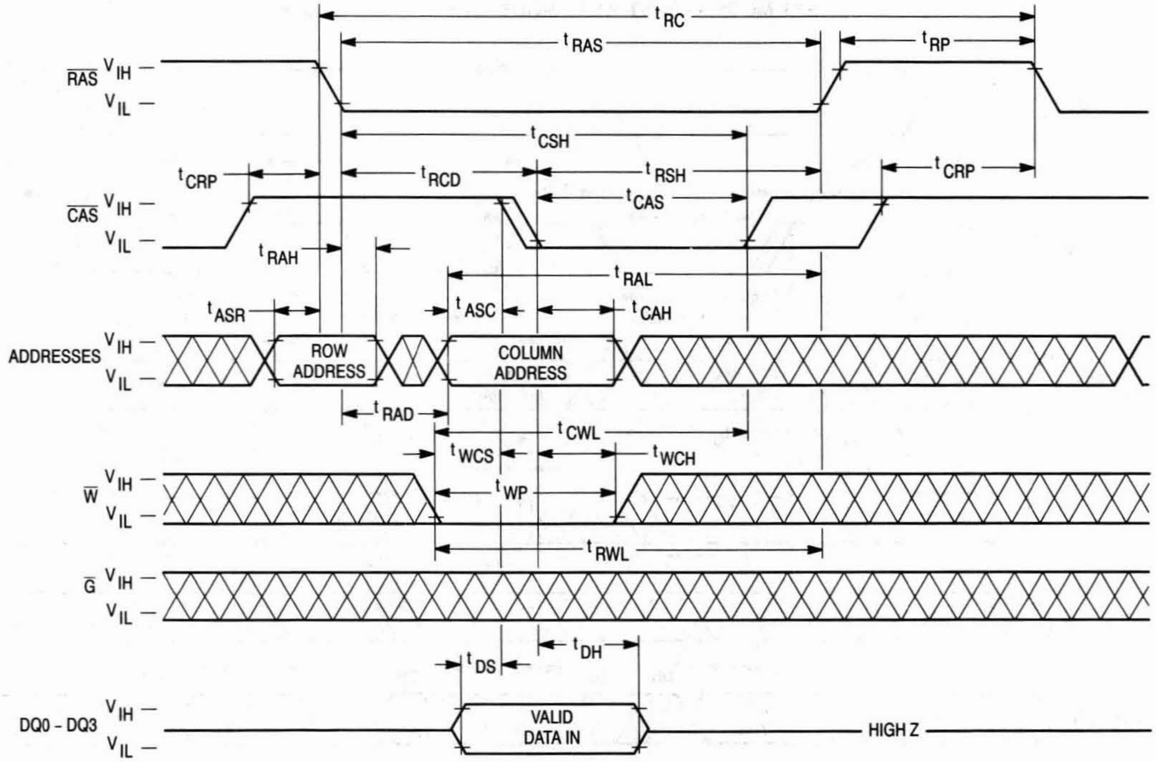
($\overline{G}$ and A0 – A9 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RPC}
t_{CHR}
t_{CP}
t_{CSR}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{WTS}
t_{WTH}
$\overline{W}$
V_{IH}
V_{IL}
t_{OFF}
DQ0 - DQ3
V_{OH}
V_{OL}
HIGH Z

TEST MODE — READ CYCLE

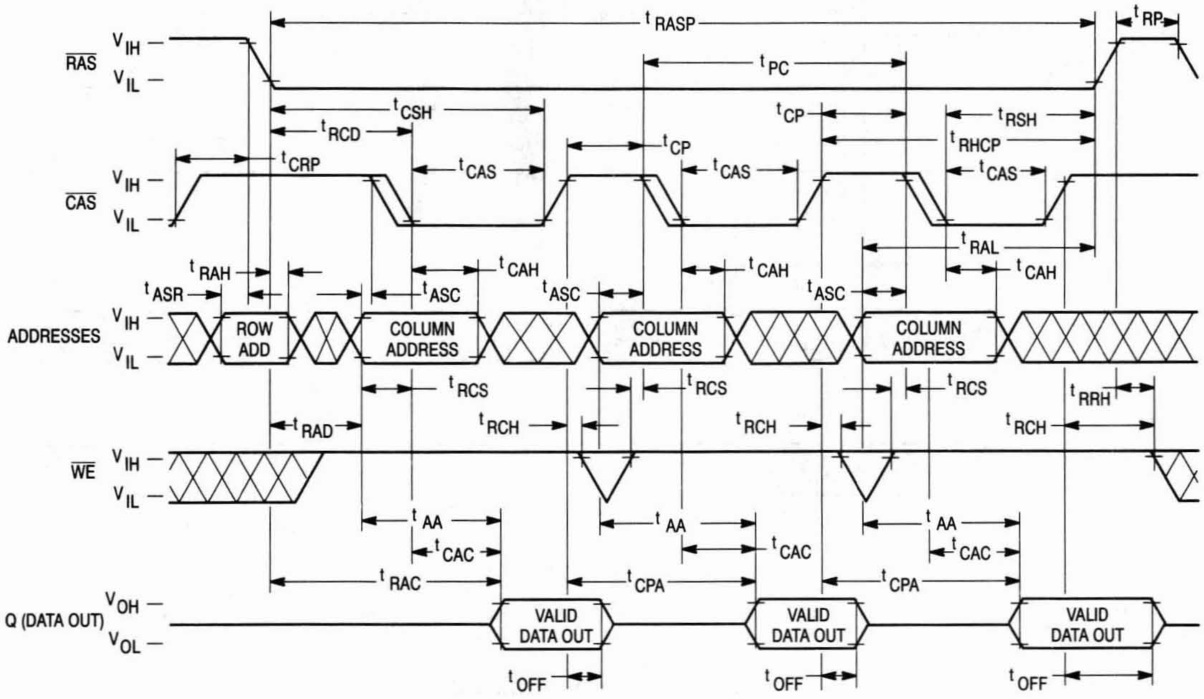

t RC
t RAS
t RP
RAS
V IH
V IL
t CSH
t CRP
t RCD
t RSH
t CRP
t CAS
CAS
V IH
V IL
t RAD
t RAL
t ASR
t ASC
t RAH
t CAH
ADDRESSES
V IH
V IL
ROW ADDRESS
COLUMN ADDRESS
t RCH
t RCS
t RRH
W
V IH
V IL
t AA
t CAC
t OFF
t RAC
DQ0 - DQ3
V OH
V OL
HIGH Z
VALID DATA OUT

TEST MODE — EARLY WRITE CYCLE

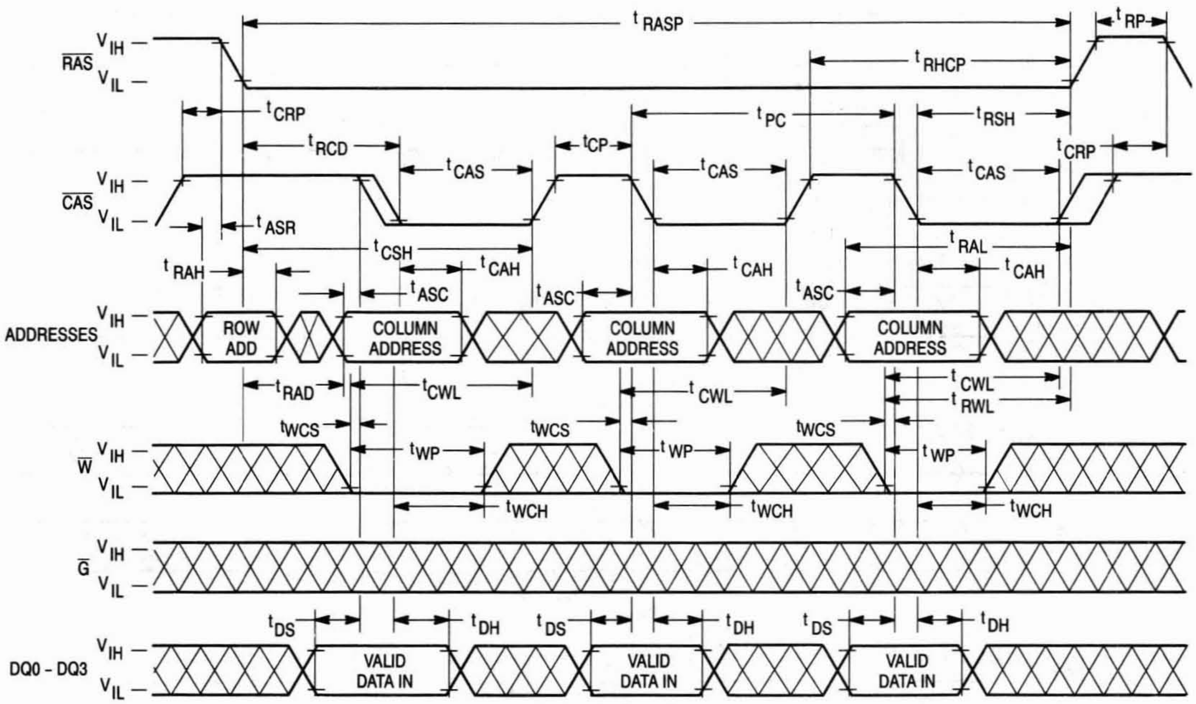

t RC
t RAS
t RP
RAS
V IH
V IL
t CSH
t CRP
t RCD
t RSH
t CRP
t CAS
CAS
V IH
V IL
t RAH
t RAL
t ASR
t ASC
t CAH
ADDRESSES
V IH
V IL
ROW ADDRESS
COLUMN ADDRESS
t RAD
t CWL
t WCS
t WCH
t WP
W
V IH
V IL
t RWL
G
V IH
V IL
t DH
t DS
DQ0 - DQ3
V IH
V IL
VALID DATA IN
HIGH Z

TEST MODE — FAST PAGE MODE READ CYCLE

($\overline{G}$ = Low)


RAS
VIH
VIL
CAS
ADDRESSES
WE
Q (DATA OUT)
VOH
VOL
tRASP
tRP
tPC
tCSH
tRCD
tCRP
tCAS
tCP
tRSH
tRHCP
tRAL
tRAH
tASR
tASC
tCAH
ROW ADD
COLUMN ADDRESS
tRCS
tRAD
tRCH
tRRH
tAA
tCAC
tRAC
tCPA
VALID DATA OUT
tOFF

TEST MODE — FAST PAGE MODE EARLY WRITE CYCLE


RAS
VIH
VIL
CAS
ADDRESSES
W
G
DQ0 - DQ3
tRASP
tRP
tRHCP
tCRP
tPC
tRCD
tCP
tRSH
tCAS
tASR
tCSH
tRAL
tRAH
tCAH
tASC
ROW ADD
COLUMN ADDRESS
tRAD
tCWL
tRWL
tWCS
tWP
tWCH
tDS
tDH
VALID DATA IN

ORDERING INFORMATION
(Order by Full Part Number)

MCM 44400 or 4L4400 X XX XX

Motorola Memory Prefix — MCM

Part Number — 44400 or 4L4400

Shipping Method (R2 = Tape and Reel, Blank = Rails)

Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns)

Package (N = 300 mil SOJ, Z = 100 mil Plastic ZIP)

Full Part Numbers —	MCM44400N60	MCM44400N60R2	MCM44400Z60
	MCM44400N70	MCM44400N70R2	MCM44400Z70
	MCM44400N80	MCM44400N80R2	MCM44400Z80
	MCM4L4400N60	MCM4L4400N60R2	MCM4L4400Z60
	MCM4L4400N70	MCM4L4400N70R2	MCM4L4400Z70
	MCM4L4400N80	MCM4L4400N80R2	MCM4L4400Z80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM54100A
MCM5L4100A

Advance Information

4M x 1 CMOS Dynamic RAM
Fast Page Mode

The MCM54100A is a 0.7µ CMOS high-speed dynamic random access memory. It is organized as 4,194,304 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM54100A requires only 11 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil J lead small outline package, 100 mil zig-zag in-line package (ZIP), and a 300 mil thin small outline package (TSOP).

- Three-State Data Output
- Fast Page Mode
- Test Mode
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM54100A = 16 ms
- Fast Access Time (t_{RAC}):
  - MCM54100A-60 and MCM5L4100A-60 = 60 ns (Max)
  - MCM54100A-70 and MCM5L4100A-70 = 70 ns (Max)
  - MCM54100A-80 and MCM5L4100A-80 = 80 ns (Max)
- Low Active Power:
  - MCM54100A-60 and MCM5L4100A-60 = 660 mW (Max)
  - MCM54100A-80 and MCM5L4100A-80 = 550 mW (Max)
  - MCM54100A-80 and MCM5L4100A-80 = 468 mW (Max)
- Low Standby Power Dissipation:
  - MCM54100A and MCM5L400A = 11 mW (Max, TTL Levels)
  - MCM54100A = 5.5 mW (Max, CMOS Levels)
  - MCM5L4100A = 1.1 mW (Max, CMOS Levels)

N PACKAGE
300 MIL SOJ
CASE 822-03

Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836-02

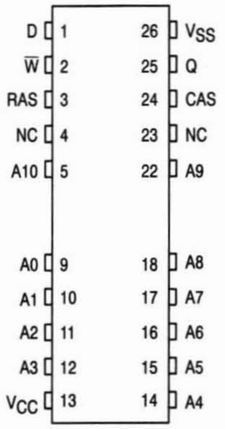
T PACKAGE
300 MIL TSOP
CASE 892-01

PIN NAMES

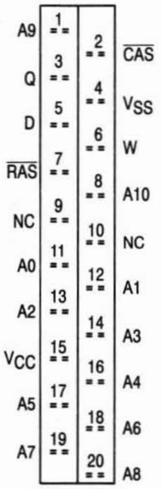
A0 – A10	Address Input
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENTS

300 MIL SOJ/TSOP

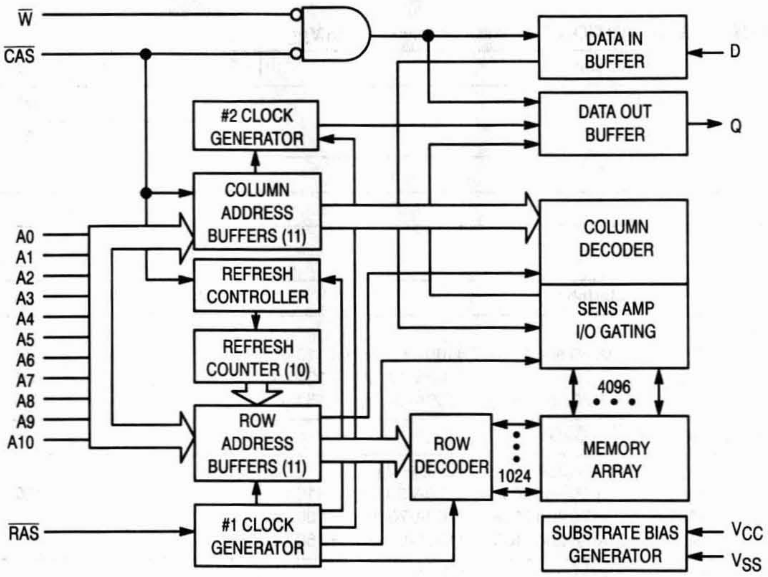


100 MIL ZIP



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM


W
CAS
#2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (11)
REFRESH CONTROLLER
REFRESH COUNTER (10)
ROW ADDRESS BUFFERS (11)
#1 CLOCK GENERATOR
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
RAS
DATA IN BUFFER
D
DATA OUT BUFFER
Q
COLUMN DECODER
SENS AMP I/O GATING
4096
ROW DECODER
1024
MEMORY ARRAY
SUBSTRATE BIAS GENERATOR
VCC
VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current	I_{out}	50	mA
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	1, 2
MCM54100A-60 and MCM5L4100A-60, t_{RC} = 110 ns		—	120		
MCM54100A-70 and MCM5L4100A-70, t_{RC} = 130 ns		—	100		
MCM54100A-80 and MCM5L4100A-80, t_{RC} = 150 ns		—	85		
V_{CC} Power Supply Current (Standby) ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{\text{RAS}}$ Only Refresh Cycles ($\overline{\text{CAS}}$ = V_{IH})	I_{CC3}			mA	1, 2
MCM54100A-60 and MCM5L4100A-60, t_{RC} = 110 ns		—	120		
MCM54100A-70 and MCM5L4100A-70, t_{RC} = 130 ns		—	100		
MCM54100A-80 and MCM5L4100A-80, t_{RC} = 150 ns		—	85		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{\text{RAS}}$ = V_{IL})	I_{CC4}			mA	1, 2
MCM54100A-60 and MCM5L4100A-60, t_{PC} = 45 ns		—	60		
MCM54100A-70 and MCM5L4100A-70, t_{PC} = 45 ns		—	70		
MCM54100A-80 and MCM5L4100A-80, t_{PC} = 50 ns		—	60		
V_{CC} Power Supply Current (Standby) ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = V_{IH} – 0.2 V)	I_{CC5}				
MCM54100A		—	1.0	mA	
MCM5L4100A		—	200	µA	
V_{CC} Power Supply Current During $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle	I_{CC6}			mA	1
MCM54100A-60 and MCM5L4100A-60, t_{RC} = 110 ns		—	120		
MCM54100A-70 and MCM5L4100A-70, t_{RC} = 130 ns		—	100		
MCM54100A-80 and MCM5L4100A-80, t_{RC} = 150 ns		—	85		
V_{CC} Power Supply Current, Battery Backup Mode — MCM5L4100A Only (t_{RC} = 125 µs; $\overline{\text{CAS}}$ = $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycling or 0.2 V; $\overline{\text{W}}$ = V_{CC} – 0.2 V; D_{in} = V_{CC} – 0.2 V or 0.2 V or OPEN; A0 – A10 = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}			µA	1, 3
t_{RAS} = 300 ns to 1 µs		—	400		
t_{RAS} = Min to 300 ns		—	300		
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current ($\overline{\text{CAS}}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Column address can be changed once or less while $\overline{\text{RAS}}$ = V_{IL} and $\overline{\text{CAS}}$ = V_{IH}.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery-back up. t_{RAS} (max) = 10 µs is applied to functional operating

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A10, D	C_{in}	5	pF
	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$		7	
I/O Capacitance ($\overline{\text{CAS}}$ = V_{IH} to Disable Output)	Q	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM54100A-60 MCM5L4100A-60		MCM54100A-70 MCM5L4100A-70		MCM54100A-80 MCM5L4100A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	140	—	155	—	175	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	50	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	65	—	70	—	75	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	40	—	40	—	45	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	45	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	200 k	70	200 k	80	200 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	20	10 k	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

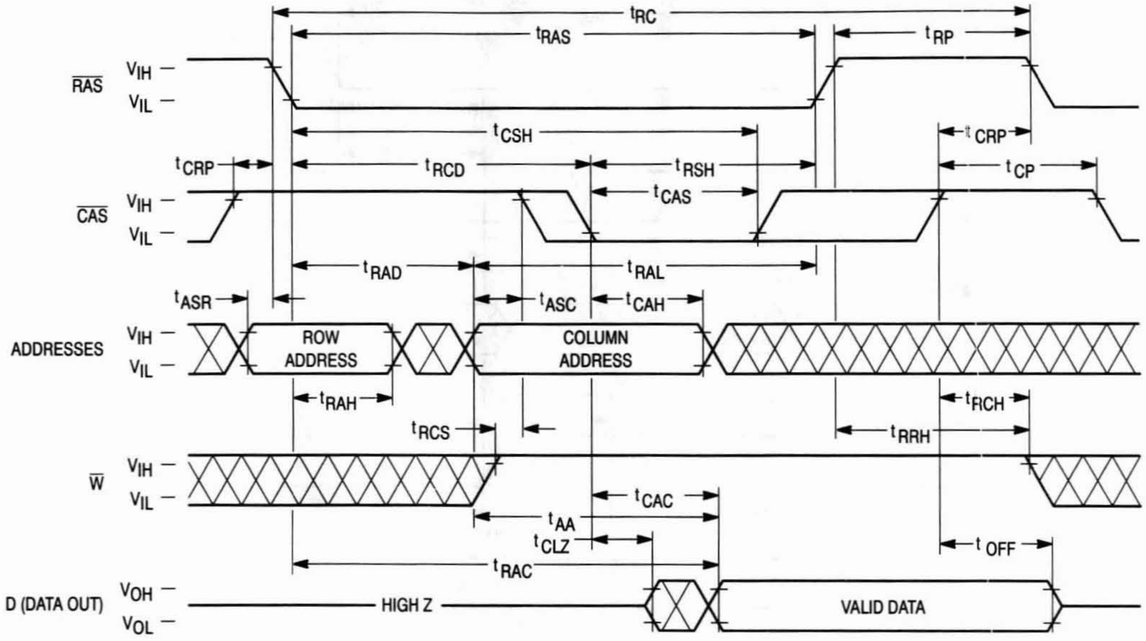
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM54100A-60 MCM5L4100A-60		MCM54100A-70 MCM5L4100A-70		MCM54100A-80 MCM5L4100A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	14
Refresh Period MCM54100A MCM5L4100A	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	20	—	20	—	20	—	ns	15
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	60	—	70	—	80	—	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	30	—	35	—	40	—	ns	15
$\overline{\text{CAS}}$ Precharge to Write Delay Time (Page Mode)	t_{CEHWL}	t_{CPWD}	40	—	40	—	40	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Time	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	

NOTES:

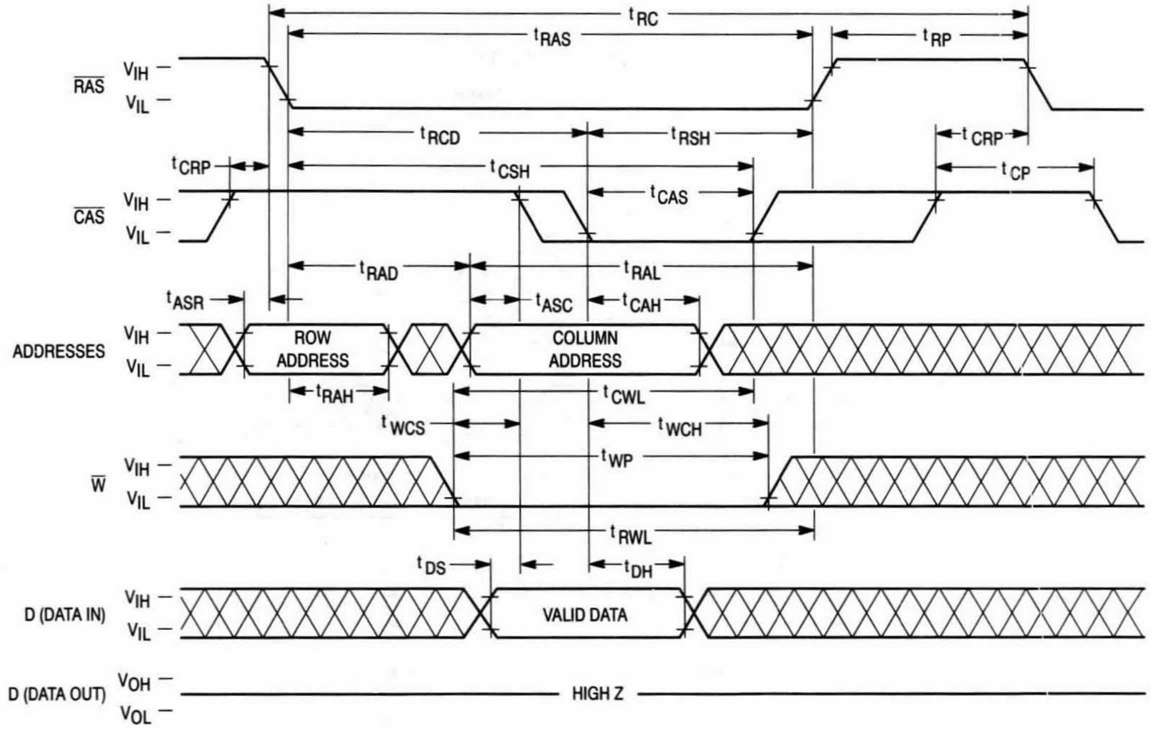
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \ge t_{CWD}$ (min), $t_{RWD} \ge t_{RWD}$ (min), $t_{AWD} \ge t_{AWD}$ (min), and $t_{CPWD} \ge t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tCRP
tRCD
tRSH
tCP
tCAS
CAS
VIH
VIL
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W
VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
D (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA

EARLY WRITE CYCLE



tRC
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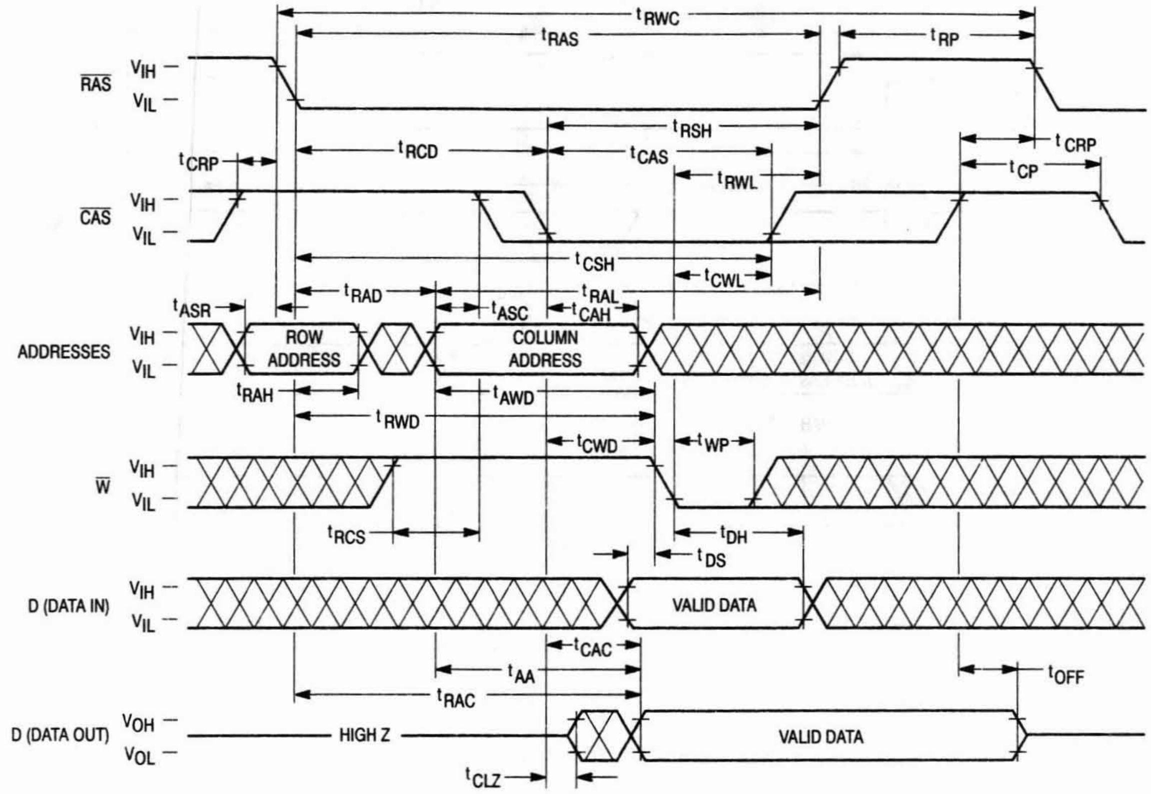
tRP
RAS
VIH
VIL
tRCD
tRSH
tCRP
tCRP
tCSH
tCP
tCAS
CAS
VIH
VIL
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWP
W
VIH
VIL
tRWL
tDS
tDH
D (DATA IN)
VIH
VIL
VALID DATA
D (DATA OUT)
VOH
VOL
HIGH Z

READ-WRITE CYCLE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RAS
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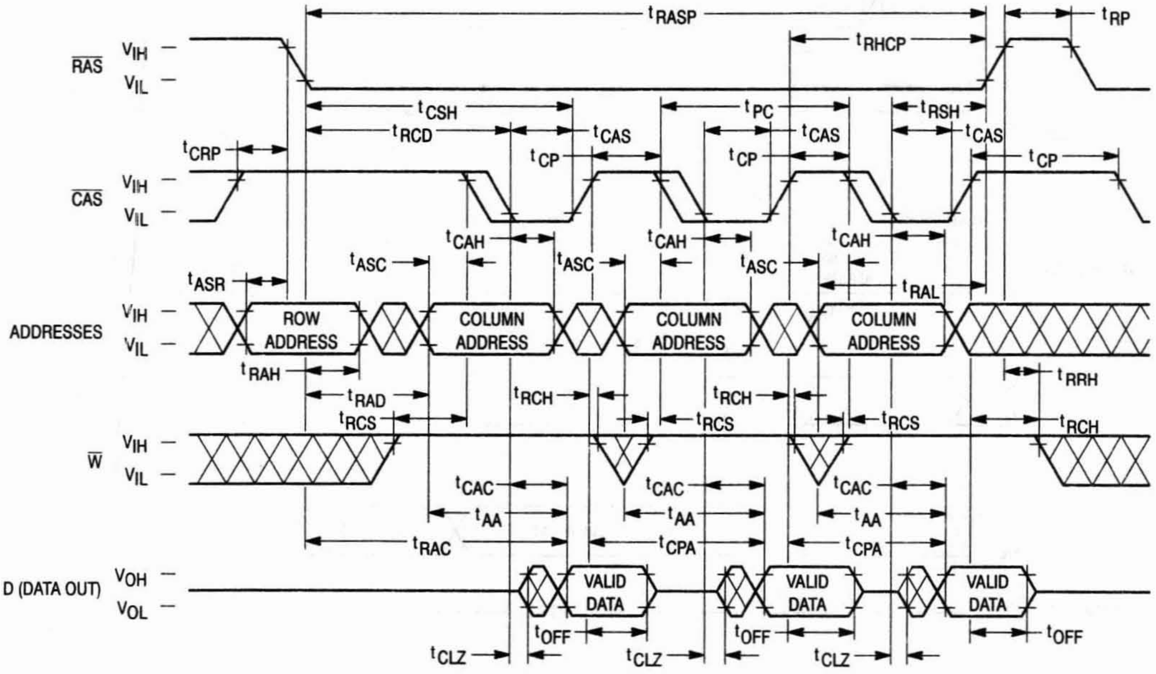
CAS
VIH
VIL
tCSH
tCWL
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tAWD
tRWD
tCWD
tWP
W
VIH
VIL
tRCS
tDH
tDS
D (DATA IN)
VIH
VIL
VALID DATA
tCAC
tAA
tOFF
tRAC
D (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA
tCLZ

FAST PAGE MODE READ CYCLE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tRHCP
RAS
VIH
VIL
tCSH
tPC
tRSH
tRCD
tCAS
tCAS
tCAS
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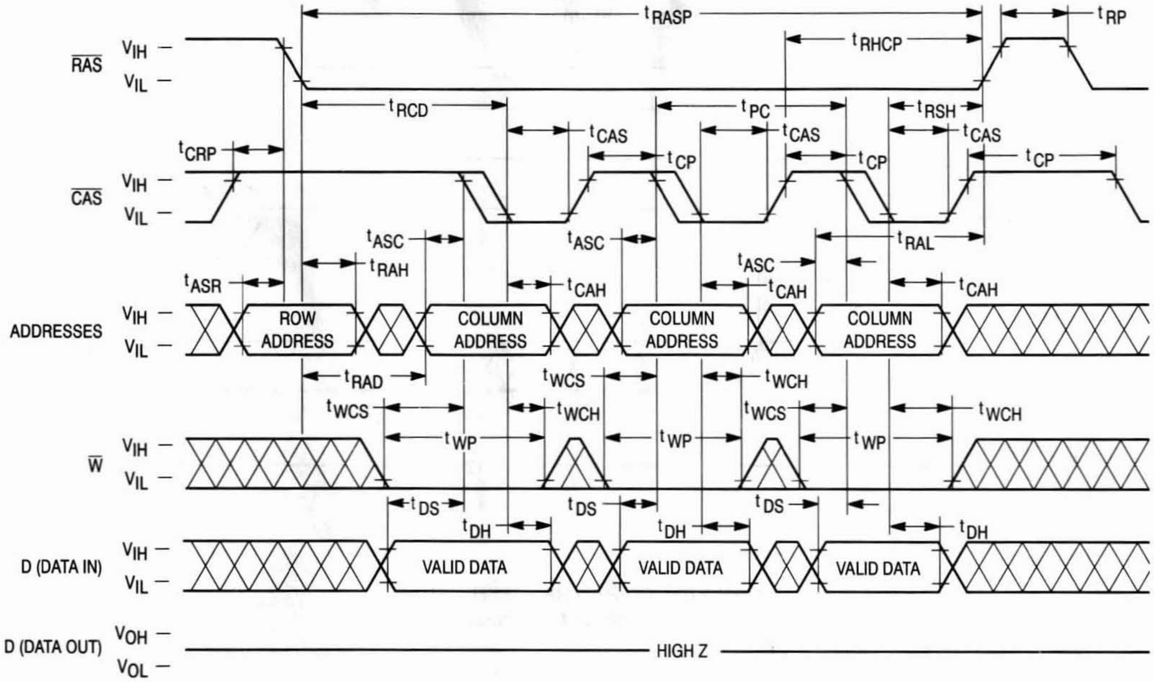
tCP
tCP
CAS
VIH
VIL
tCAH
tCAH
tCAH
tASC
tASC
tASC
tASR
tRAL
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAH
tRRH
tRAD
tRCH
tRCH
tRCS
tRCS
tRCS
tRCH
W
VIH
VIL
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
D (DATA OUT)
VOH
VOL
VALID DATA
VALID DATA
VALID DATA
tOFF
tOFF
tOFF
tCLZ
tCLZ
tCLZ

FAST PAGE MODE EARLY WRITE CYCLE


RAS
CAS
ADDRESSES
W
D (DATA IN)
D (DATA OUT)
VIH
VIL
VOH
VOL
tRASP
tRP
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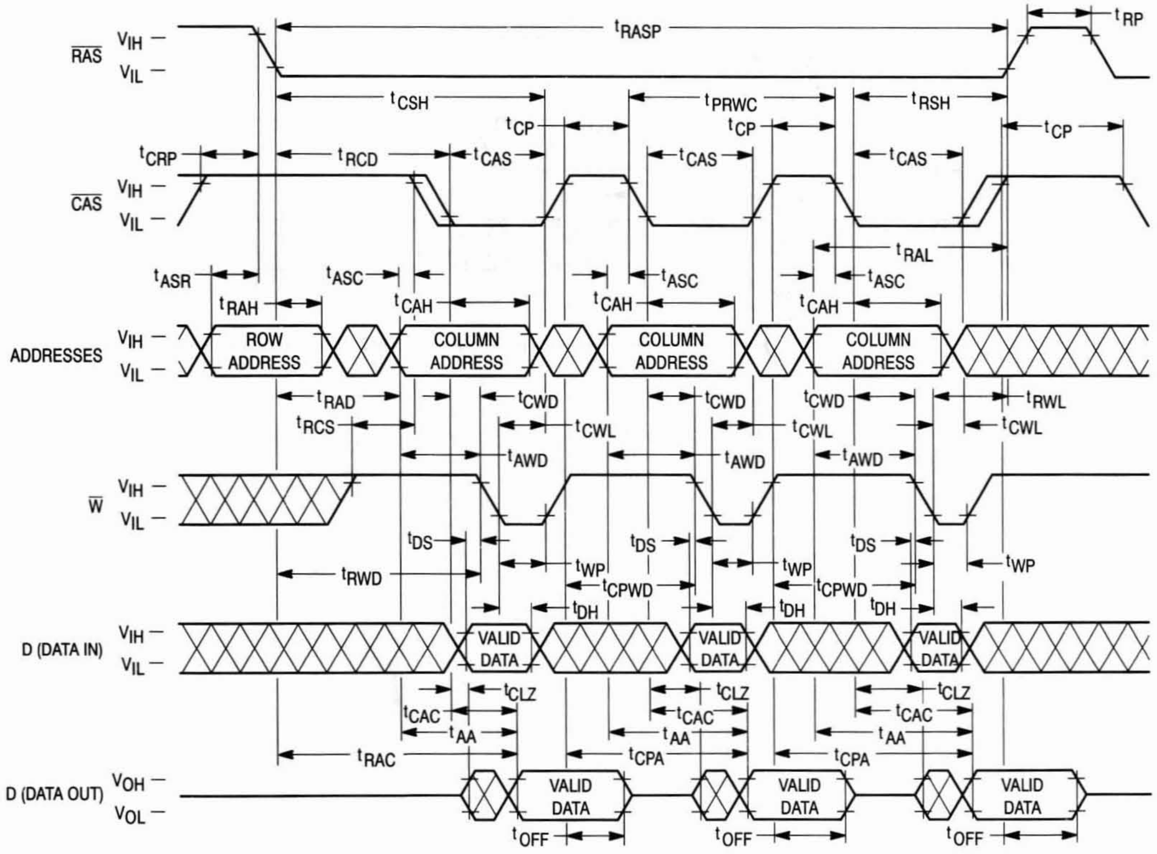
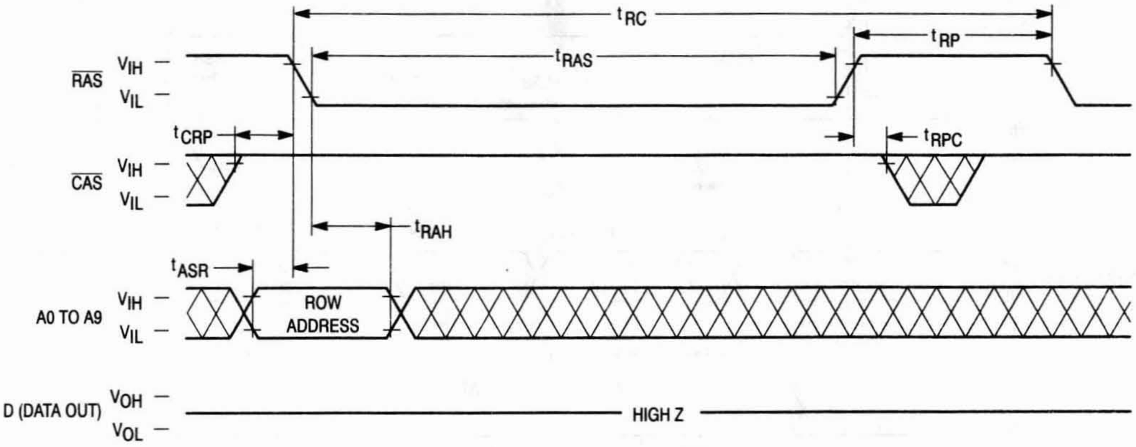
tPC
tRSH
tCAS
tCRP
tCP
tASC
tRAH
tRAL
tASR
tCAH
ROW ADDRESS
COLUMN ADDRESS
tRAD
tWCS
tWCH
tWP
tDS
tDH
VALID DATA
HIGH Z

FAST PAGE MODE READ-WRITE CYCLE


RAS
CAS
ADDRESSES
W
D (DATA IN)
D (DATA OUT)
VIH
VIL
VOH
VOL
tRASP
tRP
tCSH
tPRWC
tRSH
tCP
tCRP
tRCD
tCAS
tRAL
tASR
tASC
tRAH
tCAH
ROW ADDRESS
COLUMN ADDRESS
tRAD
tCWD
tRWL
tRCS
tCWL
tAWD
tDS
tWP
tRWD
tCPWD
tDH
VALID DATA
tCLZ
tCAC
tAA
tRAC
tCPA
tOFF

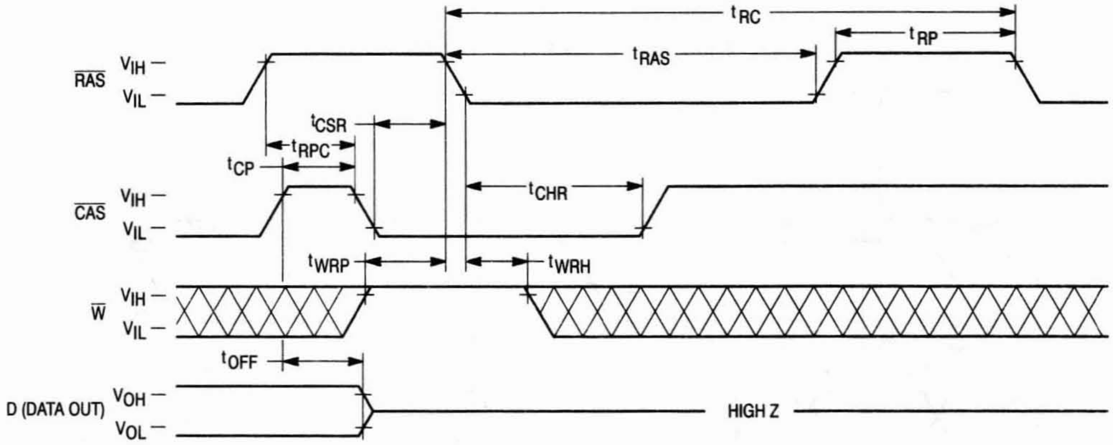
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

($\overline{\text{W}}$ and A10 are Don't Care)

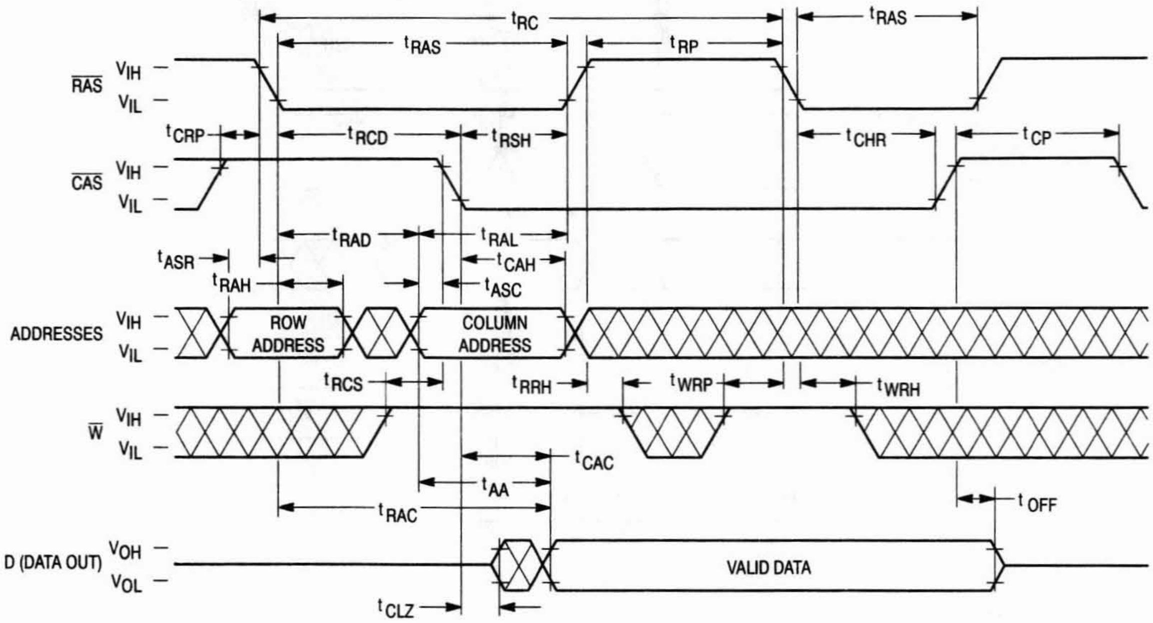

t_{RC}
t_{RP}
t_{RAS}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
A0 TO A9
V_{IH}
V_{IL}
ROW ADDRESS
D (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

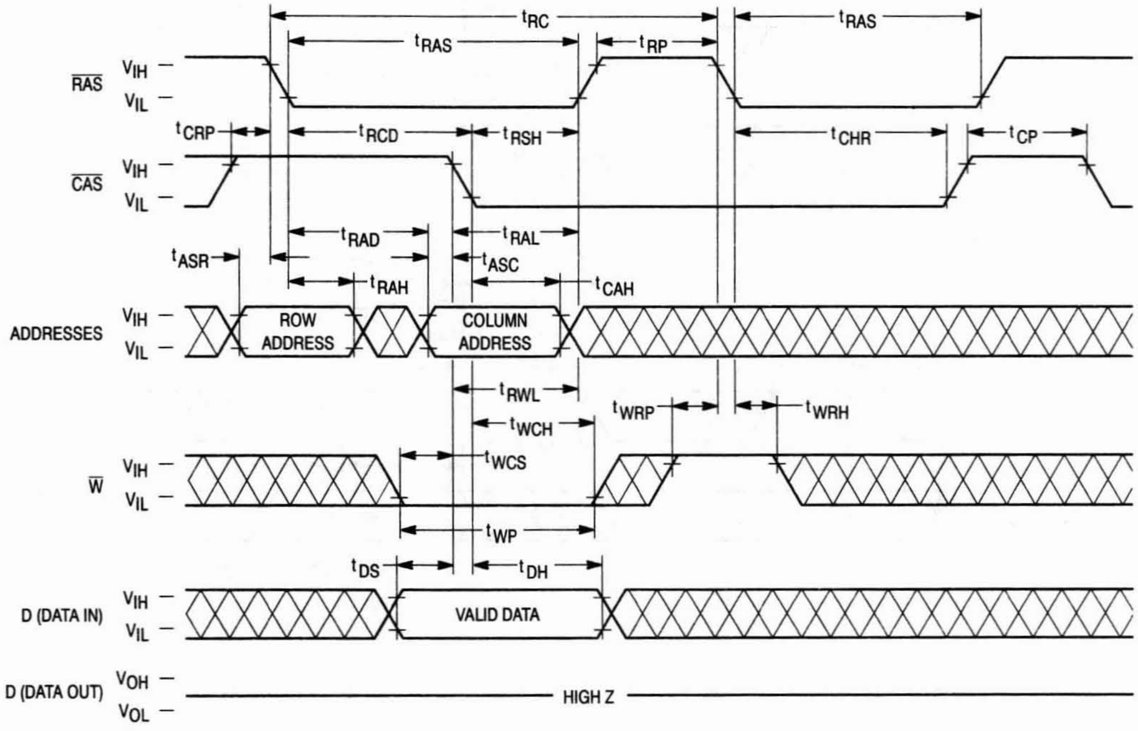
(A0 – A10 are Don't Care)


t_{RC}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RAS}
t_{CSR}
t_{RPC}
t_{CP}
t_{CHR}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{WRP}
t_{WRH}
$\overline{\text{W}}$
V_{IH}
V_{IL}
t_{OFF}
D (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

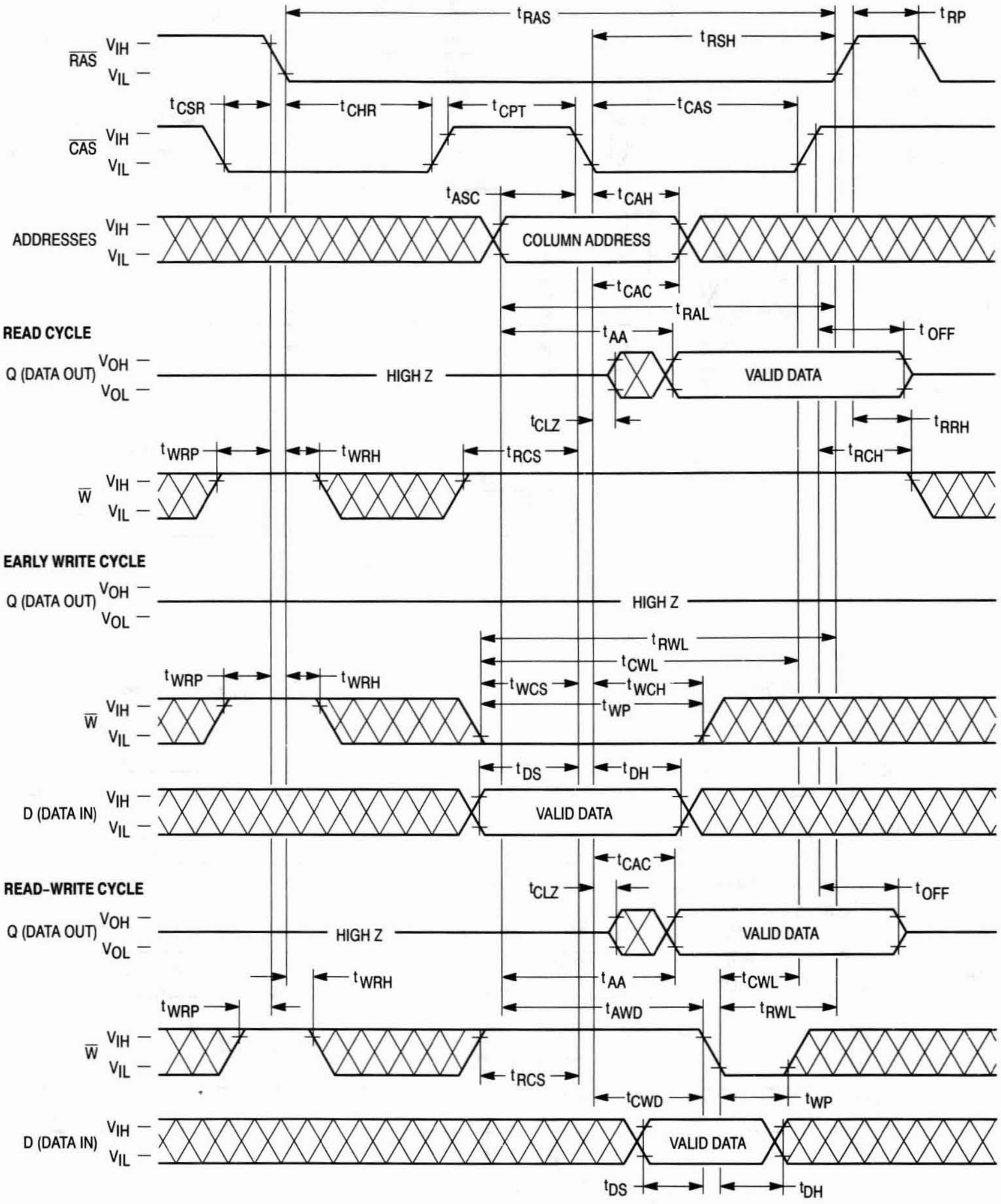
HIDDEN REFRESH CYCLE (READ)


t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CP}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAD}
t_{RAL}
t_{ASR}
t_{CAH}
t_{RAH}
t_{ASC}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RCS}
t_{RRH}
t_{WRP}
t_{WRH}
$\overline{W}$
V_{IH}
V_{IL}
t_{CAC}
t_{AA}
t_{RAC}
t_{OFF}
D (DATA OUT)
V_{OH}
V_{OL}
VALID DATA
t_{CLZ}

HIDDEN REFRESH CYCLE (EARLY WRITE)


t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CP}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RWL}
t_{WRP}
t_{WRH}
t_{WCH}
t_{WCS}
$\overline{W}$
V_{IH}
V_{IL}
t_{WP}
t_{DS}
t_{DH}
D (DATA IN)
V_{IH}
V_{IL}
VALID DATA
D (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE


tRAS
tRP
$\overline{\text{RAS}}$ VIH
VIL
tRSH
tCSR
tCHR
tCPT
tCAS
$\overline{\text{CAS}}$ VIH
VIL
tASC
tCAH
ADDRESSES VIH
VIL
COLUMN ADDRESS
tCAC
tRAL
READ CYCLE
tAA
tOFF
Q (DATA OUT) VOH
VOL
HIGH Z
VALID DATA
tCLZ
tRRH
tWRP
tWRH
tRCS
tRCH
$\overline{\text{W}}$ VIH
VIL
EARLY WRITE CYCLE
Q (DATA OUT) VOH
VOL
HIGH Z
tRWL
tCWL
tWRP
tWRH
tWCS
tWCH
tWP
$\overline{\text{W}}$ VIH
VIL
tDS
tDH
D (DATA IN) VIH
VIL
VALID DATA
READ-WRITE CYCLE
tCAC
tCLZ
tOFF
Q (DATA OUT) VOH
VOL
HIGH Z
VALID DATA
tWRH
tAA
tCWL
tWRP
tAWD
tRWL
$\overline{\text{W}}$ VIH
VIL
tRCS
tCWD
tWP
D (DATA IN) VIH
VIL
VALID DATA
tDS
tDH

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds or 128 milliseconds in case of low power device, with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 11-bit address fields. A total of twenty-two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 bit locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window,** gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the 4M RAM: **$\overline{\text{RAS}}$ only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window; however, $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ clock active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered elsewhere.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \le t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but Q may be indeterminate; see note 15 of AC Operating Conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the 4M dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum of t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by

t_{RASP}. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54100A require refresh every 16 milliseconds, while refresh time for the MCM5L4100A is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54100A, and 124.8 microseconds for the MCM5L4100A. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54100A and 128 milliseconds on the MCM5L4100A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other methods of refresh, **RAS-only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure that all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into **test mode**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode entry) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of 8 **CAS before RAS** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

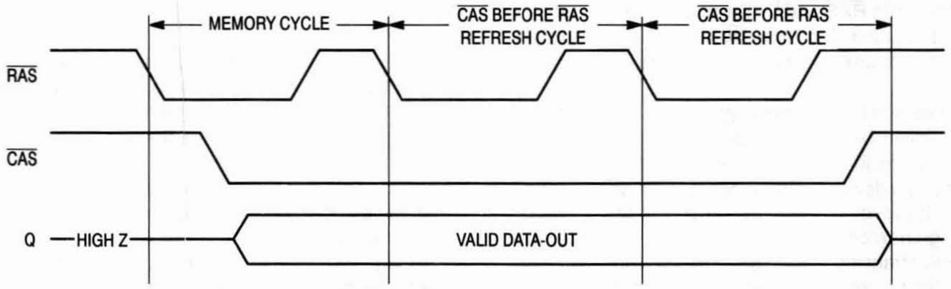


Figure 1. Hidden Refresh Cycle

TEST MODE

The internal organization of this device (512K x 8) allows it to be tested as if it were a 512K x 1 DRAM. Nineteen of the twenty-two addresses are used when operating the device in test mode. Row address A0, and column addresses A0 and A10 are ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0 – B7) in parallel. External data out is determined by the internal test mode logic of the device. See the following truth table and test mode block diagram.

W, CAS before RAS timing puts the device in **"Test Mode"** as shown in the test mode timing diagram. A **CAS before RAS** or a **RAS only** refresh cycle puts the device back into normal mode. Refresh is performed in test mode by using a **W, CAS before RAS** refresh cycle which uses internal refresh address counter.

TEST MODE TRUTH TABLE

D	B0	B1	B2	B3	B4	B5	B6	B7	Q
0	0	0	0	0	0	0	0	0	1
1	1	1	1	1	1	1	1	1	1
—	Any Other								0

TEST MODE
AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

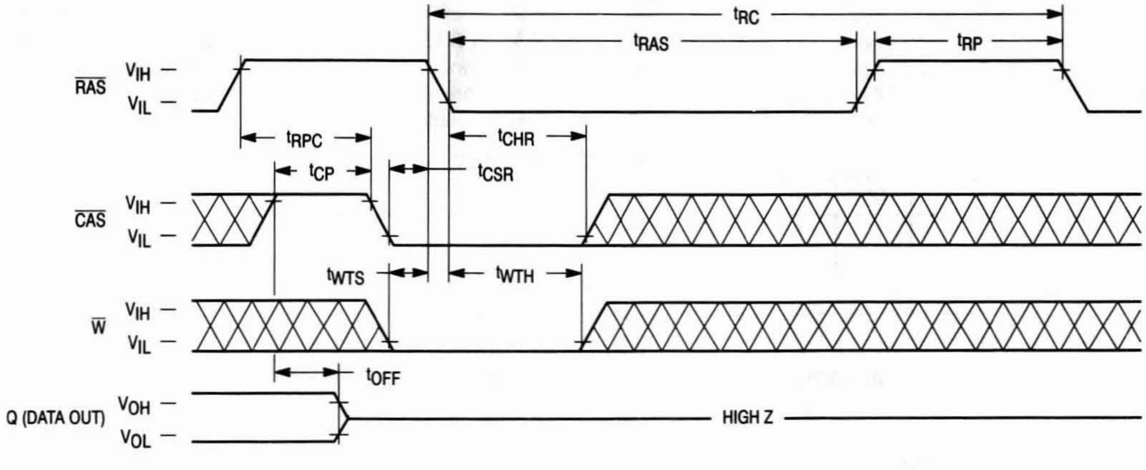
Parameter	Symbol		MCM54100A-60 MCM5L4100A-60		MCM54100A-70 MCM5L4100A-70		MCM54100A-80 MCM5L4100A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	115	—	135	—	155	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	—	50	—	55	—	ns	
Access Time from RAS	t_{RELQV}	t_{RAC}	—	65	—	75	—	85	ns	6, 7
Access Time from CAS	t_{CELQV}	t_{CAC}	—	25	—	25	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	45	ns	6, 9
Access Time from Precharge CAS	t_{CEHQV}	t_{CPA}	—	45	—	45	—	50	ns	6
RAS Pulse Width	t_{RELREH}	t_{RAS}	65	10 k	75	10 k	85	10 k	ns	
RAS Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	65	200 k	75	200 k	85	200 k	ns	
RAS Hold Time	t_{CELREH}	t_{RSH}	25	—	25	—	25	—	ns	
CAS Hold Time	t_{RELCEH}	t_{CSH}	65	—	75	—	85	—	ns	
CAS Precharge to RAS Hold Time	t_{CEHREH}	t_{RHCP}	45	—	45	—	50	—	ns	
CAS Pulse Width	t_{CELCEH}	t_{CAS}	25	10 k	25	10 k	25	10 k	ns	
Column Address to RAS Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	45	—	ns	

NOTES:

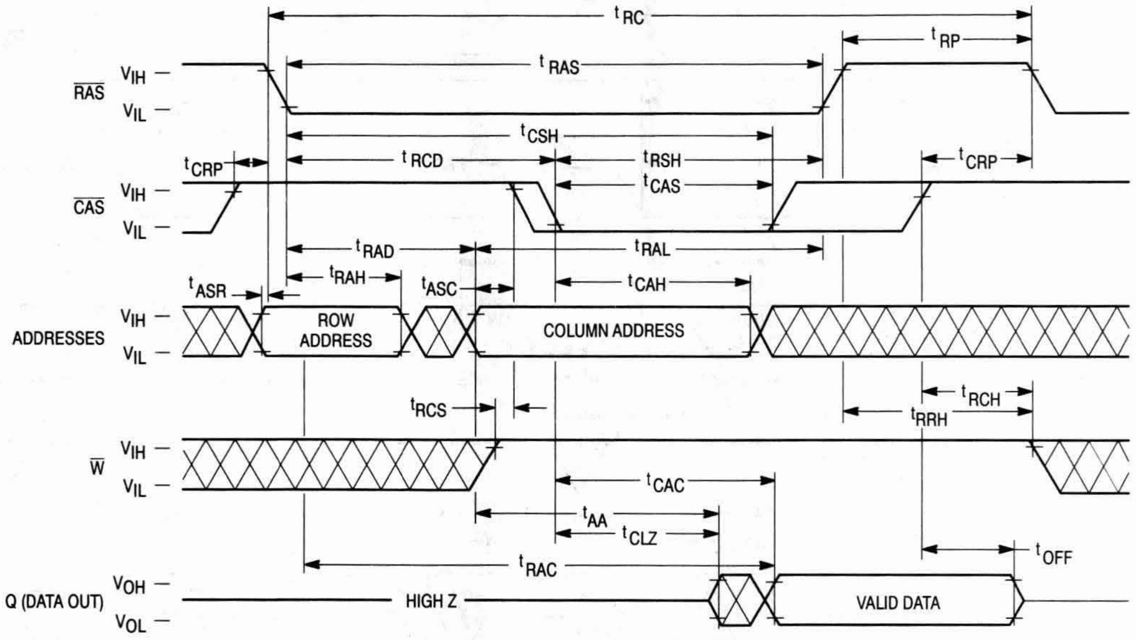
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).

$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE (TEST MODE ENTRY)

(D and A0 – A10 are Don't Care)

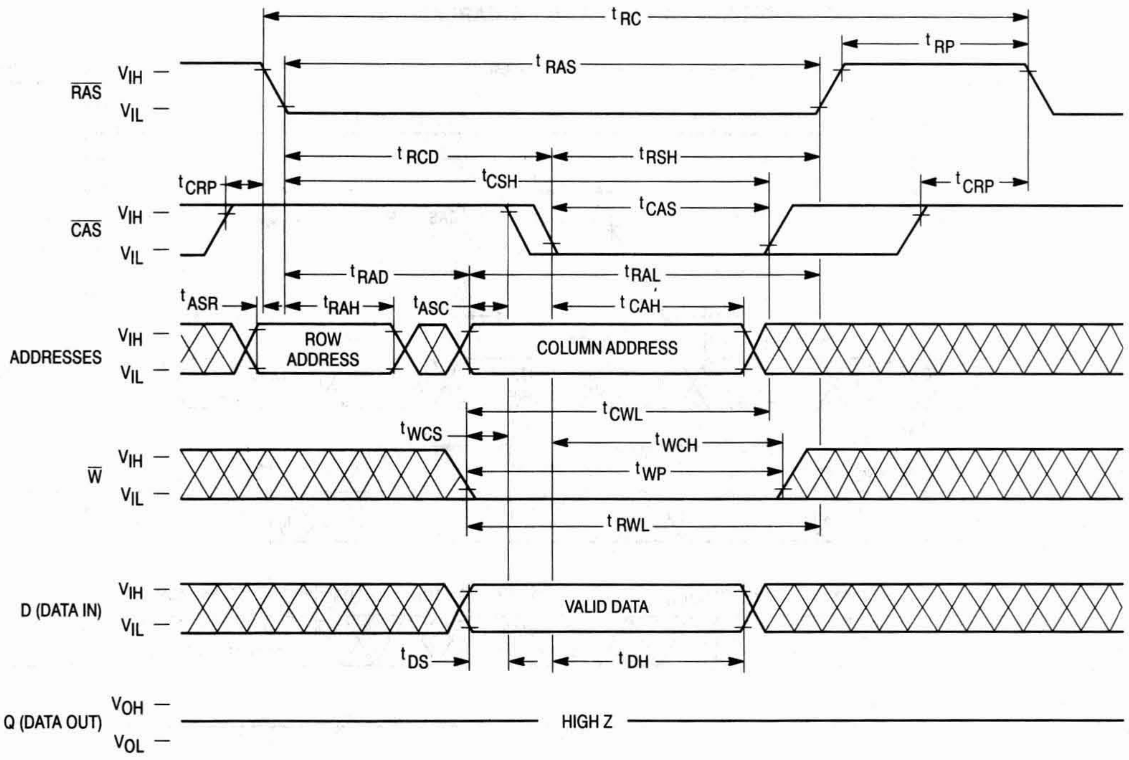

t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH} —
V_{IL} —
t_{RPC}
t_{CHR}
t_{CP}
t_{CSR}
$\overline{\text{CAS}}$
V_{IH} —
V_{IL} —
t_{WTS}
t_{WTH}
$\overline{\text{W}}$
V_{IH} —
V_{IL} —
t_{OFF}
Q (DATA OUT)
V_{OH} —
V_{OL} —
HIGH Z

TEST MODE — READ CYCLE



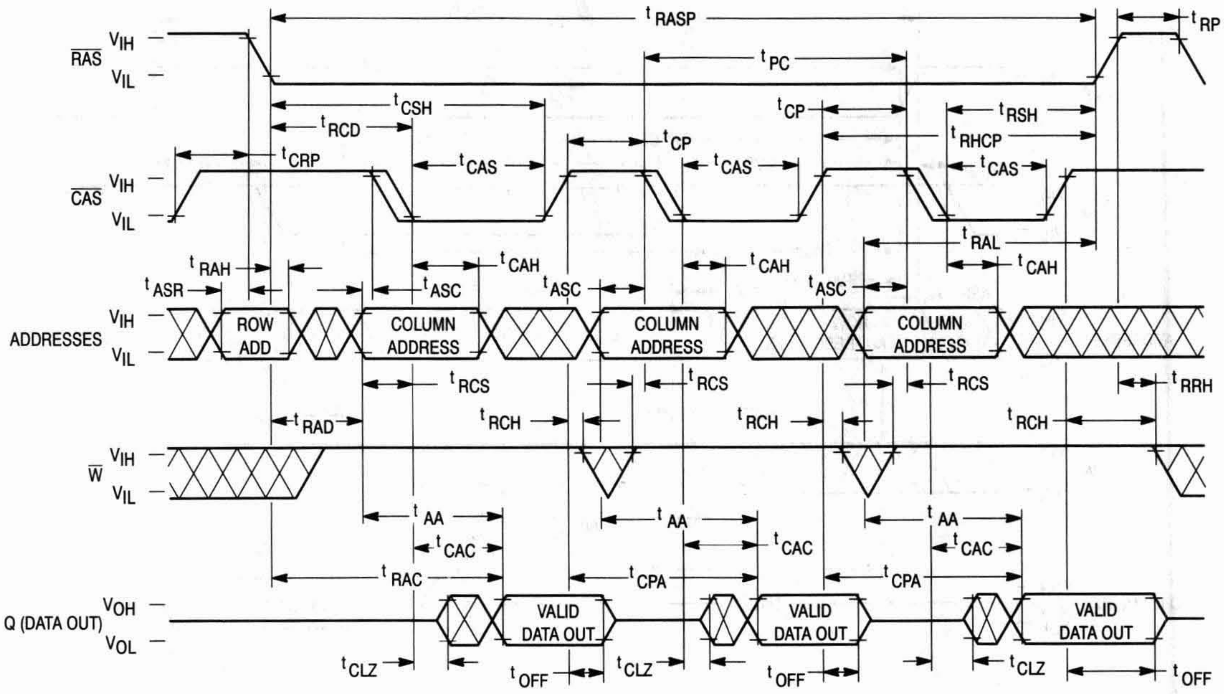
t_{RC}
t_{RP}
t_{RAS}
RAS
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
CAS
t_{RAD}
t_{RAL}
t_{ASR}
t_{RAH}
t_{ASC}
t_{CAH}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{RCS}
t_{RCH}
t_{RRH}
W
t_{CAC}
t_{AA}
t_{CLZ}
t_{OFF}
t_{RAC}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z
VALID DATA

TEST MODE — EARLY WRITE CYCLE



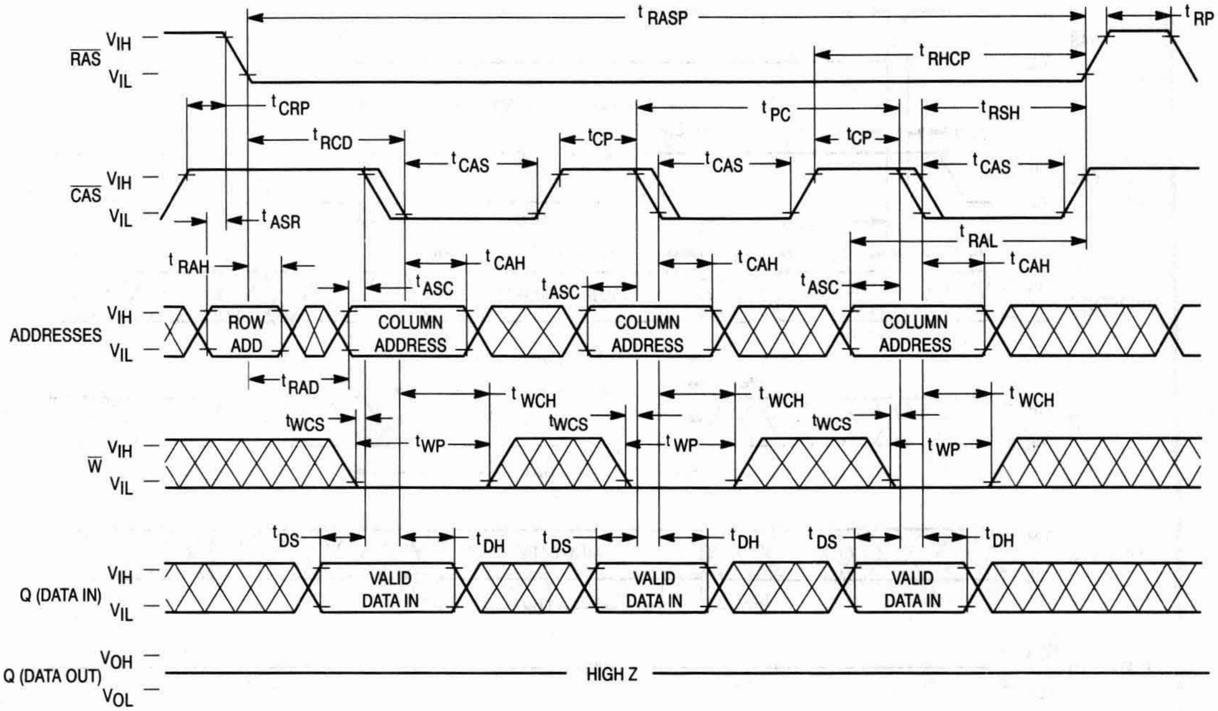
t_{RC}
t_{RP}
t_{RAS}
RAS
V_{IH}
V_{IL}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CSH}
t_{CRP}
t_{CAS}
CAS
t_{RAD}
t_{RAL}
t_{ASR}
t_{RAH}
t_{ASC}
t_{CAH}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
W
t_{RWL}
D (DATA IN)
VALID DATA
t_{DS}
t_{DH}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

TEST MODE — FAST PAGE MODE READ CYCLE



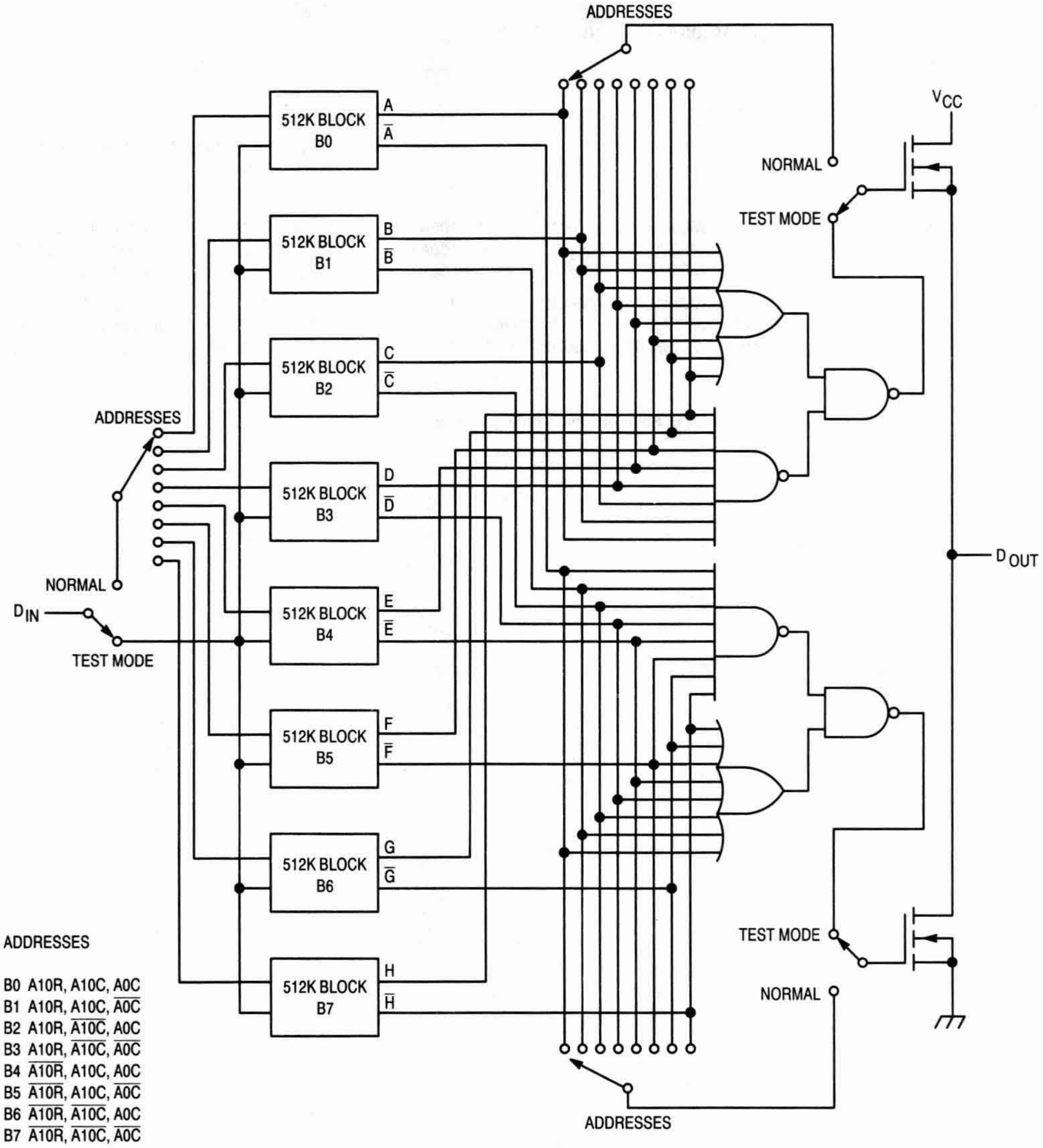
t_{RASP}
t_{RP}
$\overline{RAS}$ V_{IH} V_{IL}
t_{PC}
t_{CSH}
t_{CP}
t_{RSH}
t_{RCD}
t_{RHCP}
t_{CRP}
t_{CAS}
$\overline{CAS}$ V_{IH} V_{IL}
t_{RAL}
t_{RAH}
t_{CAH}
t_{ASR}
t_{ASC}
ADDRESSES V_{IH} V_{IL}
ROW ADD
COLUMN ADDRESS
t_{RCS}
t_{RRH}
t_{RAD}
t_{RCH}
$\overline{W}$ V_{IH} V_{IL}
t_{AA}
t_{CAC}
t_{RAC}
t_{CPA}
Q (DATA OUT) V_{OH} V_{OL}
VALID DATA OUT
t_{CLZ}
t_{OFF}

TEST MODE — FAST PAGE MODE EARLY WRITE CYCLE



t_{RASP}
t_{RP}
$\overline{RAS}$ V_{IH} V_{IL}
t_{RHCP}
t_{CRP}
t_{PC}
t_{RSH}
t_{RCD}
t_{CP}
t_{CAS}
$\overline{CAS}$ V_{IH} V_{IL}
t_{ASR}
t_{RAL}
t_{RAH}
t_{CAH}
t_{ASC}
ADDRESSES V_{IH} V_{IL}
ROW ADD
COLUMN ADDRESS
t_{RAD}
t_{WCH}
t_{WCS}
t_{WP}
$\overline{W}$ V_{IH} V_{IL}
t_{DS}
t_{DH}
Q (DATA IN) V_{IH} V_{IL}
VALID DATA IN
Q (DATA OUT) V_{OH} V_{OL}
HIGH Z

TEST MODE BLOCK DIAGRAM


ADDRESSES
512K BLOCK B0
A
$\overline{A}$
512K BLOCK B1
B
$\overline{B}$
512K BLOCK B2
C
$\overline{C}$
512K BLOCK B3
D
$\overline{D}$
512K BLOCK B4
E
$\overline{E}$
512K BLOCK B5
F
$\overline{F}$
512K BLOCK B6
G
$\overline{G}$
512K BLOCK B7
H
$\overline{H}$
ADDRESSES
NORMAL
D_{IN}
TEST MODE
V_{CC}
NORMAL
TEST MODE
D_{OUT}
TEST MODE
NORMAL
ADDRESSES

ADDRESSES

B0 A10R, A10C, A0C
B1 A10R, A10C, $\overline{\text{A0C}}$
B2 A10R, $\overline{\text{A10C}}$, A0C
B3 A10R, $\overline{\text{A10C}}$, $\overline{\text{A0C}}$
B4 $\overline{\text{A10R}}$, A10C, A0C
B5 $\overline{\text{A10R}}$, A10C, $\overline{\text{A0C}}$
B6 $\overline{\text{A10R}}$, $\overline{\text{A10C}}$, A0C
B7 $\overline{\text{A10R}}$, $\overline{\text{A10C}}$, $\overline{\text{A0C}}$

ORDERING INFORMATION

(Order by Full Part Number)

MCM 54100A or 5L4100A X XX XX

Motorola Memory Prefix — MCM

Part Number — 54100A or 5L4100A

Package (N = 300 mil SOJ, Z = 100 mil Plastic ZIP, T = 300 mil TSOP)

Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns)

Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers —

MCM54100AN60	MCM54100AN60R2	MCM54100AZ60	MCM54100AT60	MCM54100AT60R2
MCM54100AN70	MCM54100AN70R2	MCM54100AZ70	MCM54100AT70	MCM54100AT70R2
MCM54100AN80	MCM54100AN80R2	MCM54100AZ80	MCM54100AT80	MCM54100AT80R2
MCM5L4100AN60	MCM5L4100AN60R2	MCM5L4100AZ60	MCM5L4100AT60	MCM5L4100AT60R2
MCM5L4100AN70	MCM5L4100AN70R2	MCM5L4100AZ70	MCM5L4100AT70	MCM5L4100AT70R2
MCM5L4100AN80	MCM5L4100AN80R2	MCM5L4100AZ80	MCM5L4100AT80	MCM5L4100AT80R2

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM54100A-C

Advance Information

4M x 1 CMOS Dynamic RAM

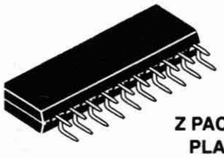
Page Mode

The MCM54100A-C is a 0.7µ CMOS high-speed dynamic random access memory. It is organized as 4,194,304 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM54100A-C requires only 11 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil and a 100 mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Fast Page Mode
- Test Mode
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM54100A-C = 16 ms
- Fast Access Time (t_{RAC}): MCM54100A-C70 = 70 ns (Max)
  MCM54100A-C80 = 80 ns (Max)
- Low Active Power: MCM54100A-C70 = 550 mW (Max)
  MCM54100A-C80 = 468 mW (Max)
- Low Standby Power Dissipation:
  MCM54100A-C = 11 mW (Max, TTL Levels)
  = 5.5 mW (Max, CMOS Levels)

N PACKAGE
300 MIL SOJ
CASE 822-03



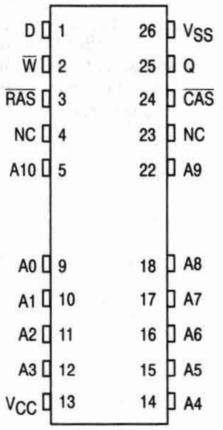
Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836-02

PIN NAMES

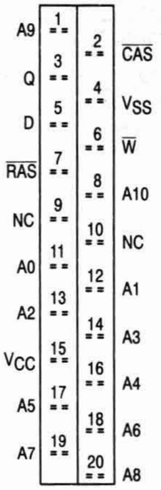
A0 – A10	Address Input
D	Data Input
Q	Data Output
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENTS

300 MIL SOJ

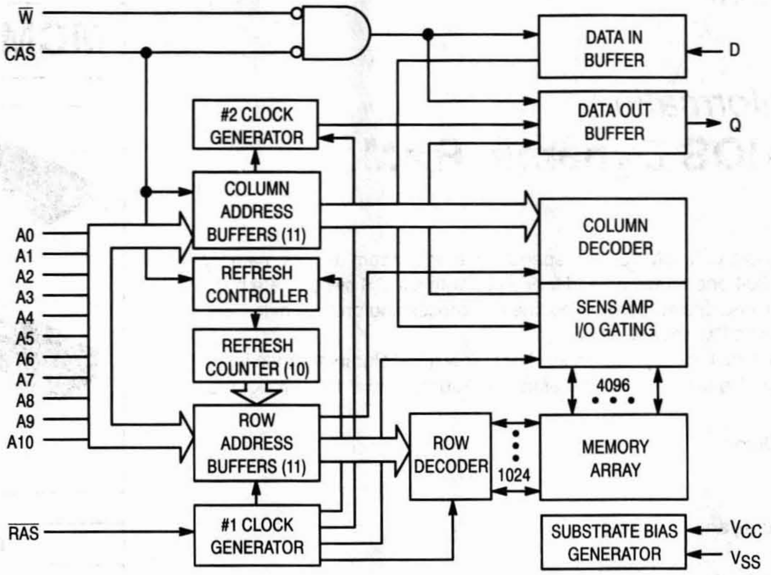

D 1
W 2
RAS 3
NC 4
A10 5
A0 9
A1 10
A2 11
A3 12
VCC 13
26 VSS
25 Q
24 CAS
23 NC
22 A9
18 A8
17 A7
16 A6
15 A5
14 A4

100 MIL ZIP


A9 1
2 CAS
Q 3
4 VSS
D 5
6 W
RAS 7
8 A10
NC 9
10 NC
A0 11
12 A1
A2 13
14 A3
VCC 15
16 A4
A5 17
18 A6
A7 19
20 A8

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM


$\overline{W}$
$\overline{CAS}$
DATA IN BUFFER
D
DATA OUT BUFFER
Q
#2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (11)
COLUMN DECODER
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
REFRESH CONTROLLER
SENS AMP I/O GATING
REFRESH COUNTER (10)
4096
ROW ADDRESS BUFFERS (11)
ROW DECODER
1024
MEMORY ARRAY
$\overline{RAS}$
#1 CLOCK GENERATOR
SUBSTRATE BIAS GENERATOR
V_{CC}
V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current	I_{out}	50	mA
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM54100A-C70, t_{RC} = 130 ns MCM54100A-C80, t_{RC} = 150 ns	I_{CC1}	— —	100 85	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles ($\overline{CAS}$ = V_{IH}) MCM54100A-C70, t_{RC} = 130 ns MCM54100A-C80, t_{RC} = 150 ns	I_{CC3}	 — —	 100 85	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL}) MCM54100A-C70, t_{PC} = 45 ns MCM54100A-C80, t_{PC} = 50 ns	I_{CC4}	 — —	 60 50	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} – 0.2 V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM54100A-C70, t_{RC} = 130 ns MCM54100A-C80, t_{RC} = 150 ns	I_{CC6}	 — —	 100 85	mA	3
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery-back up. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A10, D	C_{in}	5	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\,\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM54100A-C70		MCM54100A-C80		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	155	—	175	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	50	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	70	—	75	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	40	—	45	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	200,000	80	200,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	45	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

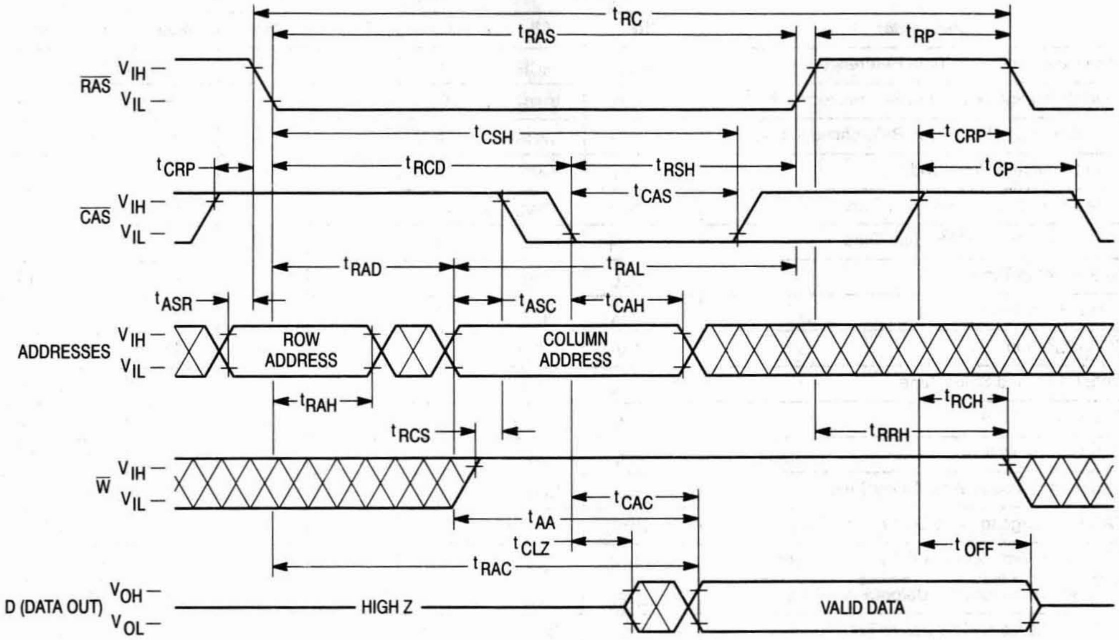
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM54100A-C70		MCM54100A-C80		Unit	Notes
	Std.	Alt.	Min	Max	Min	Max		
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14
Refresh Period	t_{RVRV}	t_{RFSH}	—	16	—	16	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	20	—	20	—	ns	15
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	70	—	80	—	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	35	—	45	—	ns	15
$\overline{\text{CAS}}$ Precharge to Write Delay Time (Page Mode)	t_{CEHWL}	t_{CPWD}	40	—	45	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Time	t_{CEHCEL}	t_{CPT}	40	—	40	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	ns	

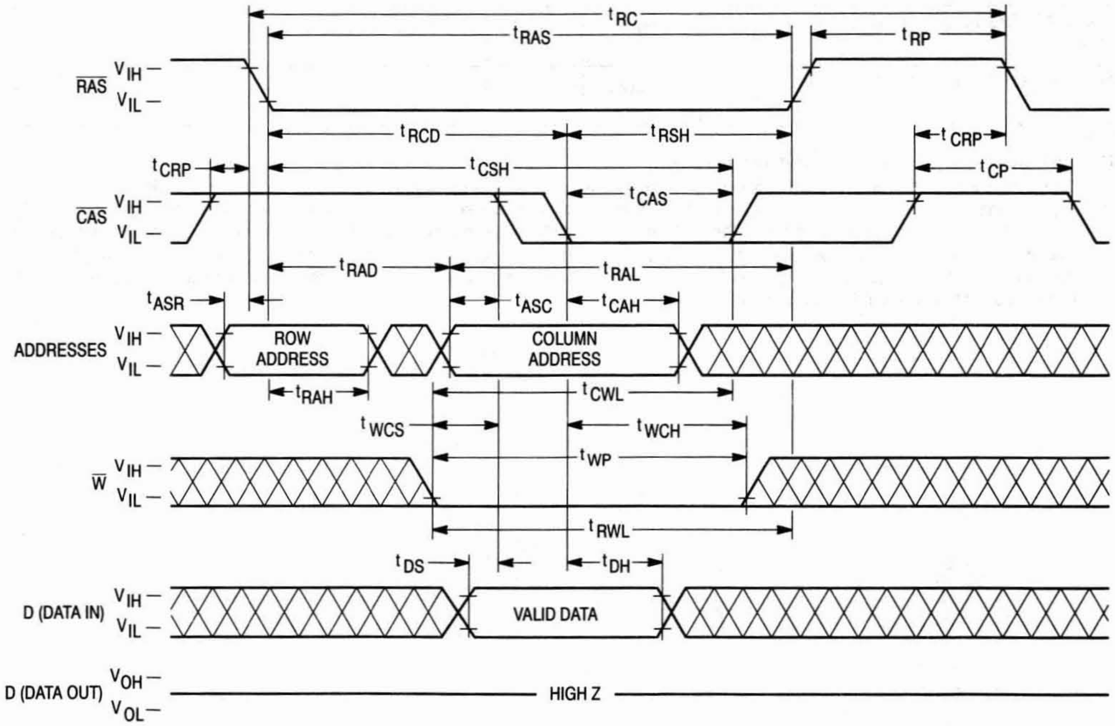
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE


RAS
VIH
VIL
CAS
ADDRESSES
W
D (DATA OUT)
VOH
VOL
tRC
tRAS
tRP
tCSH
tCRP
tRCD
tRSH
tCP
tCAS
tRAD
tRAL
tASR
tASC
tCAH
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
tCAC
tAA
tOFF
tCLZ
tRAC
HIGH Z
VALID DATA

EARLY WRITE CYCLE


RAS
VIH
VIL
CAS
ADDRESSES
W
D (DATA IN)
D (DATA OUT)
VOH
VOL
tRC
tRAS
tRP
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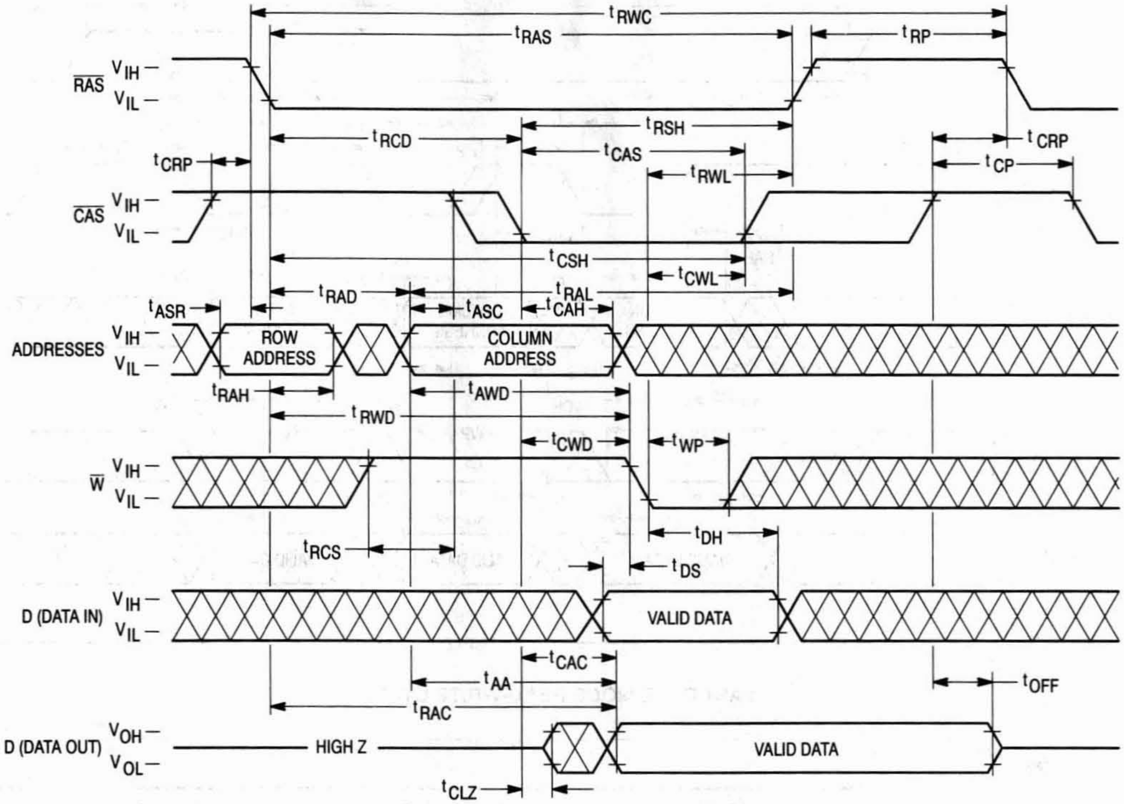
tCRP
tCSH
tCP
tCAS
tRAD
tRAL
tASR
tASC
tCAH
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWP
tRWL
tDS
tDH
VALID DATA
HIGH Z

READ-WRITE CYCLE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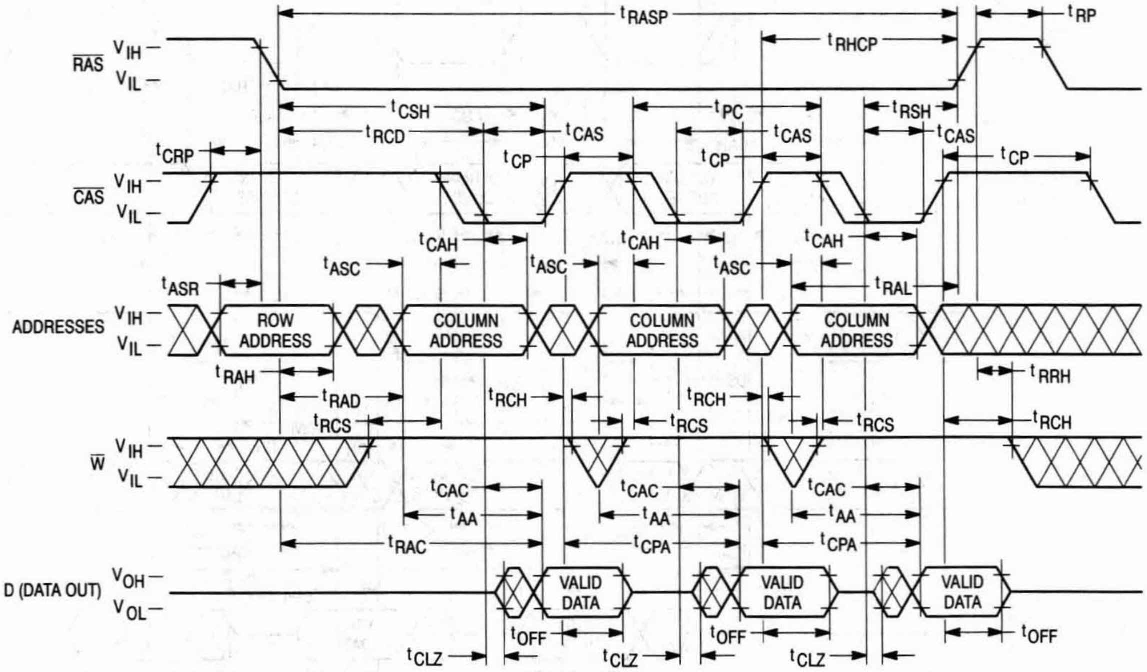
tRAS
tRP
RAS VIH
VIL
tRCD
tRSH
tCRP
tCAS
tCRP
tCP
tRWL
CAS VIH
VIL
tCSH
tCWL
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tAWD
tRWD
tCWD
tWP
W VIH
VIL
tRCS
tDH
tDS
D (DATA IN) VIH
VIL
VALID DATA
tCAC
tAA
tOFF
tRAC
D (DATA OUT) VOH
VOL
HIGH Z
VALID DATA
tCLZ

FAST PAGE MODE READ CYCLE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tRP
tRHCP
RAS VIH
VIL
tCSH
tPC
tRSH
tRCD
tCAS
tCAS
tCAS
tCRP
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tCP
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VIL
tCAH
tCAH
tCAH
tASC
tASC
tASC
tASR
tRAL
ADDRESSES VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAH
tRRH
tRAD
tRCH
tRCH
tRCS
tRCS
tRCS
tRCH
W VIH
VIL
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
D (DATA OUT) VOH
VOL
VALID DATA
VALID DATA
VALID DATA
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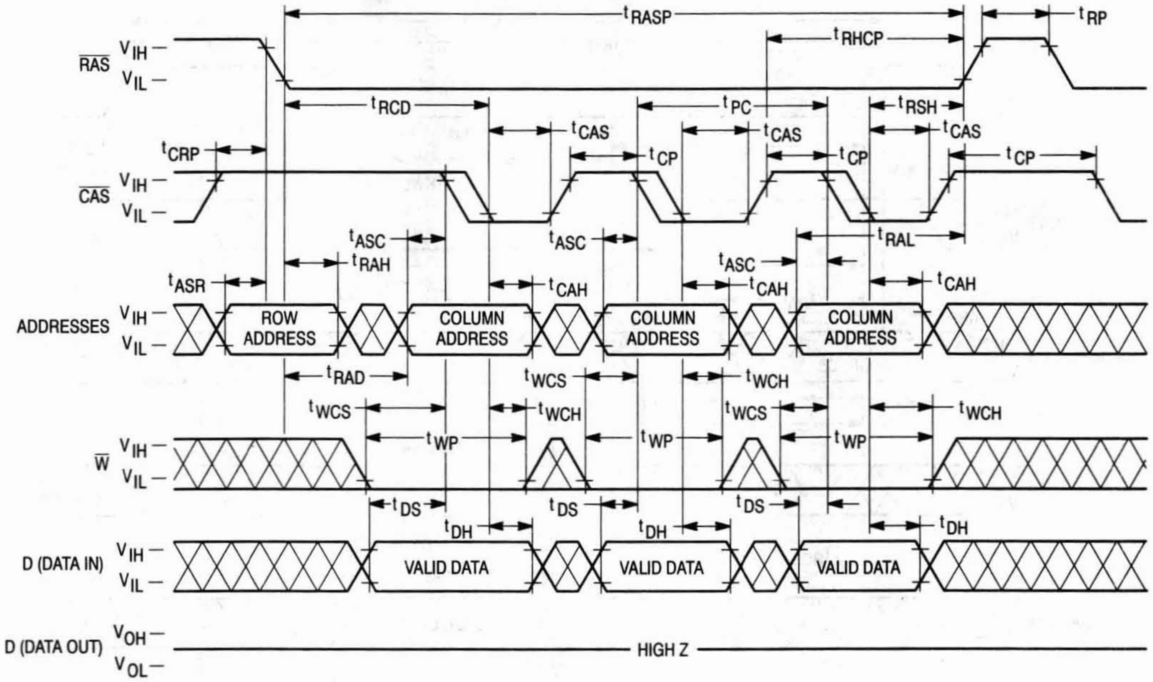
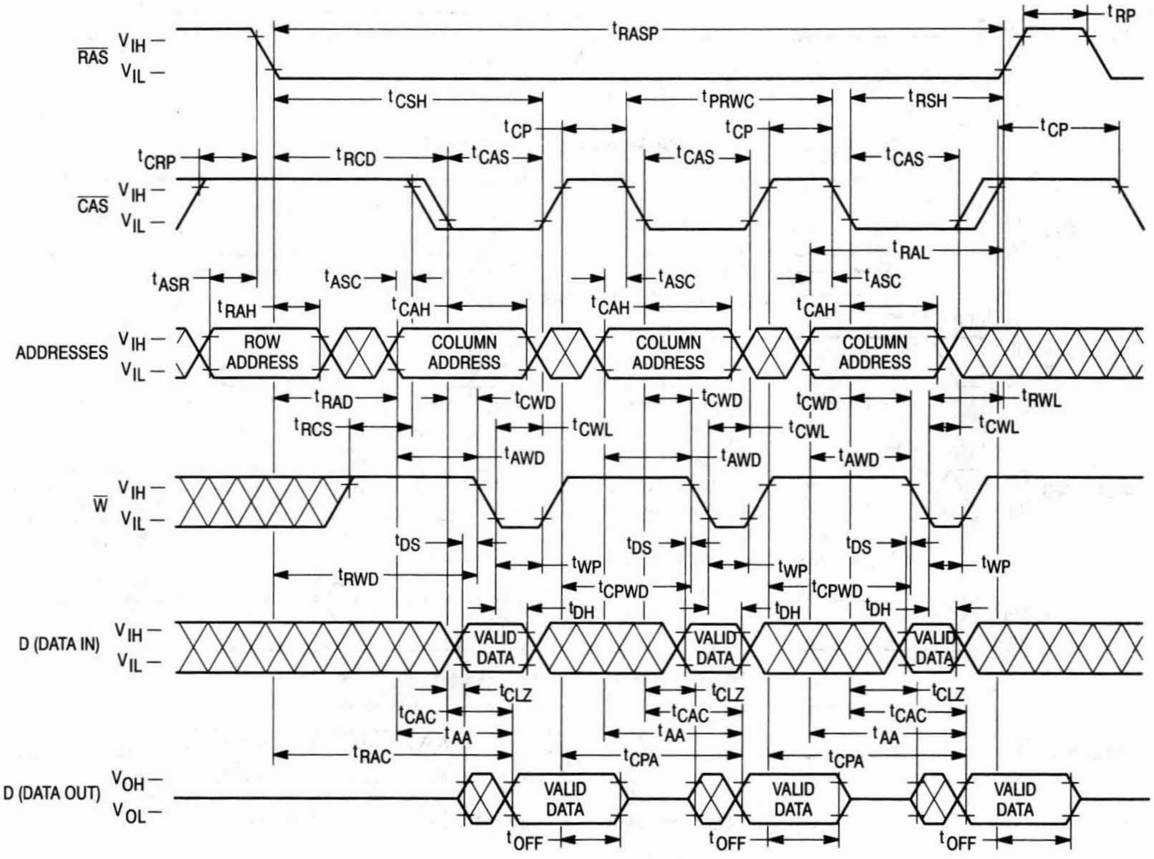
tOFF
tOFF
tCLZ
tCLZ
tCLZ

FAST PAGE MODE EARLY WRITE CYCLE



t_{RASP}
t_{RP}
t_{RHCP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RCD}
t_{PC}
t_{RSH}
t_{CAS}
t_{CAS}
t_{CAS}
t_{CRP}
t_{CP}
t_{CP}
t_{CP}
$\overline{CAS}$
t_{ASC}
t_{RAH}
t_{ASC}
t_{RAL}
t_{ASC}
t_{ASR}
t_{CAH}
t_{CAH}
t_{CAH}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
t_{RAD}
t_{WCS}
t_{WCH}
t_{WCS}
t_{WCH}
t_{WCS}
t_{WCH}
t_{WP}
t_{WP}
t_{WP}
$\overline{W}$
t_{DS}
t_{DS}
t_{DS}
t_{DH}
t_{DH}
t_{DH}
D (DATA IN)
VALID DATA
VALID DATA
VALID DATA
D (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

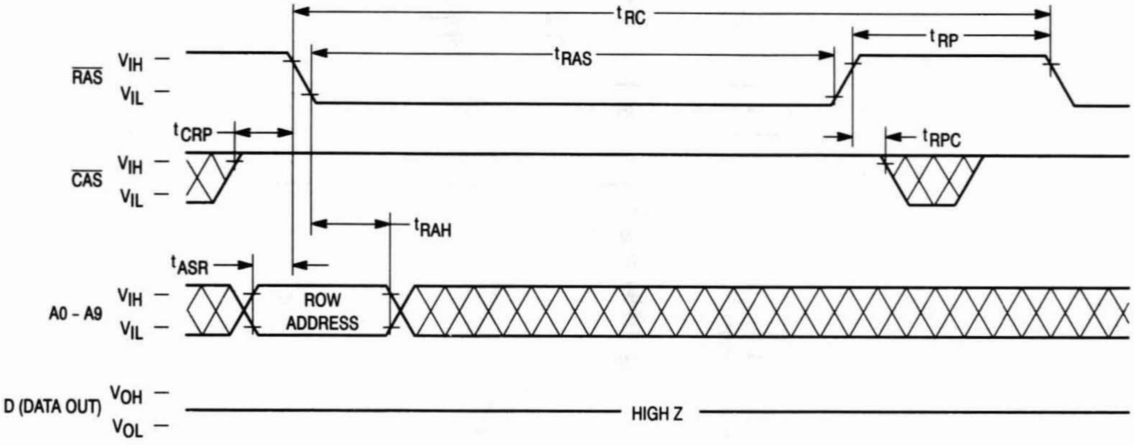
FAST PAGE MODE READ-WRITE CYCLE



t_{RASP}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{PRWC}
t_{RSH}
t_{CP}
t_{CP}
t_{CP}
t_{CRP}
t_{RCD}
t_{CAS}
t_{CAS}
t_{CAS}
$\overline{CAS}$
t_{RAL}
t_{ASR}
t_{ASC}
t_{ASC}
t_{ASC}
t_{RAH}
t_{CAH}
t_{CAH}
t_{CAH}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
t_{RAD}
t_{CWD}
t_{CWD}
t_{CWD}
t_{RWL}
t_{RCS}
t_{CWL}
t_{CWL}
t_{CWL}
t_{AWD}
t_{AWD}
t_{AWD}
$\overline{W}$
t_{DS}
t_{DS}
t_{DS}
t_{RWD}
t_{WP}
t_{WP}
t_{WP}
t_{CPWD}
t_{CPWD}
t_{DH}
t_{DH}
t_{DH}
D (DATA IN)
VALID DATA
VALID DATA
VALID DATA
t_{CLZ}
t_{CLZ}
t_{CLZ}
t_{CAC}
t_{CAC}
t_{CAC}
t_{AA}
t_{AA}
t_{AA}
t_{RAC}
t_{CPA}
t_{CPA}
D (DATA OUT)
V_{OH}
V_{OL}
VALID DATA
VALID DATA
VALID DATA
t_{OFF}
t_{OFF}
t_{OFF}

$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

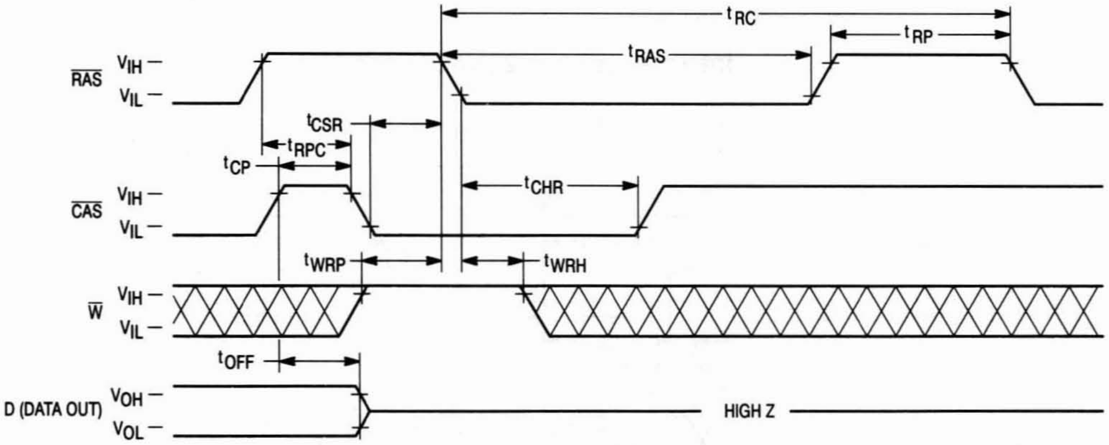
($\overline{\text{W}}$ and A10 are Don't Care)



t RC
t RP
t RAS
RAS
VIH
VIL
t CRP
t RPC
CAS
VIH
VIL
t RAH
t ASR
A0 – A9
VIH
VIL
ROW ADDRESS
D (DATA OUT)
VOH
VOL
HIGH Z

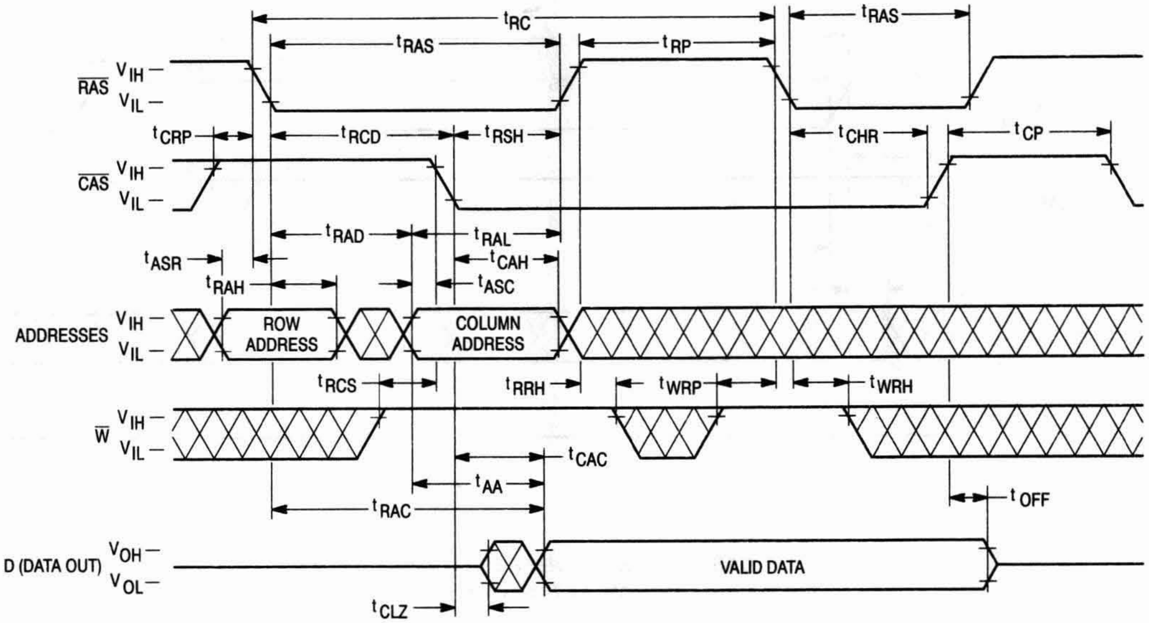
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

(A0 – A10 are Don't Care)



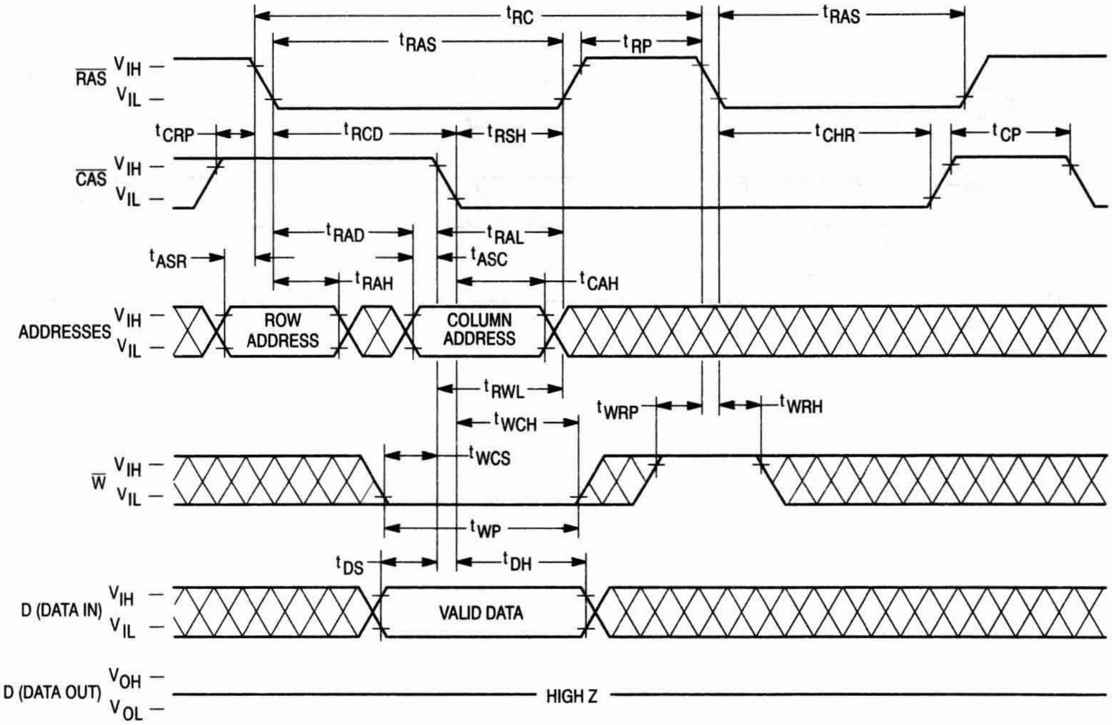
t RC
t RP
t RAS
RAS
VIH
VIL
t CSR
t RPC
t CP
t CHR
CAS
VIH
VIL
t WRP
t WRH
W
VIH
VIL
t OFF
D (DATA OUT)
VOH
VOL
HIGH Z

HIDDEN REFRESH CYCLE (READ)



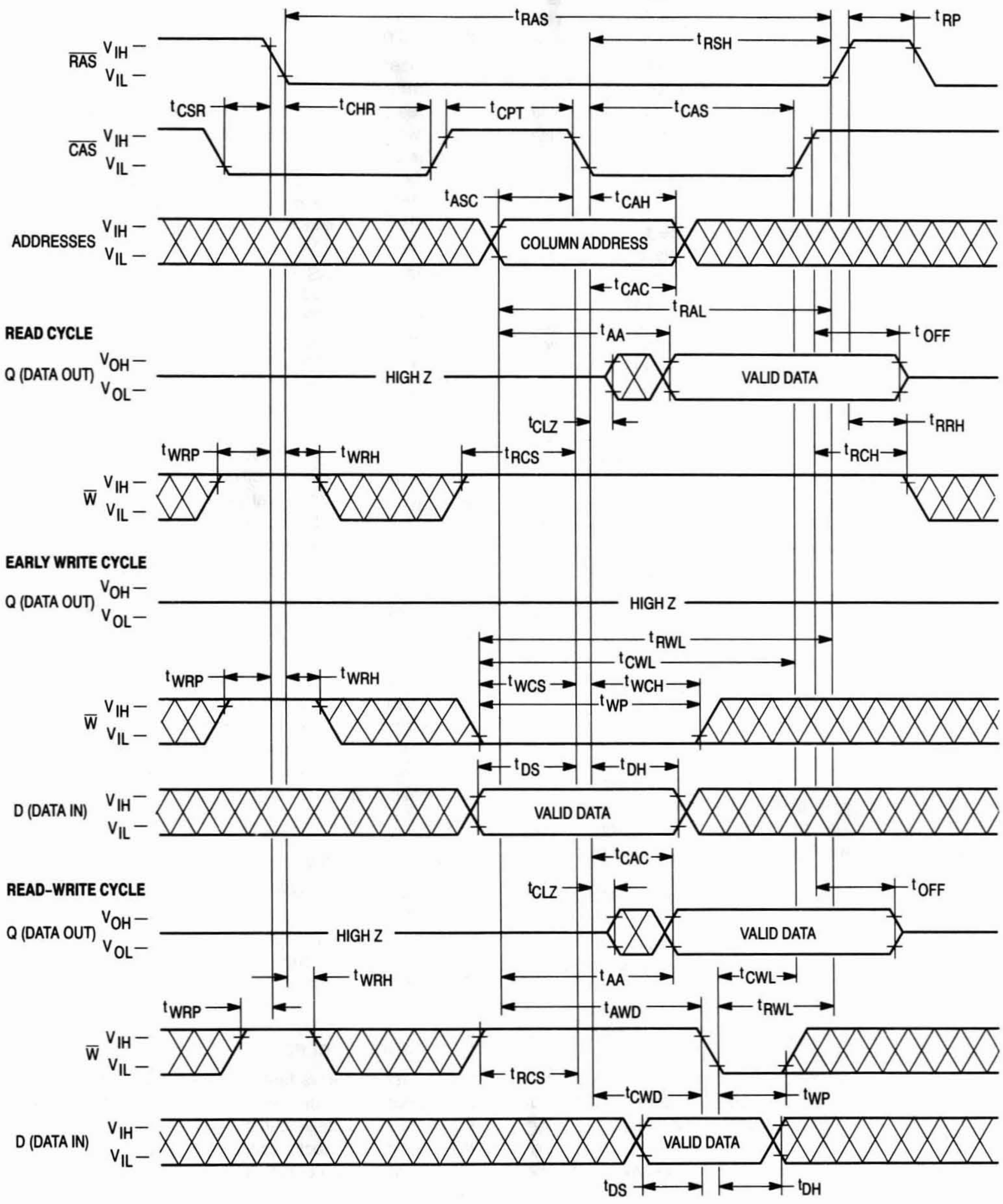
tRC
tRAS
tRAS
tRP
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCP
CAS
VIH
VIL
tRAD
tRAL
tASR
tCAH
tRAH
tASC
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRCS
tRRH
tWRP
tWRH
W
VIH
VIL
tCAC
tAA
tOFF
tRAC
D (DATA OUT)
VOH
VOL
VALID DATA
tCLZ

HIDDEN REFRESH CYCLE (EARLY WRITE)



tRC
tRAS
tRAS
tRP
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCP
CAS
VIH
VIL
tRAD
tRAL
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRWL
tWCH
tWRP
tWRH
tWCS
W
VIH
VIL
tWP
tDS
tDH
D (DATA IN)
VIH
VIL
VALID DATA
D (DATA OUT)
VOH
VOL
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



t_{RAS}
t_{RP}
t_{RSH}
$\overline{RAS}$ V_{IH} – V_{IL} –
t_{CSR}
t_{CHR}
t_{CPT}
t_{CAS}
$\overline{CAS}$ V_{IH} – V_{IL} –
t_{ASC}
t_{CAH}
ADDRESSES V_{IH} – V_{IL} –
COLUMN ADDRESS
t_{CAC}
t_{RAL}
READ CYCLE
t_{AA}
t_{OFF}
Q (DATA OUT) V_{OH} – V_{OL} –
HIGH Z
VALID DATA
t_{CLZ}
t_{RRH}
t_{WRP}
t_{WRH}
t_{RCS}
t_{RCH}
$\overline{W}$ V_{IH} – V_{IL} –
EARLY WRITE CYCLE
Q (DATA OUT) V_{OH} – V_{OL} –
HIGH Z
t_{RWL}
t_{CWL}
t_{WRP}
t_{WRH}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{W}$ V_{IH} – V_{IL} –
t_{DS}
t_{DH}
D (DATA IN) V_{IH} – V_{IL} –
VALID DATA
t_{CAC}
READ-WRITE CYCLE
t_{CLZ}
t_{OFF}
Q (DATA OUT) V_{OH} – V_{OL} –
HIGH Z
VALID DATA
t_{WRH}
t_{AA}
t_{CWL}
t_{WRP}
t_{AWD}
t_{RWL}
$\overline{W}$ V_{IH} – V_{IL} –
t_{RCS}
t_{CWD}
t_{WP}
D (DATA IN) V_{IH} – V_{IL} –
VALID DATA
t_{DS}
t_{DH}

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 11-bit address fields. A total of twenty-two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 bit locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the 4M RAM: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window; however, $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ clock active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered elsewhere.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but Q may be indeterminate — see note 15 of AC Operating Conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the 4M dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum of t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54100A-C require refresh every 16 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54100A. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54100A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{\text{RAS}}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode cycle) as in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of 8 **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

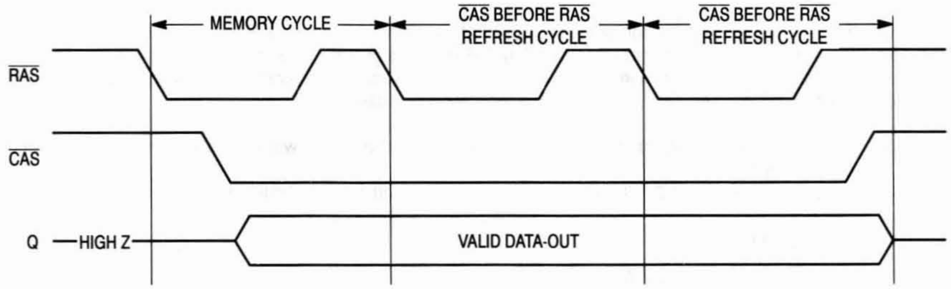

MEMORY CYCLE
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
Q
HIGH Z
VALID DATA-OUT

Figure 1. Hidden Refresh Cycle

TEST MODE

The internal organization of this device (512K x 8) allows it to be tested as if it were a 512K x 1 DRAM. Nineteen of the twenty-two addresses are used when operating the device in test mode. Row address A0, and column addresses A0 and A10 are ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0 – B7) in parallel. External data out is determined by the internal test mode logic of the device. See the following truth table and test mode block diagram.

$\overline{\text{W}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ timing puts the device in **Test Mode** as shown in the test mode timing diagram. A **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** or a **$\overline{\text{RAS}}$-only refresh cycle** puts the device back into normal mode. Refresh is performed in test mode by using a **$\overline{\text{W}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle** which uses internal refresh address counter.

TEST MODE TRUTH TABLE

D	B0	B1	B2	B3	B4	B5	B6	B7	Q
0	0	0	0	0	0	0	0	0	1
1	1	1	1	1	1	1	1	1	1
—	Any Other								0

TEST MODE
AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

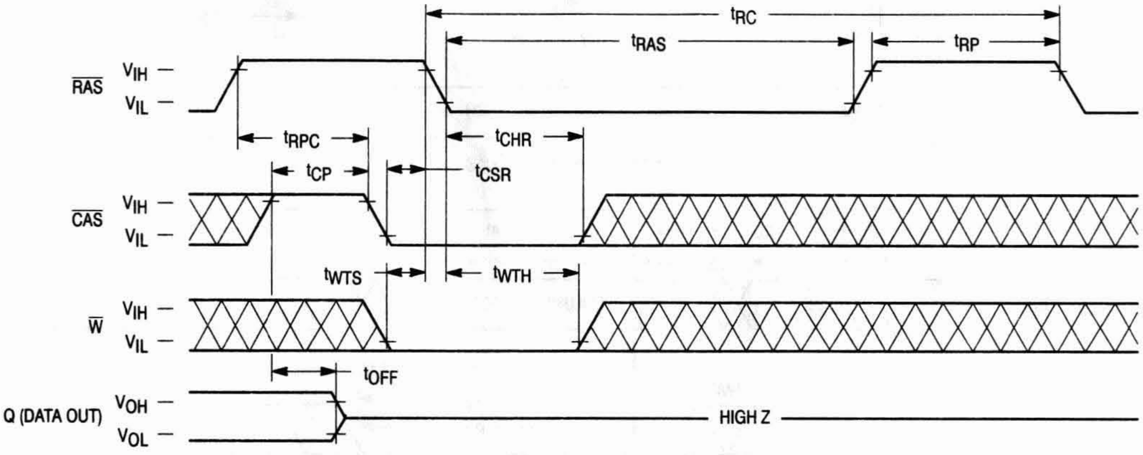
Parameter	Symbol		MCM54100A-70 MCM5L4100A-70		MCM54100A-80 MCM5L4100A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	135	—	155	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	—	55	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	75	—	85	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	25	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	40	—	45	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	45	—	50	ns	6
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	75	10,000	85	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	75	200,000	85	200,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	25	—	25	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	75	—	85	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	45	—	50	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	25	10,000	25	10,000	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	40	—	45	—	ns	

NOTES:

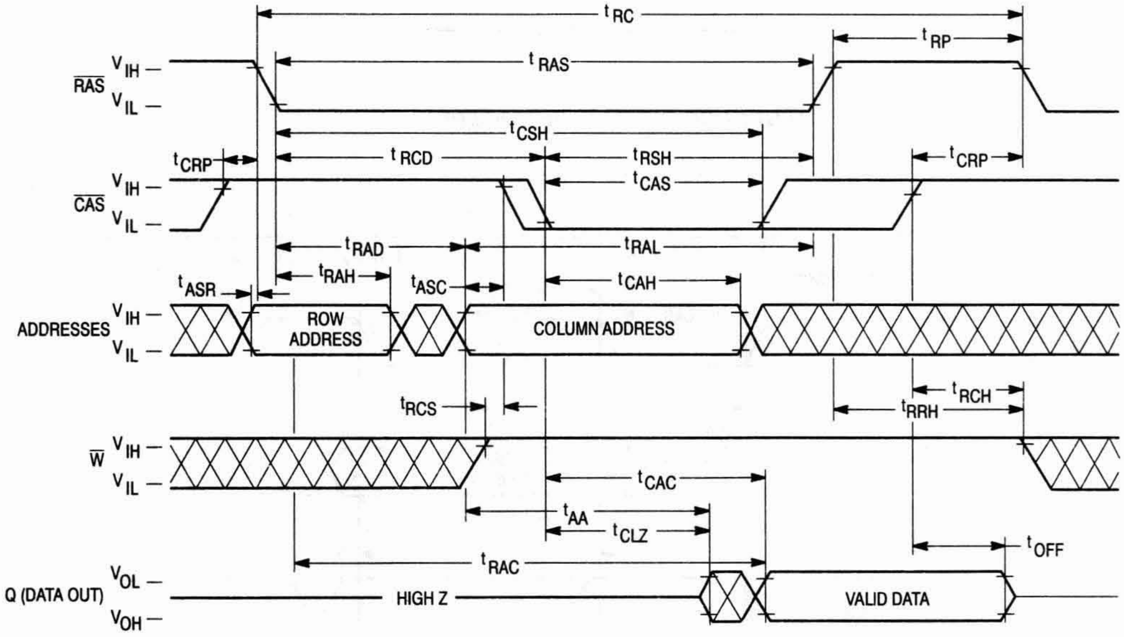
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).

W̅, C̅A̅S̅ BEFORE R̅A̅S̅ REFRESH CYCLE (TEST MODE ENTRY)

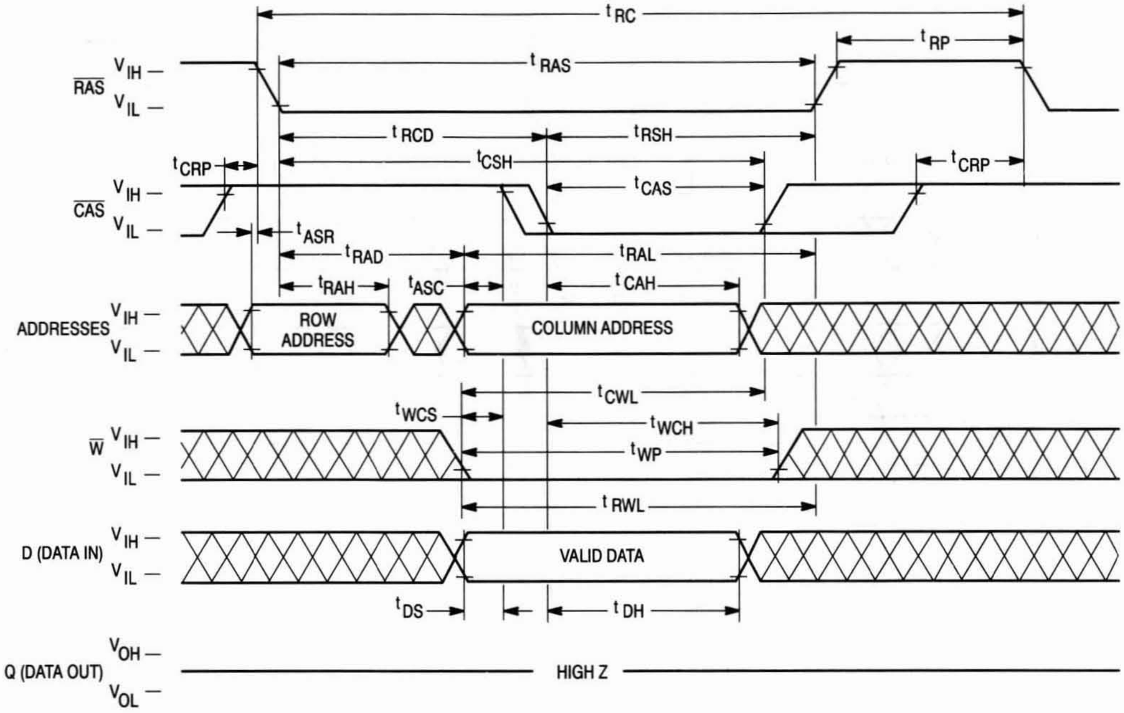
(D and A0 – A10 are Don't Care)


tRC
tRAS
tRP
RAS
VIH
VIL
tRPC
tCHR
tCP
tCSR
CAS
VIH
VIL
tWTS
tWTH
W
VIH
VIL
tOFF
Q (DATA OUT)
VOH
VOL
HIGH Z

TEST MODE — READ CYCLE

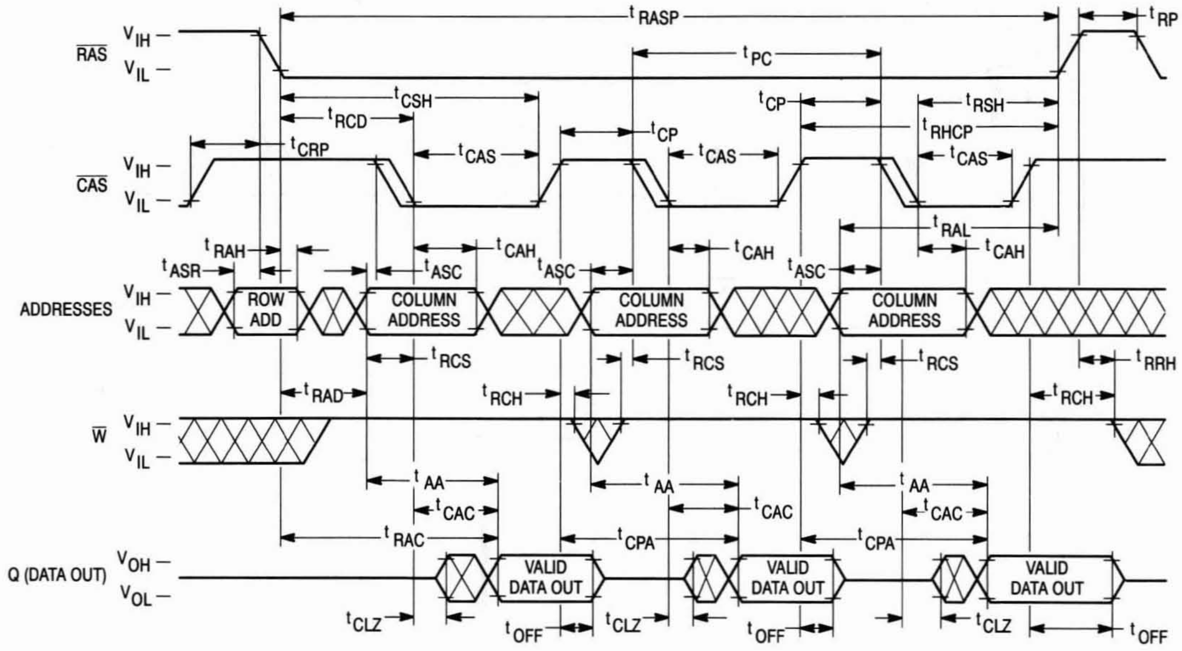

tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tRAD
tRAL
tRAH
tASC
tCAH
tASR
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRCH
tRCS
tRRH
W
VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
Q (DATA OUT)
VOL
VOH
HIGH Z
VALID DATA

TEST MODE — EARLY WRITE CYCLE



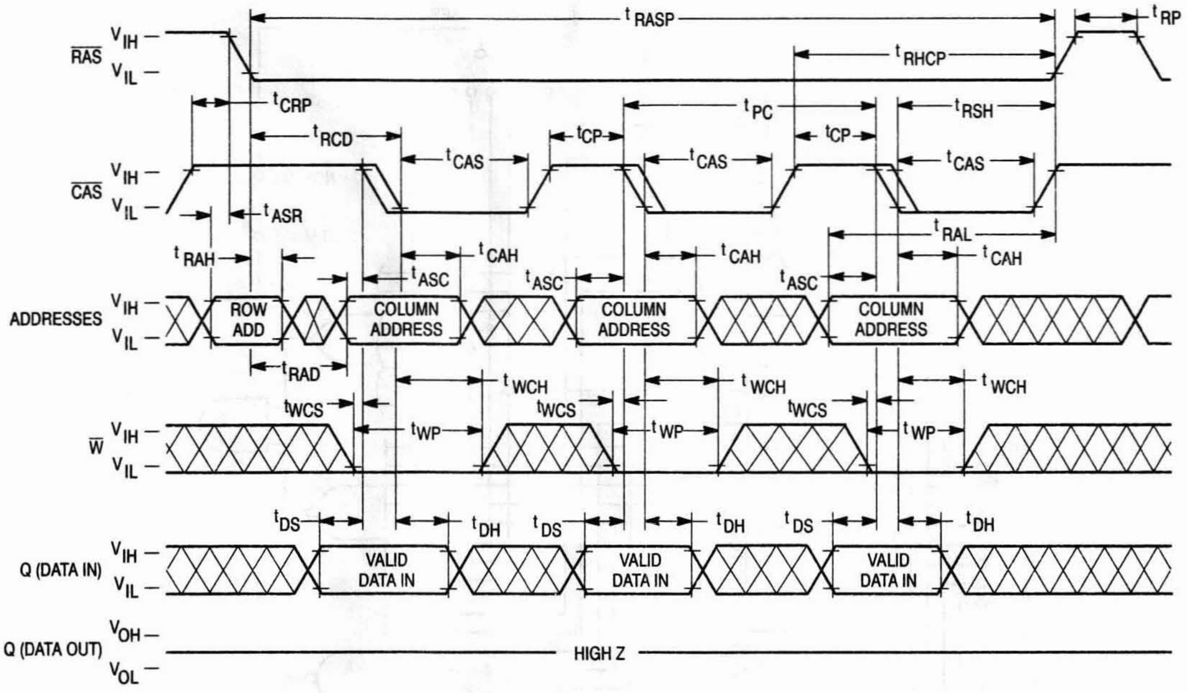
t_{RC}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RAS}
t_{RCD}
t_{RSH}
t_{CSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
t_{ASR}
t_{RAD}
t_{RAL}
t_{RAH}
t_{ASC}
t_{CAH}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{CWL}
t_{WCS}
t_{WCH}
$\overline{W}$
t_{WP}
t_{RWL}
D (DATA IN)
VALID DATA
t_{DS}
t_{DH}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

TEST MODE — FAST PAGE MODE READ CYCLE



t_{RASP}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{PC}
t_{CSH}
t_{CP}
t_{RSH}
t_{RCD}
t_{RHCP}
t_{CRP}
t_{CAS}
$\overline{CAS}$
t_{RAL}
t_{RAH}
t_{CAH}
t_{ASR}
t_{ASC}
ADDRESSES
ROW ADD
COLUMN ADDRESS
t_{RCS}
t_{RRH}
t_{RAD}
t_{RCH}
$\overline{W}$
t_{AA}
t_{CAC}
t_{RAC}
t_{CPA}
Q (DATA OUT)
V_{OH}
V_{OL}
VALID DATA OUT
t_{CLZ}
t_{OFF}

TEST MODE — FAST PAGE MODE EARLY WRITE CYCLE


RAS
CAS
ADDRESSES
W
Q (DATA IN)
Q (DATA OUT)
V_IH
V_IL
V_OH
V_OL
t_RASP
t_RP
t_RHCP
t_CRP
t_PC
t_RSH
t_RCD
t_CP
t_CAS
t_ASR
t_RAL
t_RAH
t_CAH
t_ASC
ROW ADD
COLUMN ADDRESS
t_RAD
t_WCH
t_WCS
t_WP
t_DS
t_DH
VALID DATA IN
HIGH Z

ORDERING INFORMATION
(Order by Full Part Number)

MCM 54100A-C X XX XX

Motorola Memory Prefix — MCM

Part Number — 54100A-C

Shipping Method (R2 = Tape and Reel, Blank = Rails)

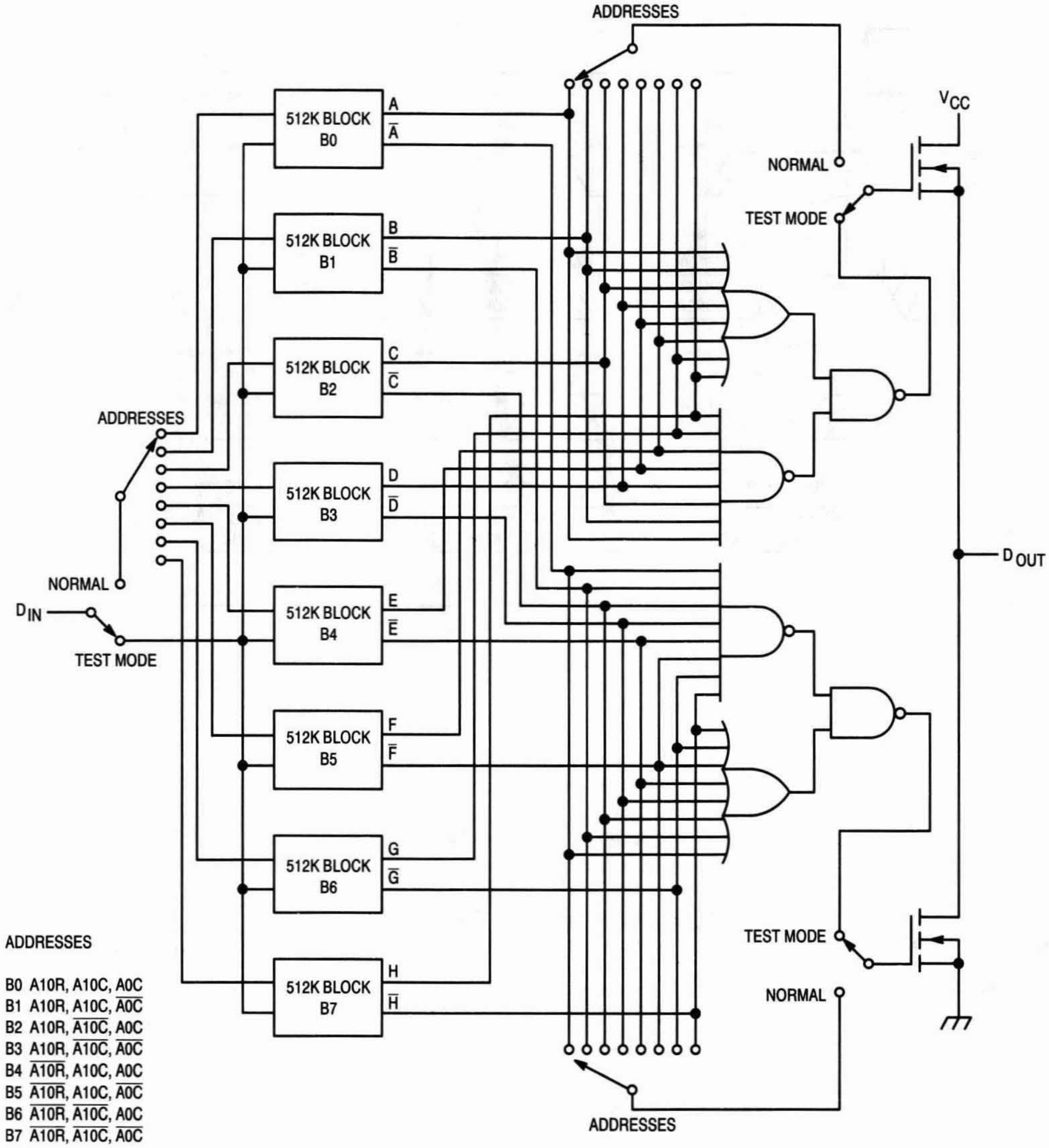
Speed (70 = 70 ns, 80 = 80 ns)

Package (N = 300 mil SOJ, Z = 100 mil Plastic ZIP)

Full Part Numbers —			
	MCM54100ANC70	MCM54100ANC70R2	MCM54100AZC70
	MCM54100ANC80	MCM54100ANC80R2	MCM54100AZC80

NOTE: For mechanical data, please see Chapter 10.

TEST MODE BLOCK DIAGRAM


ADDRESSES
512K BLOCK B0
A
$\overline{A}$
512K BLOCK B1
B
$\overline{B}$
512K BLOCK B2
C
$\overline{C}$
512K BLOCK B3
D
$\overline{D}$
512K BLOCK B4
E
$\overline{E}$
512K BLOCK B5
F
$\overline{F}$
512K BLOCK B6
G
$\overline{G}$
512K BLOCK B7
H
$\overline{H}$
ADDRESSES
NORMAL
D_{IN}
TEST MODE
NORMAL
TEST MODE
V_{CC}
D_{OUT}
TEST MODE
NORMAL
ADDRESSES

ADDRESSES

B0 A10R, A10C, A0C
B1 A10R, A10C, $\overline{\text{A0C}}$
B2 A10R, $\overline{\text{A10C}}$, A0C
B3 A10R, $\overline{\text{A10C}}$, $\overline{\text{A0C}}$
B4 $\overline{\text{A10R}}$, A10C, A0C
B5 $\overline{\text{A10R}}$, A10C, $\overline{\text{A0C}}$
B6 $\overline{\text{A10R}}$, $\overline{\text{A10C}}$, A0C
B7 $\overline{\text{A10R}}$, $\overline{\text{A10C}}$, $\overline{\text{A0C}}$

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM54101A

Advance Information

4M x 1 CMOS Dynamic RAM

Nibble Mode

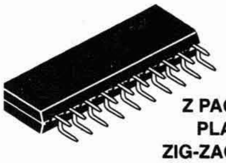
The MCM54101A is a 0.7µ CMOS high-speed dynamic random access memory. It is organized as 4,194,304 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The fast nibble mode feature allows high-speed serial access of up to 4 bits of data.

The MCM54101A requires only 11 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil small outline package, a 300 mil thin-small-outline package (TSOP), and a 100 mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Nibble Mode
- Test Mode
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM54101A = 16 ms
- Fast Access Time (t_{RAC}):
  - MCM54101A-60 = 60 ns (Max)
  - MCM54101A-70 = 70 ns (Max)
  - MCM54101A-80 = 80 ns (Max)
- Low Active Power:
  - MCM54101A-60 = 660 mW (Max)
  - MCM54101A-70 = 550 mW (Max)
  - MCM54101A-80 = 468 mW (Max)
- Low Standby Power Dissipation:
  - MCM54101A = 11 mW (Max, TTL Levels)
  - = 5.5 mW (Max, CMOS Levels)

N PACKAGE
300 MIL SOJ
CASE 822-03

T PACKAGE
300 MIL TSOP
CASE 892-01



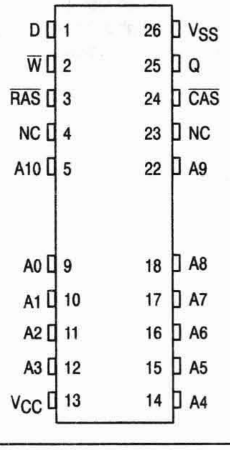
Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836-02

PIN NAMES

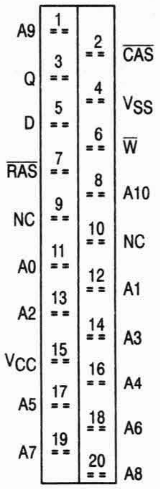
A0 – A10	Address Input
D	Data Input
Q	Data Output
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENTS

300 MIL SOJ/TSOP

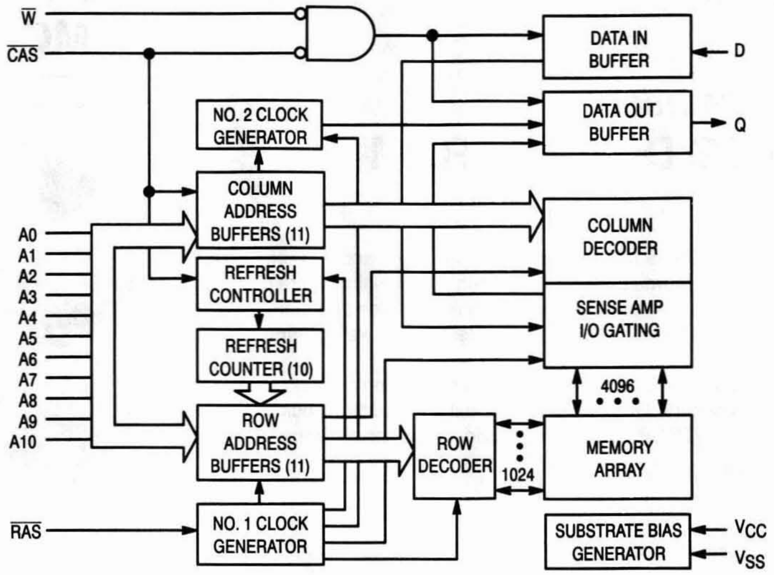


100 MIL ZIP



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM


W
CAS
NO. 2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (11)
REFRESH CONTROLLER
REFRESH COUNTER (10)
ROW ADDRESS BUFFERS (11)
NO. 1 CLOCK GENERATOR
RAS
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
DATA IN BUFFER
D
DATA OUT BUFFER
Q
COLUMN DECODER
SENSE AMP I/O GATING
4096
ROW DECODER
1024
MEMORY ARRAY
SUBSTRATE BIAS GENERATOR
VCC
VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	MCM54101A-60, t_{RC} = 110 ns MCM54101A-70, t_{RC} = 130 ns MCM54101A-80, t_{RC} = 150 ns	I_{CC1}	— — —	120 100 85	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles ($\overline{CAS}$ = V_{IH})	MCM54101A-60, t_{RC} = 110 ns MCM54101A-70, t_{RC} = 130 ns MCM54101A-80, t_{RC} = 150 ns	I_{CC3}	— — —	120 100 85	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL})	MCM54101A-60, t_{NC} = 40 ns MCM54101A-70, t_{NC} = 40 ns MCM54101A-80, t_{NC} = 40 ns	I_{CC4}	— — —	50 50 50	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)		I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	MCM54101A-60, t_{RC} = 110 ns MCM54101A-70, t_{RC} = 130 ns MCM54101A-80, t_{RC} = 150 ns	I_{CC6}	— — —	120 100 85	mA	1
Input Leakage Current (0 V ≤ V_{in} ≤ 5.5 V)		$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)		$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)		V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A10, D	C_{in}	5	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM54101A-60		MCM54101A-70		MCM54101A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	135	—	155	—	175	—	ns	5
Nibble Mode Cycle Time	t_{CEHCEH}	t_{NC}	40	—	40	—	40	—	ns	
Nibble Mode Read-Write Cycle Time	t_{CELCEL}	t_{NRWC}	65	—	65	—	65	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6, 9
Nibble Mode Access Time	t_{CELQV}	t_{NCAC}	—	20	—	20	—	20	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	20	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

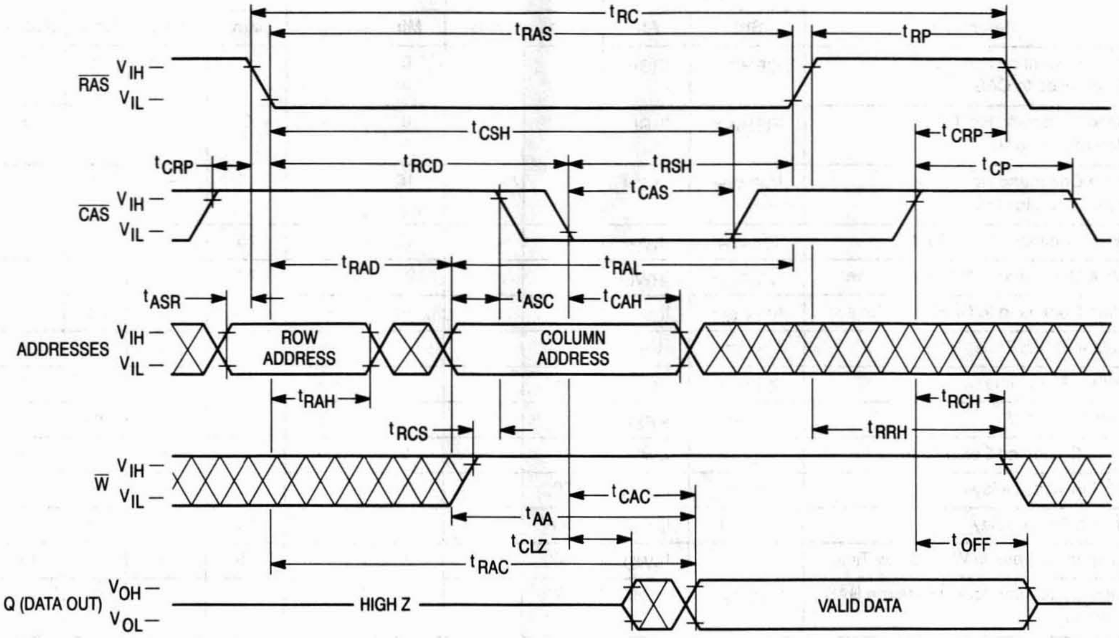
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM54101A-60		MCM54101A-70		MCM54101A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	14
Refresh Period	t_{RVRV}	t_{RFSH}	—	16	—	16	—	16	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	20	—	20	—	20	—	ns	15
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	60	—	70	—	80	—	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	30	—	35	—	45	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
Nibble Mode Pulse Width	t_{CELCEH}	t_{NCAS}	20	—	20	—	20	—	ns	
Nibble Mode $\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{NCP}	10	—	10	—	10	—	ns	
Nibble Mode $\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{NRSH}	20	—	20	—	20	—	ns	
Nibble Mode $\overline{\text{CAS}}$ to Write Delay TIme	t_{CELWL}	t_{NCWD}	20	—	20	—	20	—	ns	
Nibble Mode Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{NRWL}	20	—	20	—	20	—	ns	
Nibble Mode Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{NCWL}	20	—	20	—	20	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	

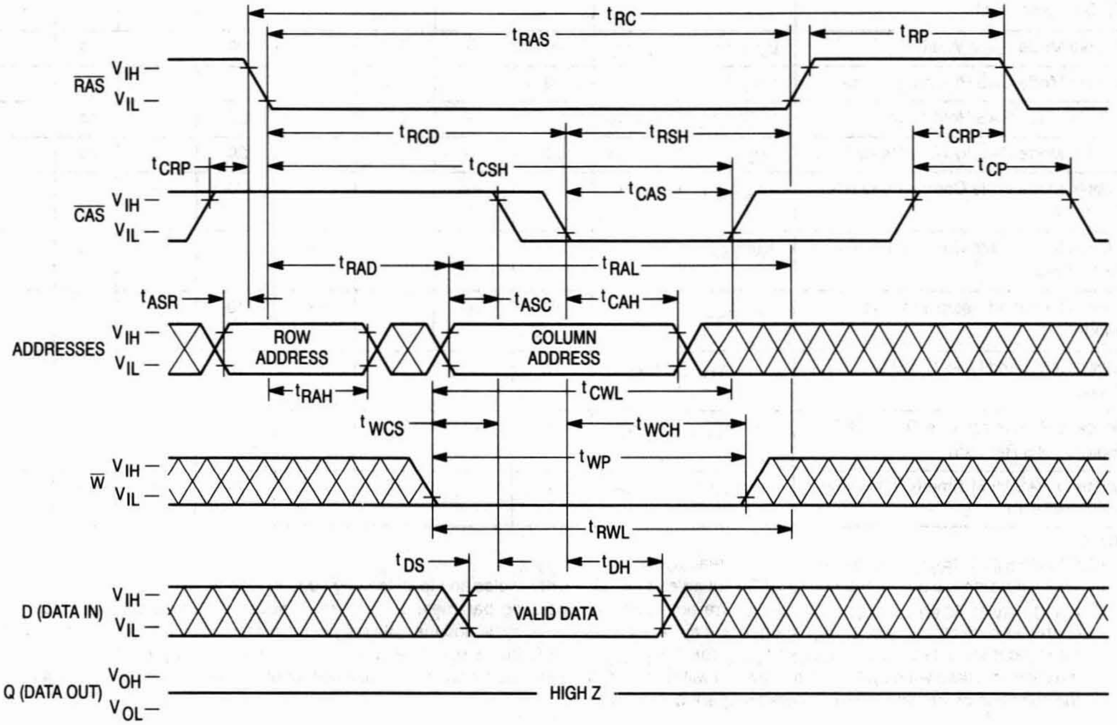
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

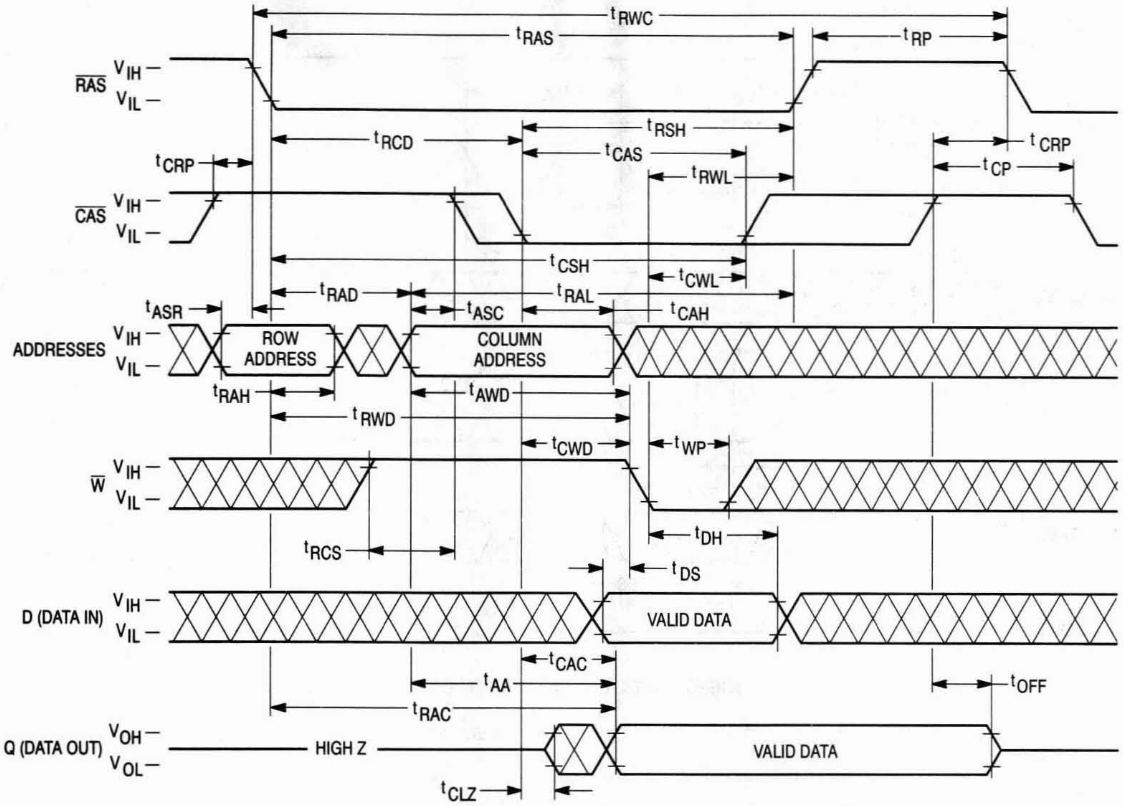
READ CYCLE


tRC
tRAS
tRP
RAS
VIH –
VIL –
tCSH
tCRP
tCRP
tRCD
tRSH
tCP
tCAS
CAS
VIH –
VIL –
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W
VIH –
VIL –
tCAC
tAA
tCLZ
tOFF
tRAC
Q (DATA OUT)
VOH –
VOL –
HIGH Z
VALID DATA

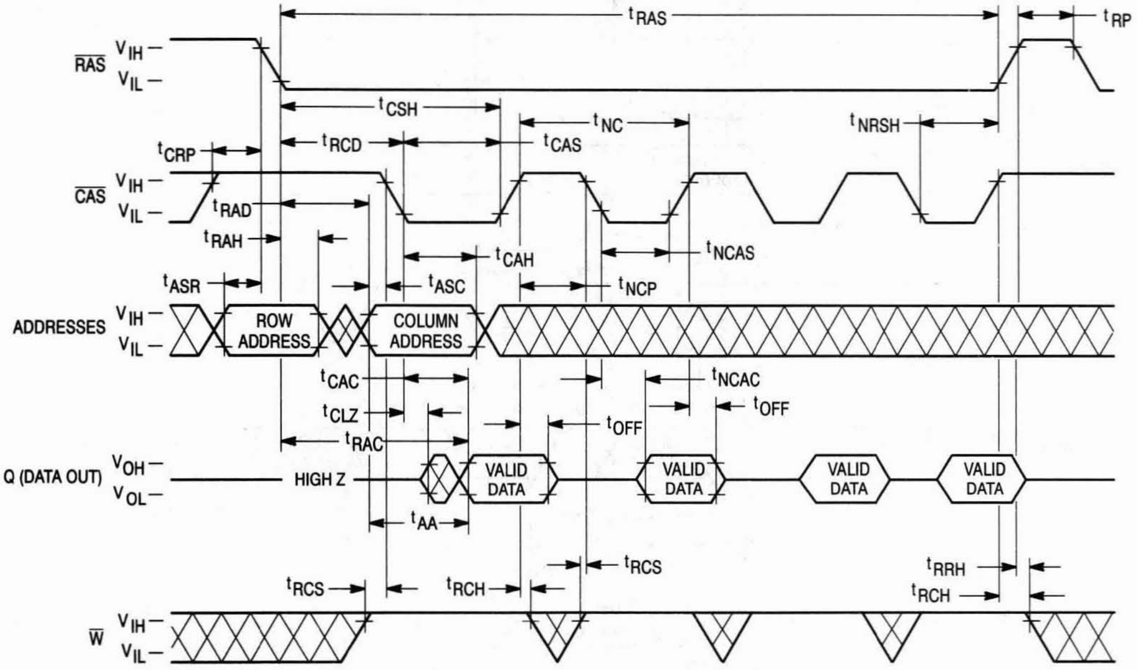
EARLY WRITE CYCLE


tRC
tRAS
tRP
RAS
VIH –
VIL –
tRCD
tRSH
tCRP
tCRP
tCSH
tCP
tCAS
CAS
VIH –
VIL –
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWP
W
VIH –
VIL –
tRWL
tDS
tDH
D (DATA IN)
VIH –
VIL –
VALID DATA
Q (DATA OUT)
VOH –
VOL –
HIGH Z

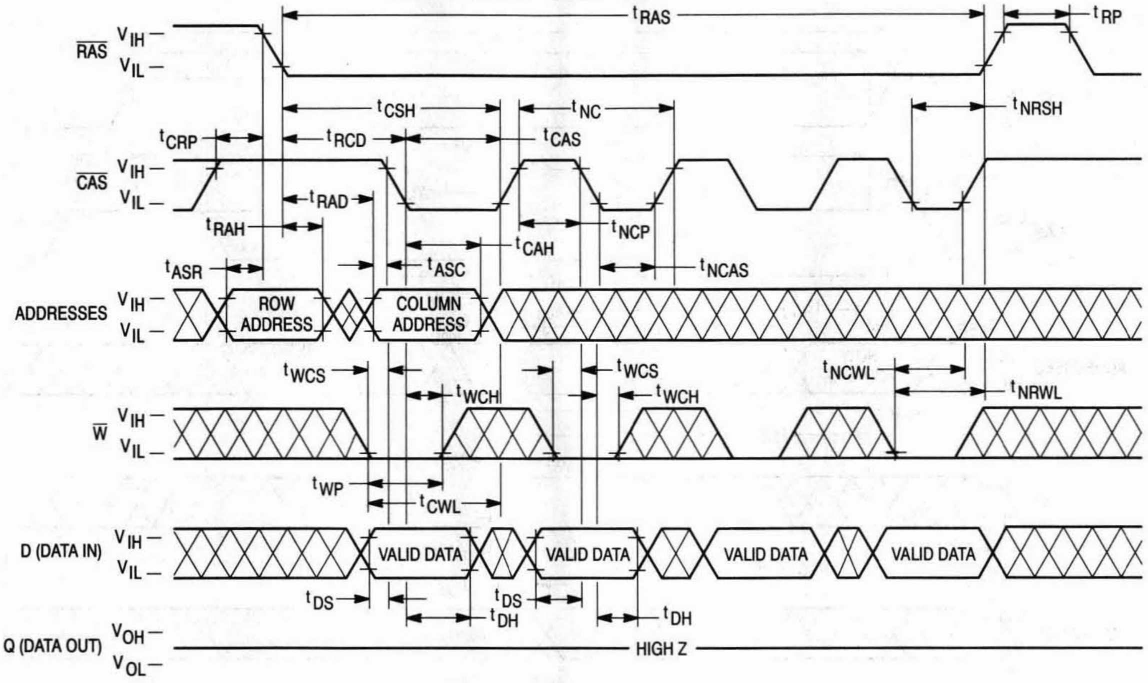
READ-WRITE CYCLE


t_{RWC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RCD}
t_{RSH}
t_{CAS}
t_{CRP}
t_{CP}
t_{RWL}
$\overline{CAS}$
t_{CSH}
t_{CWL}
t_{ASR}
t_{RAD}
t_{RAL}
t_{ASC}
t_{CAH}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{RAH}
t_{AWD}
t_{RWD}
t_{CWD}
t_{WP}
$\overline{W}$
t_{RCS}
t_{DH}
t_{DS}
D (DATA IN)
VALID DATA
t_{CAC}
t_{AA}
t_{RAC}
t_{OFF}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z
VALID DATA
t_{CLZ}

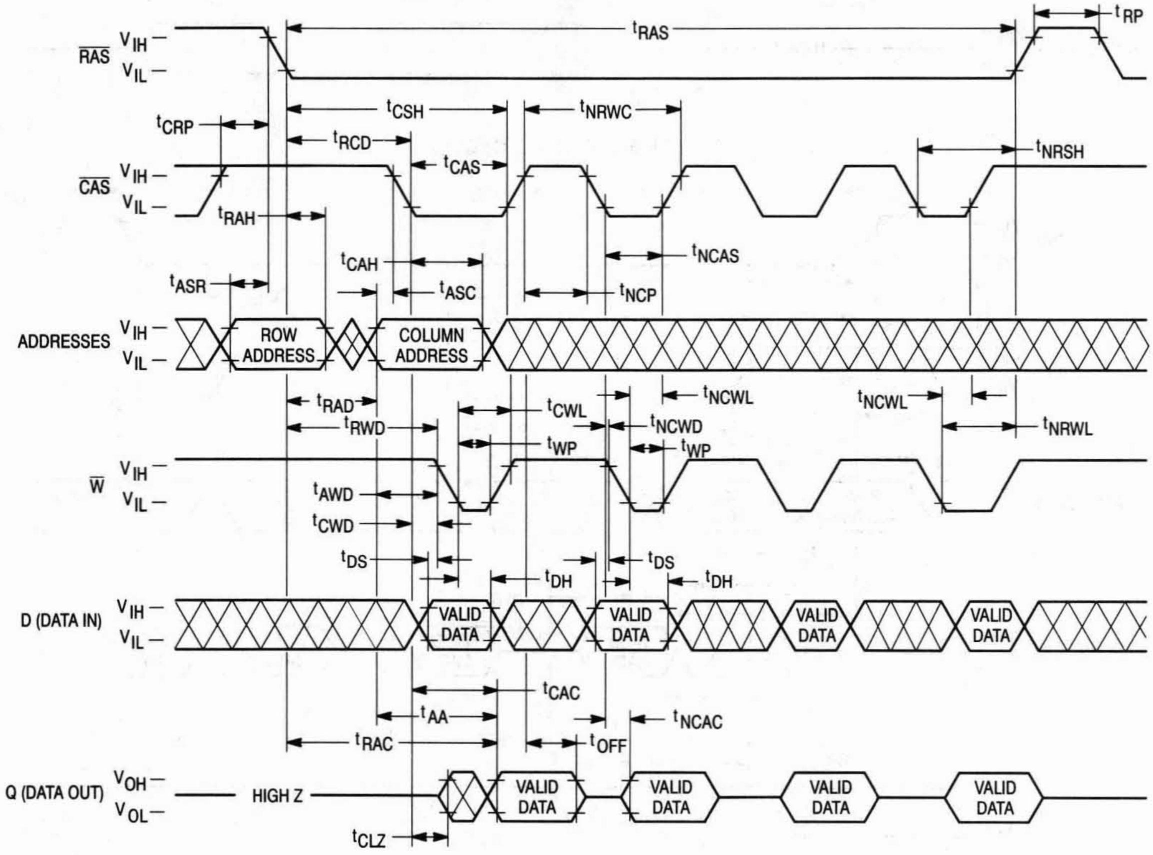
NIBBLE MODE READ CYCLE


t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{NC}
t_{NRSH}
t_{CRP}
t_{RCD}
t_{CAS}
$\overline{CAS}$
t_{RAD}
t_{RAH}
t_{CAH}
t_{NCAS}
t_{ASR}
t_{ASC}
t_{NCP}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{CAC}
t_{NCAC}
t_{CLZ}
t_{OFF}
t_{OFF}
t_{RAC}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z
VALID DATA
VALID DATA
VALID DATA
VALID DATA
t_{AA}
t_{RCS}
t_{RRH}
t_{RCS}
t_{RCH}
t_{RCH}
$\overline{W}$

NIBBLE MODE EARLY WRITE CYCLE

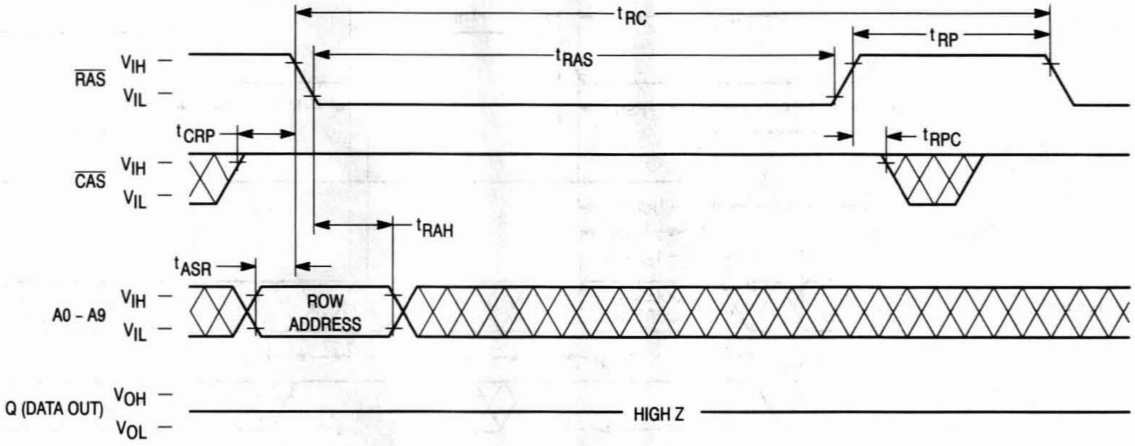

RAS
VIH
VIL
tRAS
tRP
tCSH
tNC
tNRSH
tCRP
tRCD
tCAS
CAS
tRAD
tRAH
tCAH
tNCP
tASR
tASC
tNCAS
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tWCS
tWCS
tNCWL
tWCH
tWCH
tNRWL
W
tWP
tCWL
D (DATA IN)
VALID DATA
VALID DATA
VALID DATA
VALID DATA
tDS
tDS
tDH
tDH
Q (DATA OUT)
VOH
VOL
HIGH Z

NIBBLE MODE READ-WRITE CYCLE


RAS
VIH
VIL
tRAS
tRP
tCSH
tNRWC
tCRP
tRCD
tCAS
tNRSH
CAS
tRAH
tNCAS
tCAH
tASC
tASR
tNCP
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tRAD
tRWD
tCWL
tNCWD
tNCWL
tNCWL
tNRWL
tWP
tWP
W
tAWD
tCWD
tDS
tDS
tDH
tDH
D (DATA IN)
VALID DATA
VALID DATA
VALID DATA
VALID DATA
tCAC
tAA
tNCAC
tRAC
tOFF
Q (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA
VALID DATA
VALID DATA
VALID DATA
tCLZ

$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

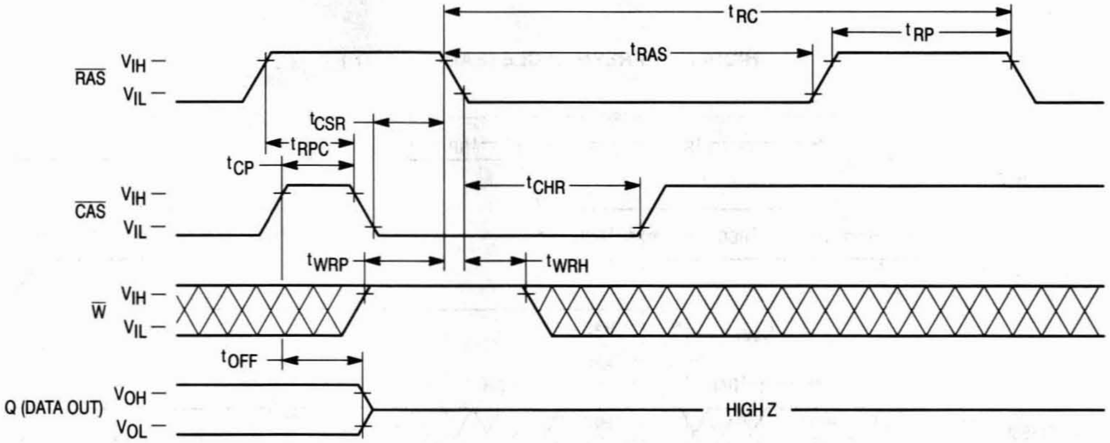
($\overline{\text{W}}$ and A10 are Don't Care)



t_RC
t_RP
$\overline{\text{RAS}}$
V_IH
V_IL
t_RAS
t_CRP
t_RPC
$\overline{\text{CAS}}$
V_IH
V_IL
t_RAH
t_ASR
A0 - A9
V_IH
V_IL
ROW ADDRESS
Q (DATA OUT)
V_OH
V_OL
HIGH Z

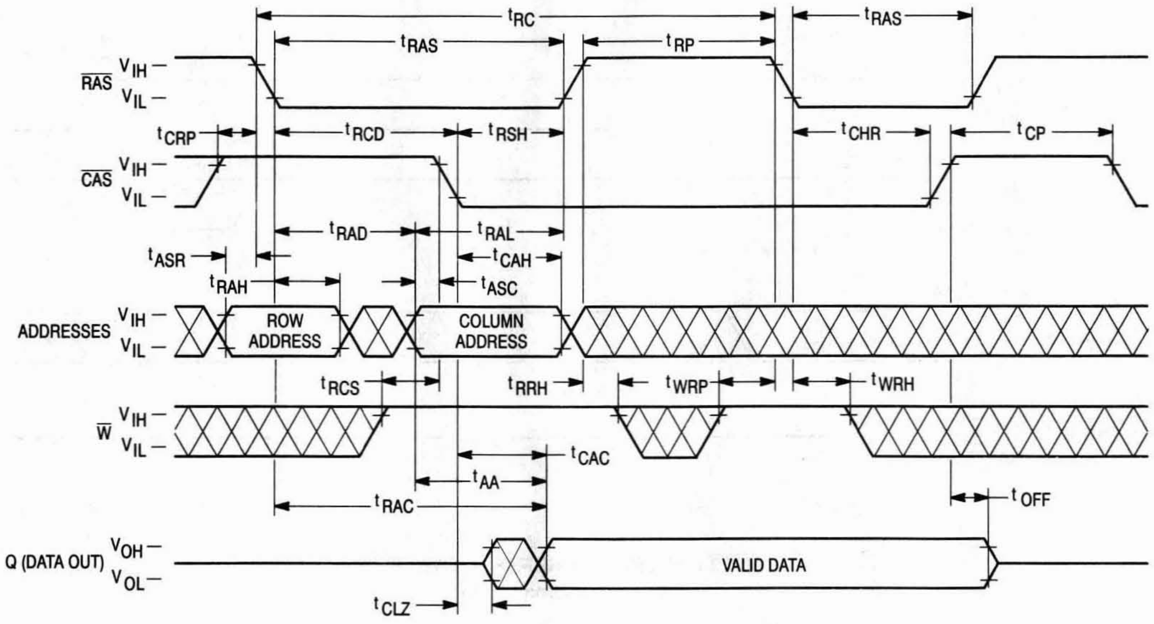
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

(A0 – A10 are Don't Care)

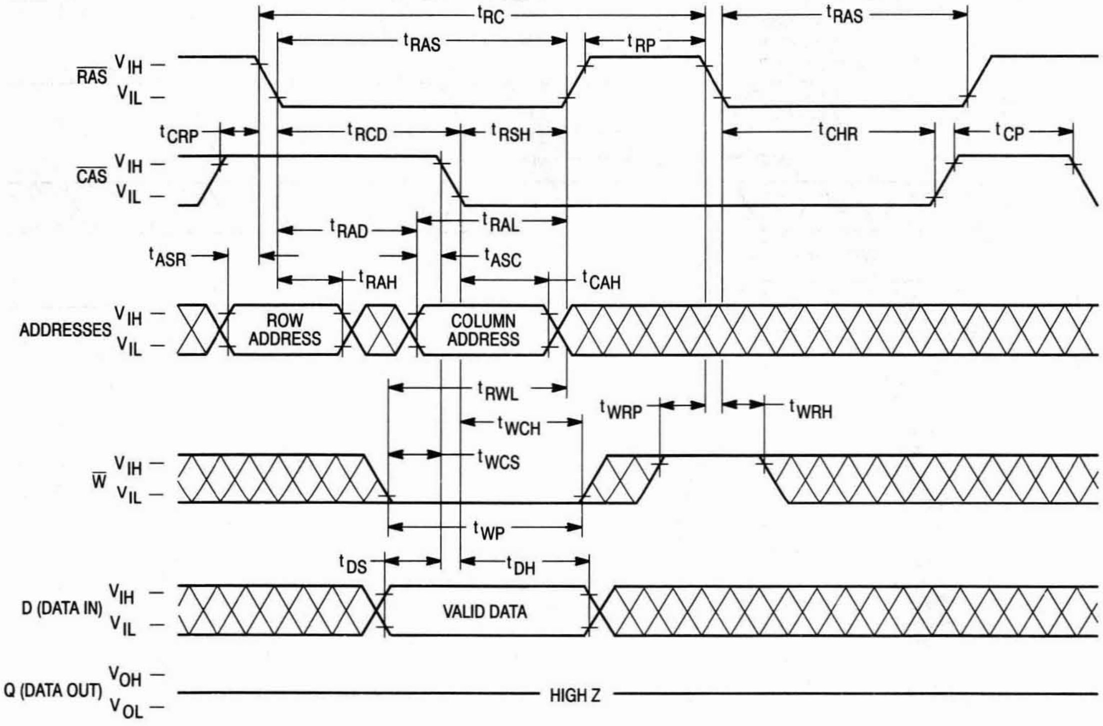


t_RC
t_RP
t_RAS
$\overline{\text{RAS}}$
V_IH
V_IL
t_CSR
t_RPC
t_CP
t_CHR
$\overline{\text{CAS}}$
V_IH
V_IL
t_WRP
t_WRH
$\overline{\text{W}}$
V_IH
V_IL
t_OFF
Q (DATA OUT)
V_OH
V_OL
HIGH Z

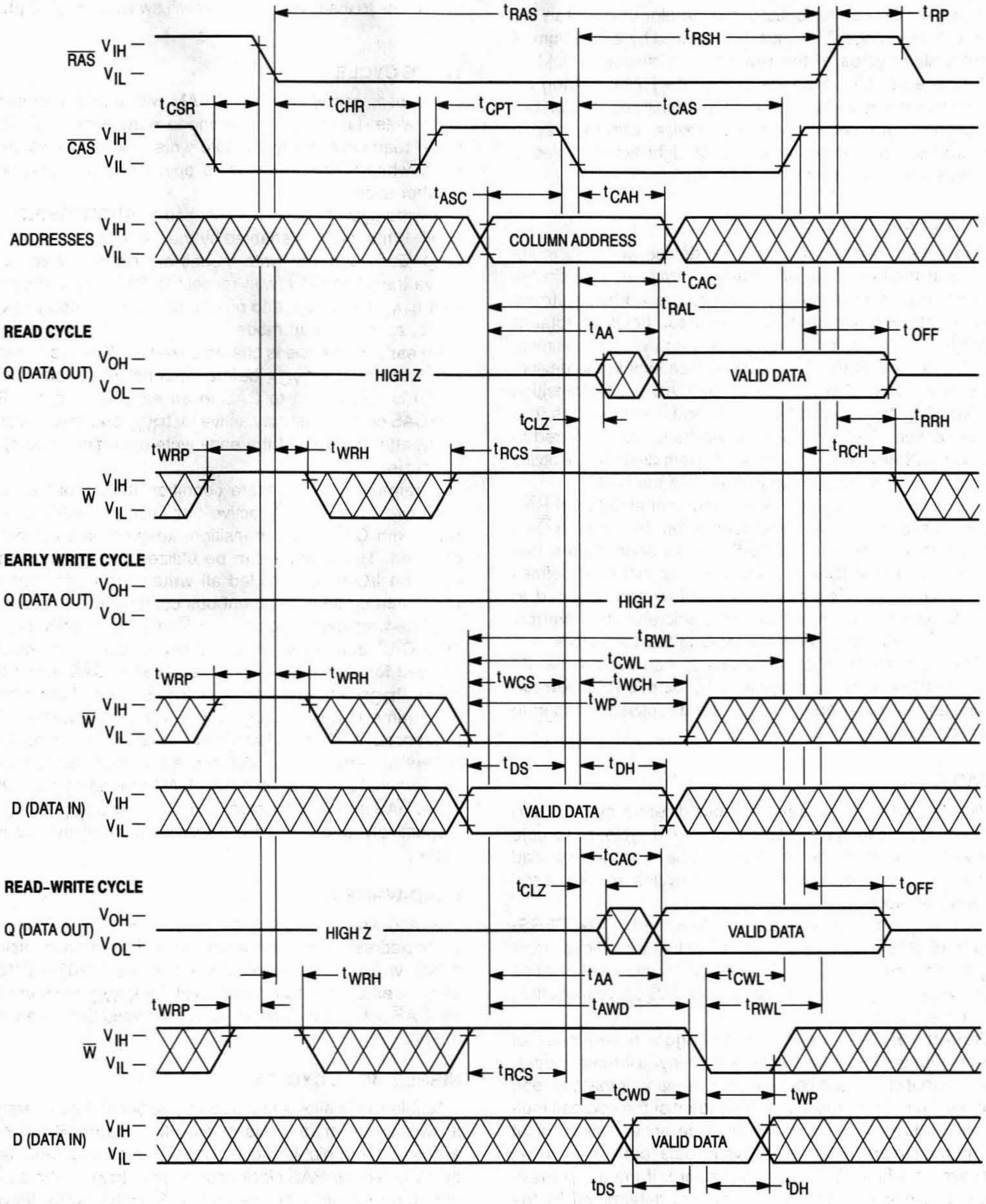
HIDDEN REFRESH CYCLE (READ)


t_RC
t_RAS
t_RAS
t_RP
RAS
V_IH
V_IL
t_CRP
t_RCD
t_RSH
t_CHR
t_CP
CAS
V_IH
V_IL
t_RAD
t_RAL
t_ASR
t_CAH
t_RAH
t_ASC
ADDRESSES
V_IH
V_IL
ROW ADDRESS
COLUMN ADDRESS
t_RCS
t_RRH
t_WRP
t_WRH
W
V_IH
V_IL
t_CAC
t_AA
t_RAC
t_OFF
Q (DATA OUT)
V_OH
V_OL
VALID DATA
t_CLZ

HIDDEN REFRESH CYCLE (EARLY WRITE)


t_RC
t_RAS
t_RAS
t_RP
RAS
V_IH
V_IL
t_CRP
t_RCD
t_RSH
t_CHR
t_CP
CAS
V_IH
V_IL
t_RAD
t_RAL
t_ASR
t_ASC
t_RAH
t_CAH
ADDRESSES
V_IH
V_IL
ROW ADDRESS
COLUMN ADDRESS
t_RWL
t_WRP
t_WRH
t_WCH
t_WCS
W
V_IH
V_IL
t_WP
t_DS
t_DH
D (DATA IN)
V_IH
V_IL
VALID DATA
Q (DATA OUT)
V_OH
V_OL
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE


tRAS
tRP
tRSH
RAS VIH VIL
tCSR
tCHR
tCPT
tCAS
CAS VIH VIL
tASC
tCAH
ADDRESSES VIH VIL
COLUMN ADDRESS
tCAC
tRAL
READ CYCLE
tAA
tOFF
Q (DATA OUT) VOH VOL
HIGH Z
VALID DATA
tCLZ
tRRH
tWRP
tWRH
tRCS
tRCH
W VIH VIL
EARLY WRITE CYCLE
Q (DATA OUT) VOH VOL
HIGH Z
tRWL
tCWL
tWRP
tWRH
tWCS
tWCH
tWP
W VIH VIL
tDS
tDH
D (DATA IN) VIH VIL
VALID DATA
READ-WRITE CYCLE
tCAC
tCLZ
tOFF
Q (DATA OUT) VOH VOL
HIGH Z
VALID DATA
tWRH
tAA
tCWL
tWRP
tAWD
tRWL
W VIH VIL
tRCS
tCWD
tWP
D (DATA IN) VIH VIL
VALID DATA
tDS
tDH

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds or 128 milliseconds in case of low power device, with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 11-bit address fields. A total of twenty-two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 bit locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the 4M RAM: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **nibble mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, nibble mode read cycle, read-write cycle, and nibble mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window; however, $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ clock active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, nibble mode early write, and nibble mode read-write. Early and late write modes are discussed here, while nibble mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_{T}) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_{T}) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but Q may be indeterminate — see note 15 of AC Operating Conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

NIBBLE MODE CYCLES

Nibble mode allows fast successive serial data operations at two, three, or four bits of the 4M dynamic RAM. Read access time in nibble mode (t_{NCAC}) is considerably faster than the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Nibble mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The address of the first nibble bit is latched by $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions. Each subsequent $\overline{\text{CAS}}$ active transition increments the row and column addresses internally to access the next bit in binary fashion. After the fourth bit is accessed, the nibble pattern repeats itself (0,0) (0,1) (1,0) (1,1) (0,0) (0,1) (1,0) (1,1). . . . The A10 address determines the starting point of the 4-bit nibble, with row address A10 the least significant of the (column, row) ordered pair. External addresses are ignored after the first nibble bit is selected.

A nibble mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum of t_{NCP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first nibble mode cycle (t_{NC} or t_{NRWC}). Either a read, write, or read-write operation can be performed in a nibble mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive nibble mode cycles and performed in any order. The maximum number of consecutive nibble mode cycles is limited by t_{RAS}. Nibble mode operation ends when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following a $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54101A require refresh every 16 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54101A. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54101A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle.

The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{\text{RAS}}$ active transition to prevent switching the device into **test mode**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode) as in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of 8 **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

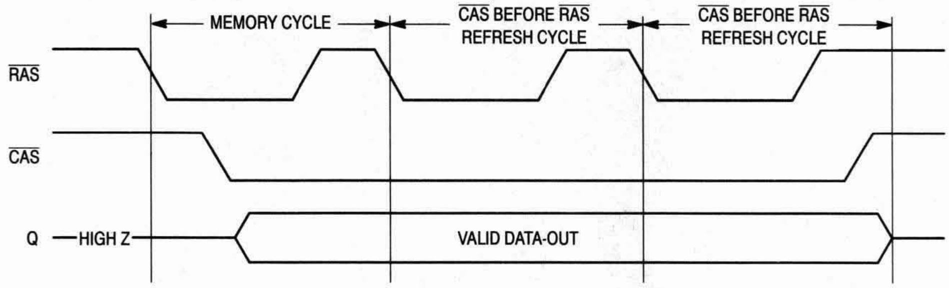


Figure 1. Hidden Refresh Cycle

TEST MODE

The internal organization of this device (512K x 8) allows it to be tested as if it were a 512K x 1 DRAM. Nineteen of the twenty-two addresses are used when operating the device in test mode. Row address A10, and column addresses A0 and A10 are ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0 – B7) in parallel. External data out is determined by the internal test mode logic of the device. See the following truth table and test mode block diagram.

$\overline{\text{W}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ timing puts the device in **Test Mode** as shown in the test mode timing diagram. A **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** or a **$\overline{\text{RAS}}$-only refresh cycle** puts the device back into normal mode. Refresh is performed in test mode by using a **$\overline{\text{W}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle** which uses internal refresh address counter.

TEST MODE TRUTH TABLE

D	B0	B1	B2	B3	B4	B5	B6	B7	Q
0	0	0	0	0	0	0	0	0	1
1	1	1	1	1	1	1	1	1	1
—	Any Other								0

TEST MODE
AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

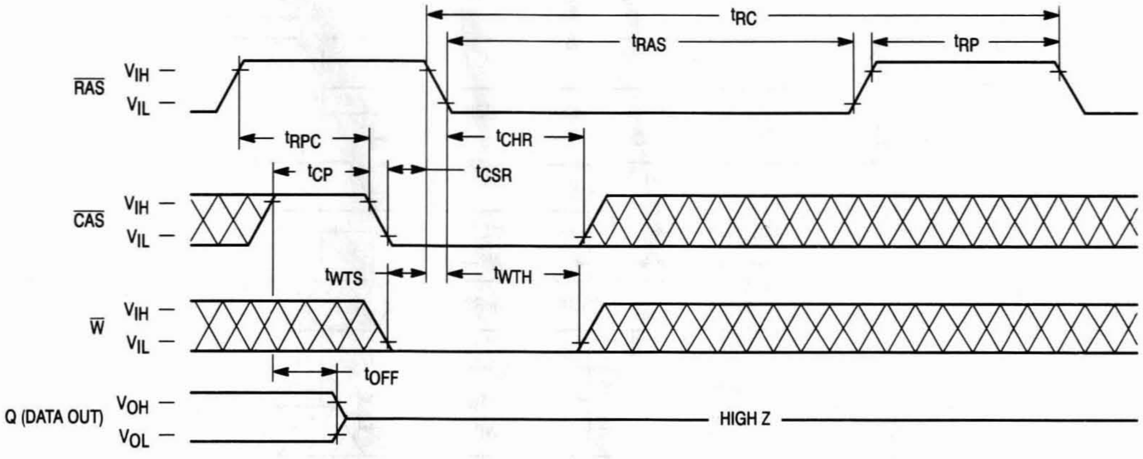
Parameter	Symbol		MCM54101A-60		MCM54101A-70		MCM54101A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	115	—	135	—	155	—	ns	5
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	65	—	75	—	85	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	25	—	25	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	45	ns	6, 9
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	65	10 k	75	10 k	85	10 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	25	—	25	—	25	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	65	—	75	—	85	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	25	10 k	25	10 k	25	10 k	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	45	—	ns	

NOTES:

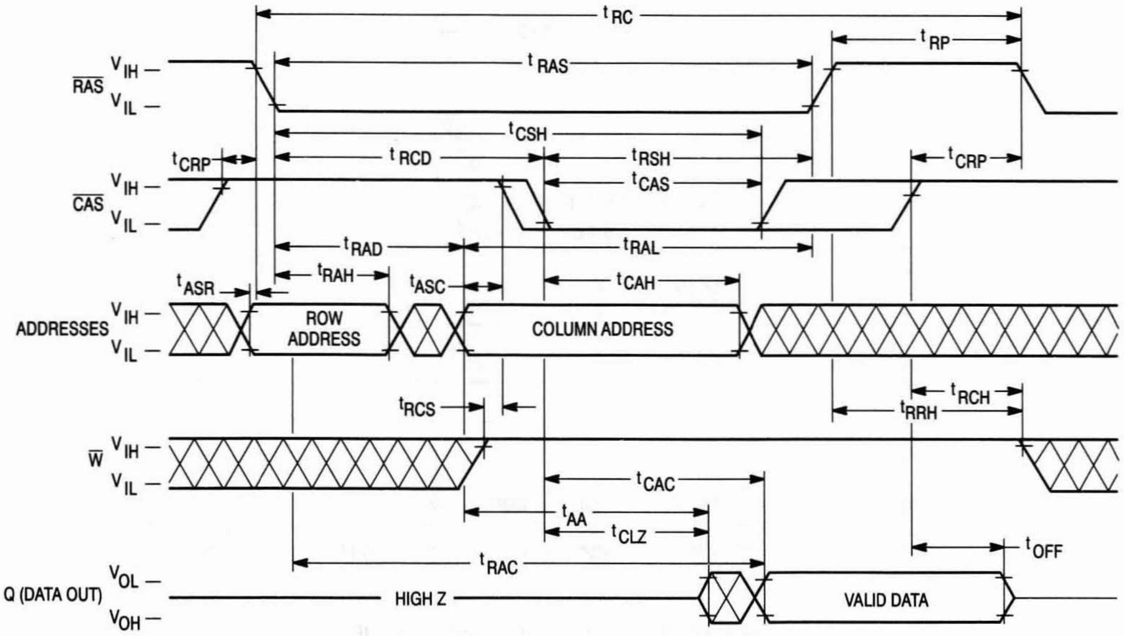
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).

W, CAS BEFORE RAS REFRESH CYCLE (TEST MODE ENTRY)

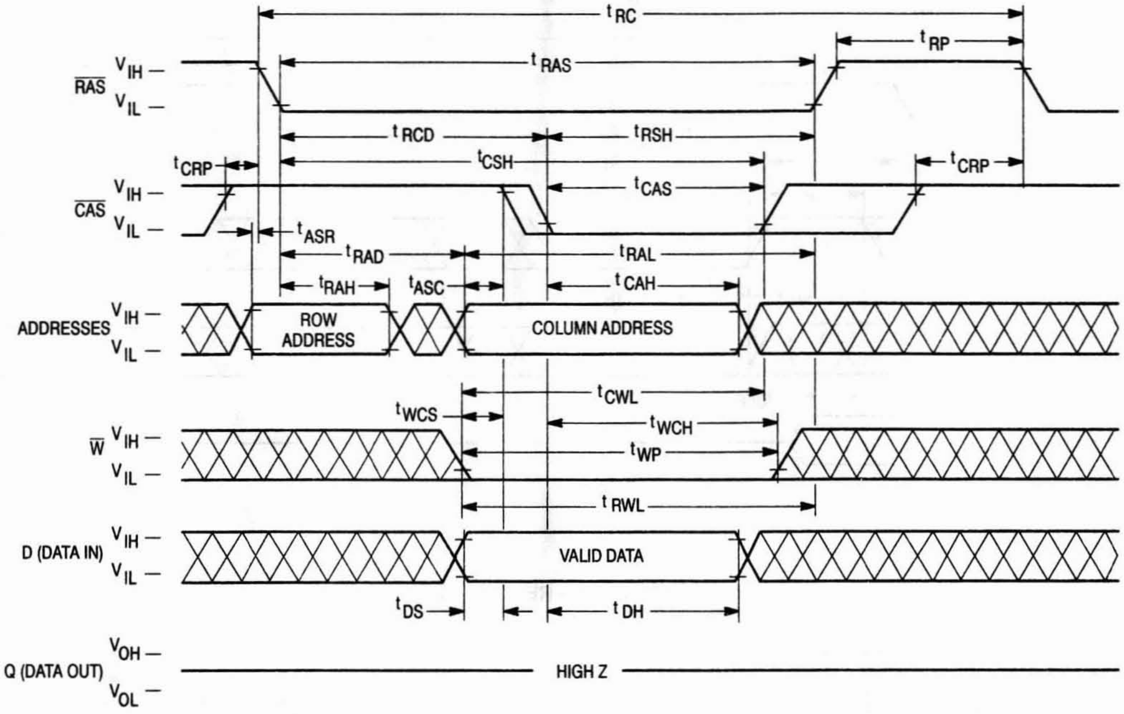
(D and A0 – A10 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
RAS
V_{IH}
V_{IL}
t_{RPC}
t_{CHR}
t_{CP}
t_{CSR}
CAS
V_{IH}
V_{IL}
t_{WTS}
t_{WTH}
W
V_{IH}
V_{IL}
t_{OFF}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

TEST MODE — READ CYCLE


t_{RC}
t_{RP}
t_{RAS}
RAS
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
CAS
V_{IH}
V_{IL}
t_{RAD}
t_{RAL}
t_{RAH}
t_{ASR}
t_{ASC}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RCS}
t_{RCH}
t_{RRH}
W
V_{IH}
V_{IL}
t_{CAC}
t_{AA}
t_{CLZ}
t_{OFF}
t_{RAC}
Q (DATA OUT)
V_{OL}
V_{OH}
HIGH Z
VALID DATA

TEST MODE — EARLY WRITE CYCLE



tRC
tRP
tRAS
RAS VIH — VIL —
tRCD
tRSH
tCRP
tCSH
tCRP
CAS VIH — VIL —
tCAS
tASR
tRAD
tRAL
tRAH
tASC
tCAH
ADDRESSES VIH — VIL —
ROW ADDRESS
COLUMN ADDRESS
tCWL
tWCS
tWCH
W VIH — VIL —
tWP
tRWL
D (DATA IN) VIH — VIL —
VALID DATA
tDS
tDH
Q (DATA OUT) VOH — VOL —
HIGH Z

ORDERING INFORMATION

(Order by Full Part Number)

MCM 54101A X XX XX

Motorola Memory Prefix — MCM

Part Number — 54101A

Package (N = 300 mil SOJ, Z = 100 mil Plastic ZIP, T = 300 mil TSOP) — X

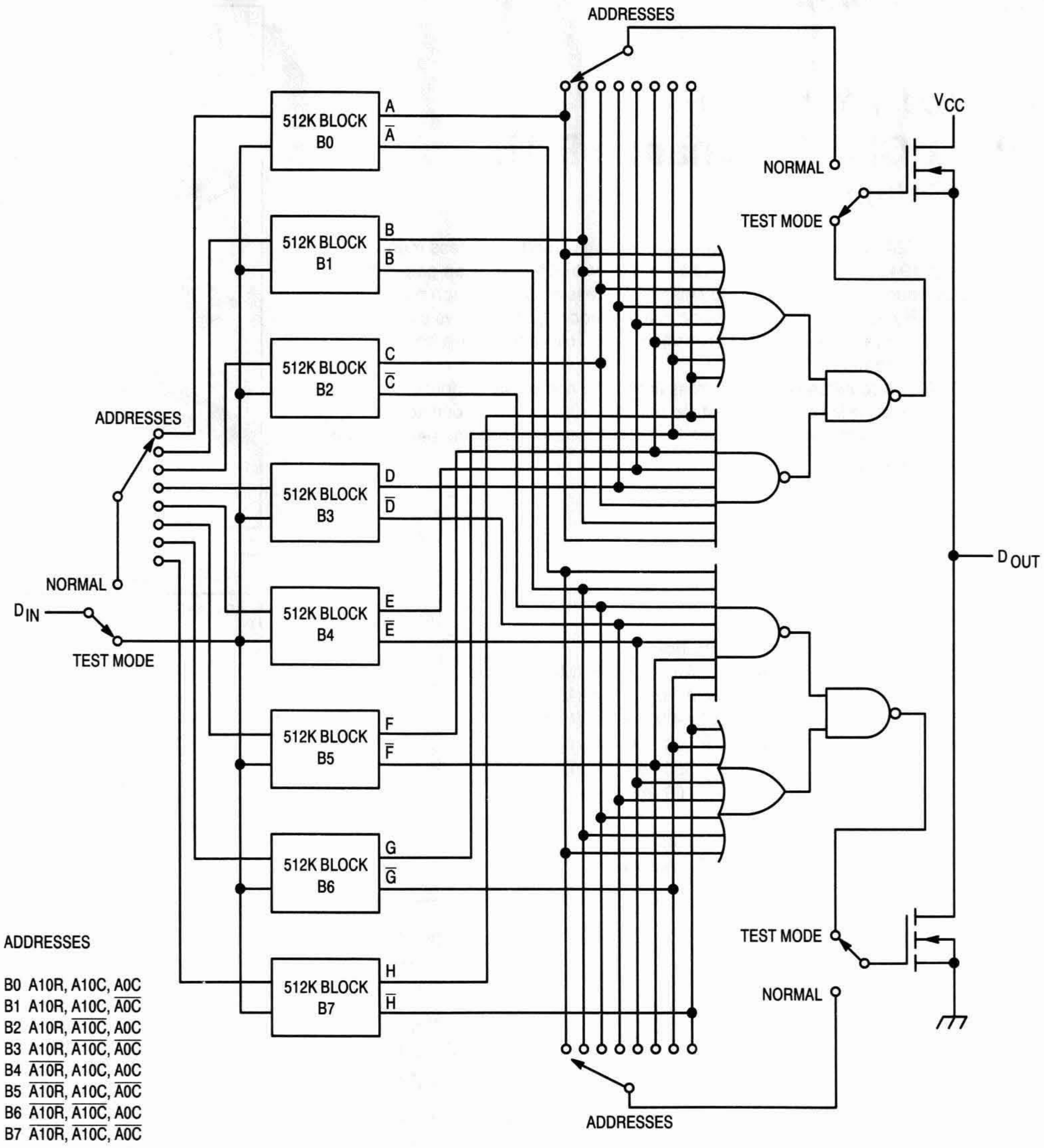
Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Shipping Method (R2 = Tape and Reel, Blank = Rails or Tray) — XX

Full Part Numbers —			
MCM54101AN60	MCM54101AN60R2	MCM54101AZ60	MCM54101AT60
MCM54101AN70	MCM54101AN70R2	MCM54101AZ70	MCM54101AT70
MCM54101AN80	MCM54101AN80R2	MCM54101AZ80	MCM54101AT80

NOTE: For mechanical data, please see Chapter 10.

TEST MODE BLOCK DIAGRAM


ADDRESSES
512K BLOCK B0
512K BLOCK B1
512K BLOCK B2
512K BLOCK B3
512K BLOCK B4
512K BLOCK B5
512K BLOCK B6
512K BLOCK B7
A
$\overline{A}$
B
$\overline{B}$
C
$\overline{C}$
D
$\overline{D}$
E
$\overline{E}$
F
$\overline{F}$
G
$\overline{G}$
H
$\overline{H}$
V_{CC}
NORMAL
TEST MODE
ADDRESSES
NORMAL
D_{IN}
TEST MODE
D_{OUT}
TEST MODE
NORMAL
ADDRESSES

ADDRESSES

B0 A10R, A10C, A0C
B1 A10R, A10C, $\overline{A0C}$
B2 A10R, $\overline{A10C}$, A0C
B3 A10R, $\overline{A10C}$, $\overline{A0C}$
B4 $\overline{A10R}$, A10C, A0C
B5 $\overline{A10R}$, A10C, $\overline{A0C}$
B6 $\overline{A10R}$, $\overline{A10C}$, A0C
B7 $\overline{A10R}$, $\overline{A10C}$, $\overline{A0C}$

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM54102A

Advance Information

4M x 1 CMOS Dynamic RAM

Static Column

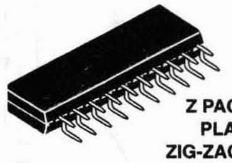
The MCM54102A is a 0.7μ CMOS high-speed dynamic random access memory. It is organized as 4,194,304 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The static column mode feature allows column data to be accessed upon the column address transition when $\overline{RAS}$ and $\overline{CS}$ are held low, similar to static RAM operation.

The MCM54102A requires only 11 address lines; row and column address inputs are multiplexed. The device is packaged in standard 300 mil J-lead small outline package, a 300 mil thin-small-outline package (TSOP), and a 100 mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Static Column Mode
- Test Mode
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM54102A = 16 ms
- Fast Access Time (t_{RAC}): MCM54102A-60 = 60 ns (Max)
  MCM54102A-70 = 70 ns (Max)
  MCM54102A-80 = 80 ns (Max)
- Low Active Power: MCM54102A-60 = 660 mW (Max)
  MCM54102A-70 = 550 mW (Max)
  MCM54102A-80 = 468 mW (Max)
- Low Standby Power Dissipation:
  MCM54102A = 11 mW (Max, TTL Levels)
  = 5.5 mW (Max, CMOS Levels)

N PACKAGE
300 MIL SOJ
CASE 822-03

T PACKAGE
300 MIL TSOP
CASE 892-01



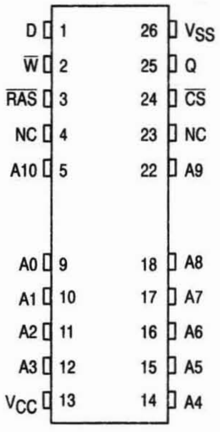
Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836-02

PIN NAMES

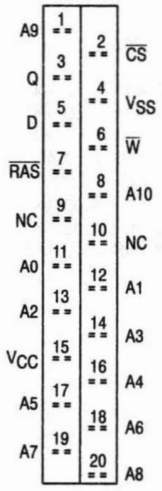
A0 – A10	Address Input
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENTS

300 MIL SOJ/TSOP

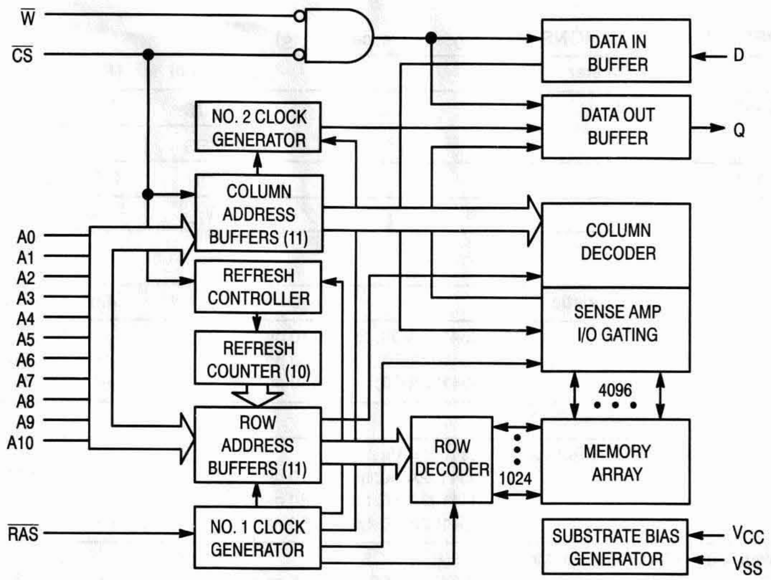


100 MIL ZIP



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM


W̄
CS̄
DATA IN BUFFER
D
DATA OUT BUFFER
Q
NO. 2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (11)
COLUMN DECODER
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
REFRESH CONTROLLER
SENSE AMP I/O GATING
REFRESH COUNTER (10)
4096
ROW ADDRESS BUFFERS (11)
ROW DECODER
1024
MEMORY ARRAY
RAS̄
NO. 1 CLOCK GENERATOR
SUBSTRATE BIAS GENERATOR
V_{CC}
V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM54102A-60, t_{RC} = 110 ns MCM54102A-70, t_{RC} = 130 ns MCM54102A-80, t_{RC} = 150 ns	I_{CC1}	— — —	120 100 85	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles ($\overline{CS}$ = V_{IH}) MCM54102A-60, t_{RC} = 110 ns MCM54102A-70, t_{RC} = 130 ns MCM54102A-80, t_{RC} = 150 ns	I_{CC3}	— — —	120 100 85	mA	1, 2
V_{CC} Power Supply Current During Static Column Mode Cycle ($\overline{RAS}$ = $\overline{CS}$ =V_{IL}) MCM54102A-60, t_{SC} = 35 ns MCM54102A-70, t_{SC} = 40 ns MCM54102A-80, t_{SC} = 45 ns	I_{CC4}	— — —	85 75 65	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle MCM54102A-60, t_{RC} = 110 ns MCM54102A-70, t_{RC} = 130 ns MCM54102A-80, t_{RC} = 150 ns	I_{CC6}	— — —	120 100 85	mA	1
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current ($\overline{CS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CS}$ = V_{IH}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A10, D	C_{in}	5	pF
	$\overline{RAS}$, $\overline{CS}$, $\overline{W}$		7	
I/O Capacitance ($\overline{CS}$ = V_{IH} to Disable Output)	Q	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM54102A-60		MCM54102A-70		MCM54102A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	135	—	155	—	175	—	ns	5
Static Column Mode Cycle Time	t_{AVAV}	t_{SC}	35	—	40	—	45	—	ns	
Static Column Mode Read-Write Cycle Time	t_{AVAV}	t_{SRWC}	60	—	70	—	80	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6, 9
Access Time from Last Write	t_{WLQV}	t_{ALW}	—	55	—	65	—	75	ns	6, 10
$\overline{\text{CS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	11
Data Out Hold from Address Change	t_{AXQX}	t_{AOH}	5	—	5	—	5	—	ns	
Data Out Enable from Write	t_{WHQV}	t_{OW}	—	20	—	20	—	20	ns	
Data Out Hold from Write	t_{WHQX}	t_{WOH}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Static Column Mode)	t_{RELREH}	t_{RASC}	60	200 k	70	200 k	80	200 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{\text{CS}}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CS}}$ Pulse Width	t_{CELCEH}	t_{CS}	20	10 k	20	10 k	20	10 k	ns	
$\overline{\text{CS}}$ Pulse Width (Static Column Mode)	t_{CELCEH}	t_{CSC}	20	200 k	20	200 k	20	200 k	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	12
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	13
$\overline{\text{CS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{CS}}$ Precharge Time (Static Column Mode)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. Assumes that $t_{LWAD} \ge t_{LWAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM54102A-60		MCM54102A-70		MCM54102A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$ (Read Cycle)	t_{RELAX}	t_{AR}	70	—	80	—	90	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Column Address Hold Time Reference to $\overline{\text{RAS}}$ High	t_{REHAX}	t_{AH}	5	—	5	—	5	—	ns	14
Write Command to $\overline{\text{CS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Last Write to Column Address Delay Time	t_{WLAV}	t_{LWAD}	20	25	20	30	20	35	ns	15
Last Write to Column Address Hold Time	t_{WLAX}	t_{AHLW}	55	—	65	—	75	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	16
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	16
Write Command Hold Time Referenced to $\overline{\text{CS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command Inactive Time	t_{WHWL}	t_{WI}	10	—	10	—	10	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	17
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	17
Refresh Period	t_{RVRV}	t_{RFSH}	—	16	—	16	—	16	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	18
$\overline{\text{CS}}$ to Write Delay	t_{CELWL}	t_{CWD}	20	—	20	—	20	—	ns	18
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	60	—	70	—	80	—	ns	18
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	30	—	35	—	40	—	ns	18
$\overline{\text{CS}}$ Setup Time for $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CS}}$ Hold Time for $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	

NOTES:

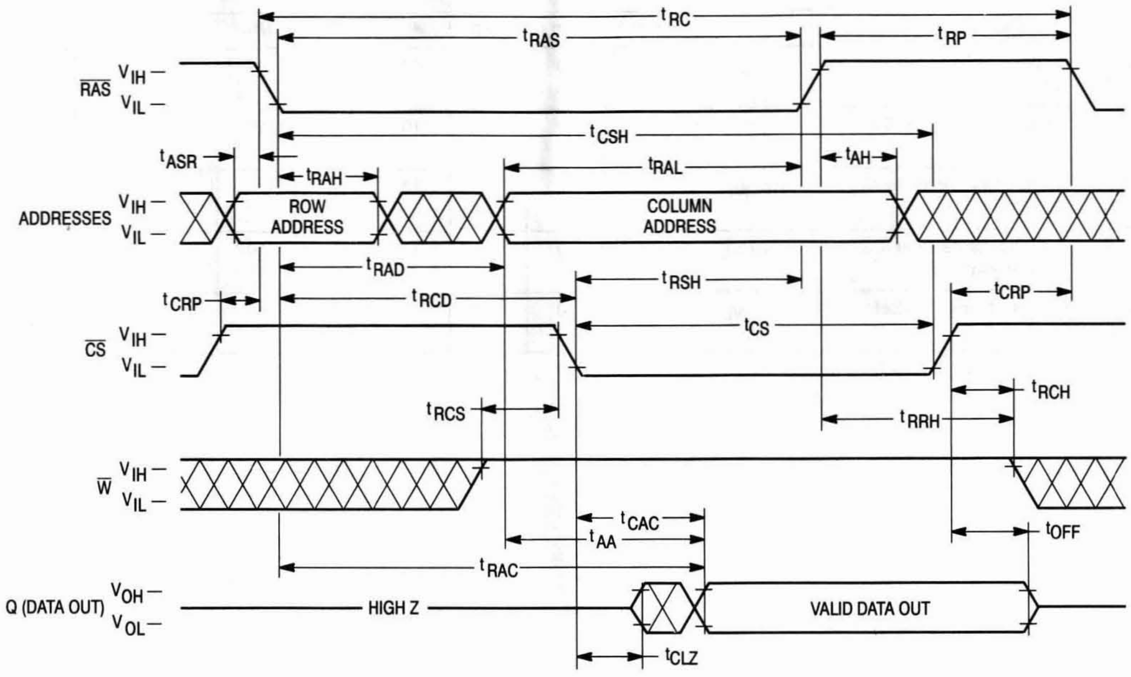
(continued)

14. t_{AH} must be met for a read cycle.
15. Operation within the t_{LWAD} (max) limit ensures that t_{ALW} can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
17. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in read-write cycles.
18. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

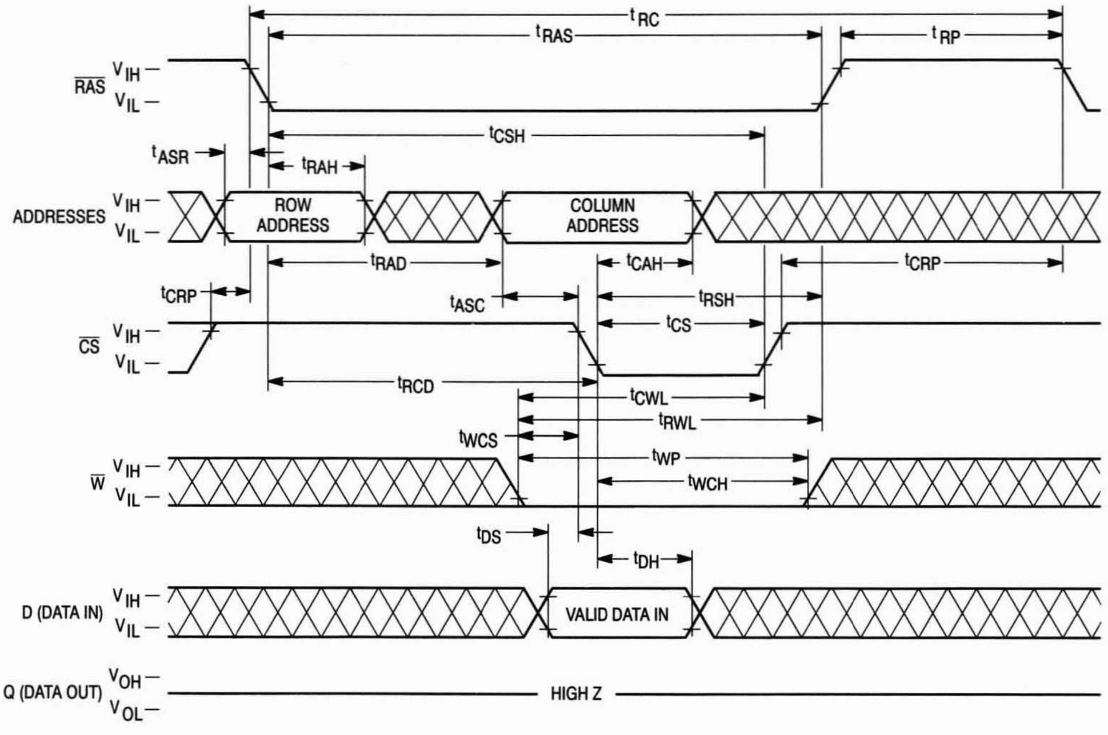
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM54102A-60		MCM54102A-70		MCM54102A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{\text{CS}}$ Precharge Time for $\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Hold Time ($\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	

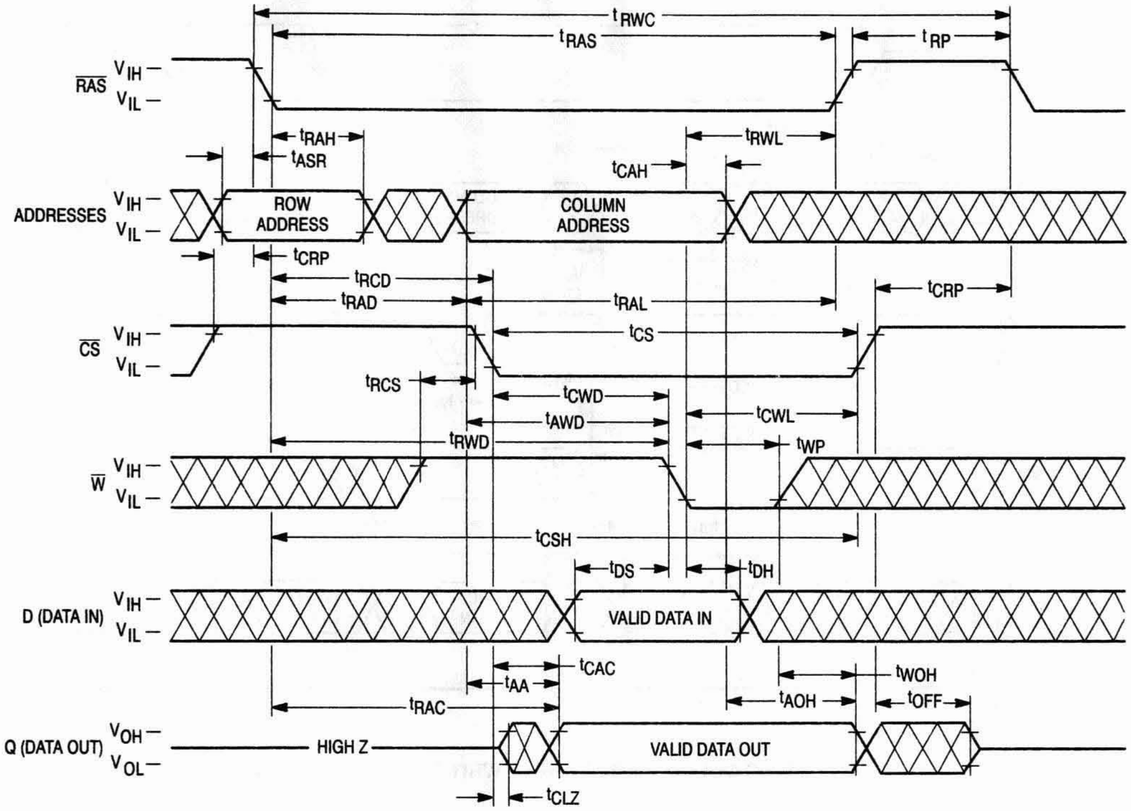
READ CYCLE


tRC
tRAS
tRP
RAS
VIH —
VIL —
tCSH
tASR
tRAH
tRAL
tAH
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tRAD
tRSH
tRCD
tCRP
tCRP
CS
tCS
tRCS
tRCH
tRRH
W
tCAC
tAA
tOFF
tRAC
Q (DATA OUT)
VOH —
VOL —
HIGH Z
VALID DATA OUT
tCLZ

EARLY WRITE CYCLE

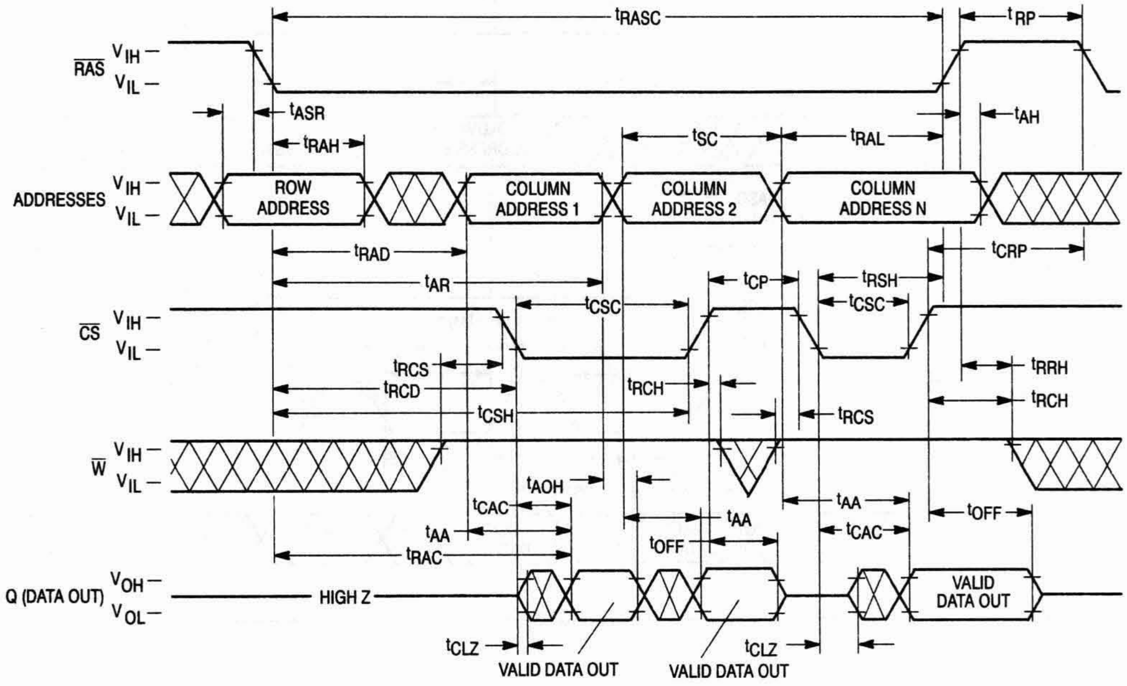

tRC
tRAS
tRP
RAS
VIH —
VIL —
tCSH
tASR
tRAH
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tRAD
tCAH
tCRP
tCRP
tASC
tRSH
CS
tCS
tRCD
tCWL
tRWL
tWCS
tWP
W
tWCH
tDS
tDH
D (DATA IN)
VALID DATA IN
Q (DATA OUT)
VOH —
VOL —
HIGH Z

READ-WRITE CYCLE



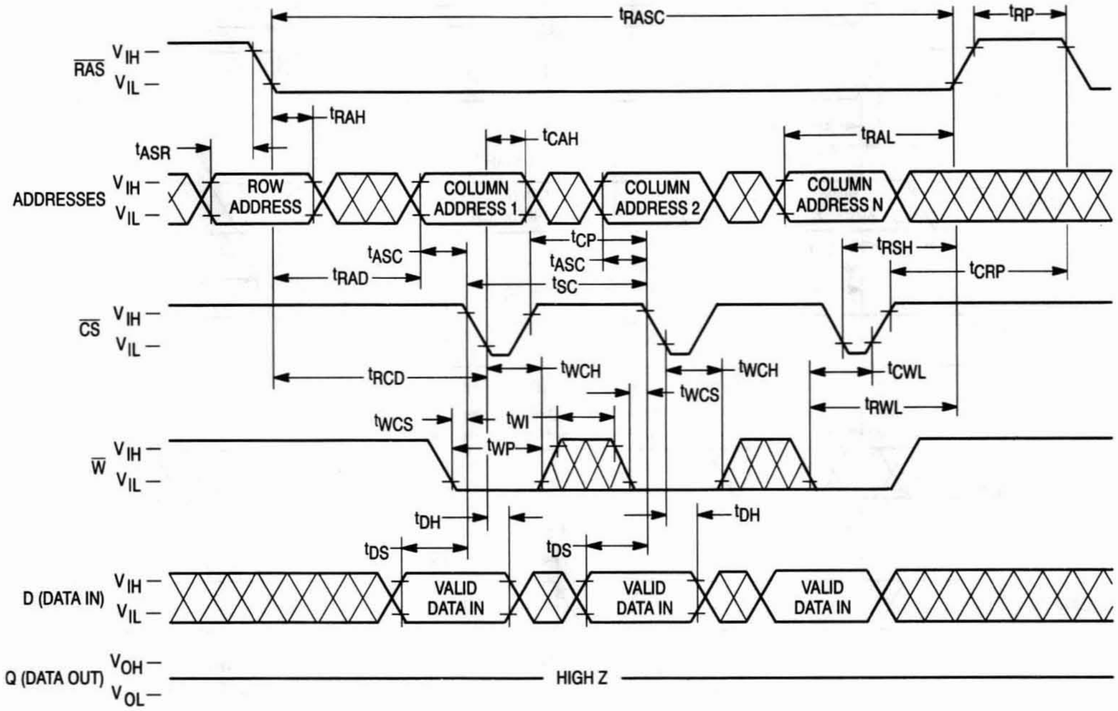
t RWC
t RAS
t RP
RAS
V IH –
V IL –
t RAH
t ASR
t RWL
t CAH
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t CRP
t RCD
t RAD
t RAL
t CRP
CS
t CS
t RCS
t CWD
t AWD
t CWL
t RWD
t WP
W
t CSH
t DS
t DH
D (DATA IN)
VALID DATA IN
t CAC
t AA
t RAC
t WOH
t AOH
t OFF
Q (DATA OUT)
V OH –
V OL –
HIGH Z
VALID DATA OUT
t CLZ

STATIC COLUMN MODE READ CYCLE

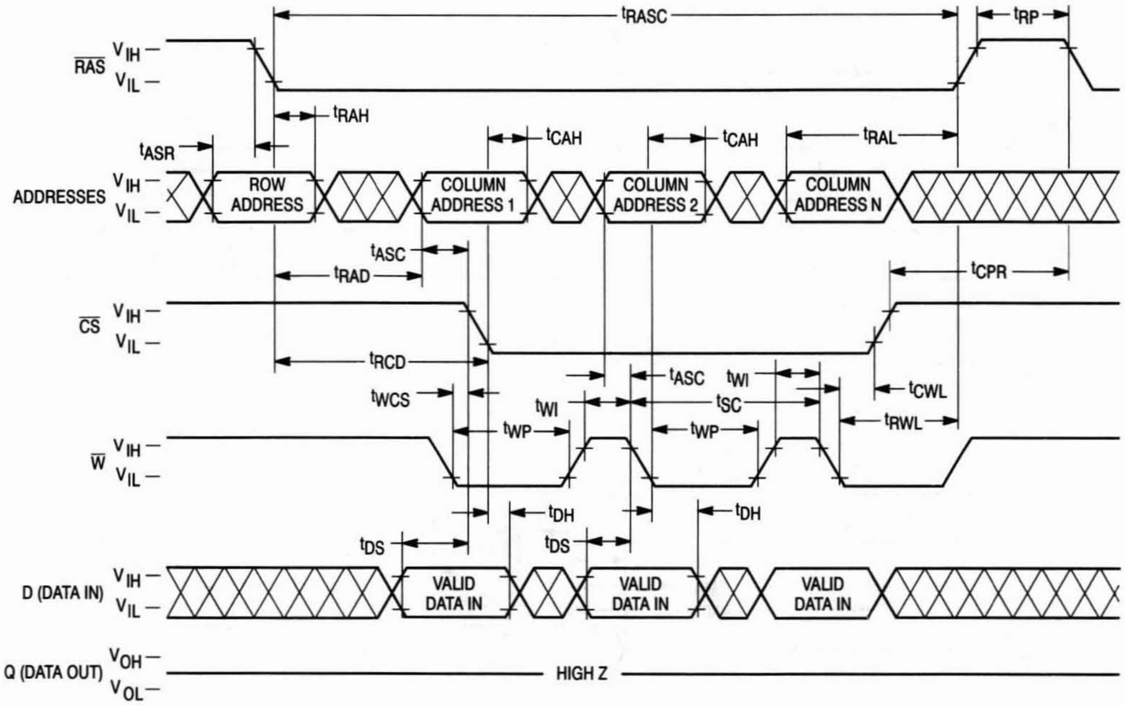


t RASC
t RP
RAS
V IH –
V IL –
t ASR
t AH
t RAH
t SC
t RAL
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS N
t RAD
t CRP
t AR
t CP
t RSH
CS
t CSC
t CSC
t RCS
t RRH
t RCD
t RCH
t RCH
t CSH
t RCS
W
t AOH
t CAC
t AA
t AA
t AA
t OFF
t CAC
t OFF
t RAC
Q (DATA OUT)
V OH –
V OL –
HIGH Z
VALID DATA OUT
t CLZ
t CLZ
VALID DATA OUT
VALID DATA OUT

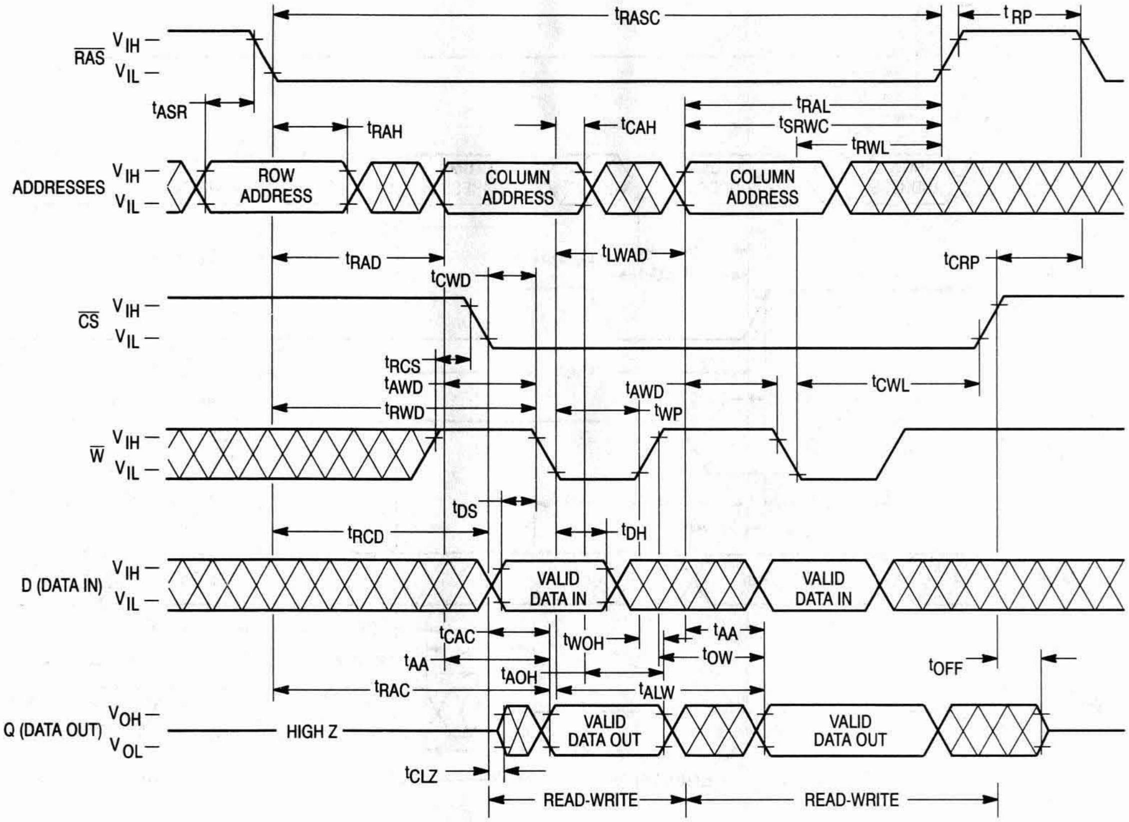
STATIC COLUMN MODE EARLY WRITE CYCLE (A)


t_{RASC}
t_{RP}
RAS
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
t_{CAH}
t_{RAL}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS N
t_{CP}
t_{ASC}
t_{ASC}
t_{RSH}
t_{RAD}
t_{SC}
t_{CRP}
CS
t_{RCD}
t_{WCH}
t_{WCH}
t_{CWL}
t_{WCS}
t_{WCS}
t_{WI}
t_{RWL}
t_{WP}
W
t_{DH}
t_{DH}
t_{DS}
t_{DS}
D (DATA IN)
VALID DATA IN
VALID DATA IN
VALID DATA IN
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

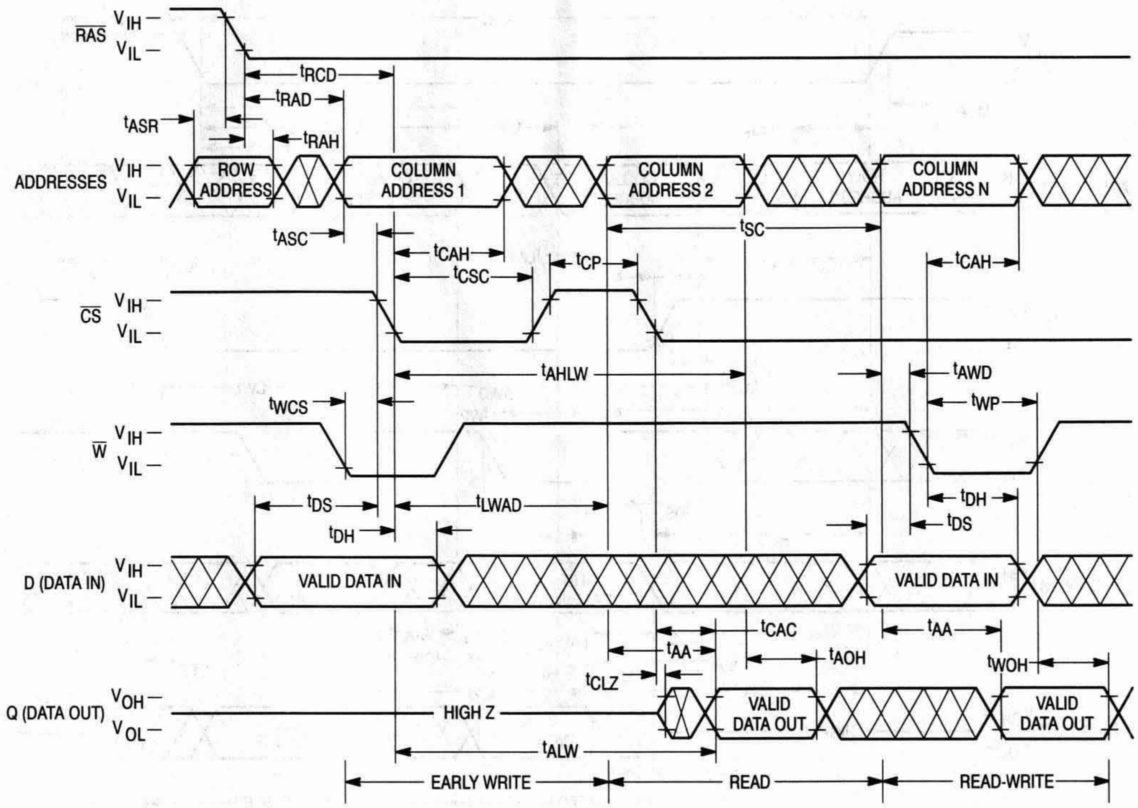
STATIC COLUMN MODE EARLY WRITE CYCLE (B)


t_{RASC}
t_{RP}
RAS
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
t_{CAH}
t_{CAH}
t_{RAL}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS N
t_{ASC}
t_{RAD}
t_{CPR}
CS
t_{RCD}
t_{ASC}
t_{WI}
t_{WCS}
t_{WI}
t_{SC}
t_{CWL}
t_{WP}
t_{WP}
t_{RWL}
W
t_{DH}
t_{DH}
t_{DS}
t_{DS}
D (DATA IN)
VALID DATA IN
VALID DATA IN
VALID DATA IN
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

STATIC COLUMN MODE READ-WRITE CYCLE

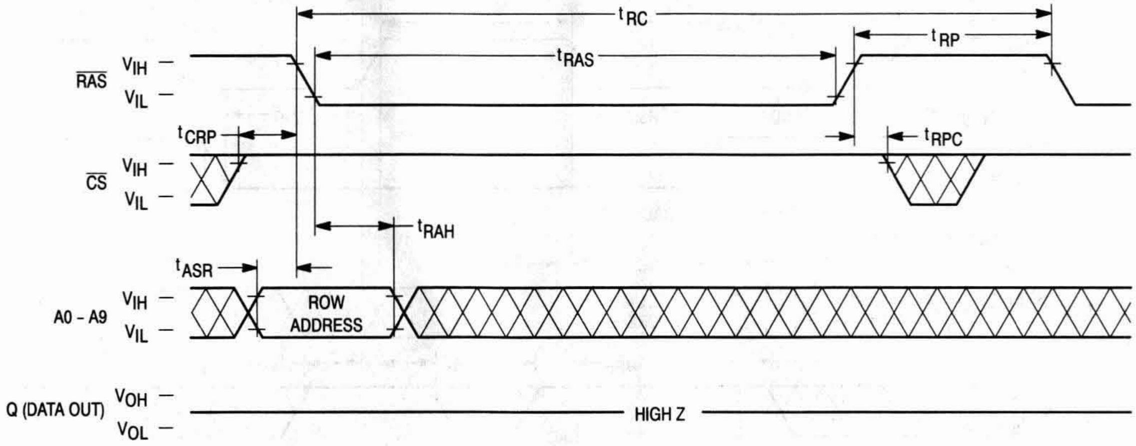

t_{RASC}
t_{RP}
$\overline{RAS}$
V_{IH} –
V_{IL} –
t_{ASR}
t_{RAH}
t_{CAH}
t_{RAL}
t_{SRWC}
t_{RWL}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
t_{RAD}
t_{LWAD}
t_{CRP}
t_{CWD}
$\overline{CS}$
t_{RCS}
t_{AWD}
t_{RWD}
t_{AWD}
t_{WP}
t_{CWL}
$\overline{W}$
t_{DS}
t_{RCD}
t_{DH}
D (DATA IN)
VALID DATA IN
VALID DATA IN
t_{CAC}
t_{WOH}
t_{AA}
t_{AA}
t_{OW}
t_{AOH}
t_{OFF}
t_{RAC}
t_{ALW}
Q (DATA OUT)
V_{OH} –
V_{OL} –
HIGH Z
VALID DATA OUT
VALID DATA OUT
t_{CLZ}
READ-WRITE
READ-WRITE

STATIC COLUMN MODE READ/WRITE MIXED CYCLE

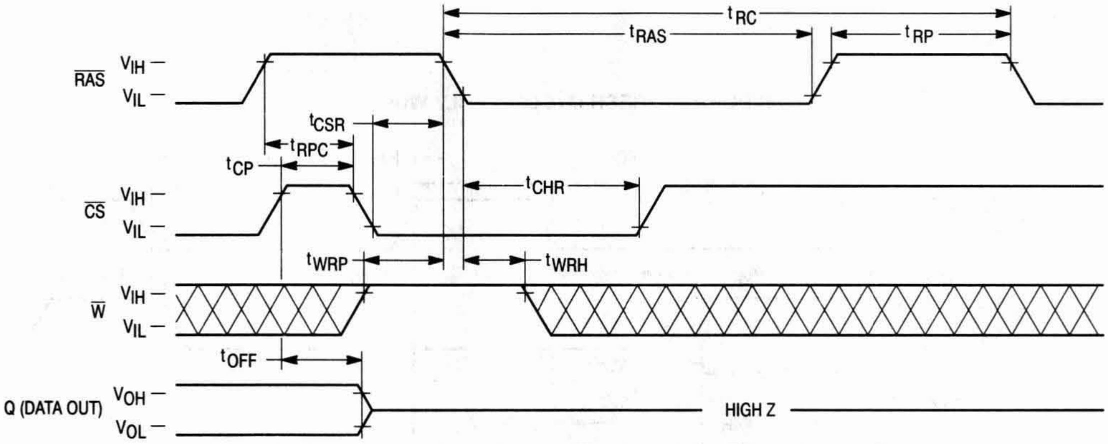


$\overline{RAS}$
V_{IH}
V_{IL}
t_{RCD}
t_{RAD}
t_{ASR}
t_{RAH}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS N
t_{ASC}
t_{CAH}
t_{CSC}
t_{CP}
t_{SC}
t_{CAH}
$\overline{CS}$
t_{AHLW}
t_{AWD}
t_{WCS}
t_{WP}
$\overline{W}$
t_{DS}
t_{LWAD}
t_{DH}
t_{DH}
t_{DS}
D (DATA IN)
VALID DATA IN
VALID DATA IN
t_{CAC}
t_{AA}
t_{AA}
t_{AOH}
t_{CLZ}
t_{WOH}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z
VALID DATA OUT
VALID DATA OUT
t_{ALW}
EARLY WRITE
READ
READ-WRITE

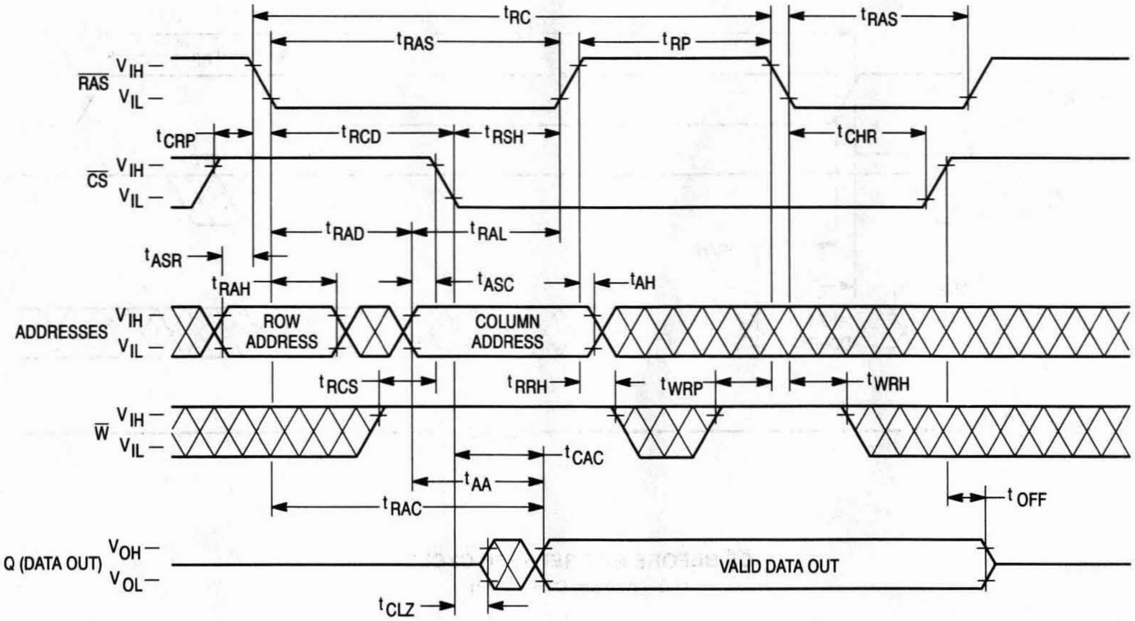
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
($\overline{\text{W}}$ and A10 are Don't Care)


t_{RC}
t_{RP}
t_{RAS}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CS}}$
t_{RAH}
t_{ASR}
A0 - A9
ROW ADDRESS
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

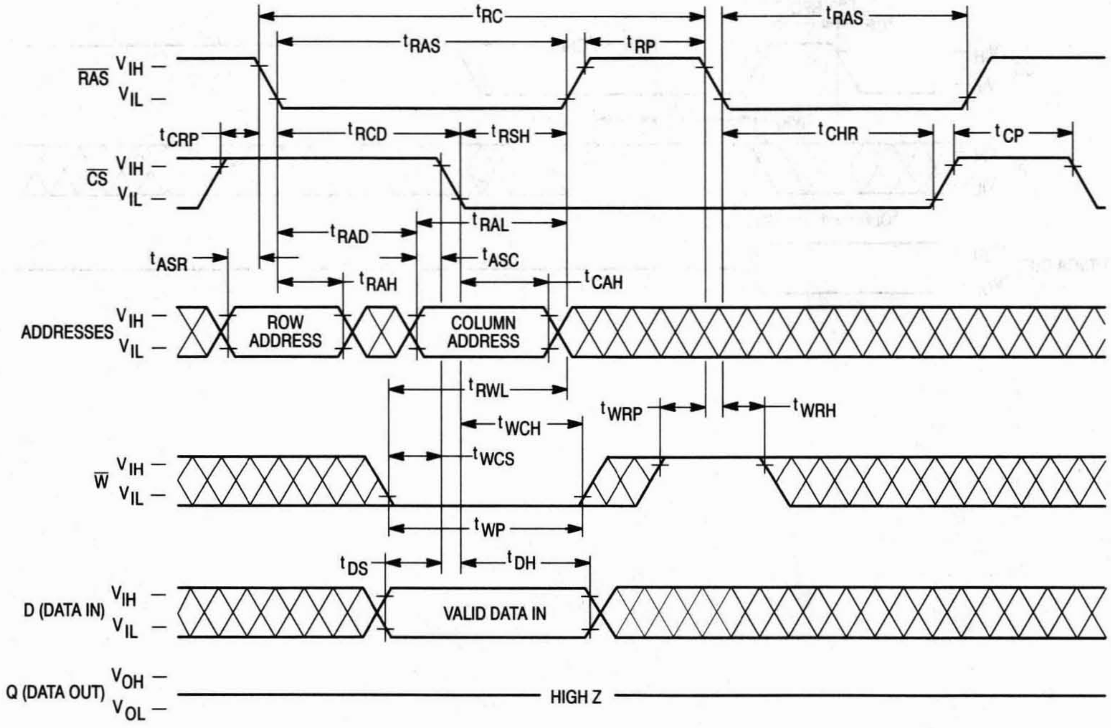
$\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
(A0 – A10 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CSR}
t_{RPC}
t_{CP}
t_{CHR}
$\overline{\text{CS}}$
t_{WRP}
t_{WRH}
$\overline{\text{W}}$
t_{OFF}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

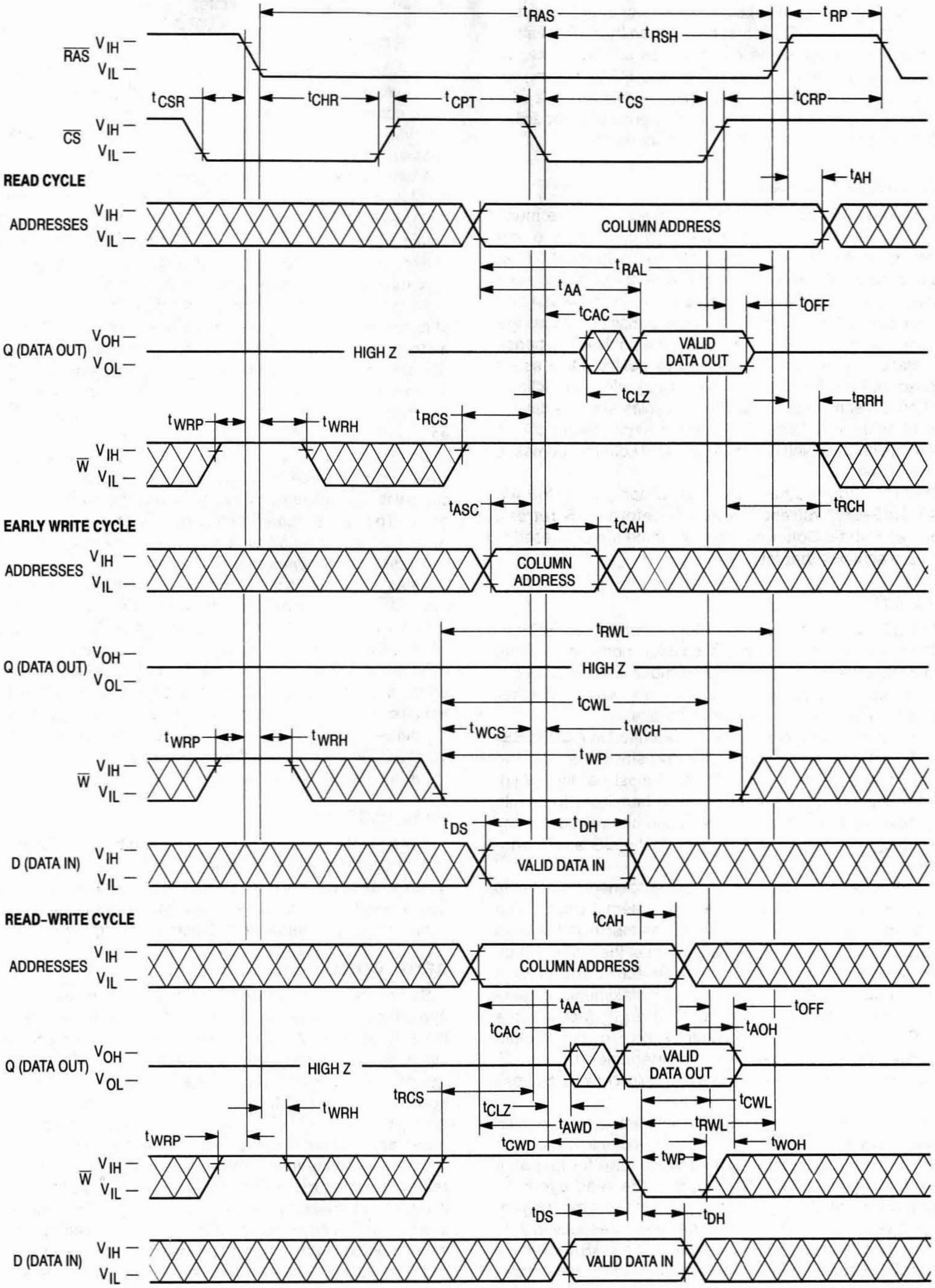
HIDDEN REFRESH CYCLE (READ)


t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
$\overline{CS}$
V_{IH}
V_{IL}
t_{RAD}
t_{RAL}
t_{ASR}
t_{RAH}
t_{ASC}
t_{AH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RCS}
t_{RRH}
t_{WRP}
t_{WRH}
$\overline{W}$
V_{IH}
V_{IL}
t_{CAC}
t_{AA}
t_{RAC}
t_{OFF}
Q (DATA OUT)
V_{OH}
V_{OL}
VALID DATA OUT
t_{CLZ}

HIDDEN REFRESH CYCLE (EARLY WRITE)


t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CP}
$\overline{CS}$
V_{IH}
V_{IL}
t_{RAL}
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RWL}
t_{WRP}
t_{WRH}
t_{WCH}
t_{WCS}
$\overline{W}$
V_{IH}
V_{IL}
t_{WP}
t_{DS}
t_{DH}
D (DATA IN)
V_{IH}
V_{IL}
VALID DATA IN
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



tRAS
tRP
tRSH
RAS
VIH
VIL
tCSR
tCHR
tCPT
tCS
tCRP
CS
VIH
VIL
READ CYCLE
tAH
ADDRESSES
VIH
VIL
COLUMN ADDRESS
tRAL
tAA
tOFF
tCAC
Q (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA OUT
tCLZ
tRRH
tWRP
tWRH
tRCS
W
VIH
VIL
tRCH
tASC
tCAH
EARLY WRITE CYCLE
ADDRESSES
VIH
VIL
COLUMN ADDRESS
tRWL
Q (DATA OUT)
VOH
VOL
HIGH Z
tCWL
tWCS
tWCH
tWRP
tWRH
tWP
W
VIH
VIL
tDS
tDH
D (DATA IN)
VIH
VIL
VALID DATA IN
READ-WRITE CYCLE
tCAH
ADDRESSES
VIH
VIL
COLUMN ADDRESS
tAA
tOFF
tCAC
tAOH
Q (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA OUT
tRCS
tCWL
tWRH
tCLZ
tAWD
tRWL
tWRP
tCWD
tWOH
tWP
W
VIH
VIL
tDS
tDH
D (DATA IN)
VIH
VIL
VALID DATA IN

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by the row address strobe ($\overline{\text{RAS}}$) clock, into two separate 11-bit address fields. A total of twenty-two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 bit locations in the device. $\overline{\text{RAS}}$ active transition latches the row address field. Column addresses are not latched, hence the "static column" designation of this device. Chip select ($\overline{\text{CS}}$) active transition (active = V_{IL}, t_{RCD} minimum) follows $\overline{\text{RAS}}$ on all read, write, or read-write cycles and is independent of column address. The static column feature allows greater flexibility in setting up the external column addresses into the RAM.

There are three other variations in addressing the 4M RAM: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **Static Column mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, static column mode read cycle, read-write cycle, and static column mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ active transition latching the desired row. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CS}}$ active transition, to enable read mode. A valid column address can be provided at any time (t_{RAD} minimum), independent of the $\overline{\text{CS}}$ active transition.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. However, $\overline{\text{CS}}$ must be active and column address must be valid by t_{RCD} and t_{RAD} maximums, respectively, to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If either t_{RCD} or t_{RAD} maximum is exceeded, read access time is determined by the $\overline{\text{CS}}$ clock active transition (t_{CAC}) and/or valid column address (t_{AA}).

The $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CS}, respectively, to complete the read cycle. The column address must remain valid for t_{AH} after $\overline{\text{RAS}}$ inactive transition to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CS}}$ clock is active. When the $\overline{\text{CS}}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, static column mode early write, and static column mode read-write. Early and late write modes are discussed here, while static column mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CS}}$ leading edge. Minimum active time t_{RAS} and t_{CS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CS}}$ active transition. Column address set up and hold times (t_{ASC}, t_{CAH}), and data in (D) set up and hold times (t_{DS}, t_{DH}) are referenced to $\overline{\text{CS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CS}}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T$) $\leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. Column address and D timing parameters are referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CS}}$ active transition but Q may be indeterminate — see note 18 of AC Operating Conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

STATIC COLUMN MODE CYCLES

Static column mode refers to multiple successive data operations performed at any or all 2048 column locations on the selected row of the 4M dynamic RAM during one $\overline{\text{RAS}}$ cycle. Read access time of multiple operations (t_{AA} or t_{CAC}) is considerably faster than the regular $\overline{\text{RAS}}$ clock access time t_{RAC}. Multiple operations can be performed simply by keeping $\overline{\text{RAS}}$ active. $\overline{\text{CS}}$ may be toggled between active and inactive states at any time within the $\overline{\text{RAS}}$ cycle.

Once the timing requirements for the initial read, write, or read-write cycle are met and $\overline{\text{RAS}}$ remains low, the device is ready for the next operation. Operations can be intermixed in any order, at any column address, subject to normal operating conditions previously described. Every write operation must be clocked with either $\overline{\text{CS}}$ or $\overline{\text{W}}$, as indicated in **static column mode early write cycle** timing diagrams **A** and **B**.

Column address and D timing parameters are referenced to the signal clocking the write operation.

$\overline{CS}$ must be toggled inactive (t_{CP}) to perform a read operation after an early write operation (to turn output on), as indicated in **static column mode read/write mixed cycle** timing diagram. The maximum number of consecutive operations is limited to t_{RASC}. The cycle ends when $\overline{RAS}$ transitions to inactive.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54102A require refresh every 16 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54102A. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54102A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$-only refresh, $\overline{CS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CS}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{CS}$ Before $\overline{RAS}$ Refresh

$\overline{CS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CS}$ active before $\overline{RAS}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle.

The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{W}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{RAS}$ active transition to prevent switching the device into **test mode**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CS}$ active the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1). $\overline{W}$ is subject to the same conditions with respect to $\overline{RAS}$ active transition (to prevent test mode cycle) as in $\overline{CS}$ before $\overline{RAS}$ refresh.

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CS}$ before $\overline{RAS}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{CS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of 8 **$\overline{CS}$ before $\overline{RAS}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{CS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{CS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0" which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

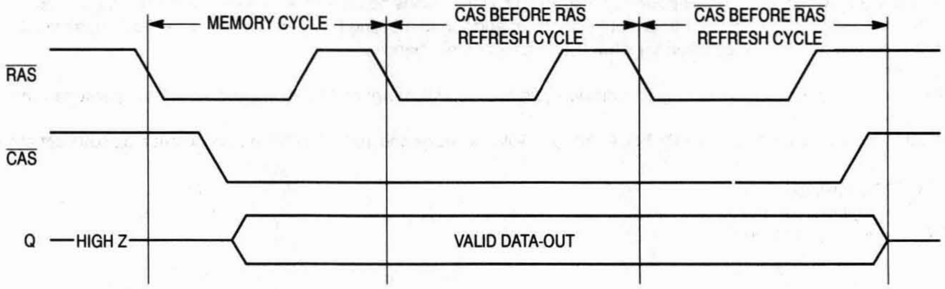

MEMORY CYCLE
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
$\overline{RAS}$
$\overline{CAS}$
Q
HIGH Z
VALID DATA-OUT

Figure 1. Hidden Refresh Cycle

TEST MODE

The internal organization of this device (512 x 8) allows it to be tested as if it were a 512K x 1 DRAM. Nineteen of the twenty-two addresses are used when operating the device in test mode. Row address A10, and column addresses A0 and A10 are ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0 – B7) in parallel. External data out is determined by the internal test mode logic of the device. See following truth table and test mode block diagram.

$\overline{W}$, $\overline{CS}$ before $\overline{RAS}$ timing puts the device in **Test Mode**, as shown in the test mode timing diagram. A **$\overline{CS}$ before $\overline{RAS}$ refresh cycle** or a **$\overline{RAS}$-only refresh cycle** puts the device back in normal mode. Refresh is performed in test mode by using a **$\overline{W}$, $\overline{CS}$ before $\overline{RAS}$ refresh cycle** which uses the internal refresh address counter.

TEST MODE TRUTH TABLE

D	B0	B1	B2	B3	B4	B5	B6	B7	Q
0	0	0	0	0	0	0	0	0	1
1	1	1	1	1	1	1	1	1	1
—	Any Other								0

TEST MODE
AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

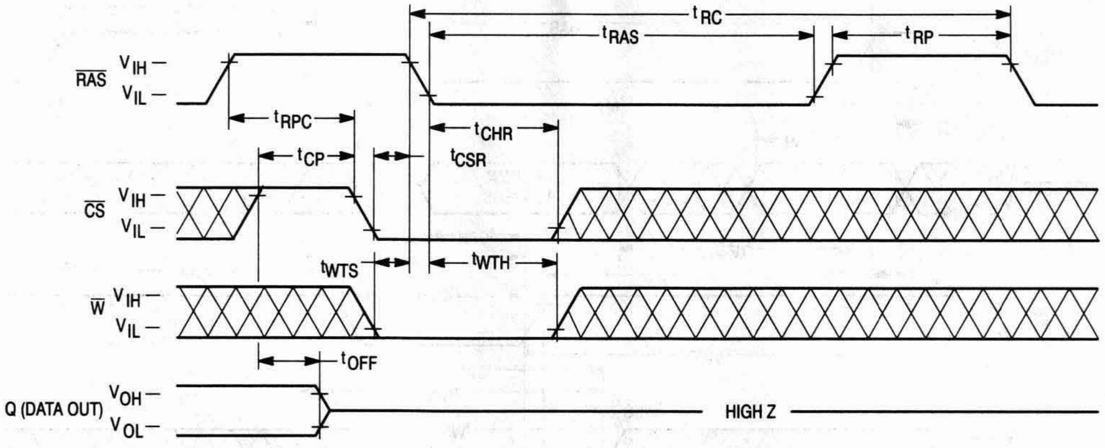
Parameter	Symbol		MCM54102A-60		MCM54102A-70		MCM54102A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	115	—	135	—	155	—	ns	5
Static Column Mode Cycle Time	t_{AVAV}	t_{SC}	40	—	45	—	50	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	65	—	75	—	85	ns	6, 7
Access Time from $\overline{CS}$	t_{CELQV}	t_{CAC}	—	25	—	25	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	45	ns	6, 9
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	65	10 k	75	10 k	85	10 k	ns	
$\overline{RAS}$ Pulse Width (Static Column Mode)	t_{RELREH}	t_{RASC}	65	200 k	75	200 k	85	200 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	25	—	25	—	25	—	ns	
$\overline{CS}$ Hold Time	t_{RELCEH}	t_{CSH}	65	—	75	—	85	—	ns	
$\overline{CS}$ Pulse Width	t_{CELCEH}	t_{CS}	25	10 k	25	10 k	25	10 k	ns	
$\overline{CS}$ Pulse Width (Static Column Mode)	t_{CELCEH}	t_{CSC}	25	200 k	25	200 k	25	200 k	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	45	—	ns	

NOTES:

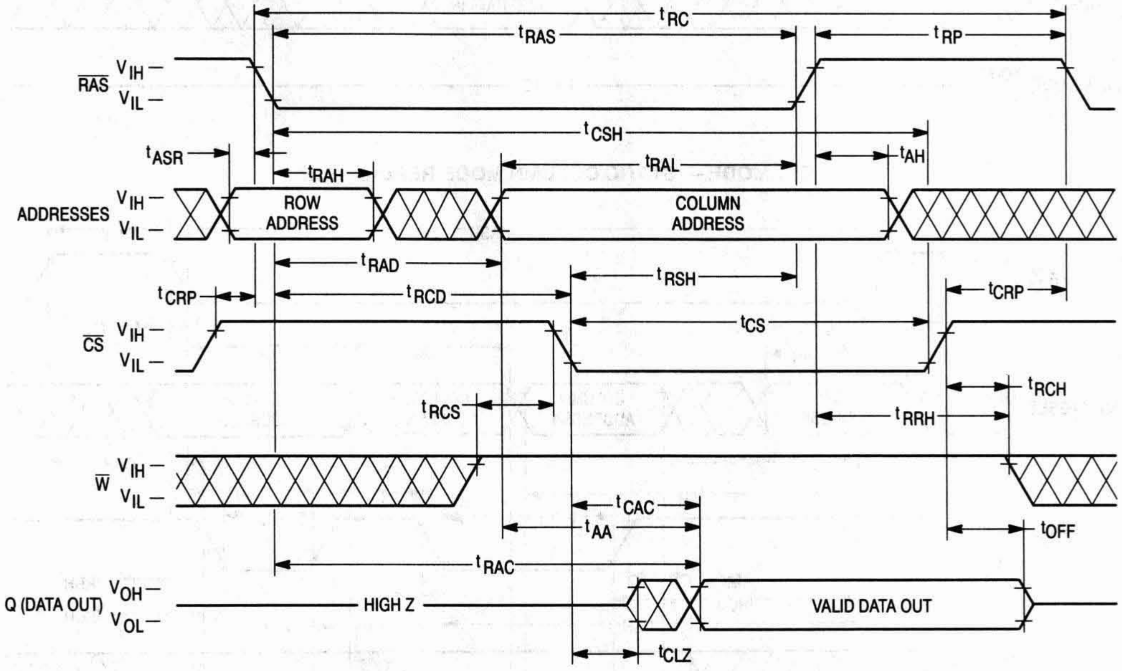
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).

$\overline{\text{W}}$, $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE (TEST MODE ENTRY)

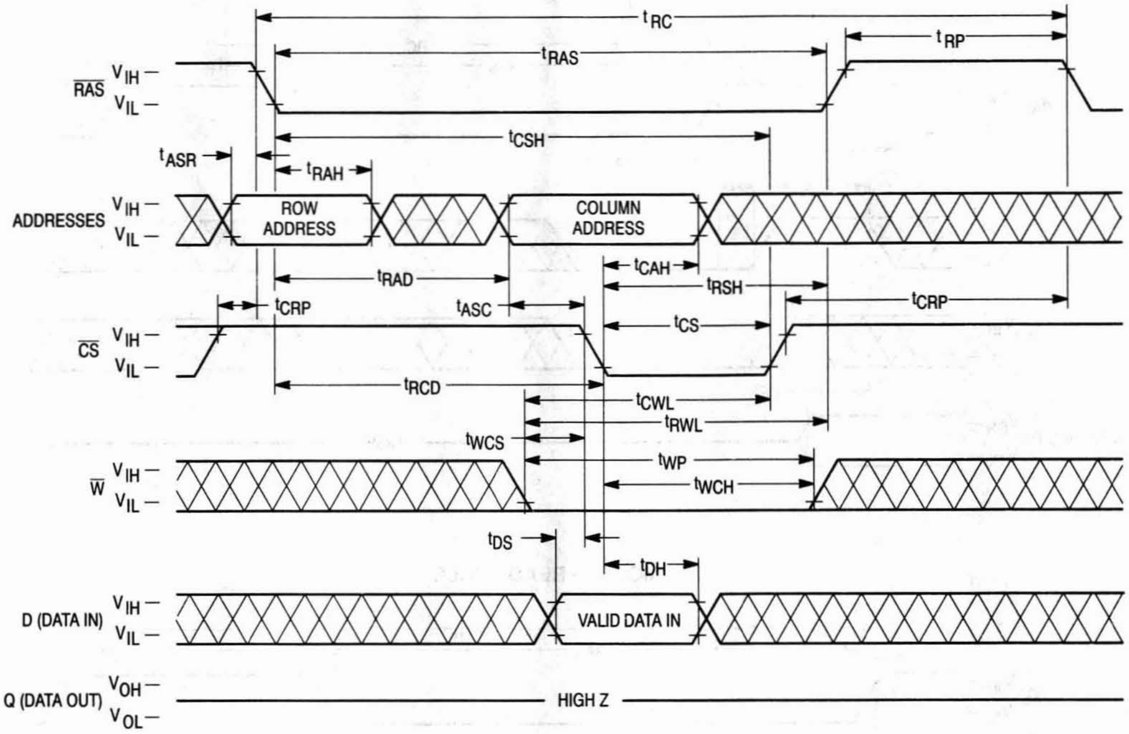
(D and A0 – A10 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH} –
V_{IL} –
t_{RPC}
t_{CP}
t_{CHR}
t_{CSR}
$\overline{\text{CS}}$
V_{IH} –
V_{IL} –
t_{WTS}
t_{WTH}
$\overline{\text{W}}$
V_{IH} –
V_{IL} –
t_{OFF}
Q (DATA OUT)
V_{OH} –
V_{OL} –
HIGH Z

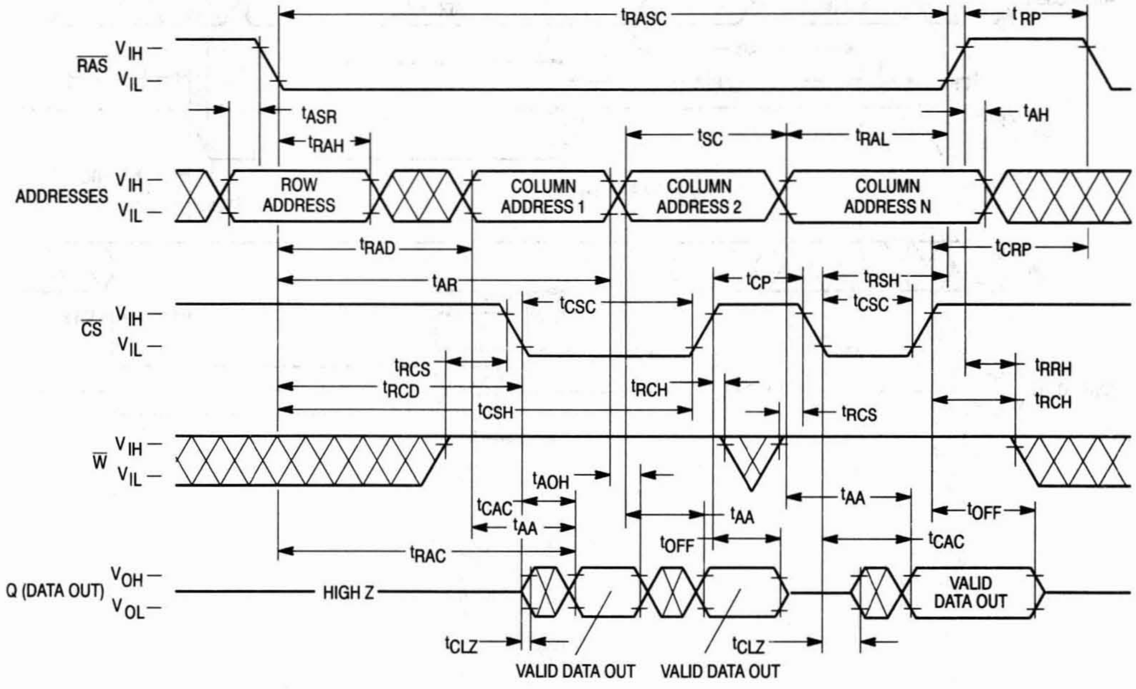
TEST MODE — READ CYCLE


t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH} –
V_{IL} –
t_{CSH}
t_{ASR}
t_{RAH}
t_{RAL}
t_{AH}
ADDRESSES
V_{IH} –
V_{IL} –
ROW ADDRESS
COLUMN ADDRESS
t_{RAD}
t_{RSH}
t_{CRP}
t_{RCD}
t_{CRP}
$\overline{\text{CS}}$
V_{IH} –
V_{IL} –
t_{CS}
t_{RCS}
t_{RCH}
t_{RRH}
$\overline{\text{W}}$
V_{IH} –
V_{IL} –
t_{CAC}
t_{AA}
t_{OFF}
t_{RAC}
Q (DATA OUT)
V_{OH} –
V_{OL} –
HIGH Z
VALID DATA OUT
t_{CLZ}

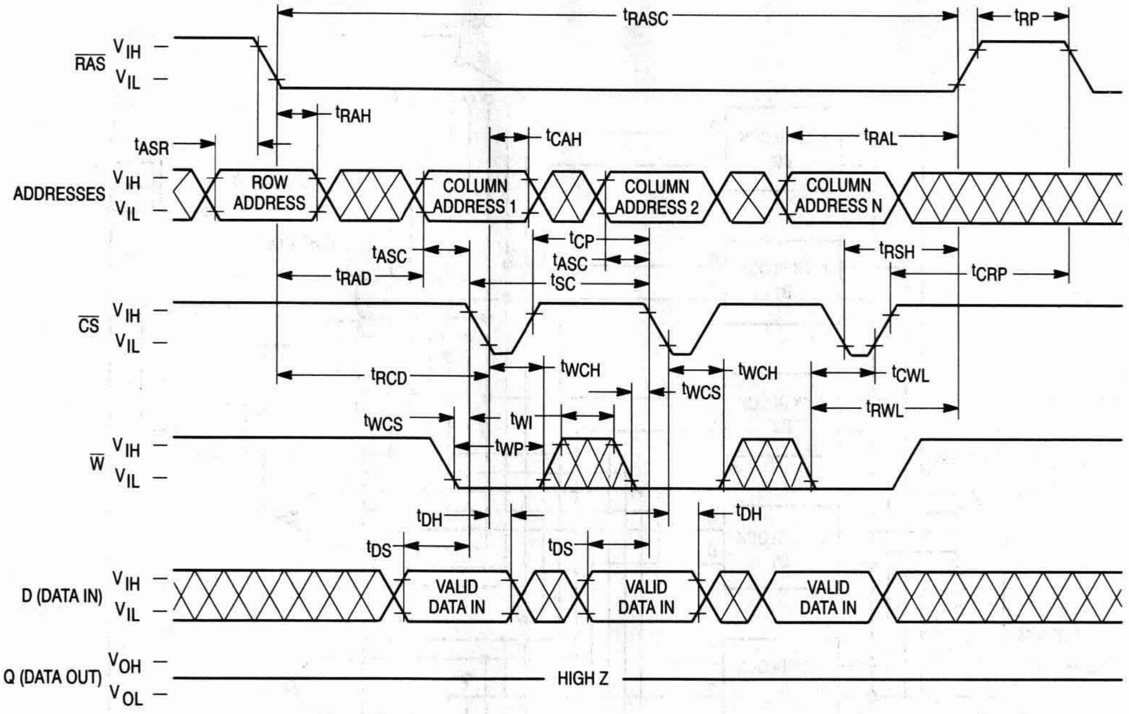
TEST MODE — EARLY WRITE CYCLE


tRC
tRAS
tRP
RAS
VIH —
VIL —
tCSH
tASR
tRAH
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tCAH
tRAD
tRSH
tCRP
tASC
tCRP
CS
tCS
tRCD
tCWL
tRWL
tWCS
W
tWP
tWCH
tDS
tDH
D (DATA IN)
VALID DATA IN
Q (DATA OUT)
VOH —
VOL —
HIGH Z

TEST MODE — STATIC COLUMN MODE READ CYCLE

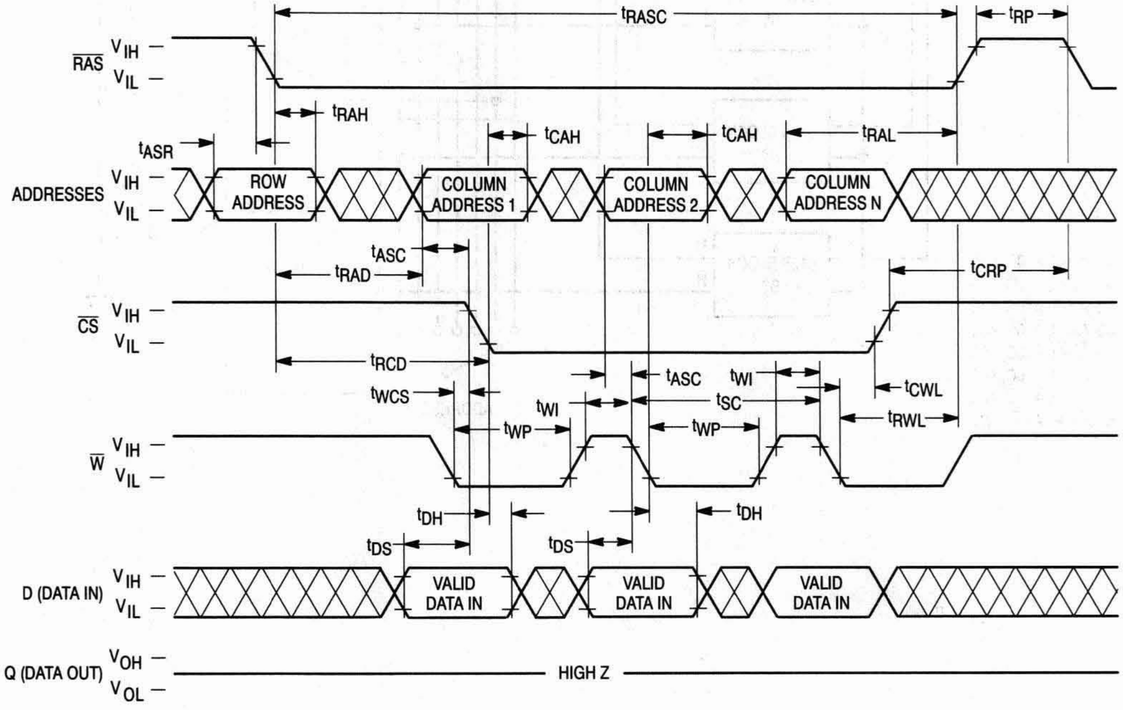

tRASC
tRP
RAS
VIH —
VIL —
tASR
tRAH
tAH
tSC
tRAL
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS N
tRAD
tCRP
tAR
tCP
tRSH
tCSC
tCSC
CS
tRCS
tRCD
tCSH
tRCH
tRCS
tRRH
tRCH
W
tAOH
tCAC
tAA
tAA
tAA
tOFF
tOFF
tCAC
tRAC
Q (DATA OUT)
VOH —
VOL —
HIGH Z
VALID DATA OUT
tCLZ
tCLZ
VALID DATA OUT
VALID DATA OUT

TEST MODE – STATIC COLUMN MODE EARLY WRITE CYCLE (A)



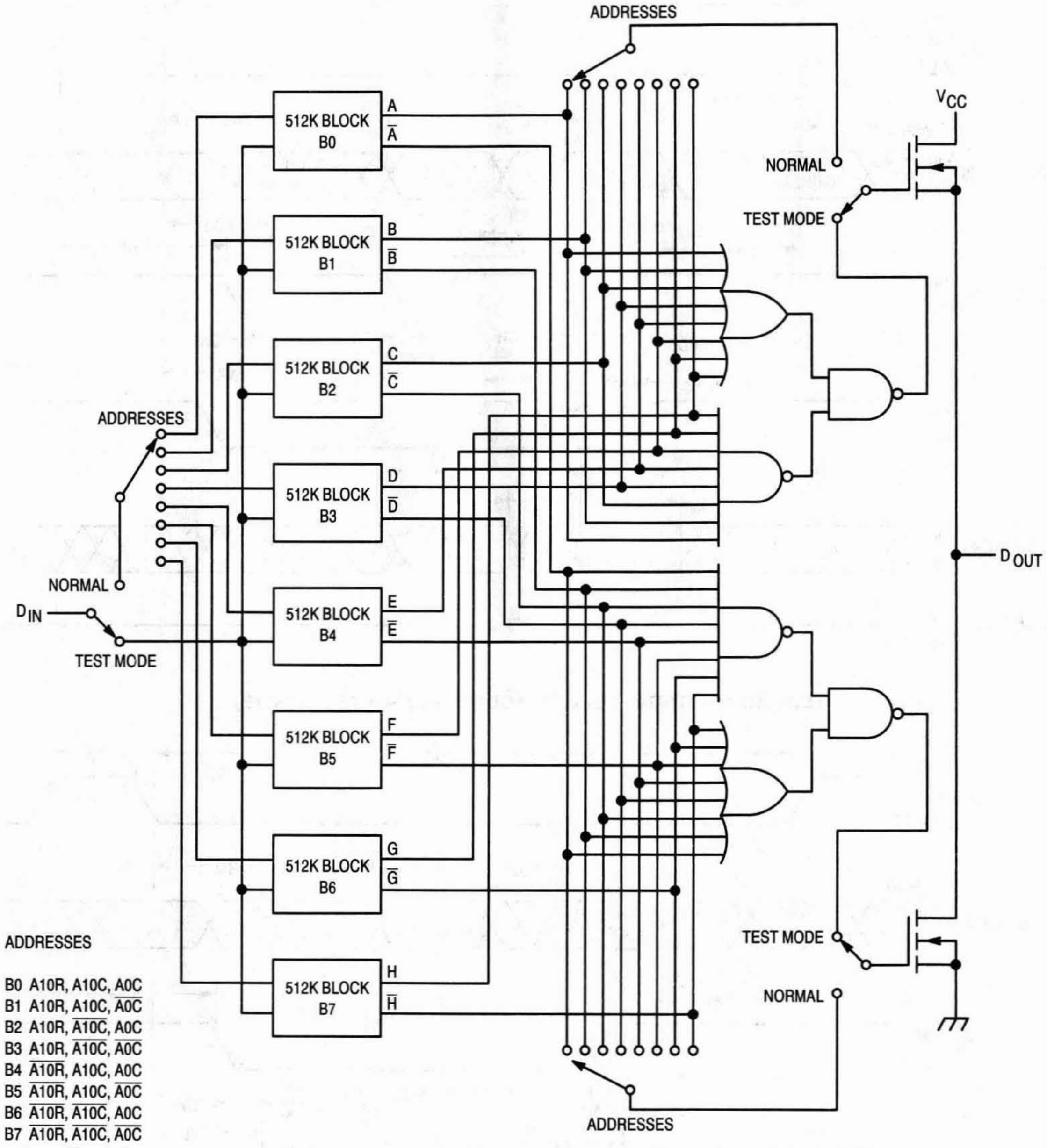
t_{RASC}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
t_{CAH}
t_{RAL}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS N
t_{ASC}
t_{CP}
t_{ASC}
t_{RSH}
t_{RAD}
t_{SC}
t_{CRP}
$\overline{CS}$
t_{RCD}
t_{WCH}
t_{WCH}
t_{CWL}
t_{WCS}
t_{RWL}
t_{WCS}
t_{WI}
t_{WP}
$\overline{W}$
t_{DH}
t_{DH}
t_{DS}
t_{DS}
D (DATA IN)
VALID DATA IN
VALID DATA IN
VALID DATA IN
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

TEST MODE – STATIC COLUMN MODE EARLY WRITE CYCLE (B)



t_{RASC}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
t_{CAH}
t_{CAH}
t_{RAL}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS N
t_{ASC}
t_{RAD}
t_{CRP}
$\overline{CS}$
t_{RCD}
t_{ASC}
t_{WI}
t_{WCS}
t_{CWL}
t_{WI}
t_{SC}
t_{RWL}
t_{WP}
t_{WP}
$\overline{W}$
t_{DH}
t_{DH}
t_{DS}
t_{DS}
D (DATA IN)
VALID DATA IN
VALID DATA IN
VALID DATA IN
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

TEST MODE BLOCK DIAGRAM


ADDRESSES
512K BLOCK B0
A
Ā
512K BLOCK B1
B
B̄
512K BLOCK B2
C
C̄
512K BLOCK B3
D
D̄
512K BLOCK B4
E
Ē
512K BLOCK B5
F
F̄
512K BLOCK B6
G
Ḡ
512K BLOCK B7
H
H̄
ADDRESSES
NORMAL
D IN
TEST MODE
ADDRESSES
NORMAL
TEST MODE
V CC
D OUT
TEST MODE
NORMAL
ADDRESSES

ADDRESSES

B0 A10R, A10C, A0C
B1 A10R, A10C, $\overline{\text{A0C}}$
B2 A10R, $\overline{\text{A10C}}$, A0C
B3 A10R, $\overline{\text{A10C}}$, $\overline{\text{A0C}}$
B4 $\overline{\text{A10R}}$, A10C, A0C
B5 $\overline{\text{A10R}}$, A10C, $\overline{\text{A0C}}$
B6 $\overline{\text{A10R}}$, $\overline{\text{A10C}}$, A0C
B7 $\overline{\text{A10R}}$, $\overline{\text{A10C}}$, $\overline{\text{A0C}}$

ORDERING INFORMATION
(Order by Full Part Number)

MCM 54102A X XX XX

Motorola Memory Prefix — MCM

Part Number — 54102A

Package (N = 300 mil SOJ, Z = 100 mil Plastic ZIP, T = 300 mil TSOP) — X

Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Shipping Method (R2 = Tape and Reel, Blank = Rails or Tray) — XX

Full Part Numbers —

MCM54102AN60
MCM54102AN70
MCM54102AN80

MCM54102AN60R2
MCM54102AN70R2
MCM54102AN80R2

MCM54102AZ60
MCM54102AZ70
MCM54102AZ80

MCM54102AT60
MCM54102AT70
MCM54102AT80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM54170B
MCM5L4170B
MCM5V4170B

Product Preview

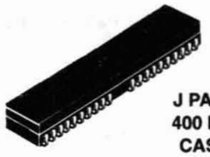
256K x 16 CMOS Dynamic RAM

Fast Page Mode – 1 CAS, 2 Write Enables

The MCM54170B is a 0.6µ CMOS high-speed dynamic random access memory. It is organized as 262,144 sixteen-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM54170B requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 400 mil SOJ plastic package and a 400 mil thin-small-outline package (TSOP).

- Three-State Data Output
- Fast Page Mode
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- Self Refresh (MCM5V4170B only)
- 1024 Cycle Refresh:
  MCM54170B = 16 ms
  MCM5L4170B and MCM5V4170B = 128 ms
- Fast Access Time (t_{RAC}):
  MCM54170B-70, MCM5L4170B-70, and MCM5V4170B-70 = 70 ns (Max)
  MCM54170B-80, MCM5L4170B-80, and MCM5V4170B-80 = 80 ns (Max)
  MCM54170B-10, MCM5L4170B-10, and MCM5V4170B-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM54170B-70, MCM5L4170B-70, and MCM5V4170B-70 = 385 mW (Max)
  MCM54170B-80, MCM5L4170B-80, and MCM5V4170B-80 = 330 mW (Max)
  MCM54170B-10, MCM5L4170B-10, and MCM5V4170B-10 = 303 mW (Max)
- Low Standby Power Dissipation:
  MCM54170B, MCM5L4170B, and MCM5V4170B = 5.5 mW (Max, TTL Levels)
- Battery Backup Power Dissipation:
  MCM5L4170B = 1.7 mW (Max, Battery Backup Mode, t_{RC} = 125 µs)
- Self Refresh Power Dissipation:
  MCM5V4170B = 1.1 mW (Max, Self Refresh Mode)



J PACKAGE
400 MIL SOJ
CASE TBD

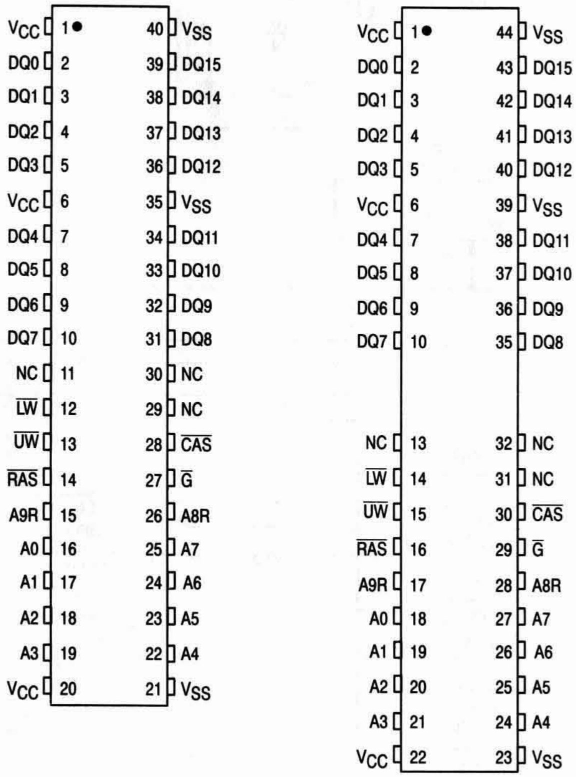
T PACKAGE
400 MIL TSOP
CASE 924-01

PIN NAMES

A0 – A7, A8R, A9R	Address Input
DQ0 – DQ15	Data Input/Output
$\overline{\text{LW}}$, $\overline{\text{UW}}$	Read/Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connection
$\overline{\text{G}}$	Output Enable

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

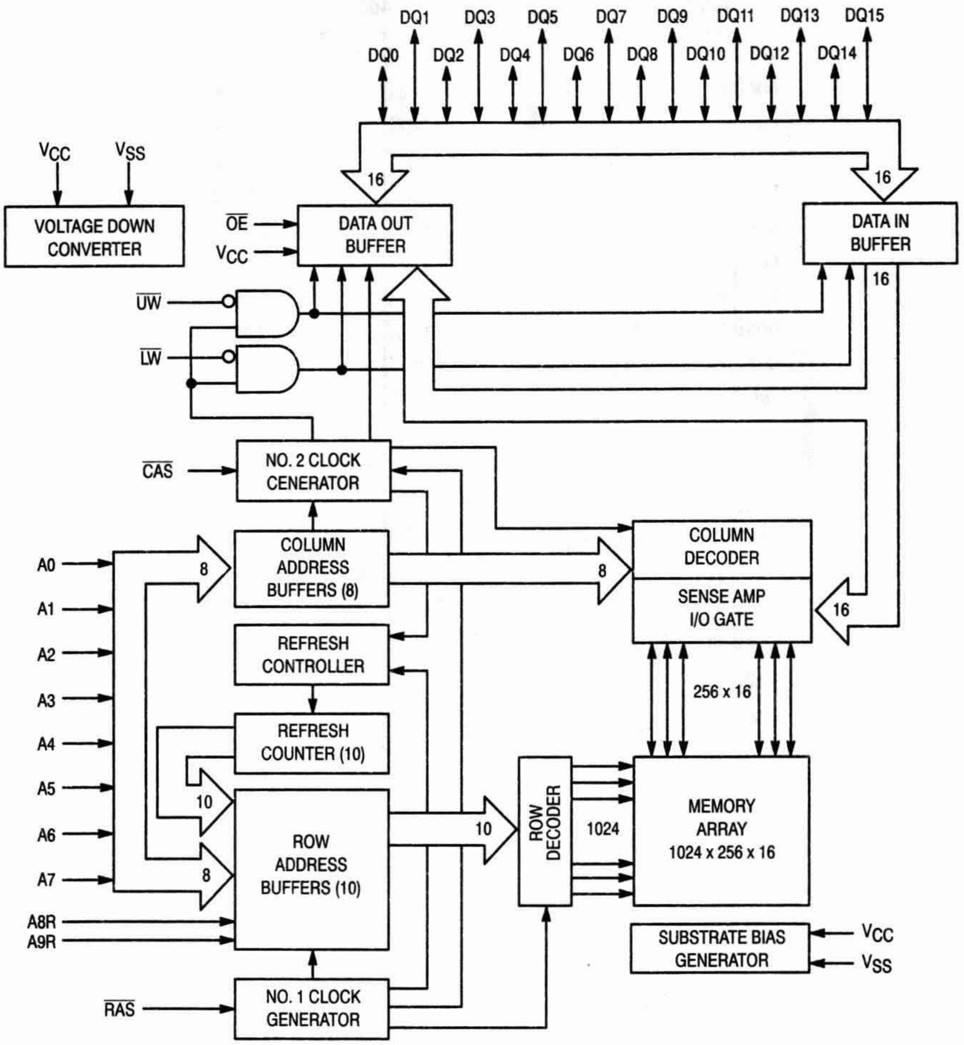
PIN ASSIGNMENTS


400 MIL SOJ

400 MIL TSOP

VCC 1
DQ0 2
DQ1 3
DQ2 4
DQ3 5
VCC 6
DQ4 7
DQ5 8
DQ6 9
DQ7 10
NC 11
LW 12
UW 13
RAS 14
A9R 15
A0 16
A1 17
A2 18
A3 19
VCC 20
40 VSS
39 DQ15
38 DQ14
37 DQ13
36 DQ12
35 VSS
34 DQ11
33 DQ10
32 DQ9
31 DQ8
30 NC
29 NC
28 CAS
27 G
26 A8R
25 A7
24 A6
23 A5
22 A4
21 VSS
VCC 1
DQ0 2
DQ1 3
DQ2 4
DQ3 5
VCC 6
DQ4 7
DQ5 8
DQ6 9
DQ7 10
NC 13
LW 14
UW 15
RAS 16
A9R 17
A0 18
A1 19
A2 20
A3 21
VCC 22
44 VSS
43 DQ15
42 DQ14
41 DQ13
40 DQ12
39 VSS
38 DQ11
37 DQ10
36 DQ9
35 DQ8
32 NC
31 NC
30 CAS
29 G
28 A8R
27 A7
26 A6
25 A5
24 A4
23 VSS

BLOCK DIAGRAM


DQ1
DQ3
DQ5
DQ7
DQ9
DQ11
DQ13
DQ15
DQ0
DQ2
DQ4
DQ6
DQ8
DQ10
DQ12
DQ14
16
16
VCC
VSS
VOLTAGE DOWN CONVERTER
OE
VCC
DATA OUT BUFFER
DATA IN BUFFER
16
UW
LW
CAS
NO. 2 CLOCK CENERATOR
A0
A1
A2
A3
A4
A5
A6
A7
A8R
A9R
8
COLUMN ADDRESS BUFFERS (8)
8
COLUMN DECODER
SENSE AMP I/O GATE
16
REFRESH CONTROLLER
256 x 16
REFRESH COUNTER (10)
10
8
ROW ADDRESS BUFFERS (10)
10
ROW DECODER
1024
MEMORY ARRAY 1024 x 256 x 16
SUBSTRATE BIAS GENERATOR
VCC
VSS
RAS
NO. 1 CLOCK GENERATOR

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.0	V
Logic Low Voltage, All Inputs Except DQ0 – DQ7	V_{IL}	– 0.5*	—	0.8	V
Logic Low Voltage, DQ0 – DQ7	V_{IL}	– 0.5*	—	0.8	V

*– 2.0 V at pulse width ≤ 20 ns

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM54170B-70, MCM5L4170B-70, and MCM5V4170B-70, t_{RC} = 130 ns MCM54170B-80, MCM5L4170B-80, and MCM5V4170B-80, t_{RC} = 150 ns MCM54170B-10, MCM5L4170B-10, and MCM5V4170B-10, t_{RC} = 180 ns	I_{CC1}	 — — —	 75 65 60	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles ($\overline{CAS}$ = V_{IH}) MCM54170B-70, MCM5L4170B-70, and MCM5V4170B-70, t_{RC} = 130 ns MCM54170B-80, MCM5L4170B-80, and MCM5V4170B-80, t_{RC} = 150 ns MCM54170B-10, MCM5L4170B-10, and MCM5V4170B-10, t_{RC} = 180 ns	I_{CC3}	 — — —	 75 65 60	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL}) MCM54170B-70, MCM5L4170B-70, and MCM5V4170B-70, t_{PC} = 45 ns MCM54170B-80, MCM5L4170B-80, and MCM5V4170B-80, t_{PC} = 50 ns MCM54170B-10, MCM5L4170B-10, and MCM5V4170B-10, t_{PC} = 60 ns	I_{CC4}	 — — —	 70 60 55	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM54170B MCM5L4170B and MCM5V4170B	I_{CC5}	— —	1.0 200	mA μA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM54170B-70, MCM5L4170B-70, and MCM5V4170B-70, t_{RC} = 130 ns MCM54170B-80, MCM5L4170B-80, and MCM5V4170B-80, t_{RC} = 150 ns MCM54170B-10, MCM5L4170B-10, and MCM5V4170B-10, t_{RC} = 180 ns	I_{CC6}	 — — —	 75 65 60	mA	1
V_{CC} Power Supply Current, Battery Backup Mode — MCM5L4170B Only (t_{RC} = 125 μs; t_{RAS} = 1 μs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0 – A8, A9R, $\overline{W}$, D = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	—	300	μA	1, 3
V_{CC} Power Supply Current, Self Refresh Mode — MCM5V4170B Only ($\overline{RAS}$ = $\overline{CAS}$ = V_{IL}; A0 – A7, A8R, A9R, $\overline{W}$, $\overline{G}$ = V_{CC} – 0.2 V or 0.2 V; DQ0–DQ7 = V_{CC} – 0.2 V, 0.2 V, or Open)	I_{CC8}	—	200	μA	
Input Leakage Current (0 V ≤ V_{in} ≤ 7.0 V)	$I_{lkg(I)}$	– 10	10	μA	
Output Leakage Current (0 V ≤ V_{out} ≤ 7.0 V, Output Disable)	$I_{lkg(O)}$	– 10	10	μA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading. Maximum currents are at the specified cycle time (min) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. t_{RAS} (max) = 1 μs is only applied to refresh of battery back-up. t_{RAS} (max) = 10 μs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, periodically sampled, not 100% tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A7, A8R, A9R	C_{in}	5	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{G}$		7	
Input/Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0 – DQ15	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM54170B-70 MCM5L4170B-70 MCM5V4170B-70		MCM54170B-80 MCM5L4170B-80 MCM5V4170B-80		MCM54170B-10 MCM5L4170B-10 MCM5V4170B-10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	180	—	ns	5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RWC}	185	—	205	—	245	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	50	—	60	—	ns	
Page Mode Read-Modify-Write Cycle Time	t_{CELCEL}	t_{PRWC}	100	—	105	—	125	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	—	100	ns	6, 8, 9
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	50	ns	6, 9
Access Time from $\overline{\text{CAS}}$ Precharge	t_{CEHQV}	t_{CPA}	—	40	—	45	—	55	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	15	0	20	ns	7
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	70	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	8
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	9
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Page Mode Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Hold Time From $\overline{\text{CAS}}$ Precharge (Page Mode Only)	t_{CEHREH}	t_{RHCP}	40	—	45	—	55	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	50	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles or 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0 \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. t_{OFF} (max) and t_{GZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM54170B-70 MCM5L4170B-70 MCM5V4170B-70		MCM54170B-80 MCM5L4170B-80 MCM5V4170B-80		MCM54170B-10 MCM5L4170B-10 MCM5V4170B-10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	10
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{CELWH}	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	11
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	20	—	ns	11
Refresh Period MCM54170B MCM5L4170B and MCM5V4170B	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	12
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	60	—	ns	12
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	100	—	110	—	135	—	ns	12
Column Address to Write Delay	t_{AVWL}	t_{AWD}	65	—	70	—	85	—	ns	12
$\overline{CAS}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	70	—	75	—	90	—	ns	12
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	t_{RELCEH}	t_{CHR}	15	—	15	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Counter Test)	t_{CEHCEL}	t_{CPT}	30	—	30	—	40	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	—	10	—	20	—	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	20	—	25	ns	6
$\overline{G}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	25	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	25	ns	7
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	25	—	ns	
Masked Write Set-Up Time	t_{MEHCEL}	t_{MCS}	0	—	0	—	0	—	ns	
Masked Write Hold Time Referenced to $\overline{RAS}$	t_{REHMX}	t_{MRH}	0	—	0	—	0	—	ns	
Masked Write Hold Time Referenced to $\overline{CAS}$	t_{CEHMX}	t_{MCH}	0	—	0	—	0	—	ns	
Output Disable Setup Time	t_{GLCEL}	t_{GDS}	0	—	0	—	0	—	ns	

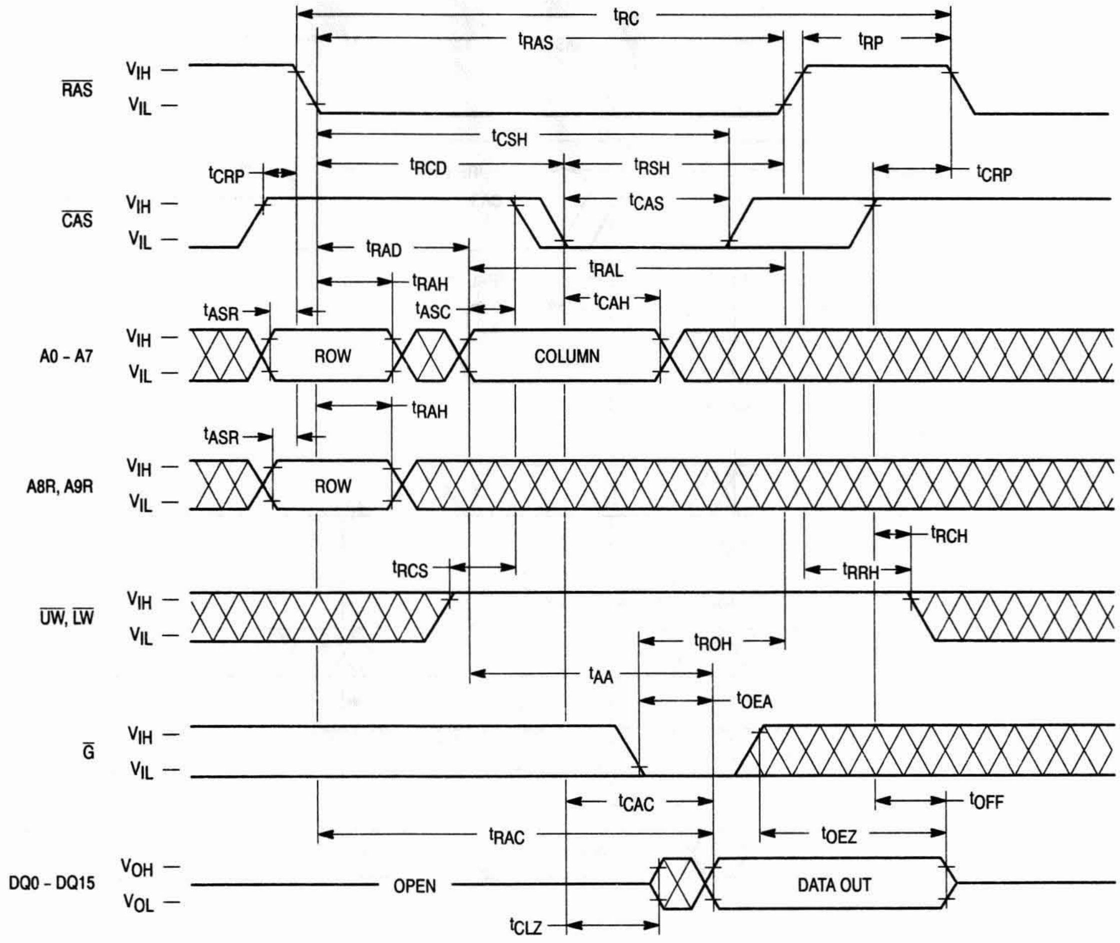
NOTES:

10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in late write or read-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

SELF REFRESH CYCLE

Parameter	Symbol		MCM54170B-70 MCM5L4170B-70 MCM5V4170B-70		MCM54170B-80 MCM5L4170B-80 MCM5V4170B-80		MCM54170B-10 MCM5L4170B-10 MCM5V4170B-10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh, MCM5V4170B Only)	$t_{RELREHS}$	t_{RASS}	100	—	100	—	100	—	µs	
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh, MCM5V4170B Only)	$t_{REHRELS}$	t_{RPS}	130	—	150	—	180	—	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh, MCM5V4170B Only)	t_{REHCEH}	t_{CHS}	– 50	—	– 60	—	– 70	—	ns	

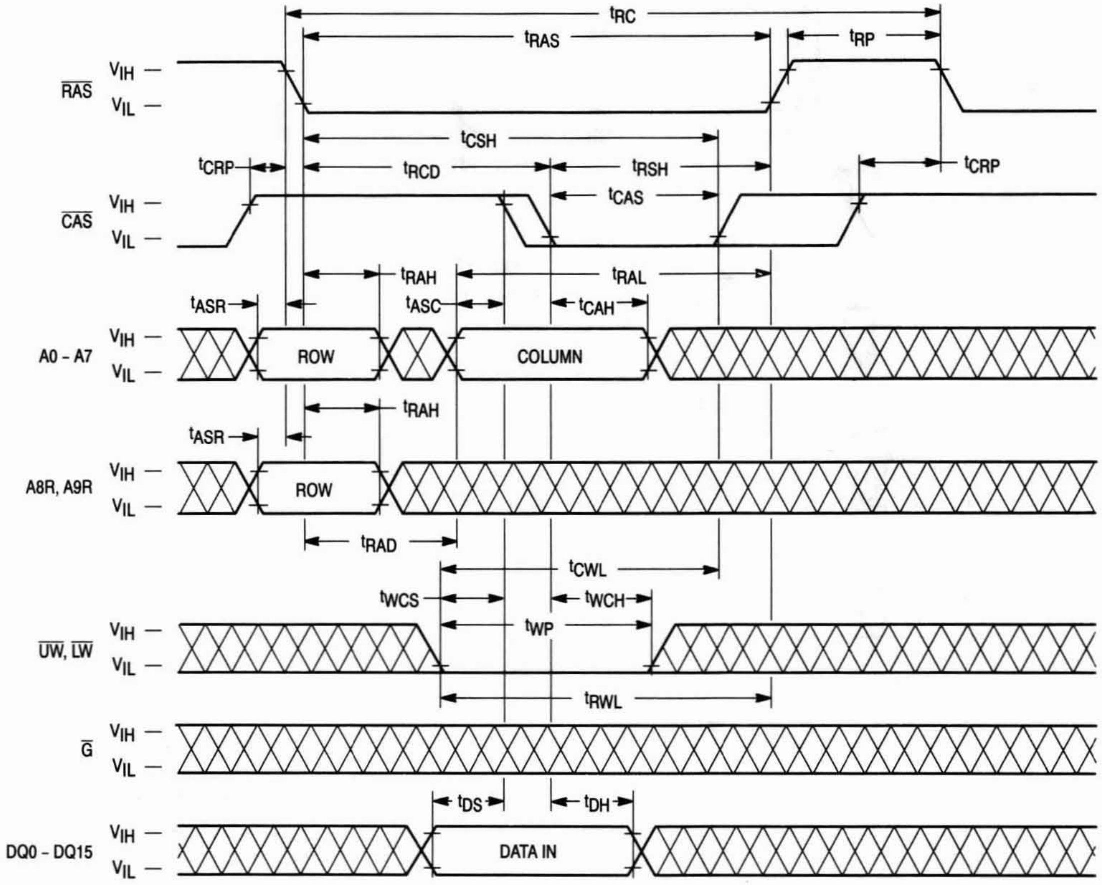
READ CYCLE



tRC
tRAS
tRP
RAS
VIH —
VIL —
tCSH
tRCD
tRSH
tCRP
tCRP
CAS
VIH —
VIL —
tCAS
tRAD
tRAL
tRAH
tASR
tASC
tCAH
A0 - A7
VIH —
VIL —
ROW
COLUMN
tRAH
tASR
A8R, A9R
VIH —
VIL —
ROW
tRCH
tRCS
tRRH
UW, LW
VIH —
VIL —
tROH
tAA
tOEA
G
VIH —
VIL —
tCAC
tOFF
tRAC
tOEZ
DQ0 - DQ15
VOH —
VOL —
OPEN
DATA OUT
tCLZ

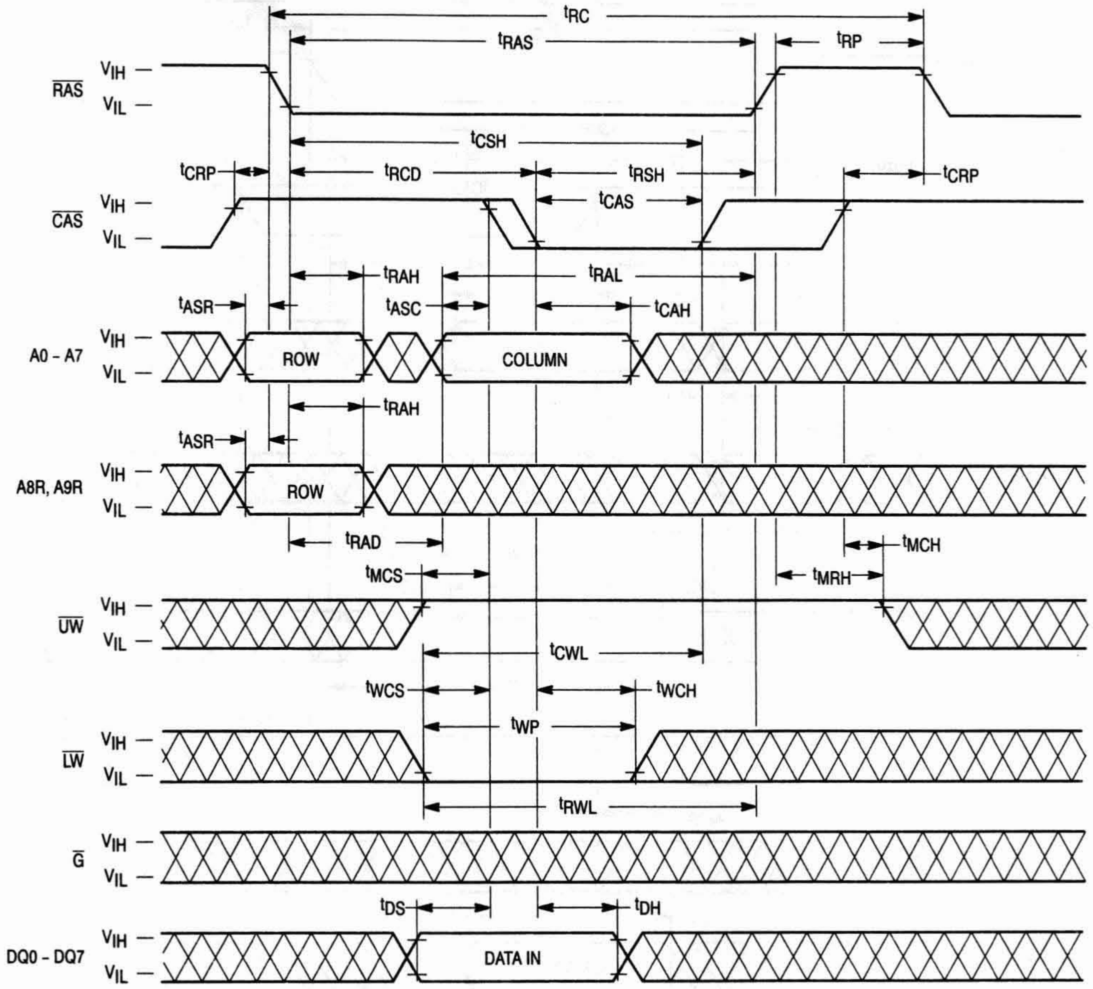
NOTE: D_{in} = Open

WRITE CYCLE (EARLY WRITE)


tRC
tRAS
tRP
RAS
VIH —
VIL —
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
tRAH
tRAL
tASR
tASC
tCAH
A0 – A7
ROW
COLUMN
tRAH
tASR
A8R, A9R
ROW
tRAD
tCWL
tWCS
tWCH
tWP
UW, LW
tRWL
G
tDS
tDH
DQ0 – DQ15
DATA IN

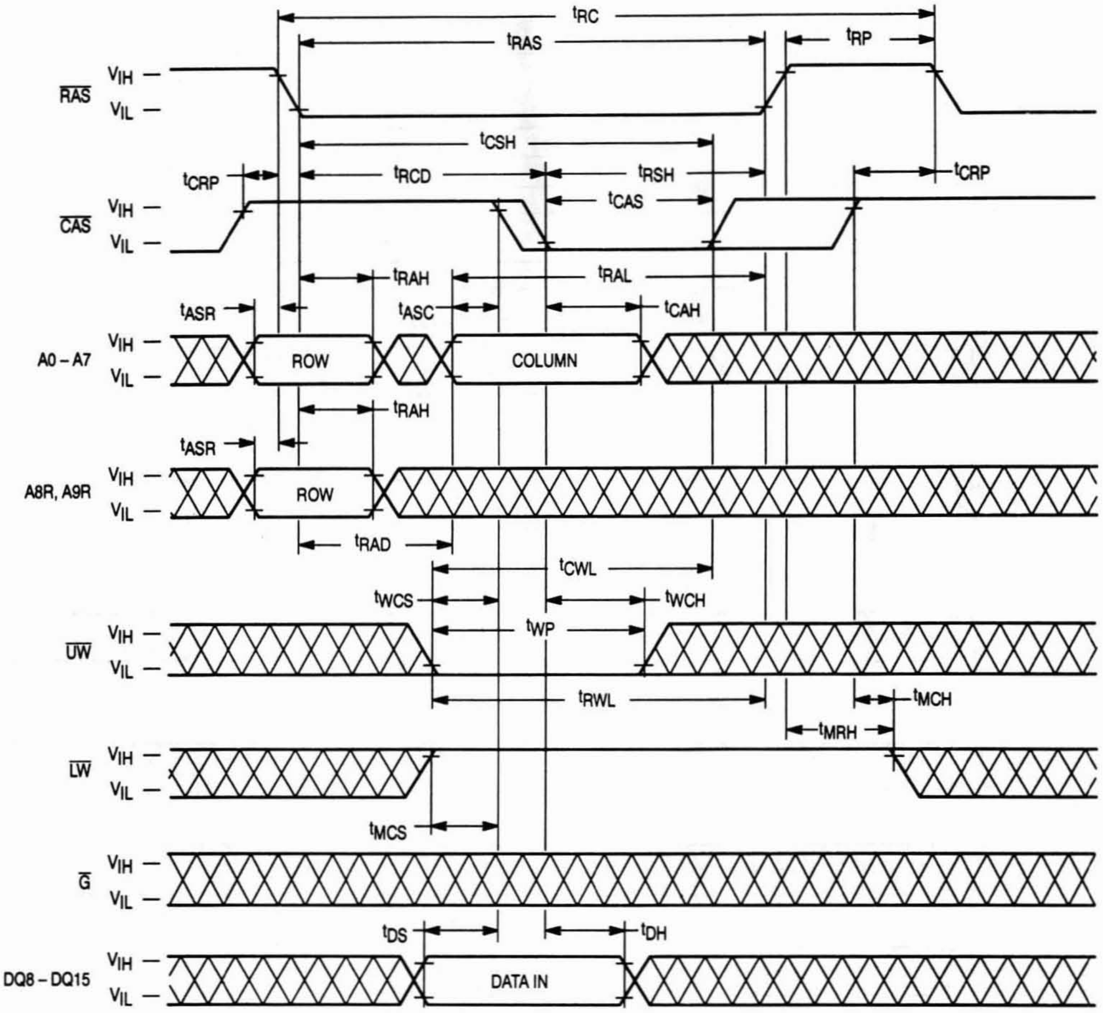
NOTE: D_{out} = Open

LOWER BYTE WRITE CYCLE (EARLY WRITE)


t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 - A7
ROW
COLUMN
t_{RAH}
t_{ASR}
A8R, A9R
ROW
t_{RAD}
t_{MCH}
t_{MCS}
t_{MRH}
$\overline{UW}$
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{LW}$
t_{RWL}
$\overline{G}$
t_{DS}
t_{DH}
DQ0 - DQ7
DATA IN

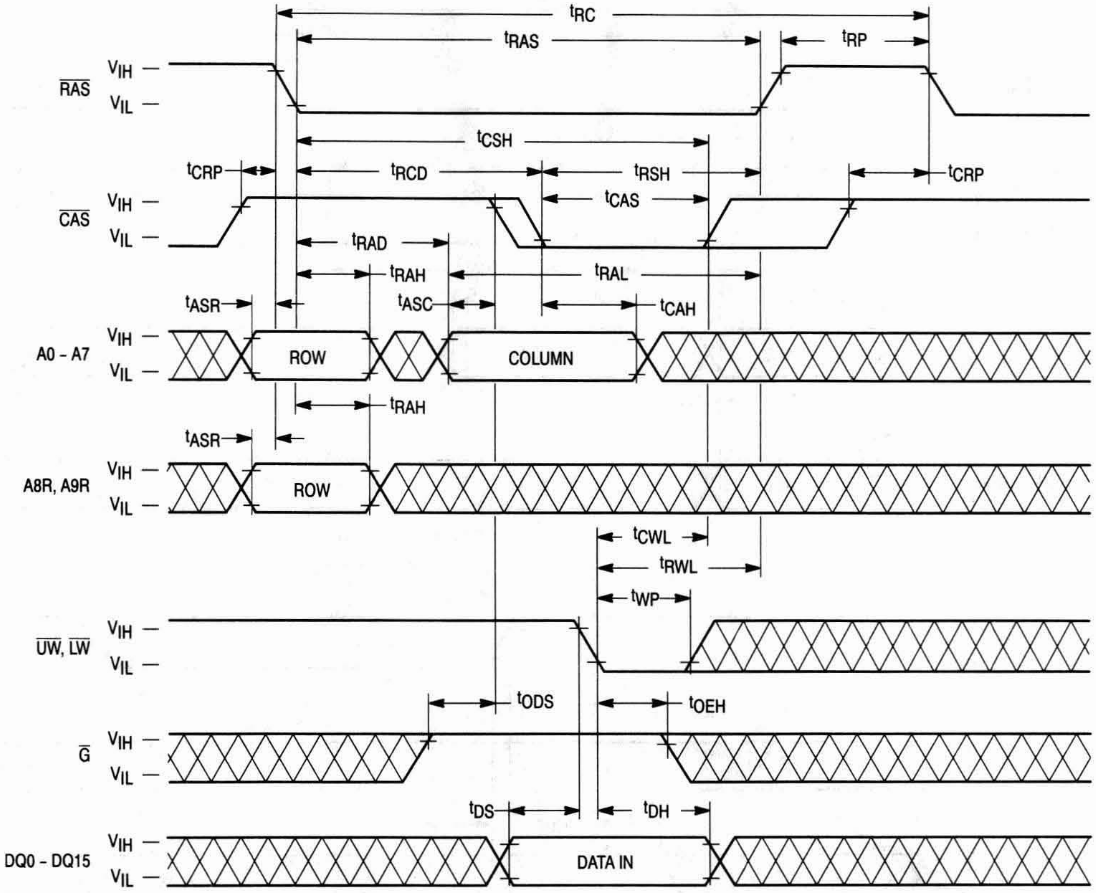
NOTE: D_{in} (DQ8 – DQ15) = Don't Care
D_{out} = Open

UPPER BYTE CYCLE (EARLY WRITE)


t_{RC}
t_{RAS}
t_{RP}
RAS
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
CAS
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 – A7
ROW
COLUMN
t_{RAH}
t_{ASR}
A8R, A9R
ROW
t_{RAD}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
UW
t_{RWL}
t_{MCH}
t_{MRH}
LW
t_{MCS}
G
t_{DS}
t_{DH}
DQ8 – DQ15
DATA IN

NOTE: D_{in} (DQ0 – DQ7) = Don't Care
D_{out} = Open

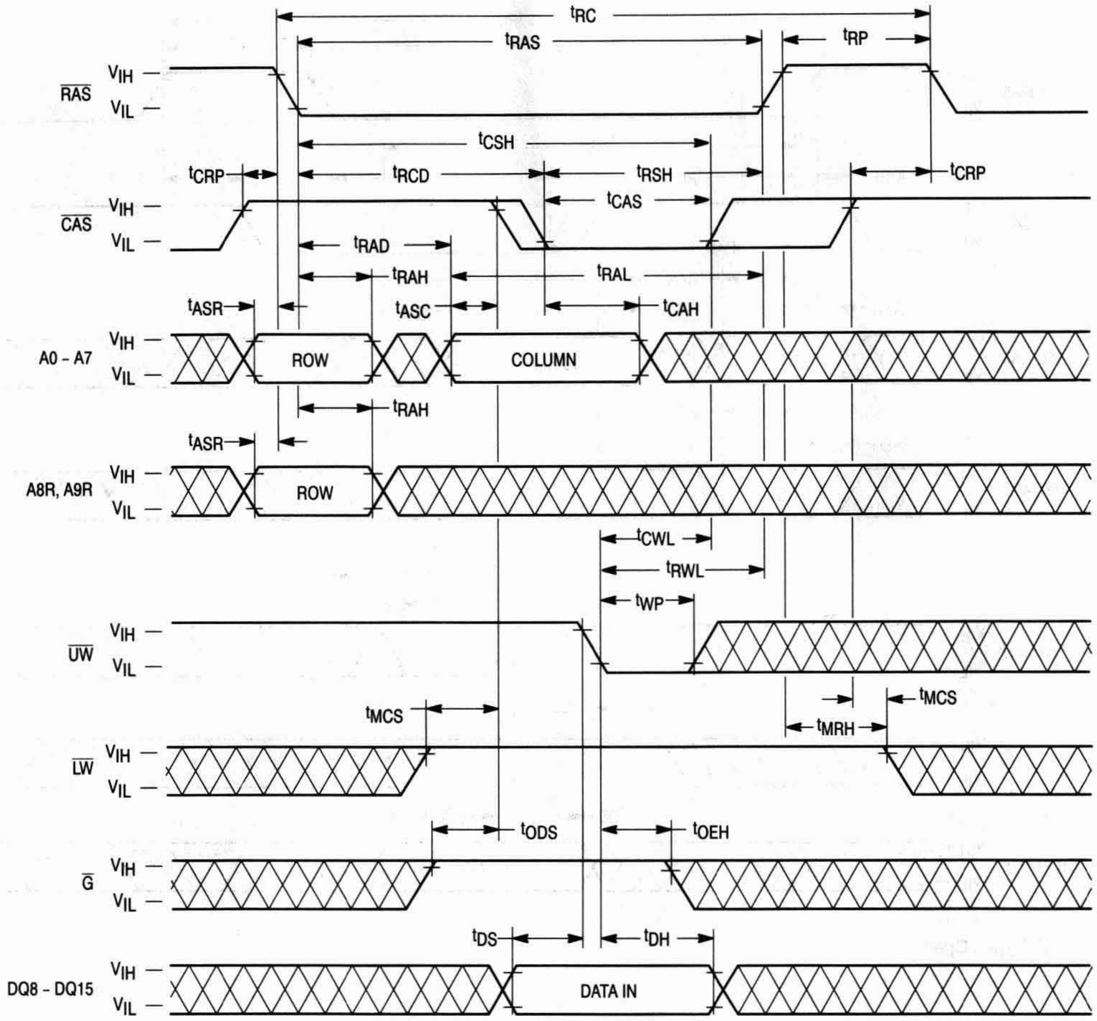
WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
t_{RAD}
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 - A7
ROW
COLUMN
t_{RAH}
t_{ASR}
A8R, A9R
ROW
t_{CWL}
t_{RWL}
t_{WP}
$\overline{UW}$, $\overline{LW}$
t_{ODS}
t_{OEH}
$\overline{G}$
t_{DS}
t_{DH}
DQ0 - DQ15
DATA IN

NOTE: D_{out} = Open

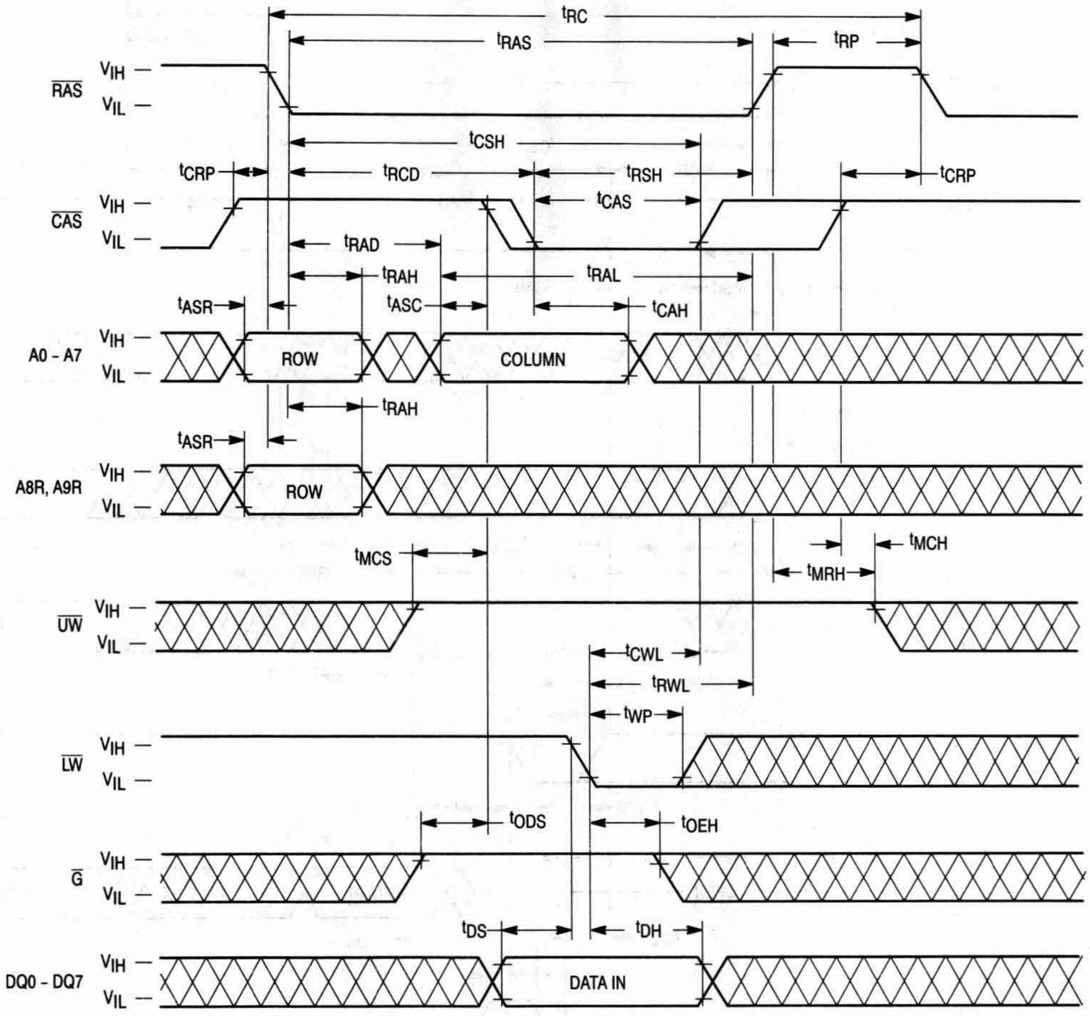
UPPER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
tRAD
tRAH
tRAL
tASR
tASC
tCAH
A0 - A7
ROW
COLUMN
tRAH
tASR
A8R, A9R
ROW
tCWL
tRWL
tWP
UW
tMCS
tMCS
tMRH
LW
tODS
tOEH
G
tDS
tDH
DQ8 - DQ15
DATA IN

NOTE: D_{in} (DQ0 – DQ7) = Don't Care
D_{out} = Open

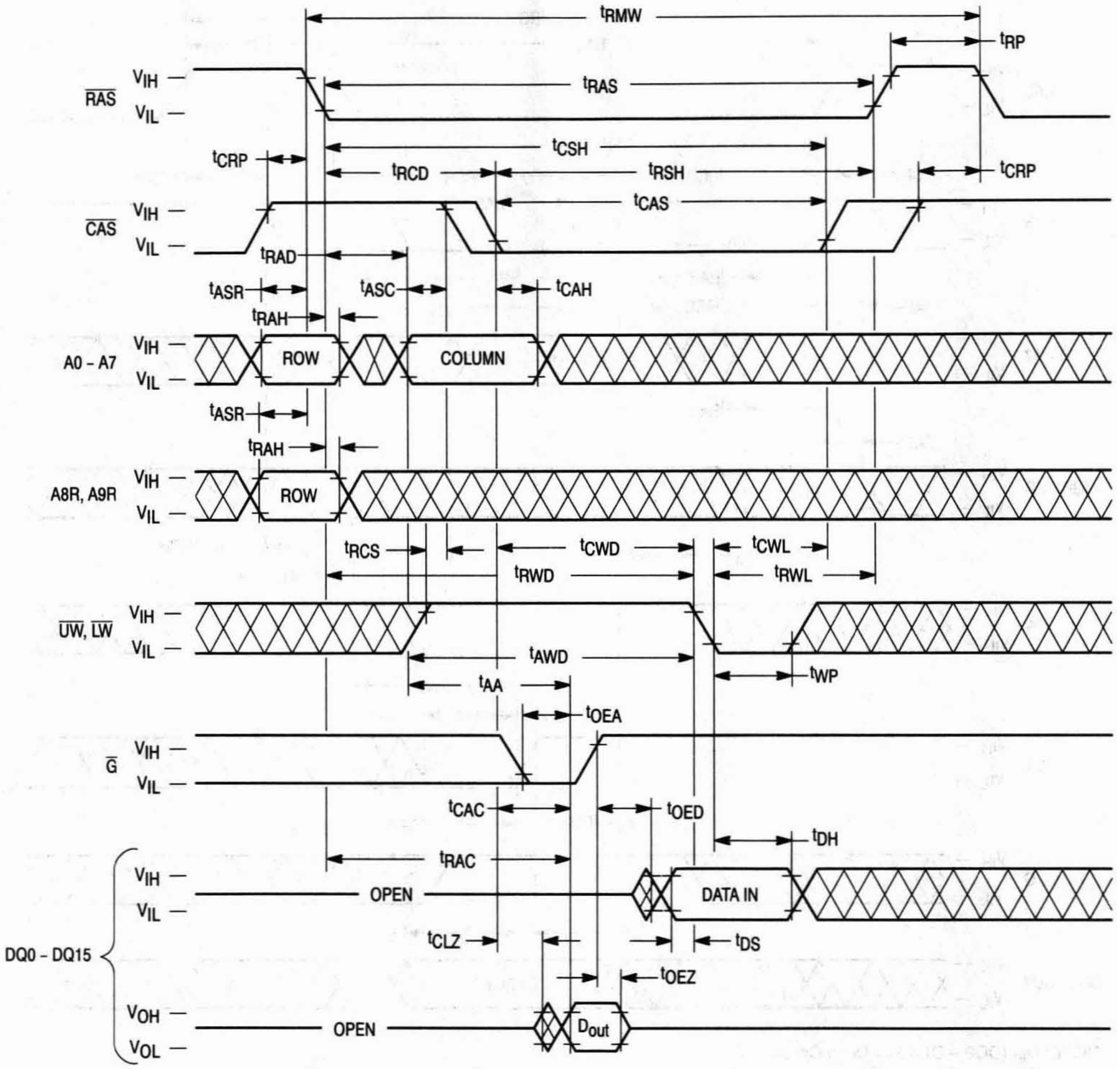
LOWER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



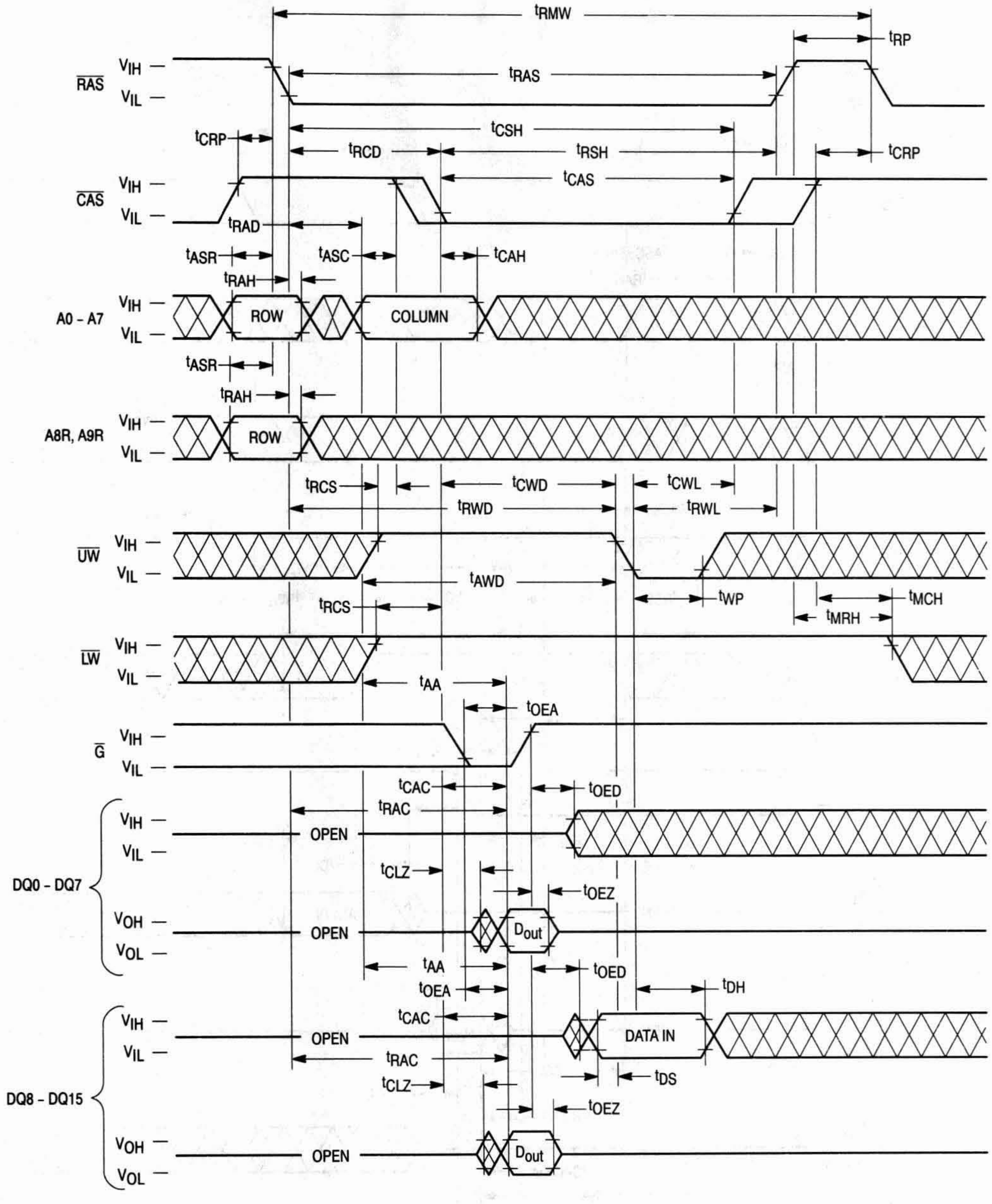
t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
$\overline{CAS}$
t_{CAS}
t_{RAD}
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 - A7
ROW
COLUMN
t_{RAH}
t_{ASR}
A8R, A9R
ROW
t_{MCS}
t_{MCH}
t_{MRH}
$\overline{UW}$
t_{CWL}
t_{RWL}
t_{WP}
$\overline{LW}$
t_{ODS}
t_{OEH}
$\overline{G}$
t_{DS}
t_{DH}
DQ0 - DQ7
DATA IN

NOTE: D_{in} (DQ8 – DQ15) = Don't Care
D_{out} = Open

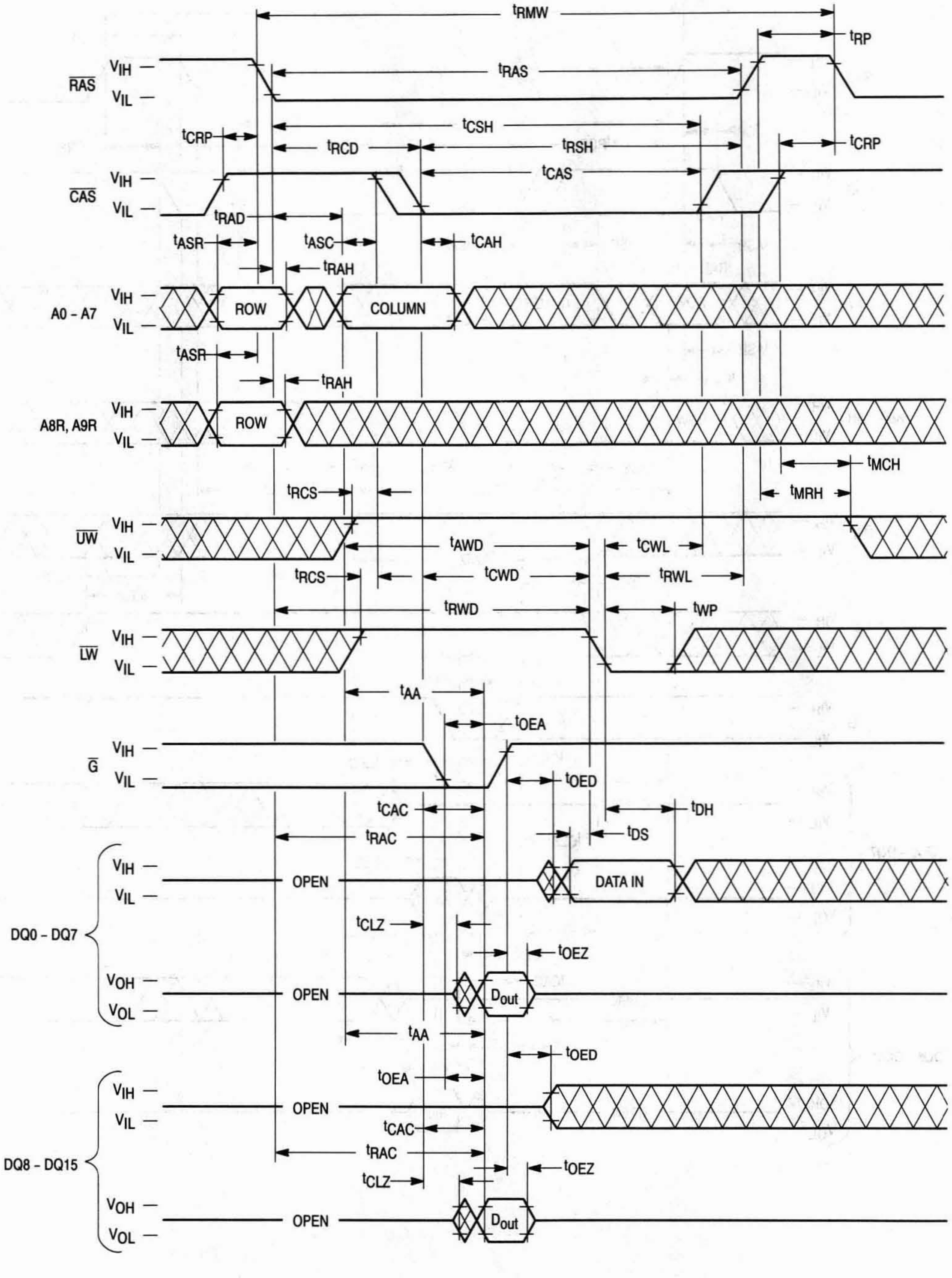
READ-MODIFY-WRITE CYCLE


t_{RMW}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RAS}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
t_{RAD}
t_{ASR}
t_{ASC}
t_{CAH}
t_{RAH}
A0 - A7
ROW
COLUMN
t_{ASR}
t_{RAH}
A8R, A9R
ROW
t_{RCS}
t_{CWD}
t_{CWL}
t_{RWD}
t_{RWL}
$\overline{UW}$, $\overline{LW}$
t_{AWD}
t_{WP}
t_{AA}
t_{OEA}
$\overline{G}$
t_{CAC}
t_{OED}
t_{DH}
t_{RAC}
DQ0 - DQ15
OPEN
DATA IN
t_{CLZ}
t_{DS}
t_{OEZ}
V_{OH}
V_{OL}
OPEN
D_{out}

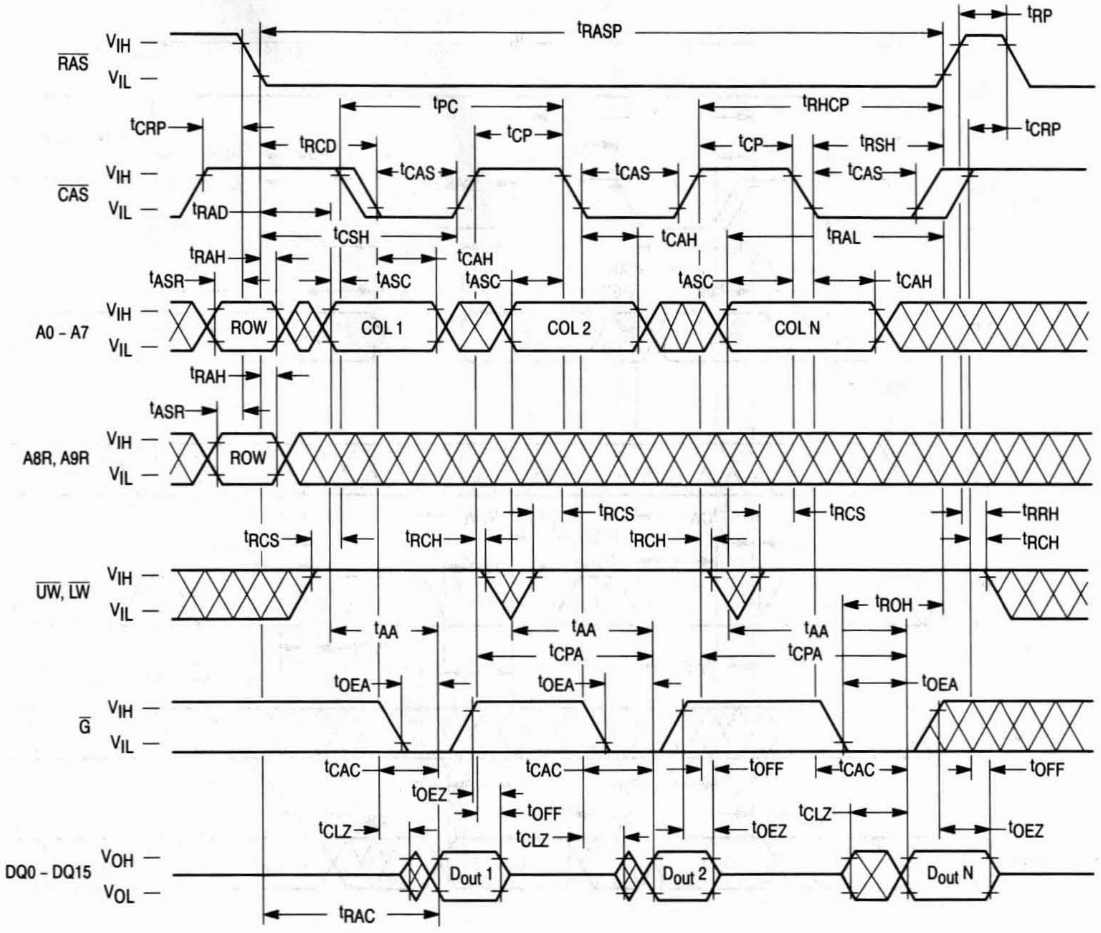
READ-MODIFY-UPPER-BYTE-WRITE CYCLE


tRMW
tRP
RAS
VIH
VIL
tRAS
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
VIH
VIL
tCAS
tRAD
tASR
tASC
tCAH
tRAH
A0 - A7
VIH
VIL
ROW
COLUMN
tASR
tRAH
A8R, A9R
VIH
VIL
ROW
tRCS
tCWD
tCWL
tRWD
tRWL
UW
VIH
VIL
tAWD
tWP
tMCH
tRCS
tMRH
LW
VIH
VIL
tAA
tOEA
G
VIH
VIL
tCAC
tOED
tRAC
DQ0 - DQ7
VIH
VIL
OPEN
tCLZ
tOEZ
VOH
VOL
OPEN
Dout
tAA
tOED
tOEA
tDH
tCAC
DQ8 - DQ15
VIH
VIL
OPEN
DATA IN
tRAC
tDS
tCLZ
tOEZ
VOH
VOL
OPEN
Dout

READ-MODIFY-LOWER-BYTE-WRITE CYCLE

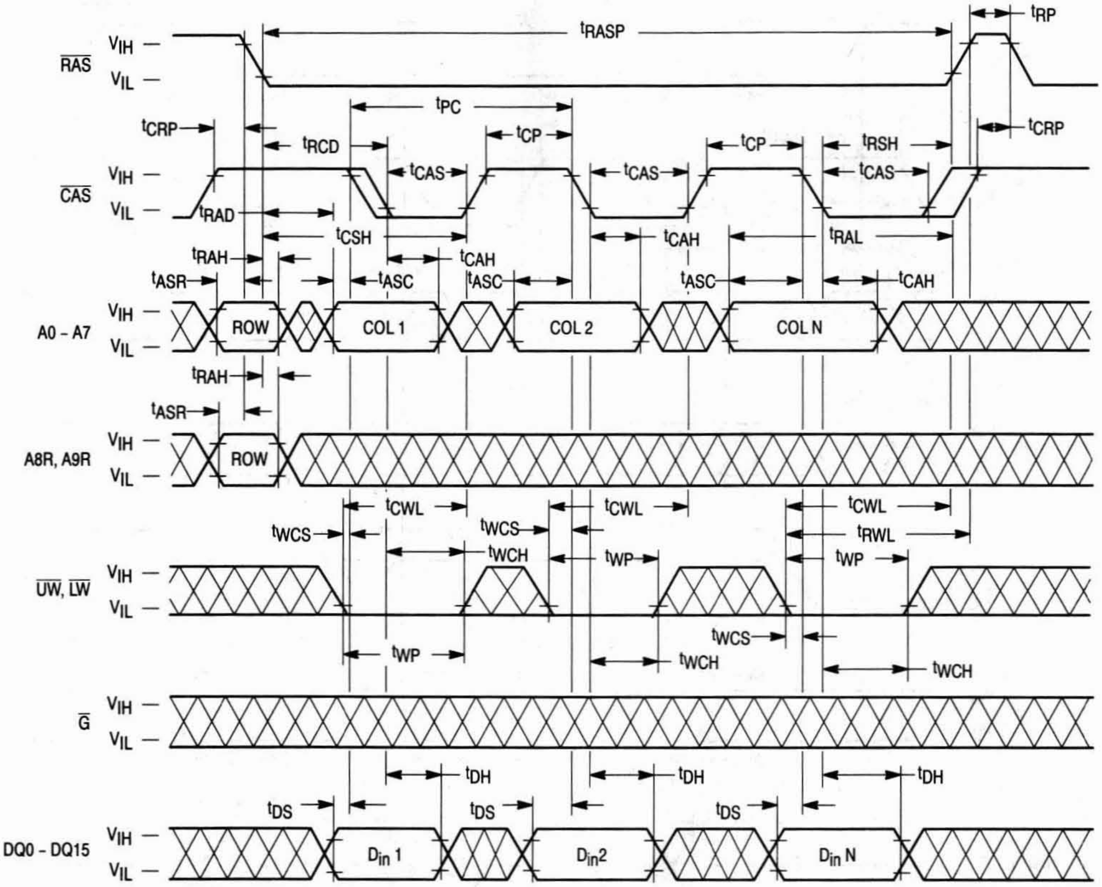

tRMW
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tRAD
tASR
tASC
tCAH
tRAH
A0 – A7
VIH
VIL
ROW
COLUMN
tASR
tRAH
A8R, A9R
VIH
VIL
ROW
tMCH
tMRH
tRCS
UW
VIH
VIL
tAWD
tCWL
tRCS
tCWD
tRWL
tRWD
tWP
LW
VIH
VIL
tAA
tOEA
G
VIH
VIL
tOED
tCAC
tDH
tRAC
tDS
DQ0 – DQ7
VIH
VIL
OPEN
DATA IN
tCLZ
tOEZ
VOH
VOL
OPEN
Dout
tAA
tOED
tOEA
DQ8 – DQ15
VIH
VIL
OPEN
tCAC
tRAC
tCLZ
tOEZ
VOH
VOL
OPEN
Dout

FAST PAGE MODE READ CYCLE


RAS
VIH
VIL
tRASP
tRP
tPC
tRHCP
tCRP
tRCD
tCP
tRSH
CAS
tCAS
tRAD
tCSH
tCAH
tRAL
tRAH
tASR
tASC
A0 - A7
ROW
COL 1
COL 2
COL N
A8R, A9R
tRCS
tRCH
tRRH
UW, LW
tROH
tAA
tCPA
tOEA
G
tCAC
tOFF
tOEZ
tCLZ
DQ0 - DQ15
VOH
VOL
Dout 1
Dout 2
Dout N
tRAC

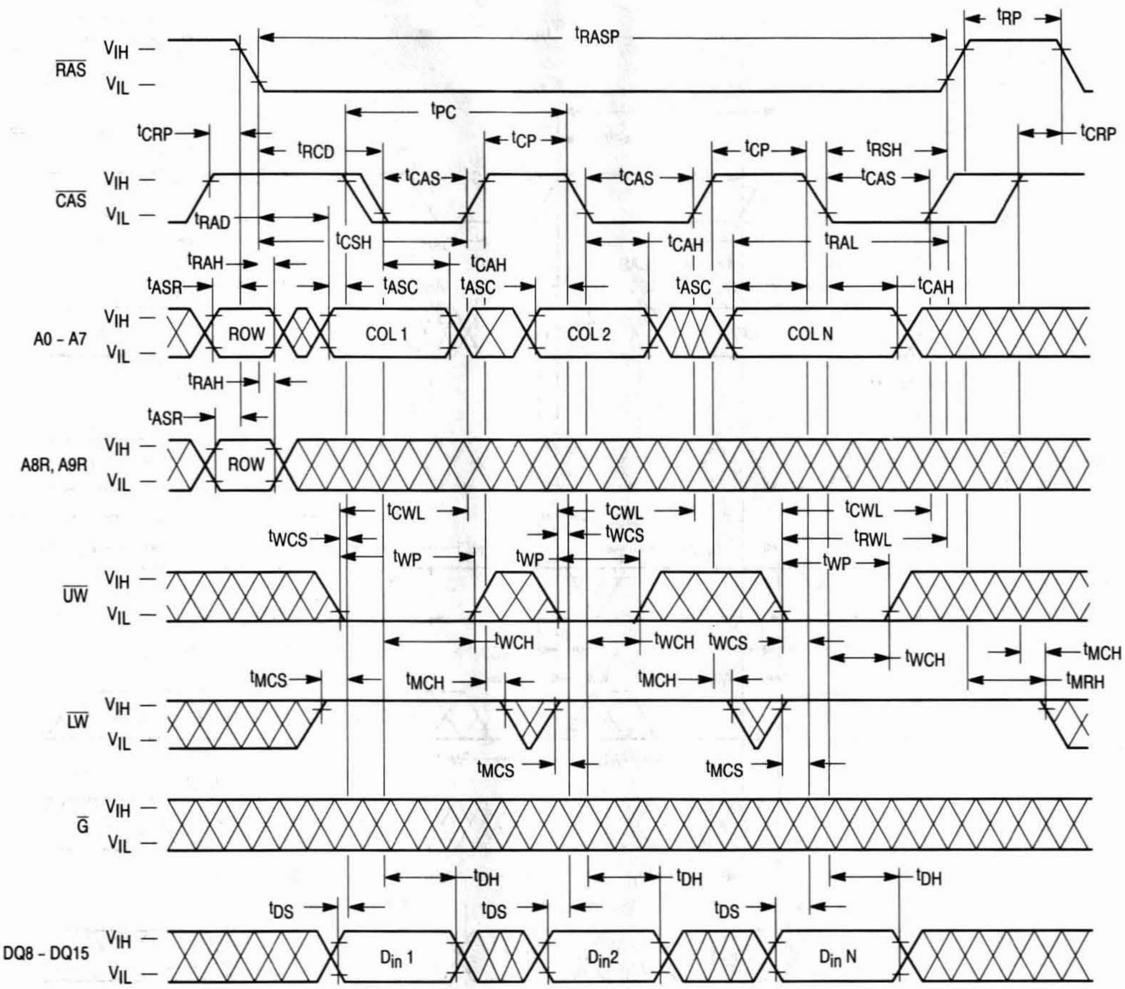
NOTE: D_{in} = Open

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)


$\overline{RAS}$
V_{IH}
V_{IL}
t_{RASP}
t_{RP}
t_{CRP}
t_{PC}
t_{RCD}
t_{CP}
t_{CAS}
t_{RSH}
$\overline{CAS}$
t_{RAD}
t_{CSH}
t_{CAH}
t_{RAL}
t_{RAH}
t_{ASR}
t_{ASC}
A0 - A7
ROW
COL 1
COL 2
COL N
A8R, A9R
t_{CWL}
t_{WCS}
t_{RWL}
t_{WCH}
t_{WP}
$\overline{UW}$, $\overline{LW}$
$\overline{G}$
t_{DH}
t_{DS}
DQ0 - DQ15
D_{in} 1
D_{in}2
D_{in} N

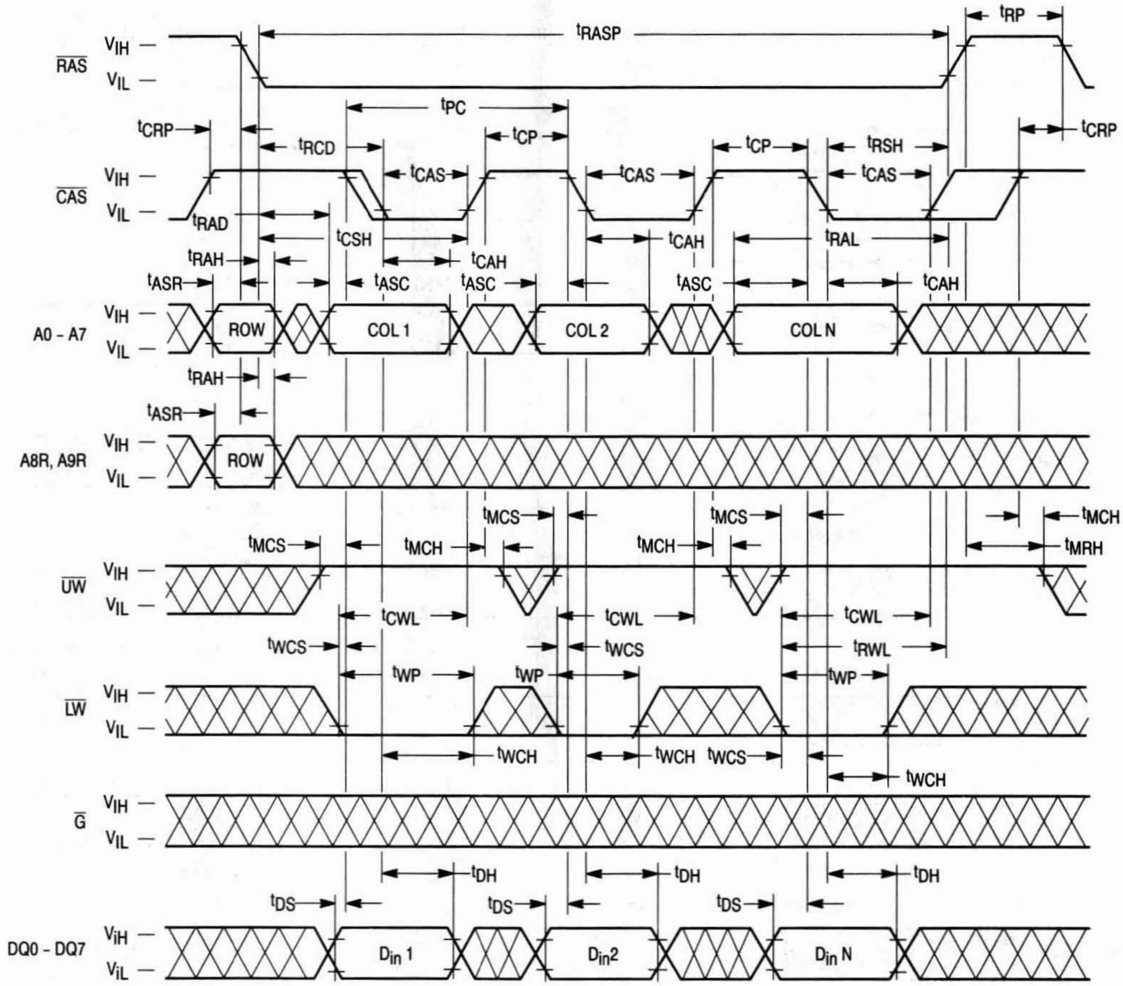
NOTE: D_{out} = Open

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)


RAS
CAS
A0 – A7
A8R, A9R
UW
LW
G
DQ8 – DQ15
VIH
VIL
tRASP
tRP
tPC
tCRP
tRCD
tCP
tRSH
tCAS
tRAD
tCSH
tCAH
tRAL
tRAH
tASR
tASC
ROW
COL 1
COL 2
COL N
tCWL
tWCS
tRWL
tWP
tWCH
tMCS
tMCH
tMRH
tDH
tDS
Din 1
Din2
Din N

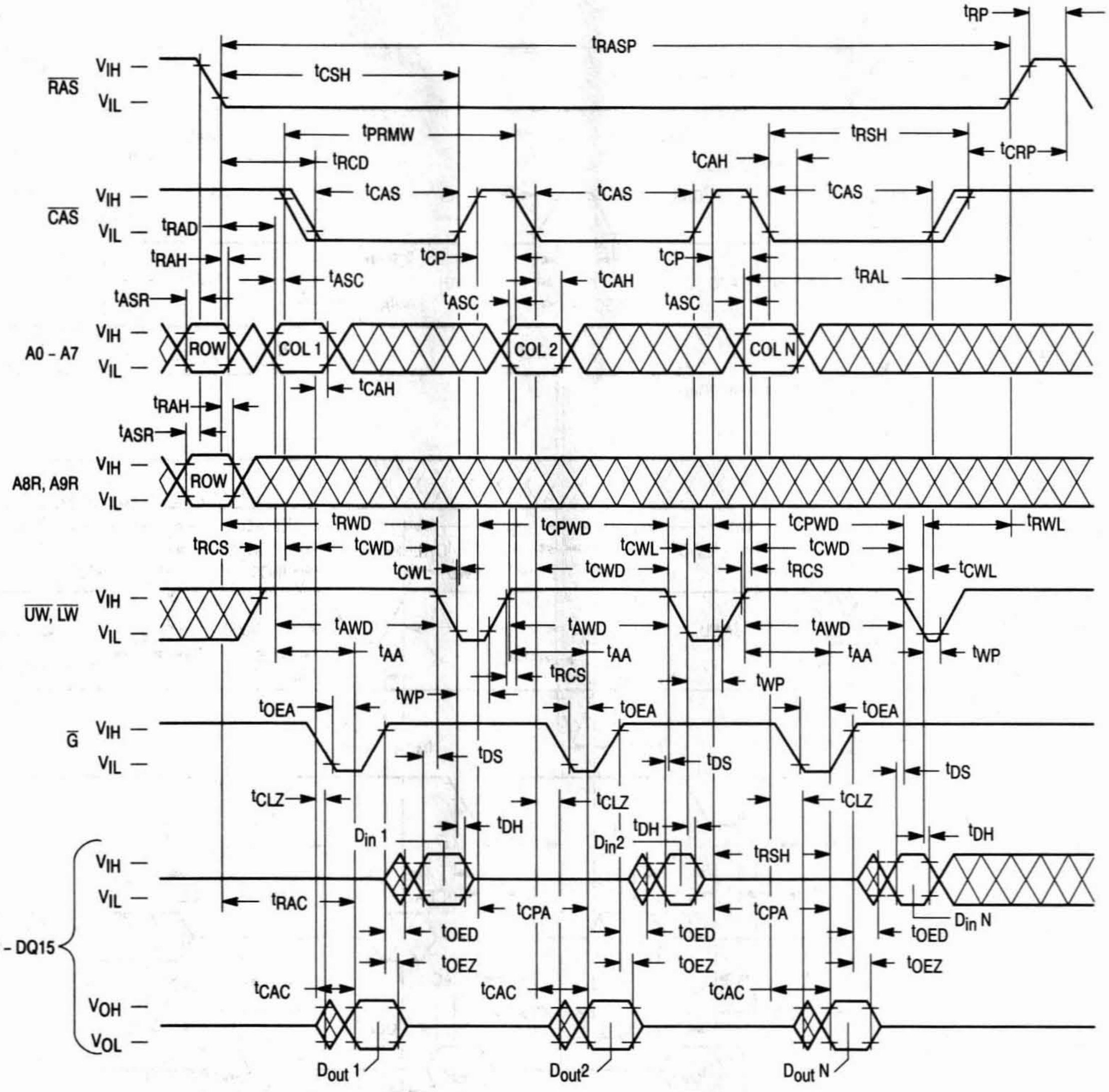
NOTE: D_{in} (DQ0 – DQ7) = Don't Care
D_{out} = Open

FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)


RAS
CAS
A0 - A7
A8R, A9R
UW
LW
G
DQ0 - DQ7
VIH
VIL
tRASP
tRP
tPC
tCRP
tRCD
tCP
tRSH
tCAS
tRAD
tCSH
tCAH
tRAL
tRAH
tASR
tASC
ROW
COL 1
COL 2
COL N
tMCS
tMCH
tMRH
tCWL
tWCS
tRWL
tWP
tWCH
tDH
tDS
Din 1
Din2
Din N

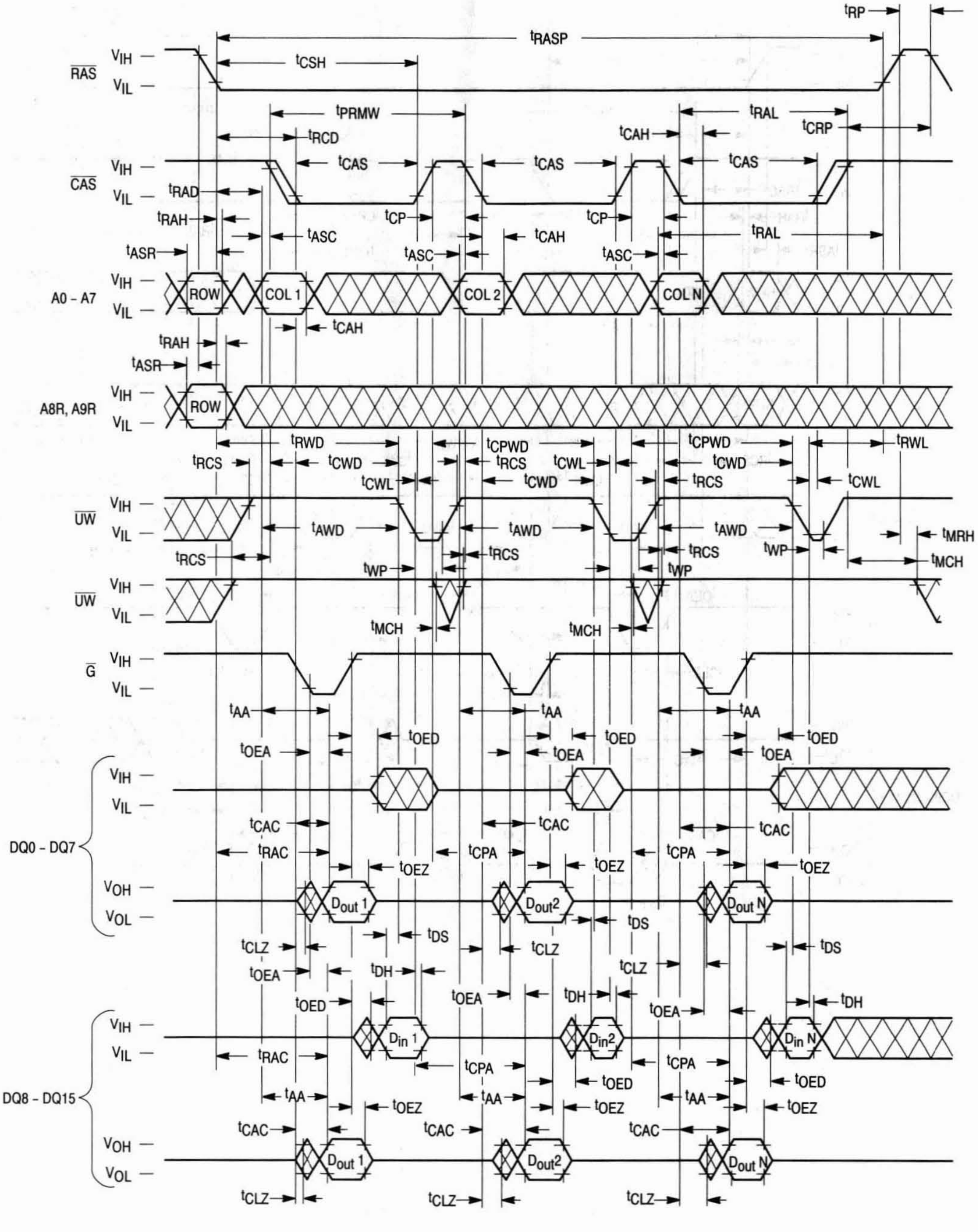
NOTE: D_{in} (DQ8 – DQ15) = Don't Care
D_{out} = Open

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

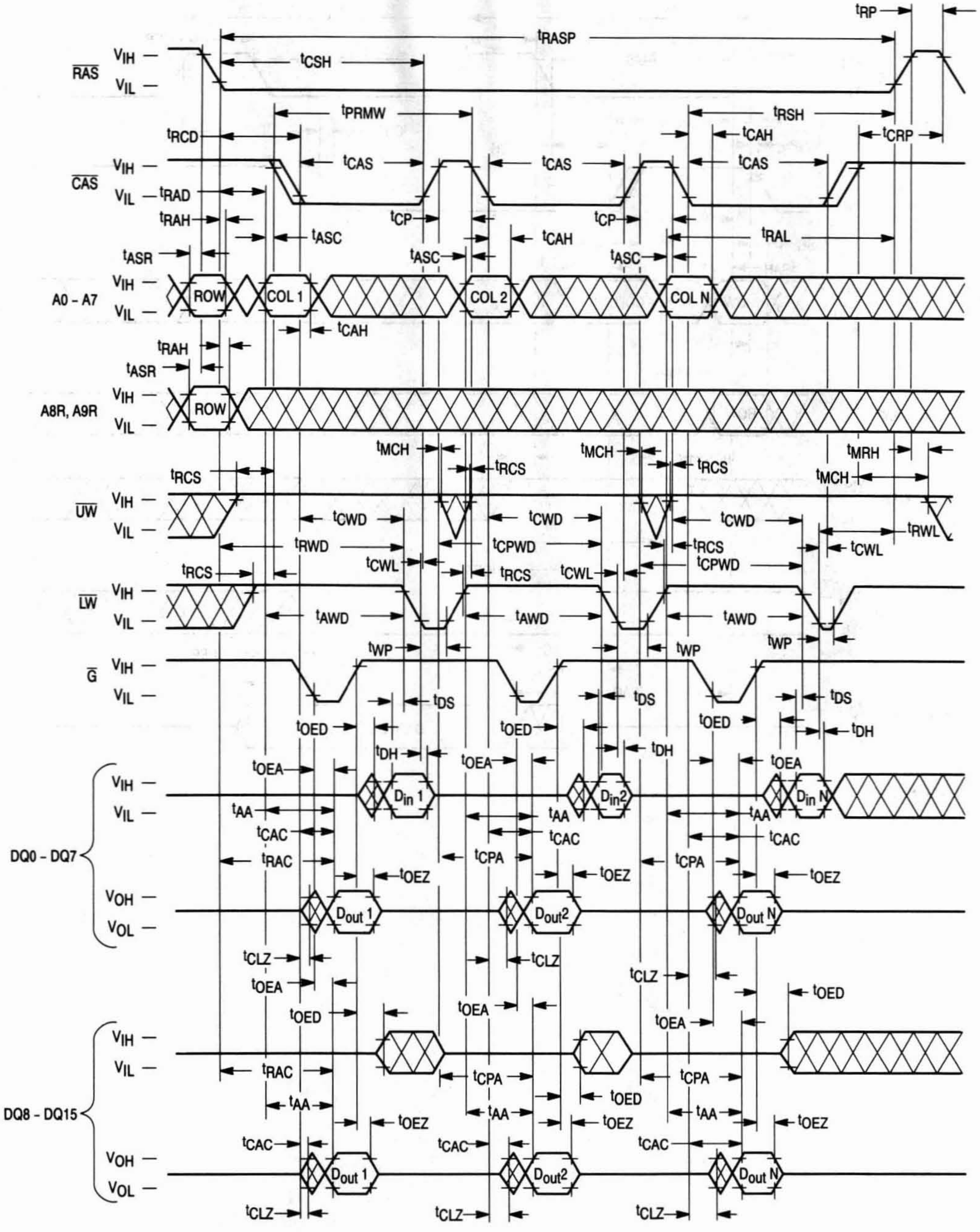


$\overline{RAS}$
$\overline{CAS}$
A0 - A7
A8R, A9R
$\overline{UW}$, $\overline{LW}$
$\overline{G}$
DQ0 - DQ15
V_{IH}
V_{IL}
V_{OH}
V_{OL}
t_{RP}
t_{RASP}
t_{CSH}
t_{PRMW}
t_{RSH}
t_{RCD}
t_{CAH}
t_{CRP}
t_{CAS}
t_{RAD}
t_{RAH}
t_{CP}
t_{ASC}
t_{RAL}
t_{ASR}
ROW
COL 1
COL 2
COL N
t_{RWD}
t_{CPWD}
t_{RWL}
t_{RCS}
t_{CWD}
t_{CWL}
t_{AWD}
t_{AA}
t_{WP}
t_{OEA}
t_{DS}
t_{CLZ}
t_{DH}
D_{in} 1
D_{in}2
D_{in} N
t_{RAC}
t_{CPA}
t_{OED}
t_{OEZ}
t_{CAC}
D_{out} 1
D_{out}2
D_{out} N

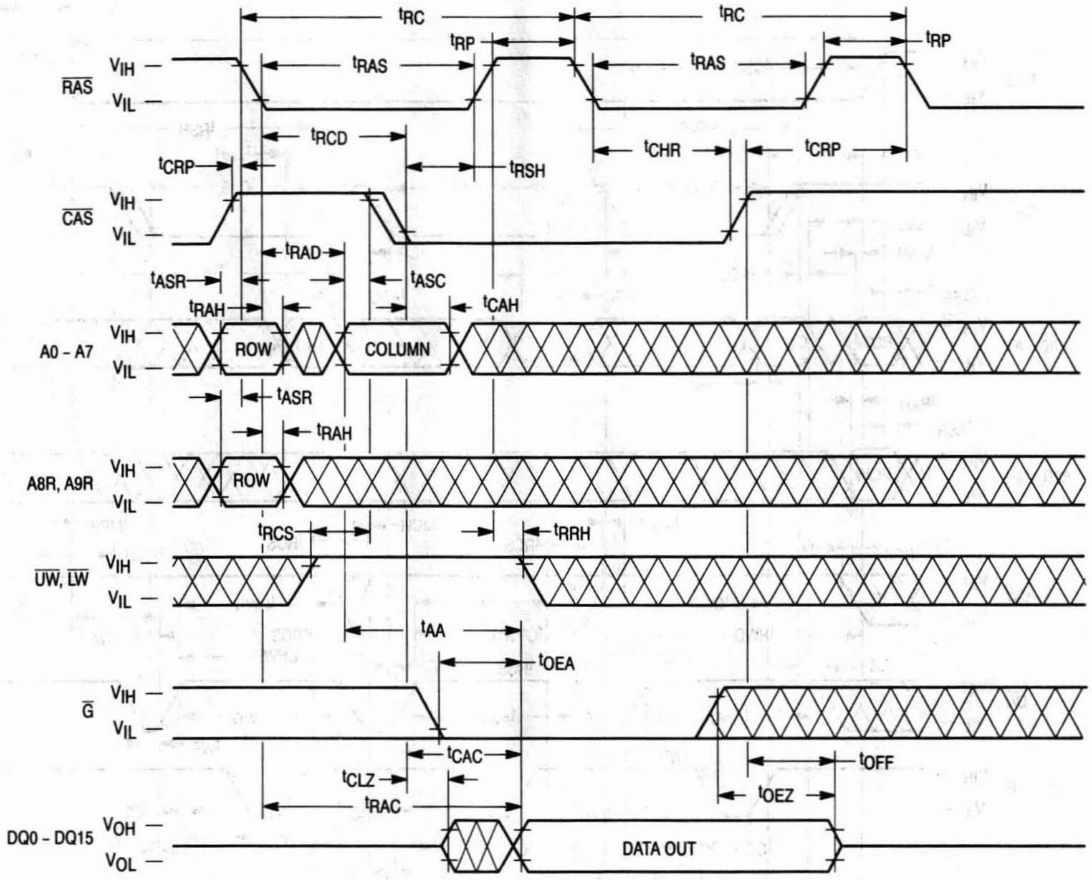
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE


RAS
CAS
A0 - A7
A8R, A9R
UW
UW
G
DQ0 - DQ7
DQ8 - DQ15
VIH
VIL
VOH
VOL
ROW
COL 1
COL 2
COL N
Dout 1
Dout2
Dout N
Din 1
Din2
Din N
tRP
tRASP
tCSH
tPRMW
tRCD
tRAL
tCAH
tCRP
tCAS
tRAD
tRAH
tCP
tASC
tASR
tRWD
tCPWD
tRWL
tRCS
tCWD
tCWL
tAWD
tWP
tMRH
tMCH
tAA
tOED
tOEA
tCAC
tRAC
tCPA
tOEZ
tDS
tCLZ
tDH

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE

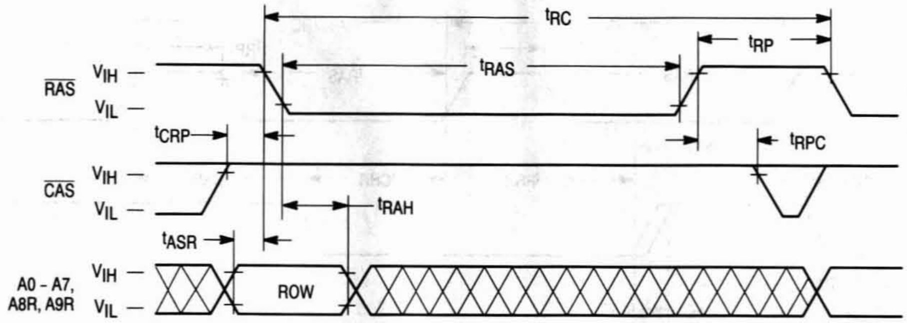

t_{RP}
t_{RASP}
t_{CSH}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{PRMW}
t_{RSH}
t_{RCD}
t_{CAH}
t_{CRP}
t_{CAS}
t_{CAS}
t_{CAS}
$\overline{CAS}$
t_{RAD}
t_{RAH}
t_{CP}
t_{CP}
t_{ASC}
t_{CAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{ASC}
A0 - A7
ROW
COL 1
COL 2
COL N
t_{CAH}
t_{RAH}
t_{ASR}
A8R, A9R
ROW
t_{MCH}
t_{RCS}
t_{MCH}
t_{RCS}
t_{MRH}
t_{RCS}
t_{MCH}
$\overline{UW}$
t_{CWD}
t_{CWD}
t_{CWD}
t_{RWL}
t_{RWD}
t_{CPWD}
t_{RCS}
t_{CWL}
t_{CWL}
t_{RCS}
t_{CWL}
t_{CPWD}
t_{RCS}
$\overline{LW}$
t_{AWD}
t_{AWD}
t_{AWD}
t_{WP}
t_{WP}
t_{WP}
$\overline{G}$
t_{DS}
t_{DS}
t_{DS}
t_{OED}
t_{OED}
t_{OED}
t_{DH}
t_{DH}
t_{DH}
t_{OEA}
t_{OEA}
t_{OEA}
DQ0 - DQ7
V_{OH}
V_{OL}
D_{in} 1
D_{in}2
D_{in} N
t_{AA}
t_{AA}
t_{AA}
t_{CAC}
t_{CAC}
t_{CAC}
t_{RAC}
t_{CPA}
t_{CPA}
t_{OEZ}
t_{OEZ}
t_{OEZ}
D_{out} 1
D_{out}2
D_{out} N
t_{CLZ}
t_{CLZ}
t_{CLZ}
t_{OEA}
t_{OEA}
t_{OEA}
t_{OED}
t_{OED}
t_{OED}
DQ8 - DQ15
t_{RAC}
t_{CPA}
t_{CPA}
t_{AA}
t_{AA}
t_{AA}
t_{OEZ}
t_{OEZ}
t_{OEZ}
t_{CAC}
t_{CAC}
t_{CAC}
D_{out} 1
D_{out}2
D_{out} N
t_{CLZ}
t_{CLZ}
t_{CLZ}

HIDDEN REFRESH CYCLE (READ)


tRC
tRC
tRP
tRP
tRAS
tRAS
RAS
VIH
VIL
tRCD
tRSH
tCHR
tCRP
tCRP
CAS
tRAD
tASR
tASC
tRAH
tCAH
A0 - A7
ROW
COLUMN
tASR
tRAH
A8R, A9R
ROW
tRCS
tRRH
UW, LW
tAA
tOEA
G
tCAC
tOFF
tCLZ
tOEZ
tRAC
DQ0 - DQ15
VOH
VOL
DATA OUT

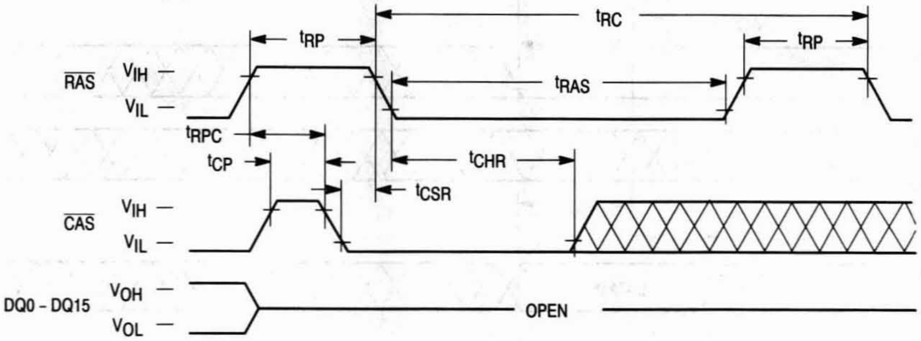
NOTE: D_{in} = Open

$\overline{\text{RAS}}$-ONLY REFRESH CYCLE


t_{RC}
t_{RP}
t_{RAS}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
A0 - A7, A8R, A9R
V_{IH}
V_{IL}
ROW

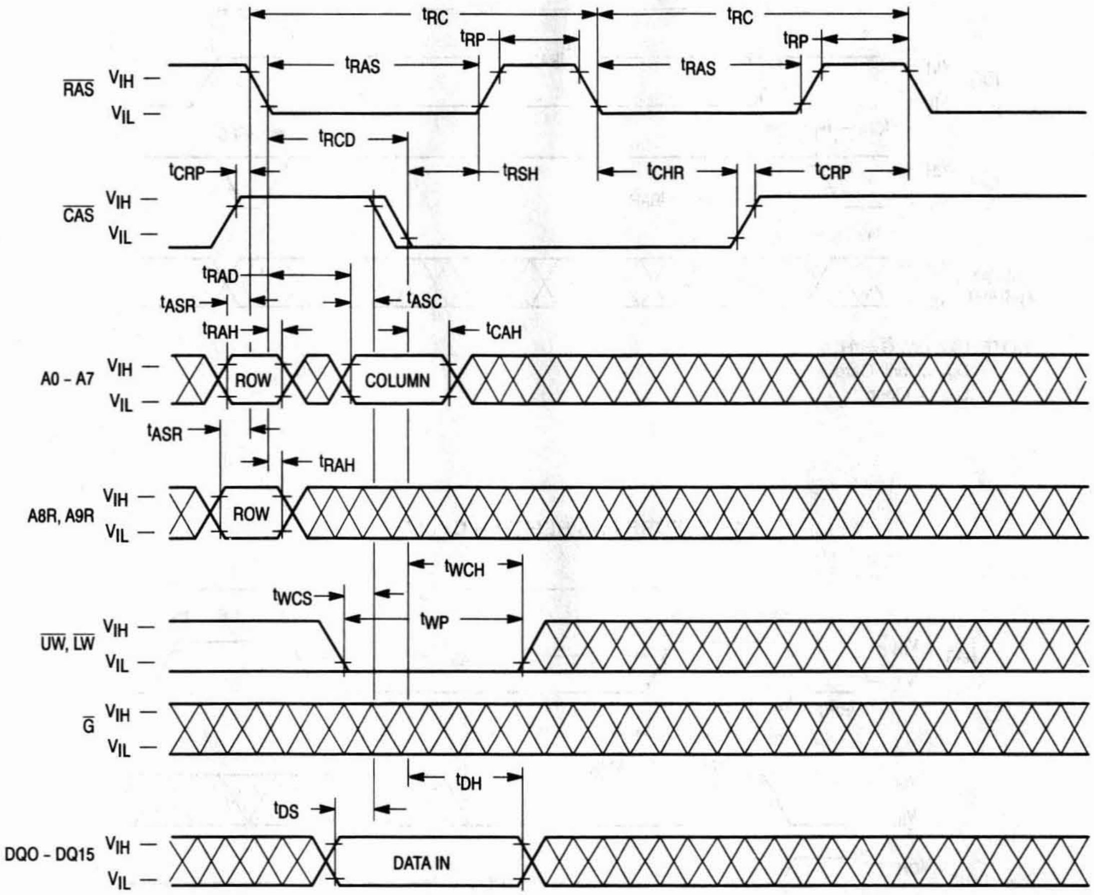
NOTE: $\overline{\text{UW}}$, $\overline{\text{LW}}$, $\overline{\text{G}}$ = "H" or "L"
D_{in} = Don't Care
D_{out} = Open

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE


t_{RC}
t_{RP}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RAS}
t_{RPC}
t_{CP}
t_{CHR}
t_{CSR}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
DQ0 - DQ15
V_{OH}
V_{OL}
OPEN

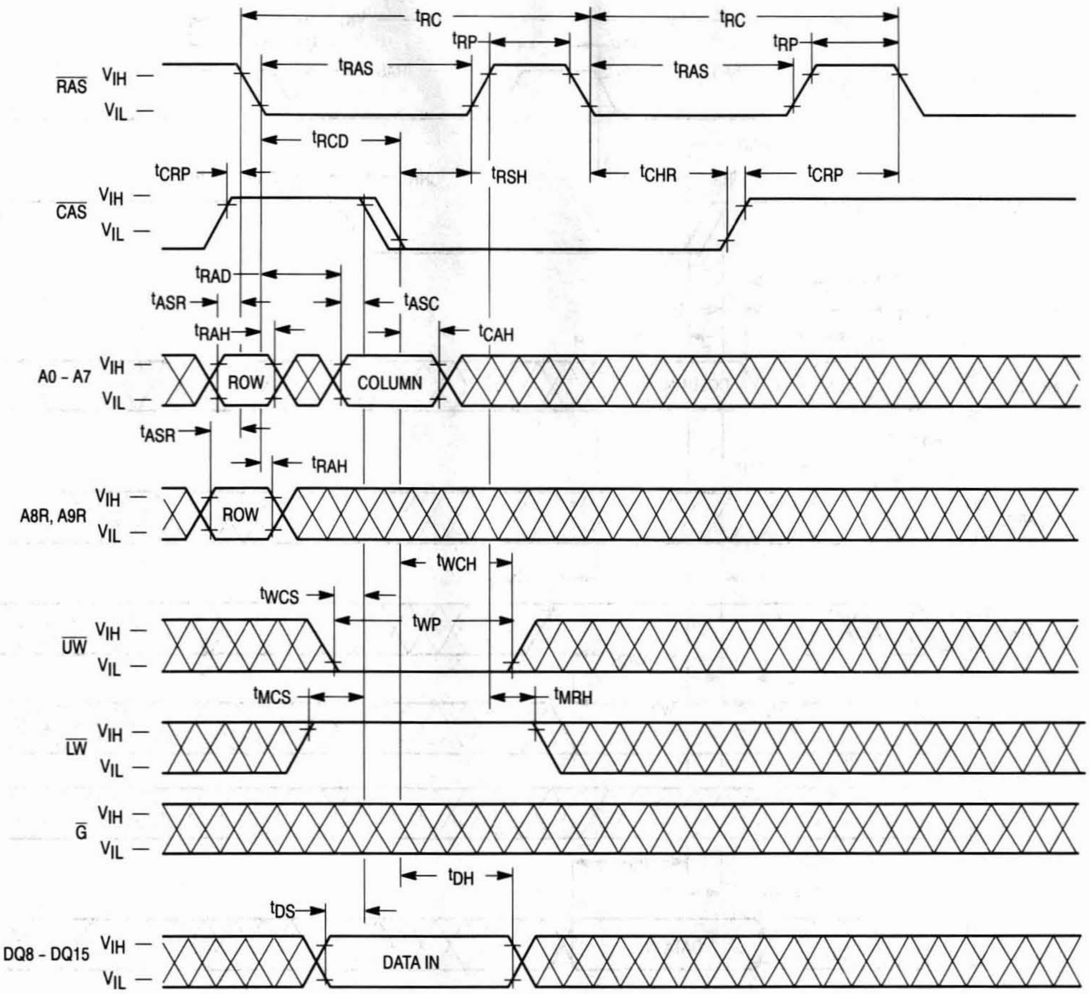
NOTE: $\overline{\text{UW}}$, $\overline{\text{LW}}$, $\overline{\text{G}}$, A0 – A7, A8R, A9R = "H" or "L"
D_{in} = Open

HIDDEN REFRESH CYCLE (WRITE)


tRC
tRC
tRP
tRP
tRAS
tRAS
RAS
VIH
VIL
tRCD
tCRP
tRSH
tCHR
tCRP
CAS
VIH
VIL
tRAD
tASR
tASC
tRAH
tCAH
A0 - A7
VIH
VIL
ROW
COLUMN
tASR
tRAH
A8R, A9R
VIH
VIL
ROW
tWCH
tWCS
tWP
UW, LW
VIH
VIL
G
VIH
VIL
tDH
tDS
DQ0 - DQ15
VIH
VIL
DATA IN

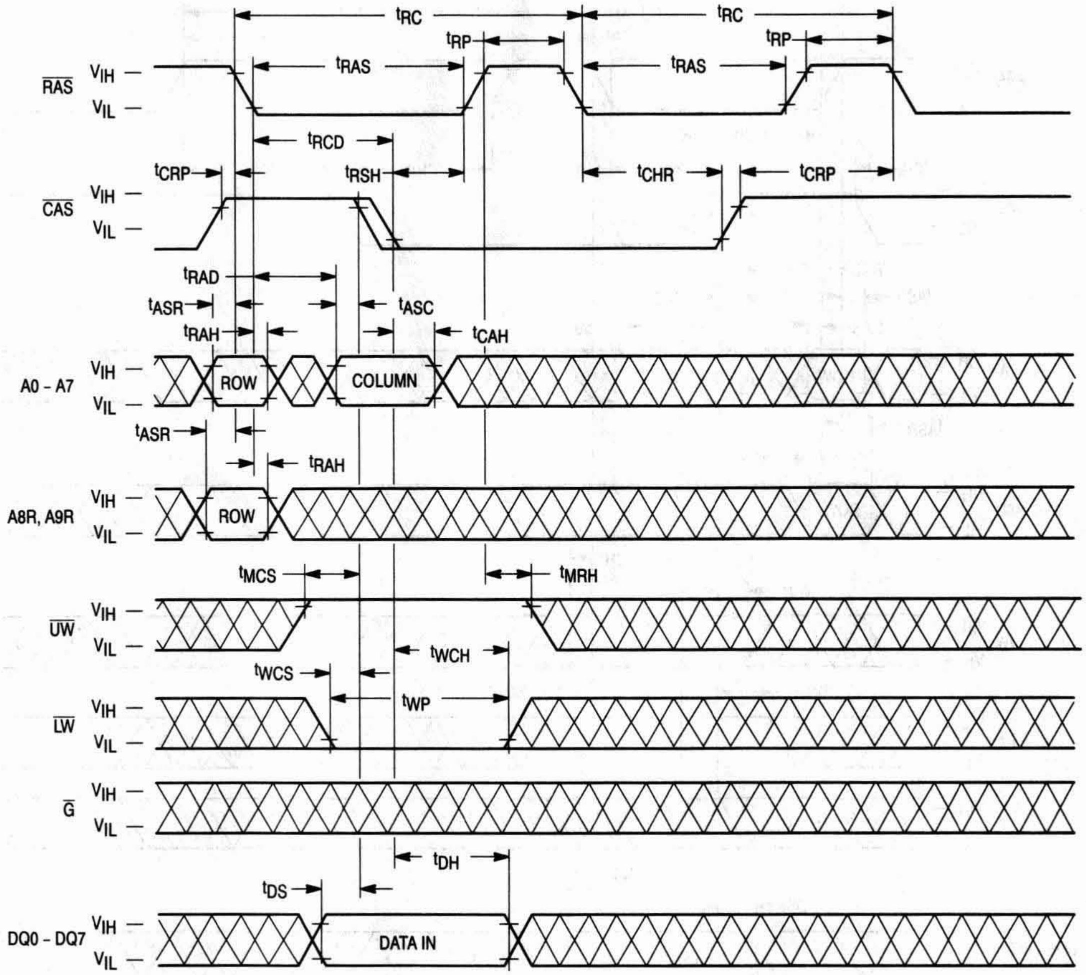
D_{out} = Open

HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)


tRC
tRC
tRP
tRP
tRAS
tRAS
RAS
VIH
VIL
tRCD
tCRP
tRSH
tCHR
tCRP
CAS
VIH
VIL
tRAD
tASR
tASC
tRAH
tCAH
A0 - A7
VIH
VIL
ROW
COLUMN
tASR
tRAH
A8R, A9R
VIH
VIL
ROW
tWCH
tWCS
tWP
UW
VIH
VIL
tMCS
tMRH
LW
VIH
VIL
G
VIH
VIL
tDH
tDS
DQ8 - DQ15
VIH
VIL
DATA IN

NOTE: D_{in} (DQ0 – DQ7) = Don't Care
D_{out} = Open

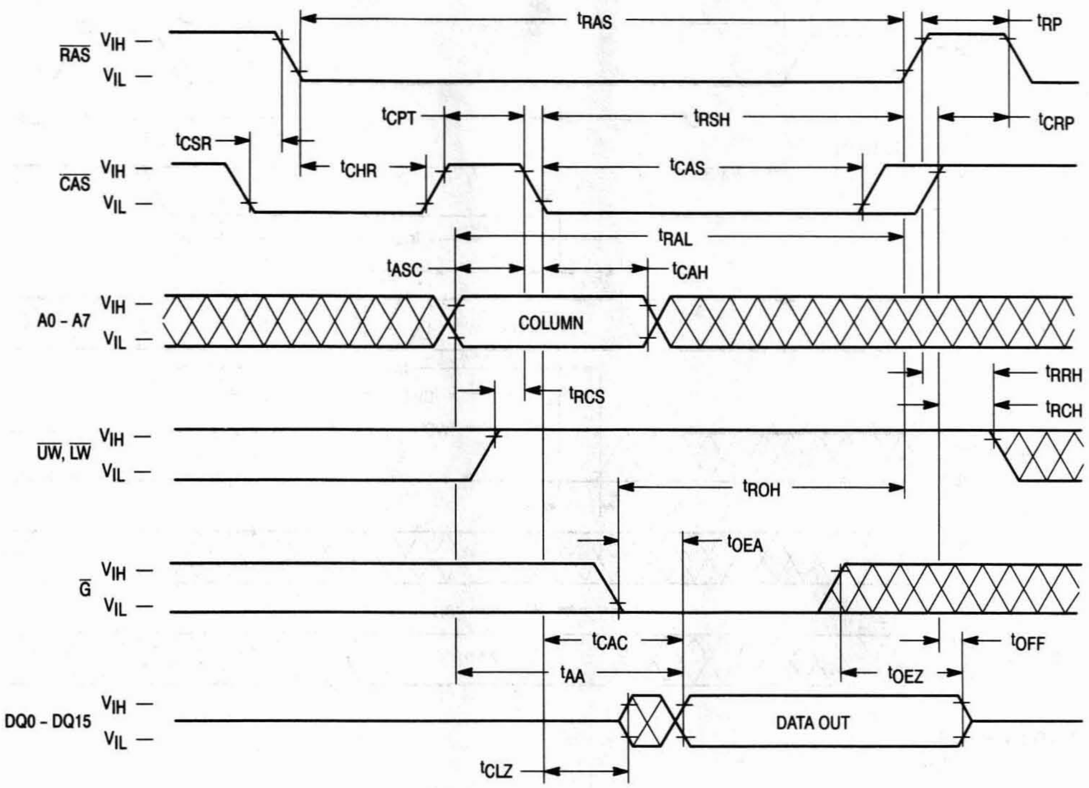
HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



t_{RC}
t_{RC}
t_{RP}
t_{RP}
t_{RAS}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RCD}
t_{CRP}
t_{RSH}
t_{CHR}
t_{CRP}
$\overline{CAS}$
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
A0 - A7
ROW
COLUMN
t_{ASR}
t_{RAH}
A8R, A9R
ROW
t_{MCS}
t_{MRH}
$\overline{UW}$
t_{WCH}
t_{WCS}
t_{WP}
$\overline{LW}$
$\overline{G}$
t_{DH}
t_{DS}
DQ0 - DQ7
DATA IN

NOTE: D_{in} (DQ8 – DQ15) = Don't Care
D_{out} = Open

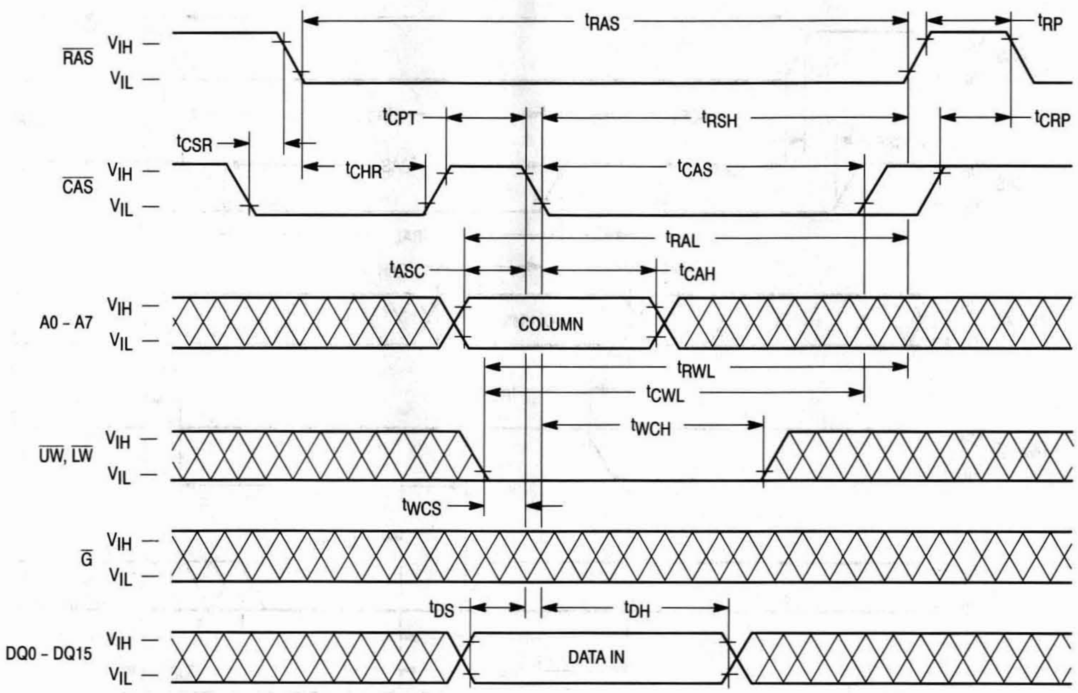
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



$\overline{RAS}$
V_{IH} —
V_{IL} —
$\overline{CAS}$
V_{IH} —
V_{IL} —
A0 - A7
V_{IH} —
V_{IL} —
$\overline{UW}$, $\overline{LW}$
V_{IH} —
V_{IL} —
$\overline{G}$
V_{IH} —
V_{IL} —
DQ0 - DQ15
V_{IH} —
V_{IL} —
t_{RAS}
t_{RP}
t_{CPT}
t_{RSH}
t_{CRP}
t_{CSR}
t_{CHR}
t_{CAS}
t_{RAL}
t_{ASC}
t_{CAH}
COLUMN
t_{RRH}
t_{RCS}
t_{RCH}
t_{ROH}
t_{OEA}
t_{CAC}
t_{OFF}
t_{AA}
t_{OEZ}
DATA OUT
t_{CLZ}

NOTE: A8R, A9R = "H" or "L"
D_{out} = Open

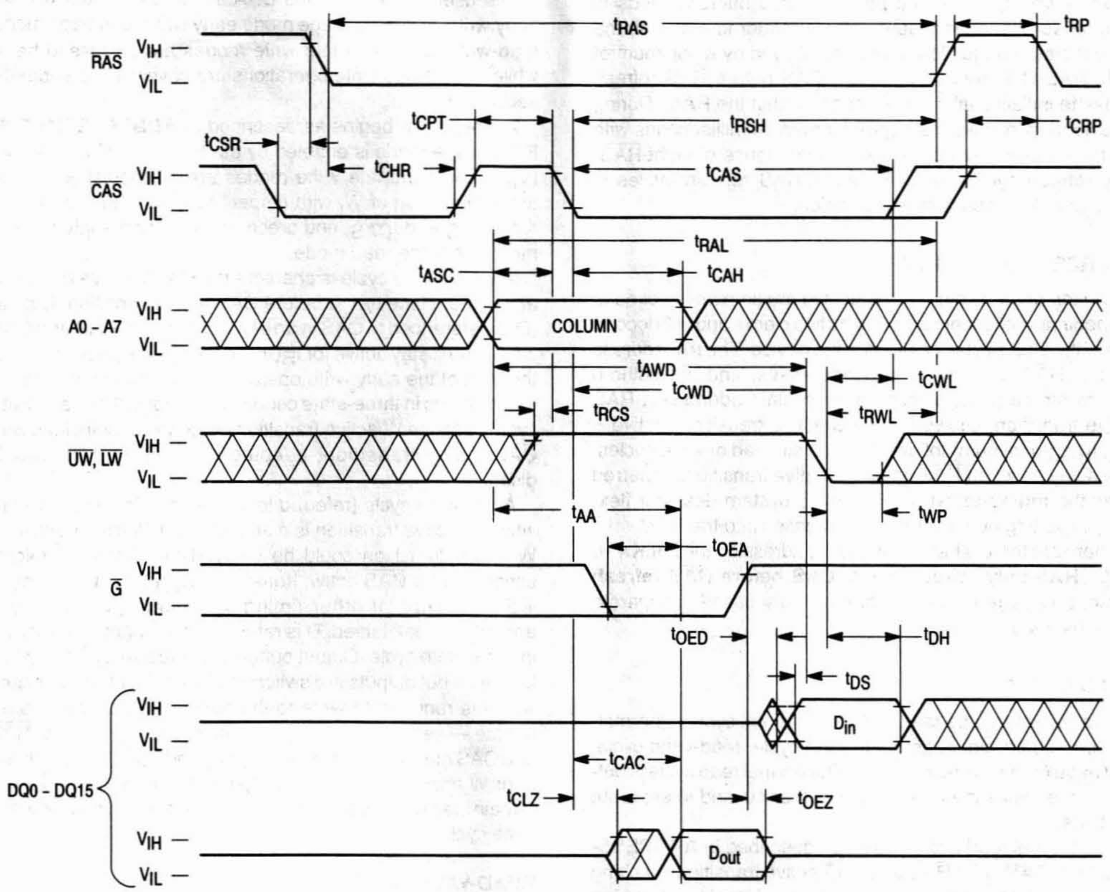
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST WRITE CYCLE



t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CPT}
t_{RSH}
t_{CRP}
t_{CSR}
t_{CHR}
t_{CAS}
$\overline{\text{CAS}}$
t_{RAL}
t_{ASC}
t_{CAH}
A0 – A7
COLUMN
t_{RWL}
t_{CWL}
t_{WCH}
$\overline{\text{UW}}$, $\overline{\text{LW}}$
t_{WCS}
$\overline{\text{G}}$
t_{DS}
t_{DH}
DQ0 – DQ15
DATA IN

NOTE: A8R, A9R = "H" or "L"
D_{out} = Open

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE


tRAS
tRP
RAS
VIH
VIL
tCPT
tRSH
tCRP
tCSR
tCHR
tCAS
CAS
tRAL
tASC
tCAH
A0 - A7
COLUMN
tAWD
tCWL
tCWD
tRCS
tRWL
UW, LW
tAA
tWP
tOEA
G
tOED
tDH
tDS
Din
DQ0 - DQ15
tCAC
tCLZ
tOEZ
Dout

NOTE: A8R, A9R = "H" or "L"

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight $\overline{\text{RAS}}$-Only refresh cycles or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight $\overline{\text{RAS}}$-only refresh cycles or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks and will decode one of the 262,144 bit locations in the device. The row address strobe ($\overline{\text{RAS}}$) latches 10 row addresses, and the column access strobe ($\overline{\text{CAS}}$) latches eight column addresses. $\overline{\text{RAS}}$ active transition followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) follows $\overline{\text{RAS}}$ on all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

There are three other variations in addressing the 256K x 16 RAM: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{\text{CAS}}$ and output enable ($\overline{\text{G}}$) control read access time: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum, and $\overline{\text{G}}$ must be active t_{RAC}-t_{GA} (both minimum) to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{\text{G}}$ active transition does not occur in time, read access time is determined by either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ and $\overline{\text{G}}$ clocks are active. When either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers and $\overline{\text{G}}$ disabled.

A late write cycle (referred to as $\overline{\text{G}}$-controlled write) occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but outputs are switched off by $\overline{\text{G}}$ inactive transition, which is required to write to the device. Q may be indeterminate — see note 12 of AC Operating Conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle. $\overline{\text{G}}$ must remain inactive for t_{GH} after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the 256K x 16 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in the prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order.

The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54170B require refresh every 16 milliseconds, while refresh for the MCM5L4170B and MCM5V4170B is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54170B, and 124.8 microseconds for the MCM5L4170B and MCM5V4170B. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54170B, and 128 milliseconds for the MCM5L4170B and MCM5V4170B.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decodes. Three other methods of refresh, **$\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh,** and **self refresh** (MCM5V4170B only) are available on this device for greater system flexibility.

$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure that all rows are refreshed within the specified limit.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before $\overline{RAS}$. This clock order actives an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CAS}$ active at the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CAS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1).

Self Refresh (MCM5V4170B Only)

The self refresh is a $\overline{CAS}$ before $\overline{RAS}$ refresh where $\overline{RAS}$ is held low for a period greater than t_{RASS} (100 microseconds). After this time, an internal timer activates a refresh operation of consecutive row addresses in the dynamic RAM. The self refresh mode is exited when either $\overline{RAS}$ or $\overline{CAS}$ transitions to high (V_{IH}). Because of the long periods involved for this method of refresh, it is recommended that the self refresh mode only be used for long periods of standby, such as a battery backup.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **eight $\overline{CAS}$ before $\overline{RAS}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

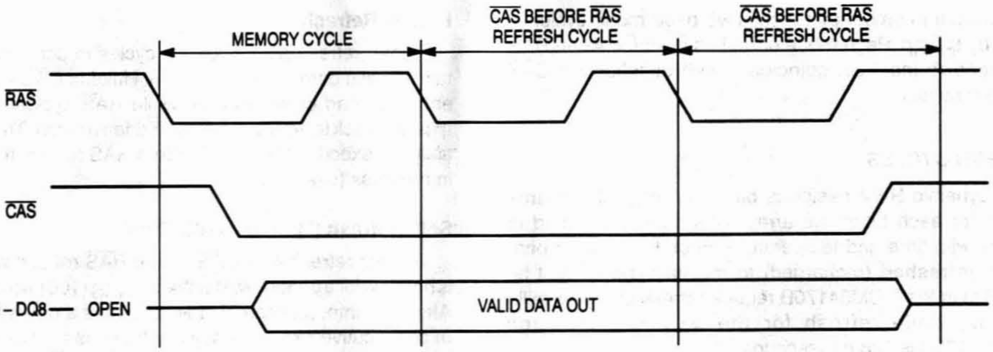
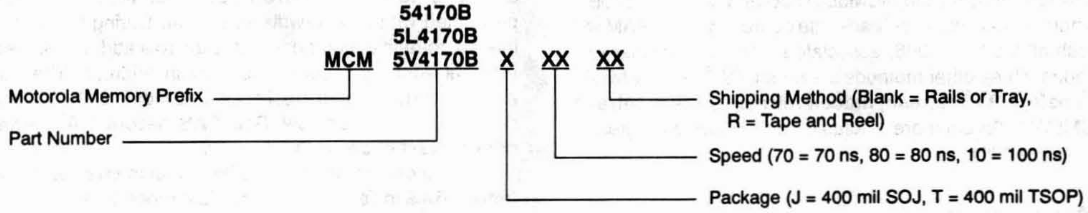

MEMORY CYCLE
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
$\overline{RAS}$
$\overline{CAS}$
DQ0 – DQ8 — OPEN
VALID DATA OUT

Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)


54170B
5L4170B
MCM 5V4170B X XX XX
Motorola Memory Prefix
Part Number
Shipping Method (Blank = Rails or Tray, R = Tape and Reel)
Speed (70 = 70 ns, 80 = 80 ns, 10 = 100 ns)
Package (J = 400 mil SOJ, T = 400 mil TSOP)

Full Part Numbers —	MCM54170BJ70	MCM5L4170BJ70	MCM5V4170BJ70
	MCM54170BJ80	MCM5L4170BJ80	MCM5V4170BJ80
	MCM54170BJ10	MCM5L4170BJ10	MCM5V4170BJ10
	MCM54170BT70	MCM5L4170BT70	MCM5V4170BT70
	MCM54170BT80	MCM5L4170BT80	MCM5V4170BT80
	MCM54170BT10	MCM5L4170BT10	MCM5V4170BT10
	MCM54170BJ70R	MCM5L4170BJ70R	MCM5V4170BJ70R
	MCM54170BJ80R	MCM5L4170BJ80R	MCM5V4170BJ80R
	MCM54170BJ10R	MCM5L4170BJ10R	MCM5V4170BJ10R
	MCM54170BT70R	MCM5L4170BT70R	MCM5V4170BT70R
	MCM54170BT80R	MCM5L4170BT80R	MCM5V4170BT80R
	MCM54170BT10R	MCM5L4170BT10R	MCM5V4170BT10R

NOTE: For mechanical data, please see Chapter 10.

MCM54190B
MCM5L4190B
MCM5V4190B

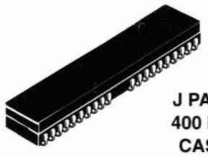
Product Preview

256K x 18 CMOS Dynamic RAM
Fast Page Mode – 1 CAS, 2 Write Enables

The MCM54190B is a 0.6μ CMOS high-speed dynamic random access memory. It is organized as 262,144 eighteen-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM54190B requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 400 mil SOJ plastic package and a 400 mil thin-small-outline package (TSOP).

- Three-State Data Output
- Fast Page Mode
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- Self Refresh (MCM5V4190B only)
- 1024 Cycle Refresh:
  MCM54190B = 16 ms
  MCM5L4190B and MCM5V4190B = 128 ms
- Fast Access Time (t_{RAC}):
  MCM54190B-70, MCM5L4190B-70, and MCM5V4190B-70 = 70 ns (Max)
  MCM54190B-80, MCM5L4190B-80, and MCM5V4190B-80 = 80 ns (Max)
  MCM54190B-10, MCM5L4190B-10, and MCM5V4190B-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM54190B-70, MCM5L4190B-70, and MCM5V4190B-70 = 385 mW (Max)
  MCM54190B-80, MCM5L4190B-80, and MCM5V4190B-80 = 330 mW (Max)
  MCM54190B-10, MCM5L4190B-10, and MCM5V4190B-10 = 303 mW (Max)
- Low Standby Power Dissipation:
  MCM54190B, MCM5L4190B, and MCM5V4190B = 5.5 mW (Max, TTL Levels)
- Battery Backup Power Dissipation:
  MCM5L4190B = 1.7 mW (Max, Battery Backup Mode, t_{RC} =125 μs)
- Self Refresh Power Dissipation:
  MCM5V4190B = 1.1 mW (Max, Self Refresh Mode)



**J PACKAGE
400 MIL SOJ
CASE TBD**

**T PACKAGE
400 MIL TSOP
CASE TBD**

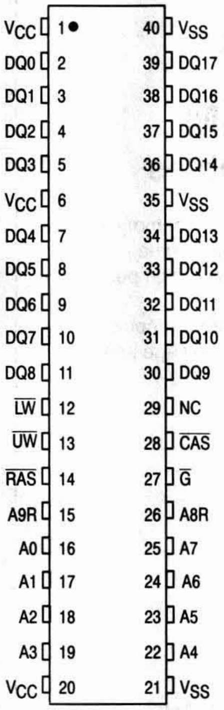
PIN NAMES

A0 – A7, A8R, A9R	Address Input
DQ0 – DQ17	Data Input/Output
$\overline{\text{LW}}$, $\overline{\text{UW}}$	Read/Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connection
$\overline{\text{G}}$	Output Enable

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

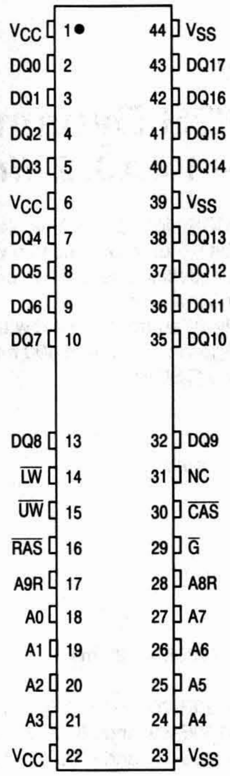
PIN ASSIGNMENTS

400 MIL SOJ



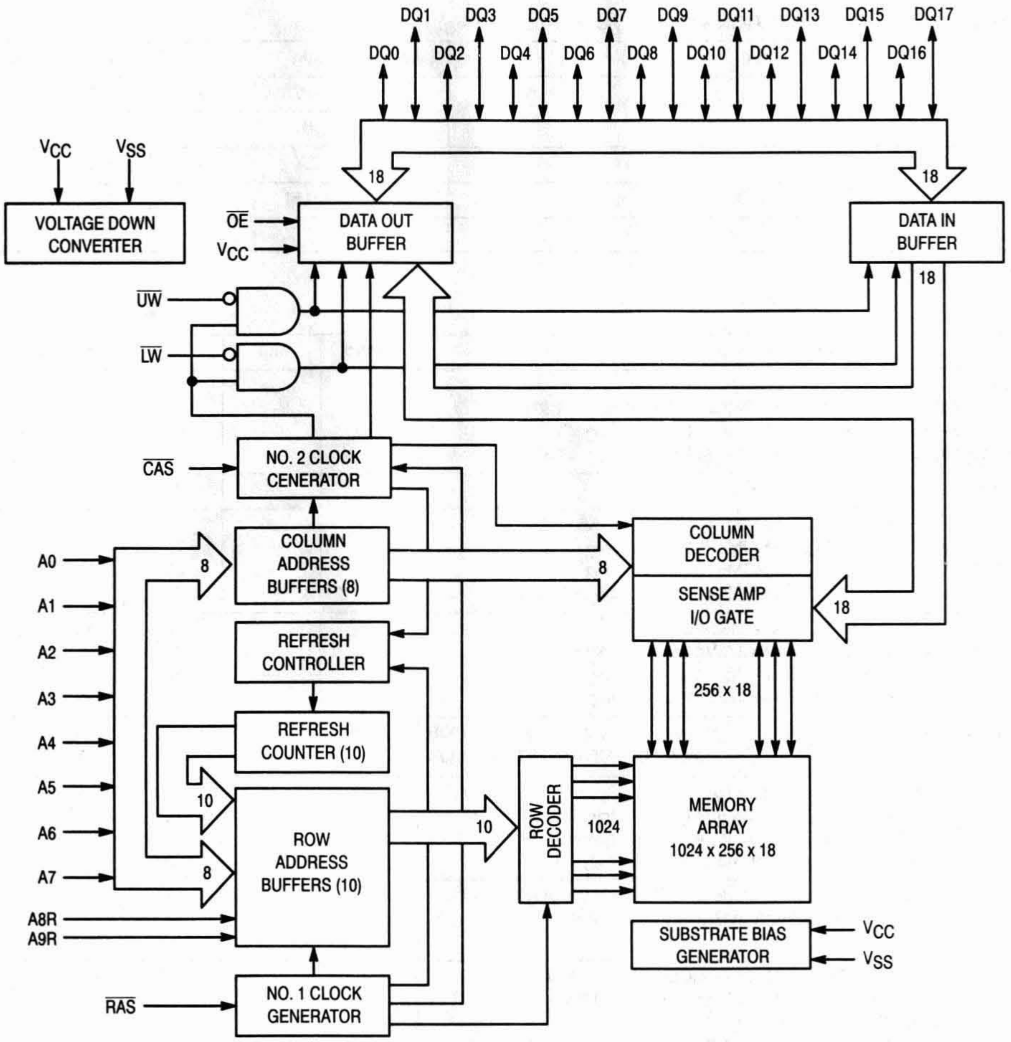
VCC 1 40 VSS
DQ0 2 39 DQ17
DQ1 3 38 DQ16
DQ2 4 37 DQ15
DQ3 5 36 DQ14
VCC 6 35 VSS
DQ4 7 34 DQ13
DQ5 8 33 DQ12
DQ6 9 32 DQ11
DQ7 10 31 DQ10
DQ8 11 30 DQ9
LW 12 29 NC
UW 13 28 CAS
RAS 14 27 G
A9R 15 26 A8R
A0 16 25 A7
A1 17 24 A6
A2 18 23 A5
A3 19 22 A4
VCC 20 21 VSS

400 MIL TSOP



VCC 1 44 VSS
DQ0 2 43 DQ17
DQ1 3 42 DQ16
DQ2 4 41 DQ15
DQ3 5 40 DQ14
VCC 6 39 VSS
DQ4 7 38 DQ13
DQ5 8 37 DQ12
DQ6 9 36 DQ11
DQ7 10 35 DQ10
DQ8 13 32 DQ9
LW 14 31 NC
UW 15 30 CAS
RAS 16 29 G
A9R 17 28 A8R
A0 18 27 A7
A1 19 26 A6
A2 20 25 A5
A3 21 24 A4
VCC 22 23 VSS

BLOCK DIAGRAM


DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
18
18
VCC
VSS
VOLTAGE DOWN CONVERTER
OE
VCC
DATA OUT BUFFER
DATA IN BUFFER
18
UW
LW
CAS
NO. 2 CLOCK GENERATOR
A0
A1
A2
A3
A4
A5
A6
A7
A8R
A9R
8
COLUMN ADDRESS BUFFERS (8)
8
COLUMN DECODER
SENSE AMP I/O GATE
18
256 x 18
REFRESH CONTROLLER
REFRESH COUNTER (10)
10
8
ROW ADDRESS BUFFERS (10)
10
ROW DECODER
1024
MEMORY ARRAY 1024 x 256 x 18
SUBSTRATE BIAS GENERATOR
VCC
VSS
RAS
NO. 1 CLOCK GENERATOR

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.0	V
Logic Low Voltage, All Inputs Except DQ0 – DQ7	V_{IL}	– 0.5*	—	0.8	V
Logic Low Voltage, DQ0 – DQ7	V_{IL}	– 0.5*	—	0.8	V

*– 2.0 V at pulse width ≤ 20 ns

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM54190B-70, MCM5L4190B-70, and MCM5V4190B-70, t_{RC} = 130 ns MCM54190B-80, MCM5L4190B-80, and MCM5V4190B-80, t_{RC} = 150 ns MCM54190B-10, MCM5L4190B-10, and MCM5V4190B-10, t_{RC} = 180 ns	I_{CC1}	 — — —	 75 65 60	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles ($\overline{CAS}$ = V_{IH}) MCM54190B-70, MCM5L4190B-70, and MCM5V4190B-70, t_{RC} = 130 ns MCM54190B-80, MCM5L4190B-80, and MCM5V4190B-80, t_{RC} = 150 ns MCM54190B-10, MCM5L4190B-10, and MCM5V4190B-10, t_{RC} = 180 ns	I_{CC3}	 — — —	 75 65 60	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL}) MCM54190B-70, MCM5L4190B-70, and MCM5V4190B-70, t_{PC} = 45 ns MCM54190B-80, MCM5L4190B-80, and MCM5V4190B-80, t_{PC} = 50 ns MCM54190B-10, MCM5L4190B-10, and MCM5V4190B-10, t_{PC} = 60 ns	I_{CC4}	 — — —	 70 60 55	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM54190B MCM5L4190B and MCM5V4190B	I_{CC5}	— —	1.0 200	mA µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM54190B-70, MCM5L4190B-70, and MCM5V4190B-70, t_{RC} = 130 ns MCM54190B-80, MCM5L4190B-80, and MCM5V4190B-80, t_{RC} = 150 ns MCM54190B-10, MCM5L4190B-10, and MCM5V4190B-10, t_{RC} = 180 ns	I_{CC6}	 — — —	 75 65 60	mA	1
V_{CC} Power Supply Current, Battery Backup Mode — MCM5L4190B Only (t_{RC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0 – A8, A9R, $\overline{W}$, D = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	—	300	µA	1, 3
V_{CC} Power Supply Current, Self Refresh Mode — MCM5V4190B Only ($\overline{RAS}$ = $\overline{CAS}$ = V_{IL}; A0 – A7, A8R, A9R, $\overline{W}$, $\overline{G}$ = V_{CC} – 0.2 V or 0.2 V; DQ0–DQ7 = V_{CC} – 0.2 V, 0.2 V, or Open)	I_{CC8}	—	200	µA	
Input Leakage Current (0 V ≤ V_{in} ≤ 7.0 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ 7.0 V, Output Disable)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading. Maximum currents are at the specified cycle time (min) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery back-up. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, periodically sampled, not 100% tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A7, A8R, A9R	C_{in}	5	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{G}$		7	
Input/Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0 – DQ15	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM54190B-70 MCM5L4190B-70 MCM5V4190B-70		MCM54190B-80 MCM5L4190B-80 MCM5V4190B-80		MCM54190B-10 MCM5L4190B-10 MCM5V4190B-10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	180	—	ns	5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RWC}	185	—	205	—	245	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	50	—	60	—	ns	
Page Mode Read-Modify-Write Cycle Time	t_{CELCEL}	t_{PRWC}	100	—	105	—	125	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	—	100	ns	6, 8, 9
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	50	ns	6, 9
Access Time from $\overline{\text{CAS}}$ Precharge	t_{CEHQV}	t_{CPA}	—	40	—	45	—	55	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	15	0	20	ns	7
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	70	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	8
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	9
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Page Mode Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Hold Time From $\overline{\text{CAS}}$ Precharge (Page Mode Only)	t_{CEHREH}	t_{RHCP}	40	—	45	—	55	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	50	—	ns	

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles or 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0 \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. t_{OFF} (max) and t_{GZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM54190B-70 MCM5L4190B-70 MCM5V4190B-70		MCM54190B-80 MCM5L4190B-80 MCM5V4190B-80		MCM54190B-10 MCM5L4190B-10 MCM5V4190B-10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	10
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{CELWH}	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	11
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	20	—	ns	11
Refresh Period MCM54190B MCM5L4190B and MCM5V4190B	t_{RVRV}	t_{RFSH}	—	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	12
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	60	—	ns	12
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	100	—	110	—	135	—	ns	12
Column Address to Write Delay	t_{AVWL}	t_{AWD}	65	—	70	—	85	—	ns	12
$\overline{CAS}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	70	—	75	—	90	—	ns	12
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	t_{RELCEH}	t_{CHR}	15	—	15	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Counter Test)	t_{CEHCEL}	t_{CPT}	30	—	30	—	40	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	—	10	—	20	—	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	20	—	25	ns	6
$\overline{G}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	25	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	25	ns	7
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	25	—	ns	
Masked Write Set-Up Time	t_{MEHCEL}	t_{MCS}	0	—	0	—	0	—	ns	
Masked Write Hold Time Referenced to $\overline{RAS}$	t_{REHMX}	t_{MRH}	0	—	0	—	0	—	ns	
Masked Write Hold Time Referenced to $\overline{CAS}$	t_{CEHMX}	t_{MCH}	0	—	0	—	0	—	ns	
Output Disable Setup Time	t_{GLCEL}	t_{GDS}	0	—	0	—	0	—	ns	

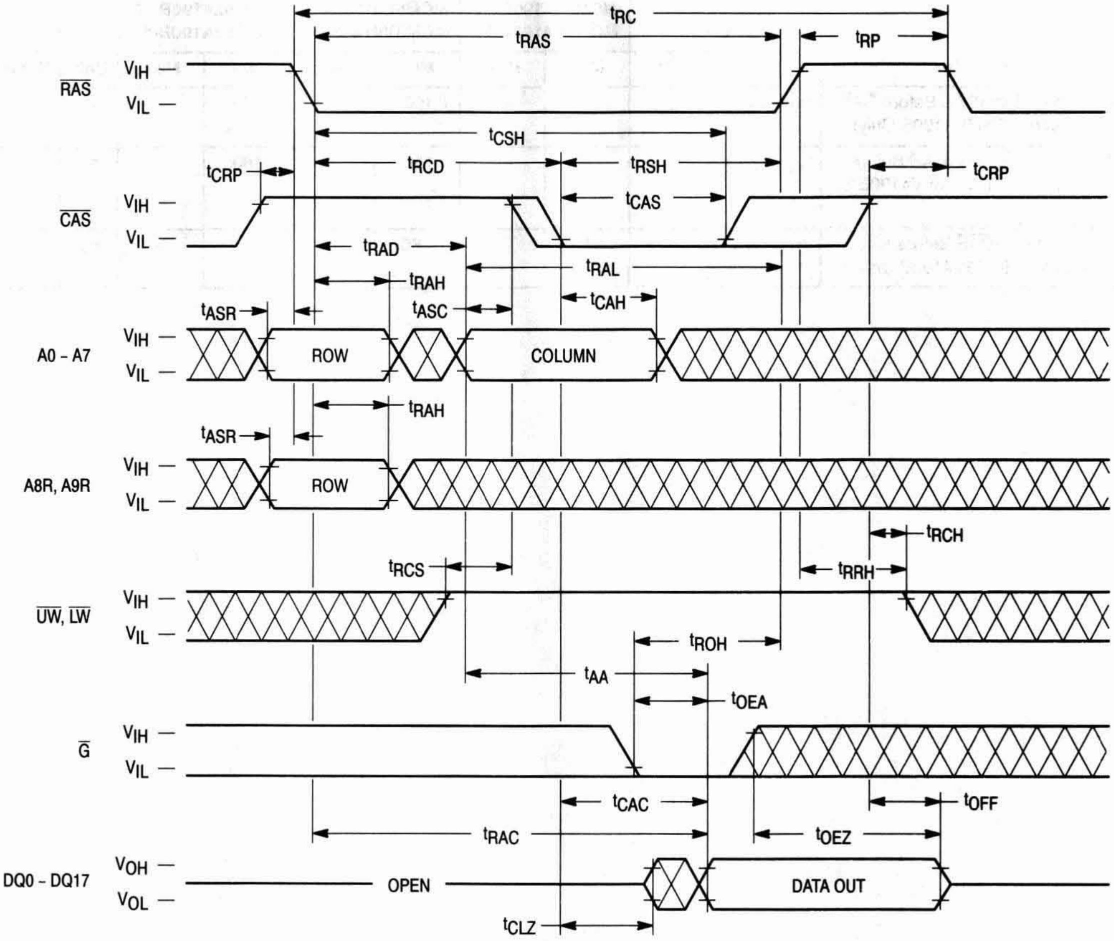
NOTES:

10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in late write or read-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

SELF REFRESH CYCLE

Parameter	Symbol		MCM54190B-70 MCM5L4190B-70 MCM5V4190B-70		MCM54190B-80 MCM5L4190B-80 MCM5V4190B-80		MCM54190B-10 MCM5L4190B-10 MCM5V4190B-10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ Before $\overline{RAS}$ Self Refresh, MCM5V4190B Only)	$t_{RELREHS}$	t_{RASS}	100	—	100	—	100	—	μs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Self Refresh, MCM5V4190B Only)	$t_{REHRELS}$	t_{RPS}	130	—	150	—	180	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Self Refresh, MCM5V4190B Only)	t_{REHCEH}	t_{CHS}	– 50	—	– 60	—	– 70	—	ns	

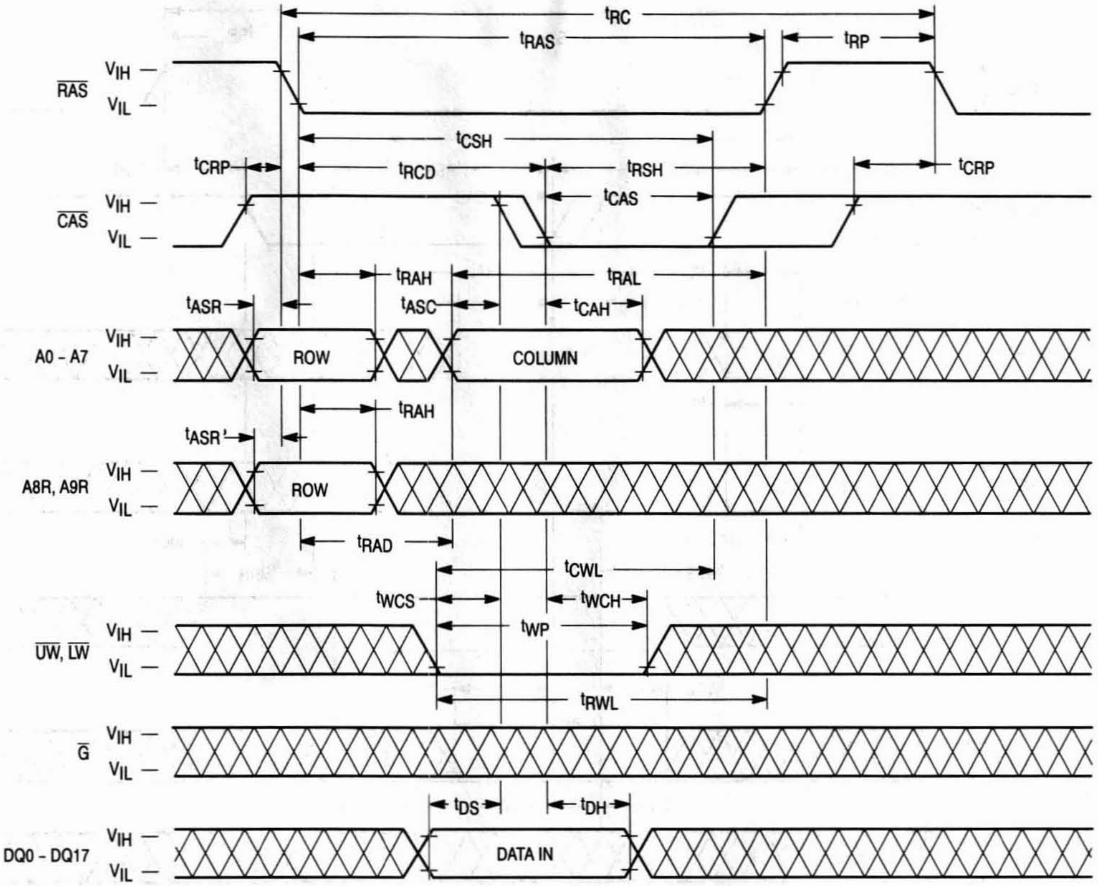
READ CYCLE



t_{RC}
t_{RAS}
t_{RP}
RAS
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
CAS
t_{RAD}
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 - A7
ROW
COLUMN
t_{RAH}
t_{ASR}
A8R, A9R
ROW
t_{RCH}
t_{RCS}
t_{RRH}
UW, LW
t_{ROH}
t_{AA}
t_{OEA}
G
t_{CAC}
t_{OFF}
t_{RAC}
t_{OEZ}
DQ0 - DQ17
V_{OH}
V_{OL}
OPEN
DATA OUT
t_{CLZ}

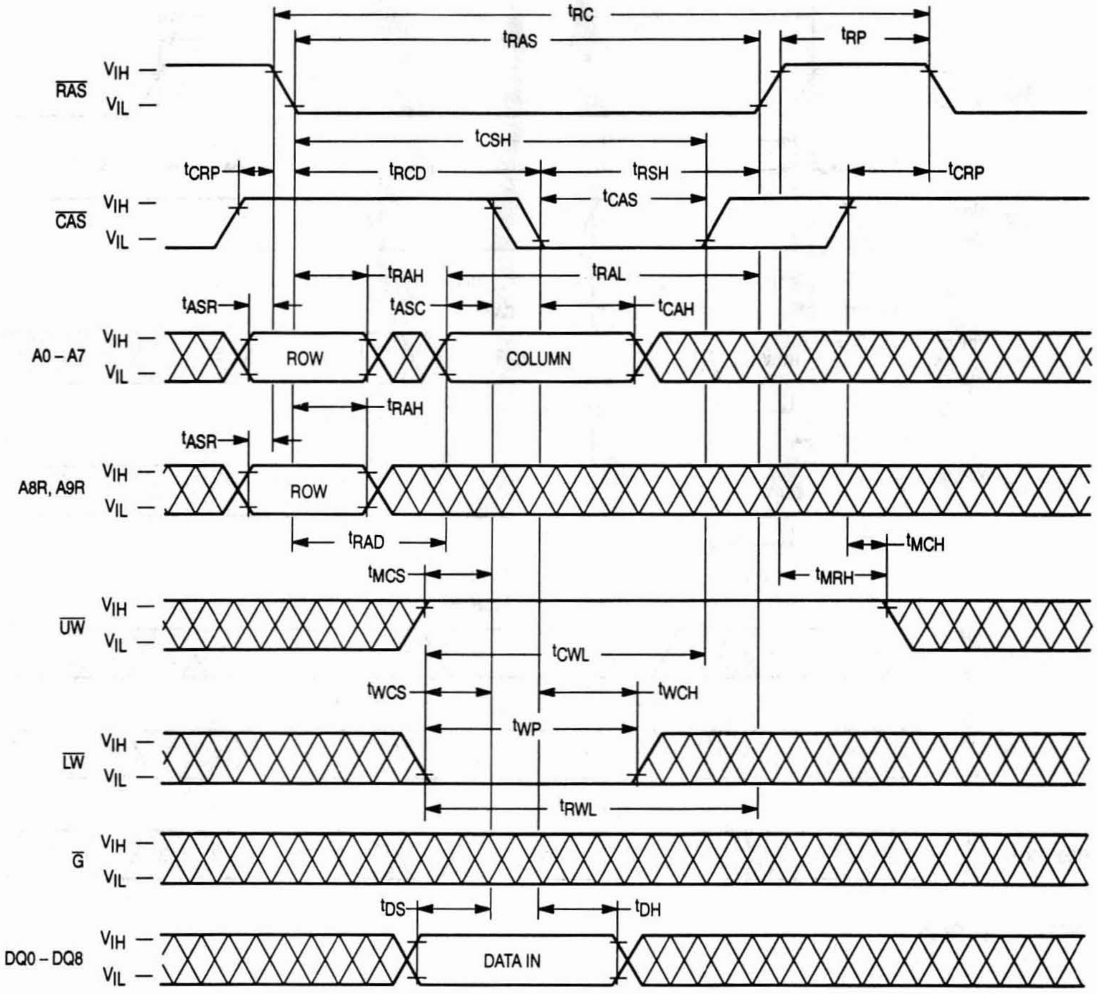
NOTE: D_{in} = Open

WRITE CYCLE (EARLY WRITE)


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tRAH
tRAL
tASR
tASC
tCAH
A0 - A7
VIH
VIL
ROW
COLUMN
tRAH
tASR'
A8R, A9R
VIH
VIL
ROW
tRAD
tCWL
tWCS
tWCH
tWP
UW, LW
VIH
VIL
tRWL
G
VIH
VIL
tDS
tDH
DQ0 - DQ17
VIH
VIL
DATA IN

NOTE: D_{out} = Open

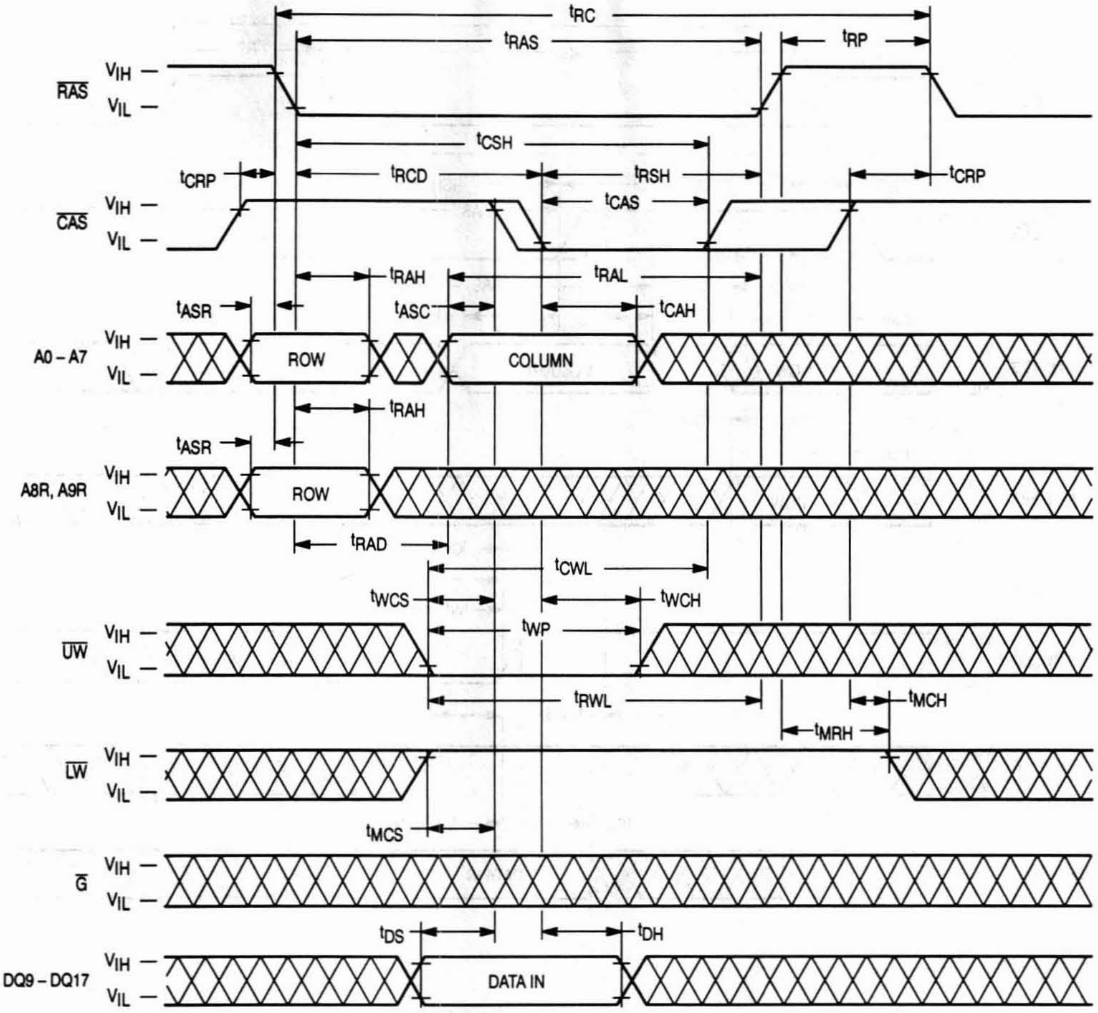
LOWER BYTE WRITE CYCLE (EARLY WRITE)



t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 – A7
ROW
COLUMN
t_{RAH}
t_{ASR}
A8R, A9R
ROW
t_{RAD}
t_{MCH}
t_{MCS}
t_{MRH}
$\overline{UW}$
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{LW}$
t_{RWL}
$\overline{G}$
t_{DS}
t_{DH}
DQ0 – DQ8
DATA IN

NOTE: D_{in} (DQ9 – DQ17) = Don't Care
D_{out} = Open

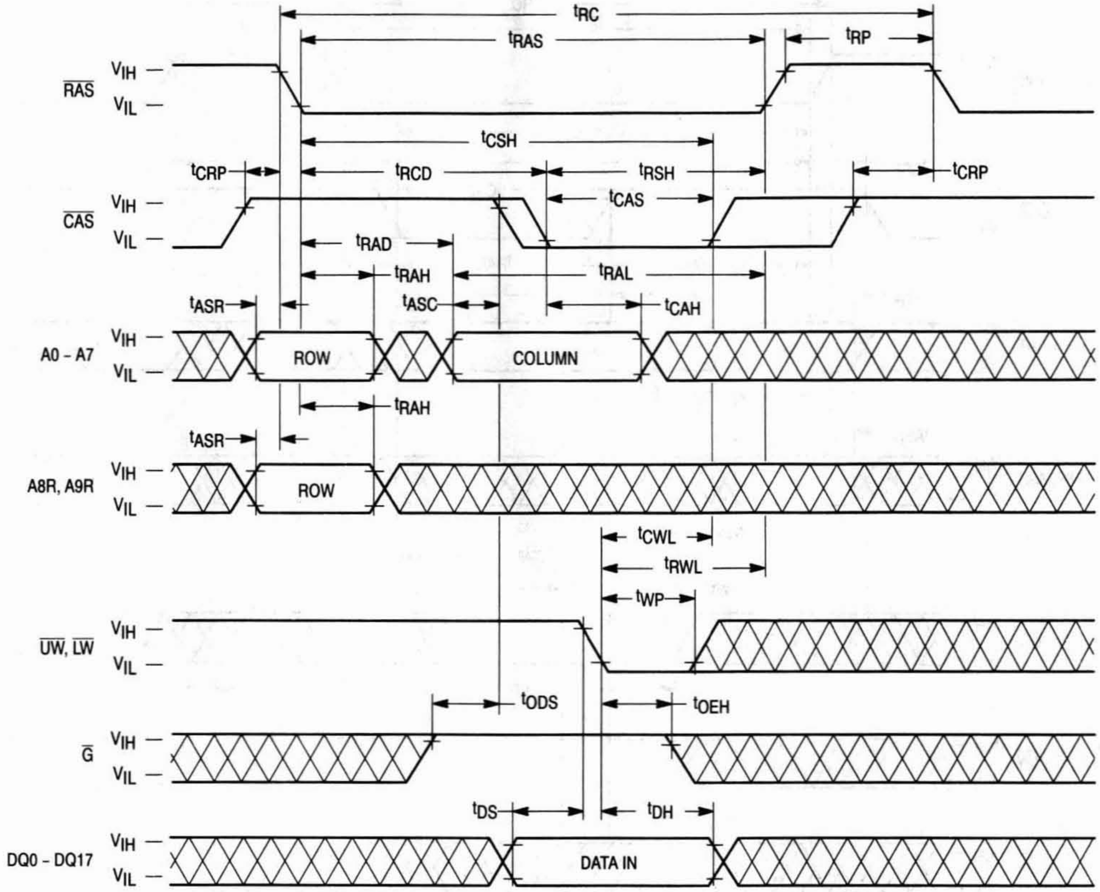
UPPER BYTE CYCLE (EARLY WRITE)



tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tRAH
tRAL
tASR
tASC
tCAH
A0 – A7
VIH
VIL
ROW
COLUMN
tRAH
tASR
A8R, A9R
VIH
VIL
ROW
tRAD
tCWL
tWCS
tWCH
tWP
UW
VIH
VIL
tRWL
tMCH
tMRH
LW
VIH
VIL
tMCS
G
VIH
VIL
tDS
tDH
DQ9 – DQ17
VIH
VIL
DATA IN

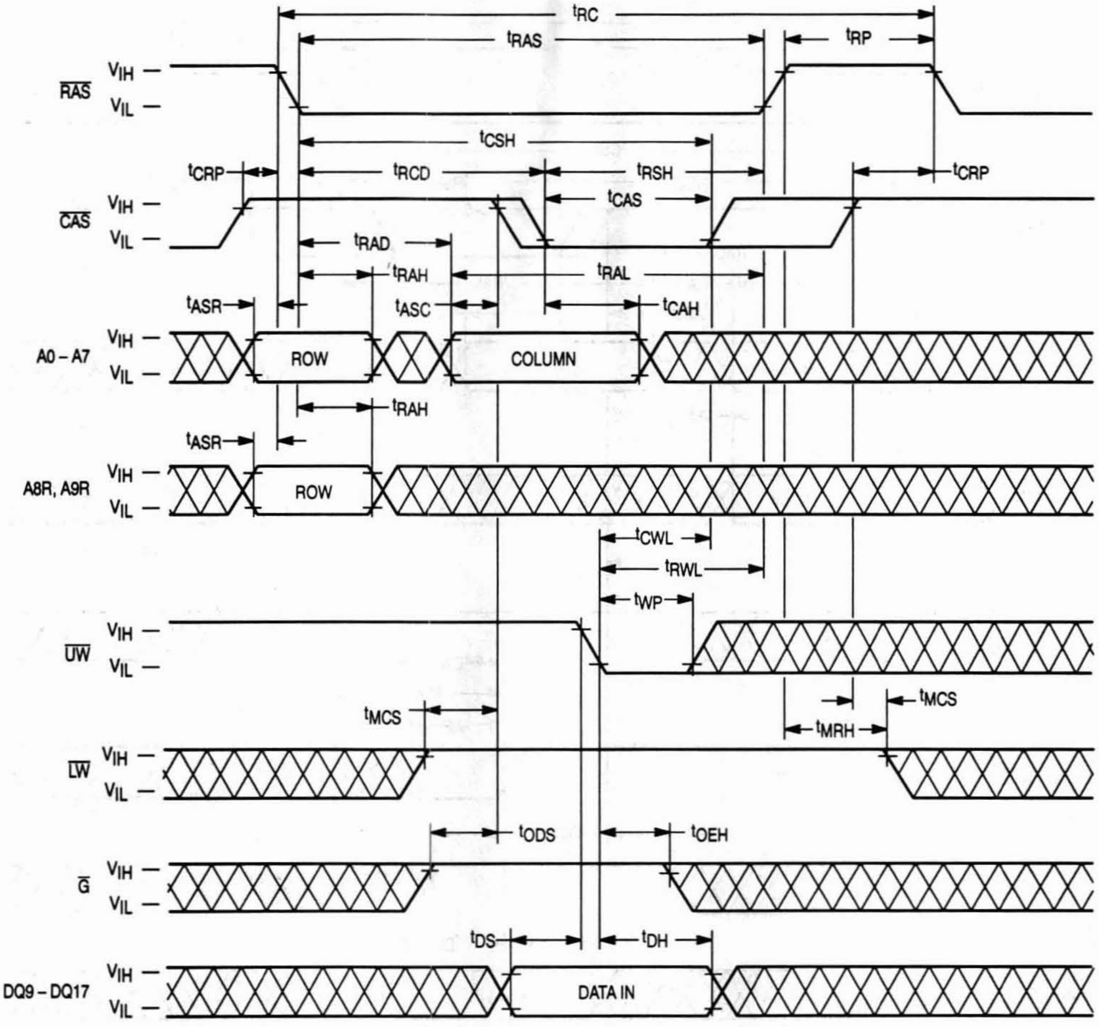
NOTE: D_{in} (DQ0 – DQ8) = Don't Care
D_{out} = Open

WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)


t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAD}
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 – A7
V_{IH}
V_{IL}
ROW
COLUMN
t_{RAH}
t_{ASR}
A8R, A9R
V_{IH}
V_{IL}
ROW
t_{CWL}
t_{RWL}
t_{WP}
$\overline{UW}$, $\overline{LW}$
V_{IH}
V_{IL}
t_{ODS}
t_{OEH}
$\overline{G}$
V_{IH}
V_{IL}
t_{DS}
t_{DH}
DQ0 – DQ17
V_{IH}
V_{IL}
DATA IN

NOTE: D_{out} = Open

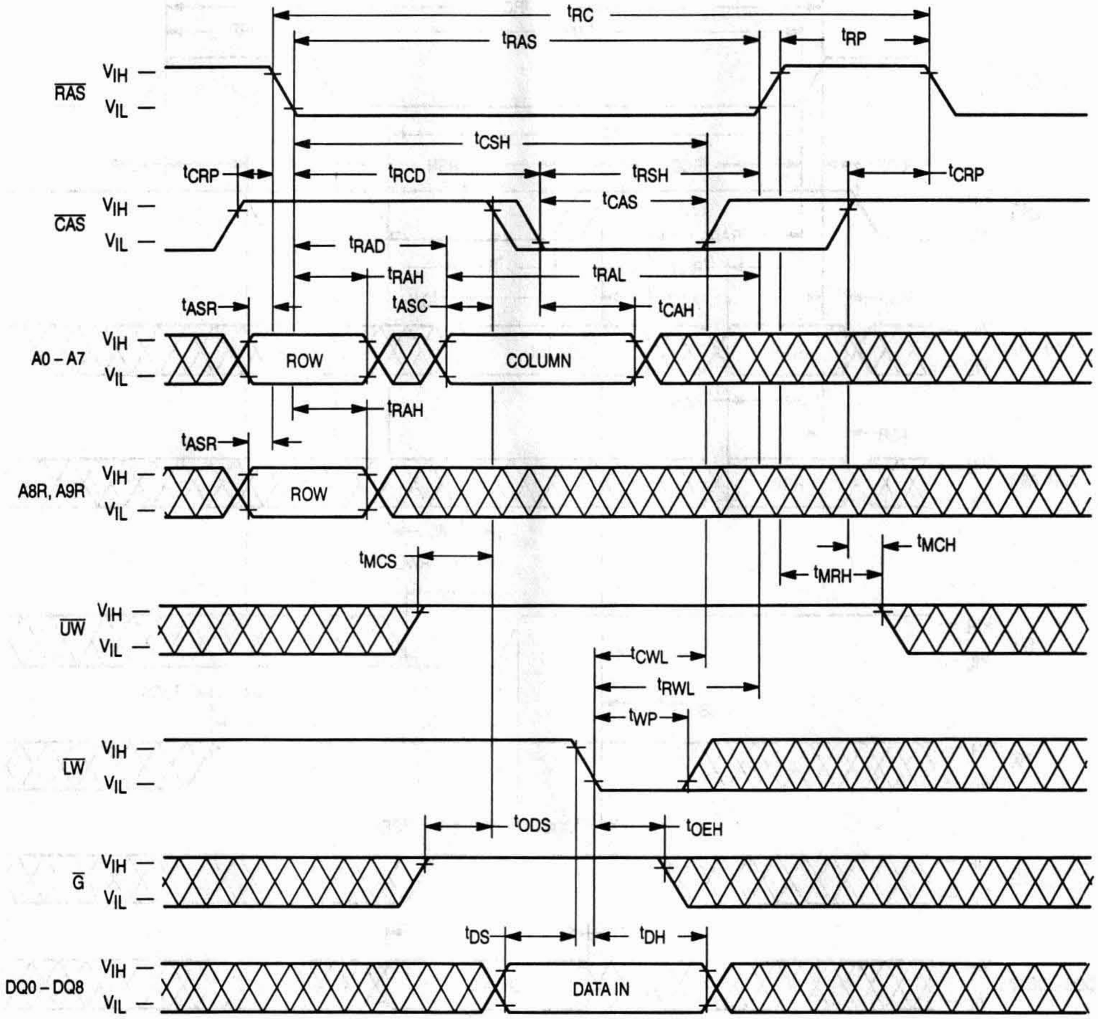
UPPER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tRAD
tRAH
tRAL
tASR
tASC
tCAH
A0 – A7
VIH
VIL
ROW
COLUMN
tRAH
tASR
A8R, A9R
VIH
VIL
ROW
tCWL
tRWL
tWP
UW
VIH
VIL
tMCS
tMCS
tMRH
LW
VIH
VIL
tODS
tOEH
G
VIH
VIL
tDS
tDH
DQ9 – DQ17
VIH
VIL
DATA IN

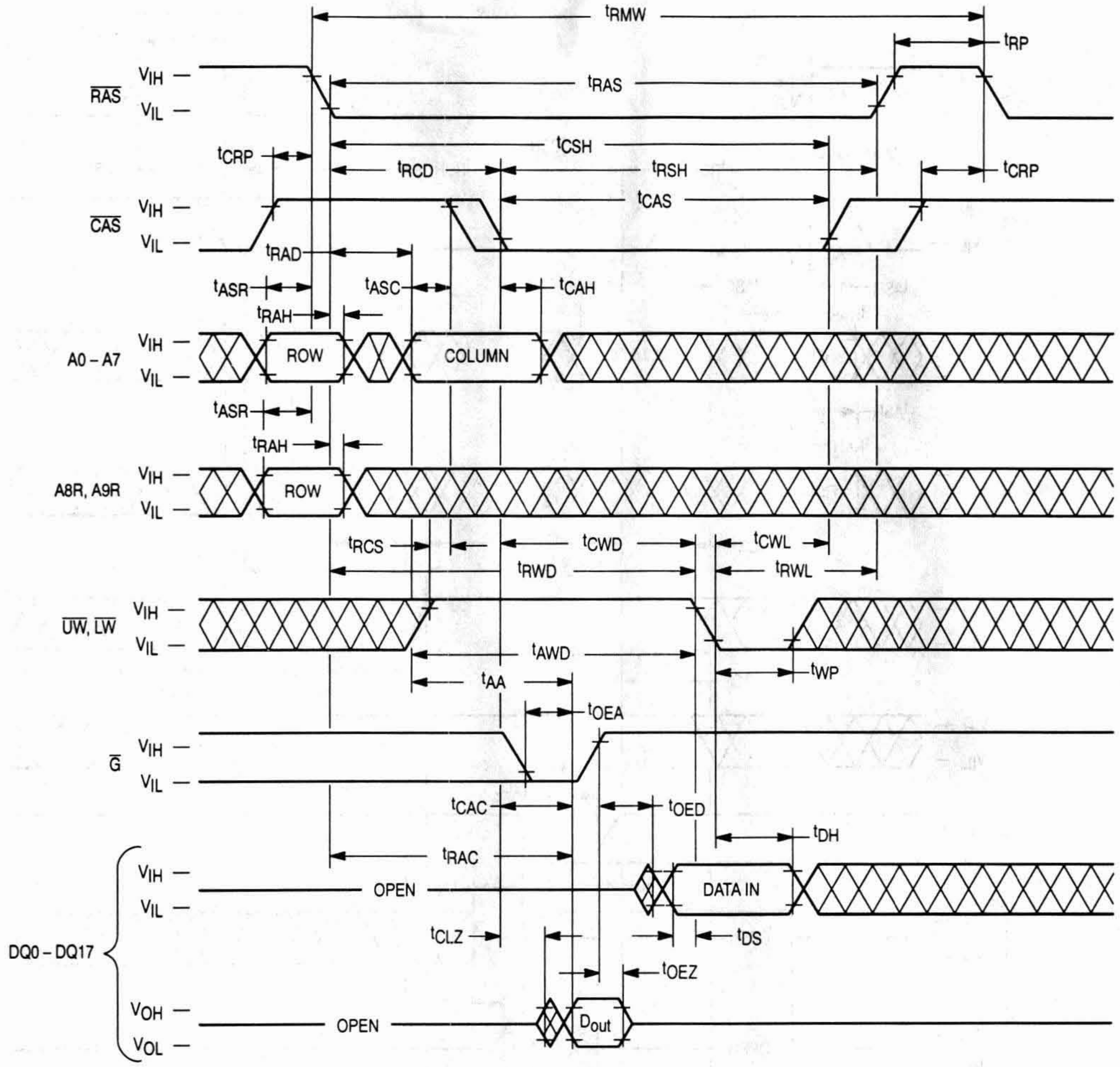
NOTE: D_{in} (DQ0 – DQ8) = Don't Care
D_{out} = Open

LOWER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)

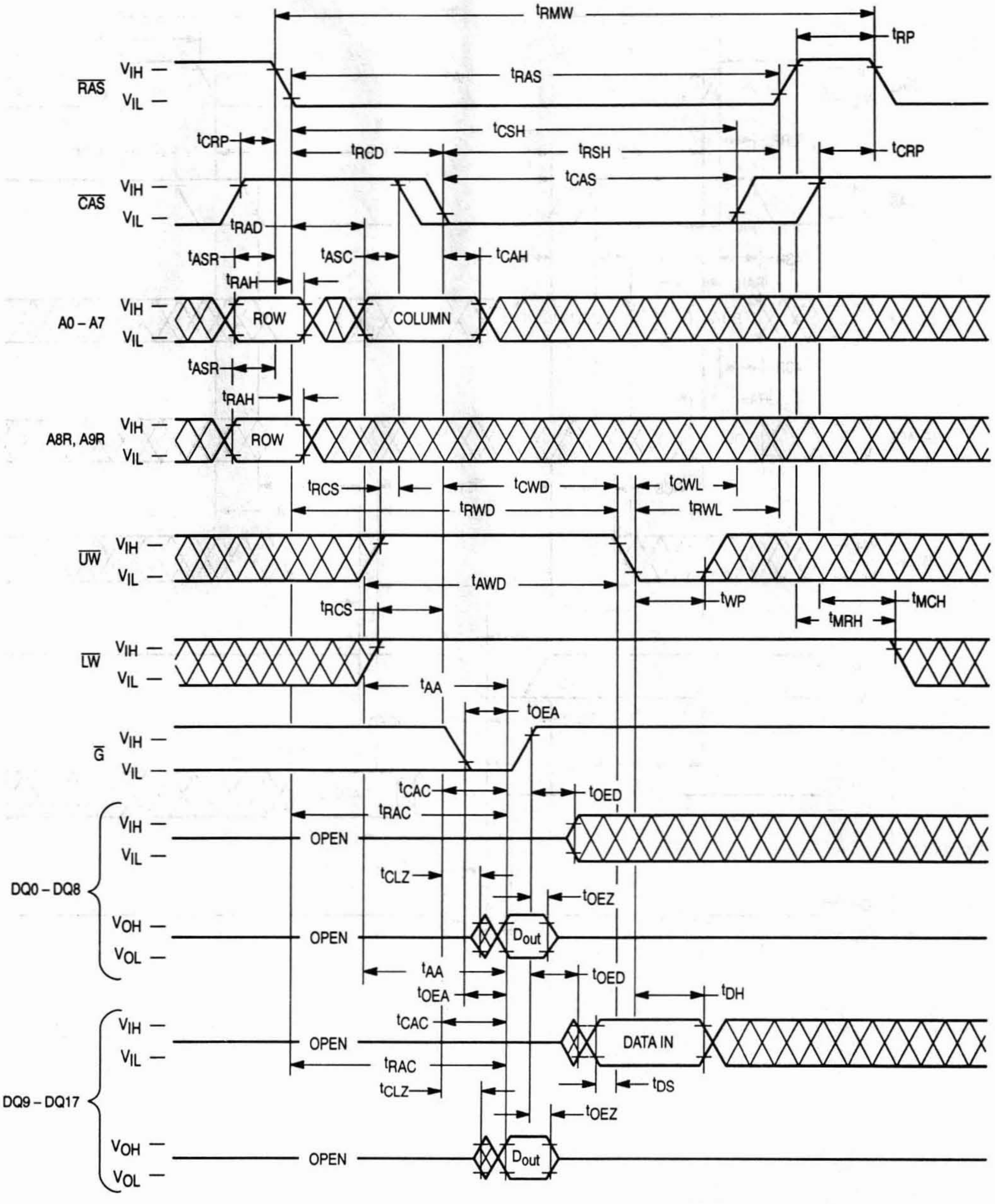

tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tRAD
tRAH
tRAL
tASR
tASC
tCAH
A0 – A7
VIH
VIL
ROW
COLUMN
tRAH
tASR
A8R, A9R
VIH
VIL
ROW
tMCH
tMCS
tMRH
UW
VIH
VIL
tCWL
tRWL
tWP
LW
VIH
VIL
tODS
tOEH
G
VIH
VIL
tDS
tDH
DQ0 – DQ8
VIH
VIL
DATA IN

NOTE: D_{in} (DQ9 – DQ17) = Don't Care
D_{out} = Open

READ-MODIFY-WRITE CYCLE

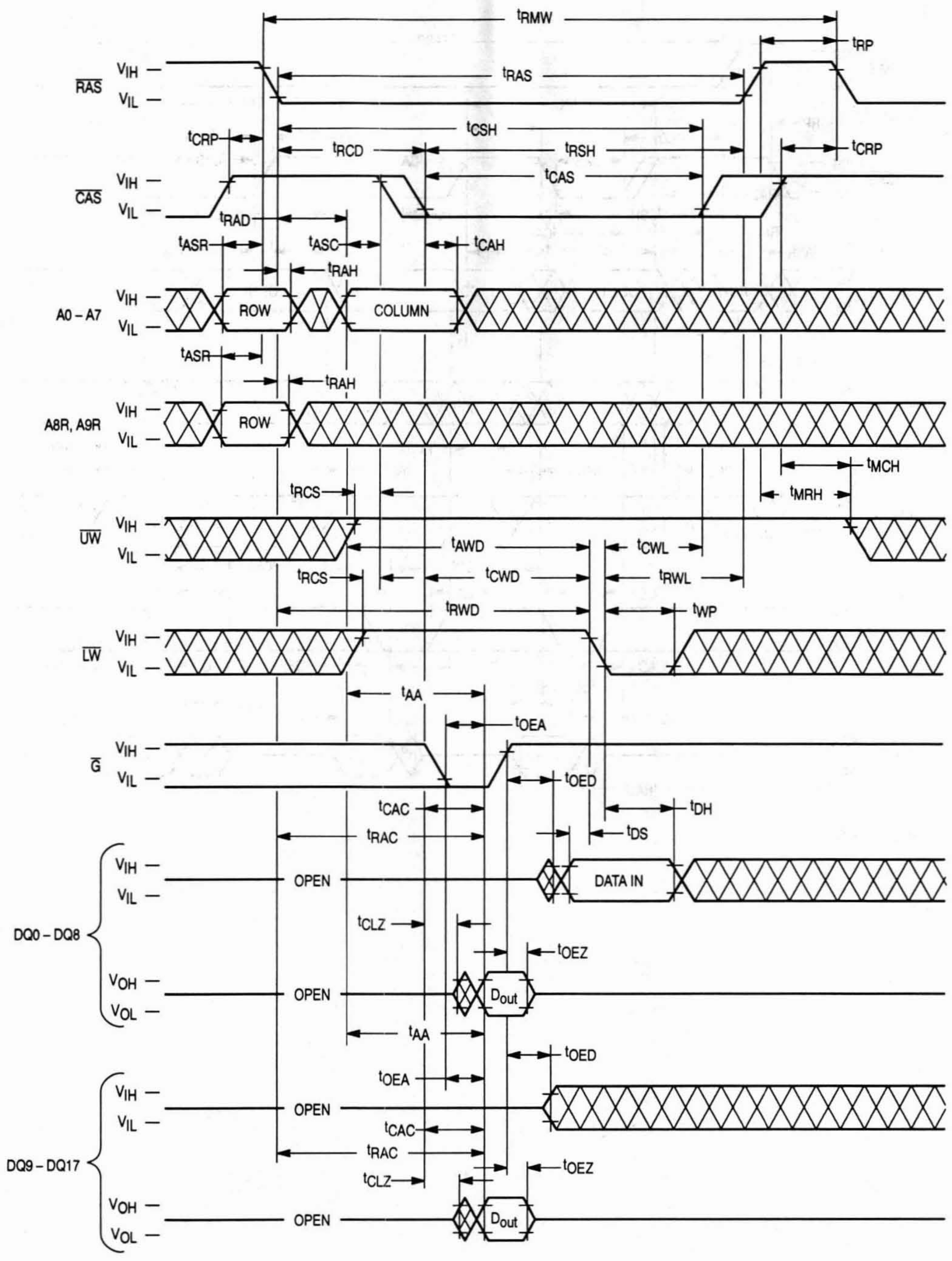

t_{RMW}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RAS}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{CAS}
t_{RAD}
t_{ASR}
t_{ASC}
t_{CAH}
t_{RAH}
A0 – A7
V_{IH}
V_{IL}
ROW
COLUMN
t_{ASR}
t_{RAH}
A8R, A9R
V_{IH}
V_{IL}
ROW
t_{RCS}
t_{CWD}
t_{CWL}
t_{RWD}
t_{RWL}
$\overline{UW}$, $\overline{LW}$
V_{IH}
V_{IL}
t_{AWD}
t_{WP}
t_{AA}
t_{OEA}
$\overline{G}$
V_{IH}
V_{IL}
t_{CAC}
t_{OED}
t_{DH}
t_{RAC}
DQ0 – DQ17
V_{IH}
V_{IL}
OPEN
DATA IN
t_{CLZ}
t_{DS}
t_{OEZ}
V_{OH}
V_{OL}
OPEN
D_{out}

READ-MODIFY-UPPER-BYTE-WRITE CYCLE



tRMW
tRP
$\overline{RAS}$
VIH
VIL
tRAS
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
$\overline{CAS}$
tRAD
tASR
tASC
tCAH
tRAH
A0 – A7
ROW
COLUMN
tASR
tRAH
A8R, A9R
ROW
tRCS
tCWD
tCWL
tRWD
tRWL
$\overline{UW}$
tAWD
tWP
tRCS
tMCH
tMRH
$\overline{LW}$
tAA
tOEA
$\overline{G}$
tCAC
tOED
tRAC
OPEN
tCLZ
tOEZ
DQ0 – DQ8
VOH
VOL
Dout
tAA
tOED
tOEA
tDH
tCAC
DATA IN
tRAC
tDS
tCLZ
tOEZ
DQ9 – DQ17
Dout

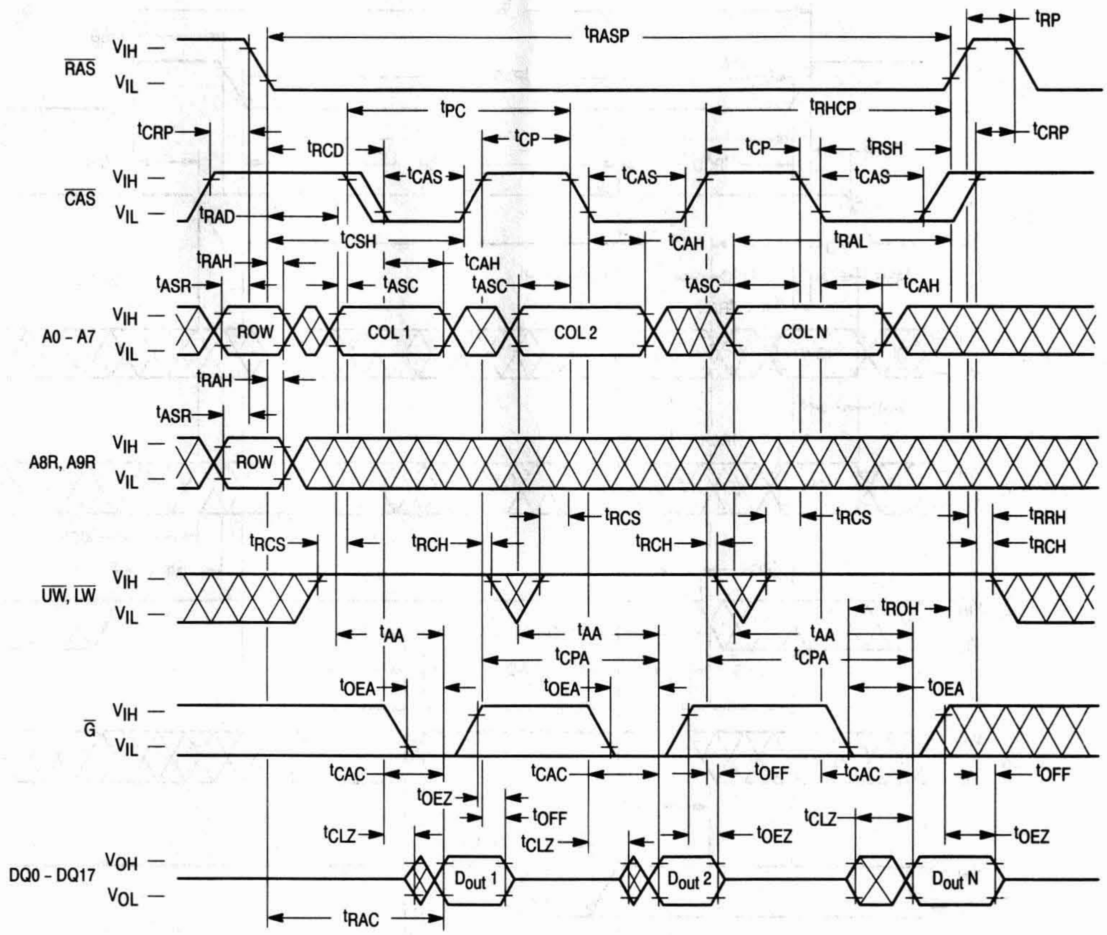
READ-MODIFY-LOWER-BYTE-WRITE CYCLE



t_{RMW}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RAS}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
t_{RAD}
t_{ASR}
t_{ASC}
t_{CAH}
t_{RAH}
A0 – A7
ROW
COLUMN
t_{ASR}
t_{RAH}
A8R, A9R
ROW
t_{MCH}
t_{RCS}
t_{MRH}
$\overline{UW}$
t_{AWD}
t_{CWL}
t_{RCS}
t_{CWD}
t_{RWL}
t_{RWD}
t_{WP}
$\overline{LW}$
t_{AA}
t_{OEA}
$\overline{G}$
t_{OED}
t_{CAC}
t_{DH}
t_{RAC}
t_{DS}
OPEN
DATA IN
DQ0 – DQ8
t_{CLZ}
t_{OEZ}
V_{OH}
V_{OL}
OPEN
D_{out}
t_{AA}
t_{OED}
t_{OEA}
OPEN
t_{CAC}
DQ9 – DQ17
t_{RAC}
t_{CLZ}
t_{OEZ}
OPEN
D_{out}

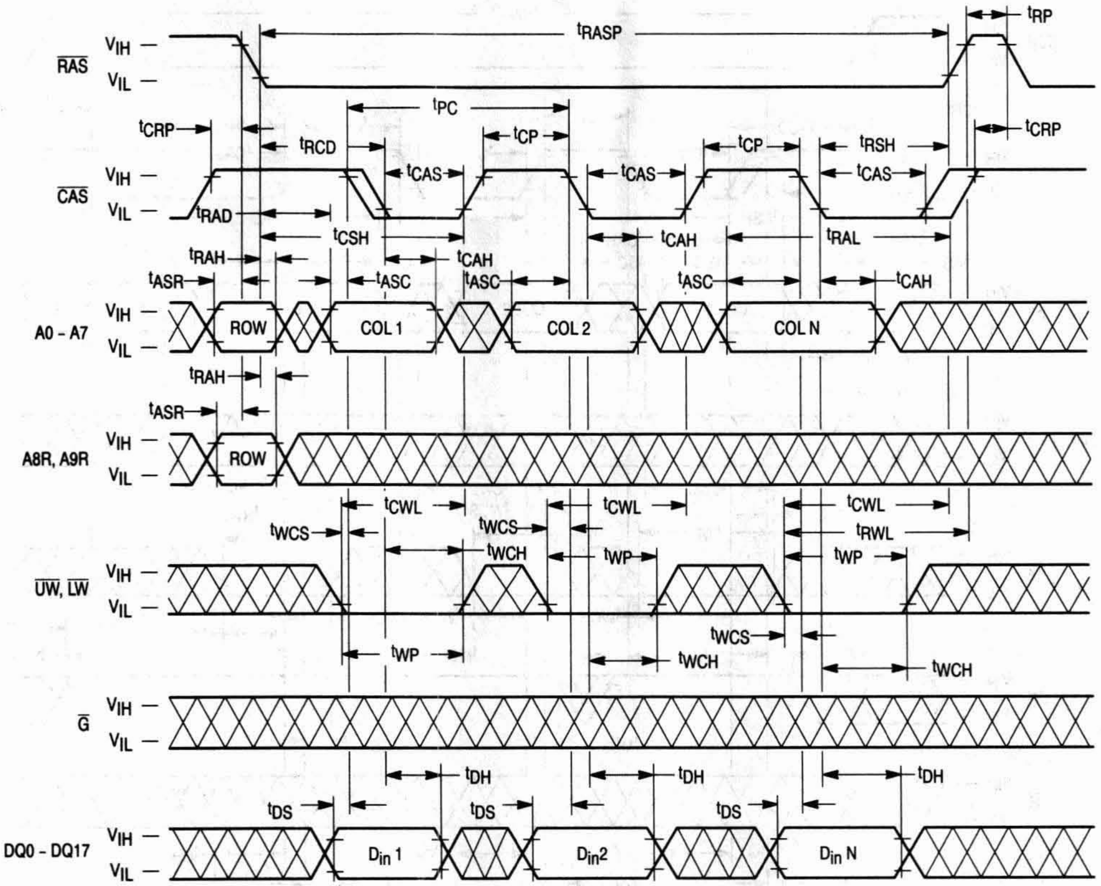
3

FAST PAGE MODE READ CYCLE


tRASP
tRP
RAS
VIH
VIL
tPC
tRHCP
tCRP
tRCD
tCP
tCP
tRSH
tCRP
CAS
VIH
VIL
tCAS
tCAS
tCAS
tRAD
tCSH
tCAH
tRAL
tRAH
tCAH
tASR
tASC
tASC
tASC
tCAH
A0 - A7
VIH
VIL
ROW
COL 1
COL 2
COL N
tRAH
tASR
A8R, A9R
VIH
VIL
ROW
tRCS
tRCS
tRRH
tRCS
tRCH
tRCH
tRCH
UW, LW
VIH
VIL
tROH
tAA
tAA
tAA
tCPA
tCPA
tOEA
tOEA
tOEA
G
VIH
VIL
tCAC
tCAC
tOFF
tCAC
tOFF
tOEZ
tOFF
tCLZ
tCLZ
tCLZ
tOEZ
tOEZ
DQ0 - DQ17
VOH
VOL
Dout 1
Dout 2
Dout N
tRAC

NOTE: D_{in} = Open

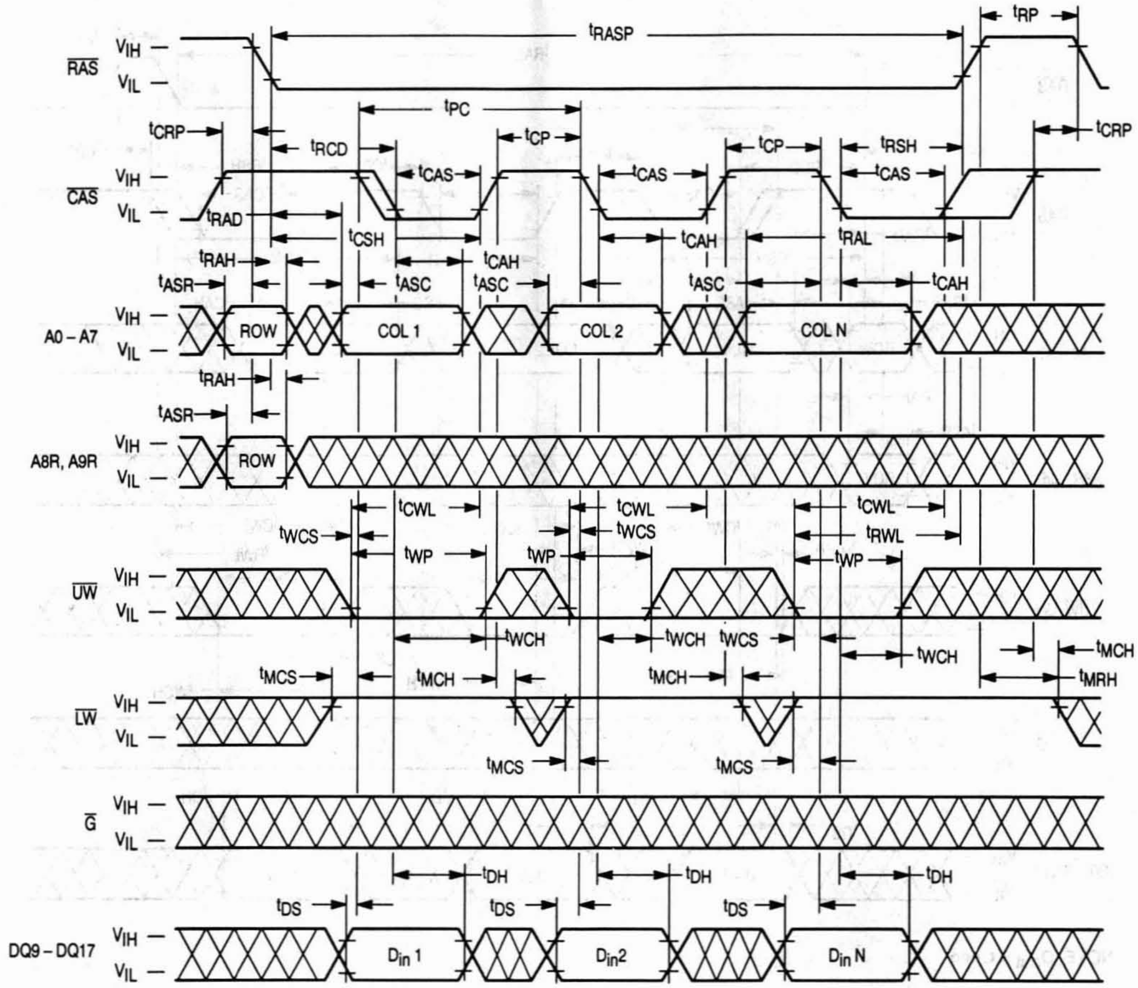
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



$\overline{RAS}$
$\overline{CAS}$
A0 - A7
A8R, A9R
$\overline{UW}$, $\overline{LW}$
$\overline{G}$
DQ0 - DQ17
V_{IH}
V_{IL}
t_{RASP}
t_{RP}
t_{CRP}
t_{PC}
t_{RCD}
t_{CP}
t_{CAS}
t_{RSH}
t_{RAD}
t_{CSH}
t_{CAH}
t_{RAL}
t_{RAH}
t_{ASR}
t_{ASC}
ROW
COL 1
COL 2
COL N
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
t_{RWL}
t_{DH}
t_{DS}
D_{in} 1
D_{in}2
D_{in} N

NOTE: D_{out} = Open

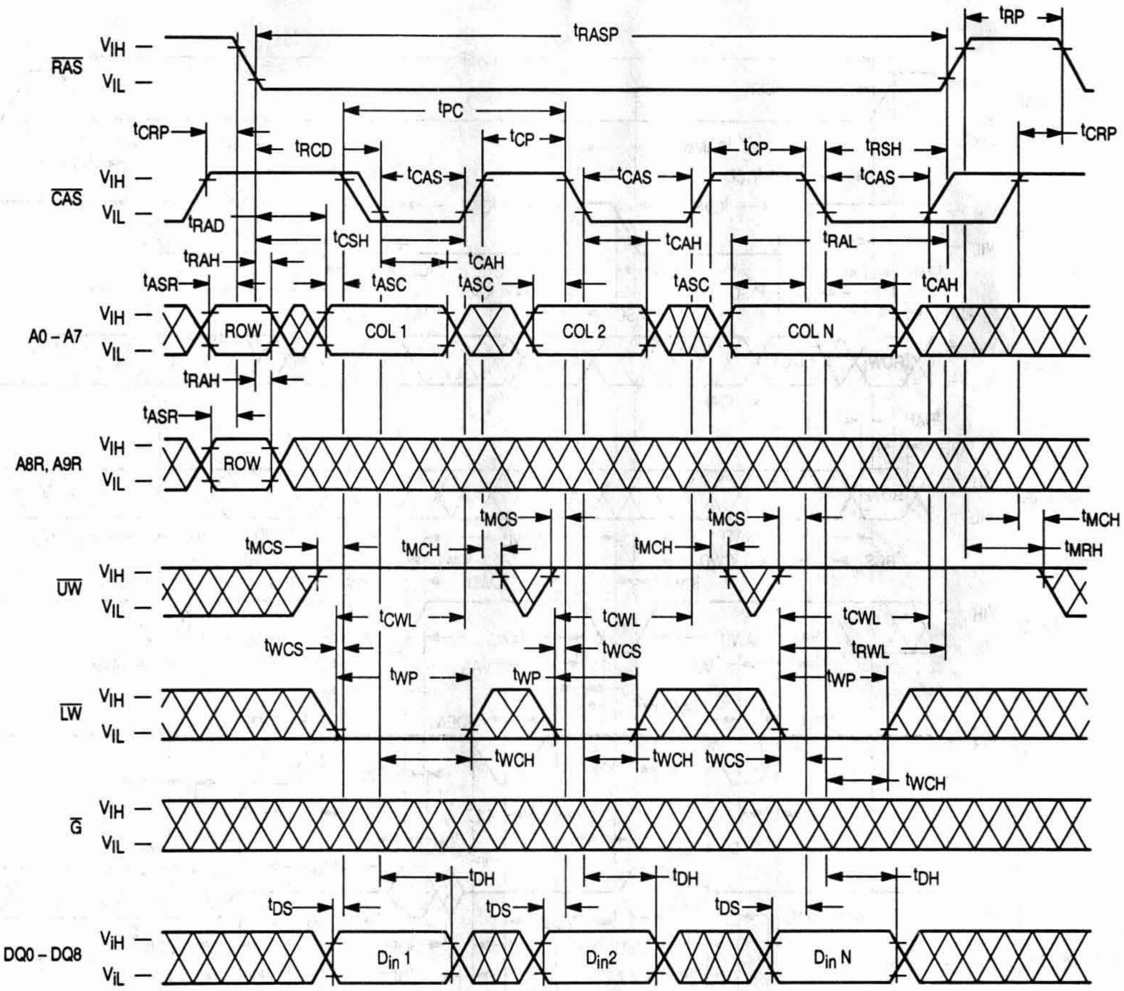
FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



t_{RASP}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{PC}
t_{CRP}
t_{RCD}
t_{CP}
t_{RSH}
t_{CAS}
$\overline{CAS}$
t_{RAD}
t_{CSH}
t_{CAH}
t_{RAL}
t_{RAH}
t_{ASR}
t_{ASC}
A0 – A7
ROW
COL 1
COL 2
COL N
A8R, A9R
t_{CWL}
t_{WCS}
t_{WP}
t_{RWL}
$\overline{UW}$
t_{WCH}
t_{MCH}
t_{MCS}
t_{MRH}
$\overline{LW}$
$\overline{G}$
t_{DH}
t_{DS}
DQ9 – DQ17
D_{in} 1
D_{in}2
D_{in} N

NOTE: D_{in} (DQ0 – DQ8) = Don't Care
D_{out} = Open

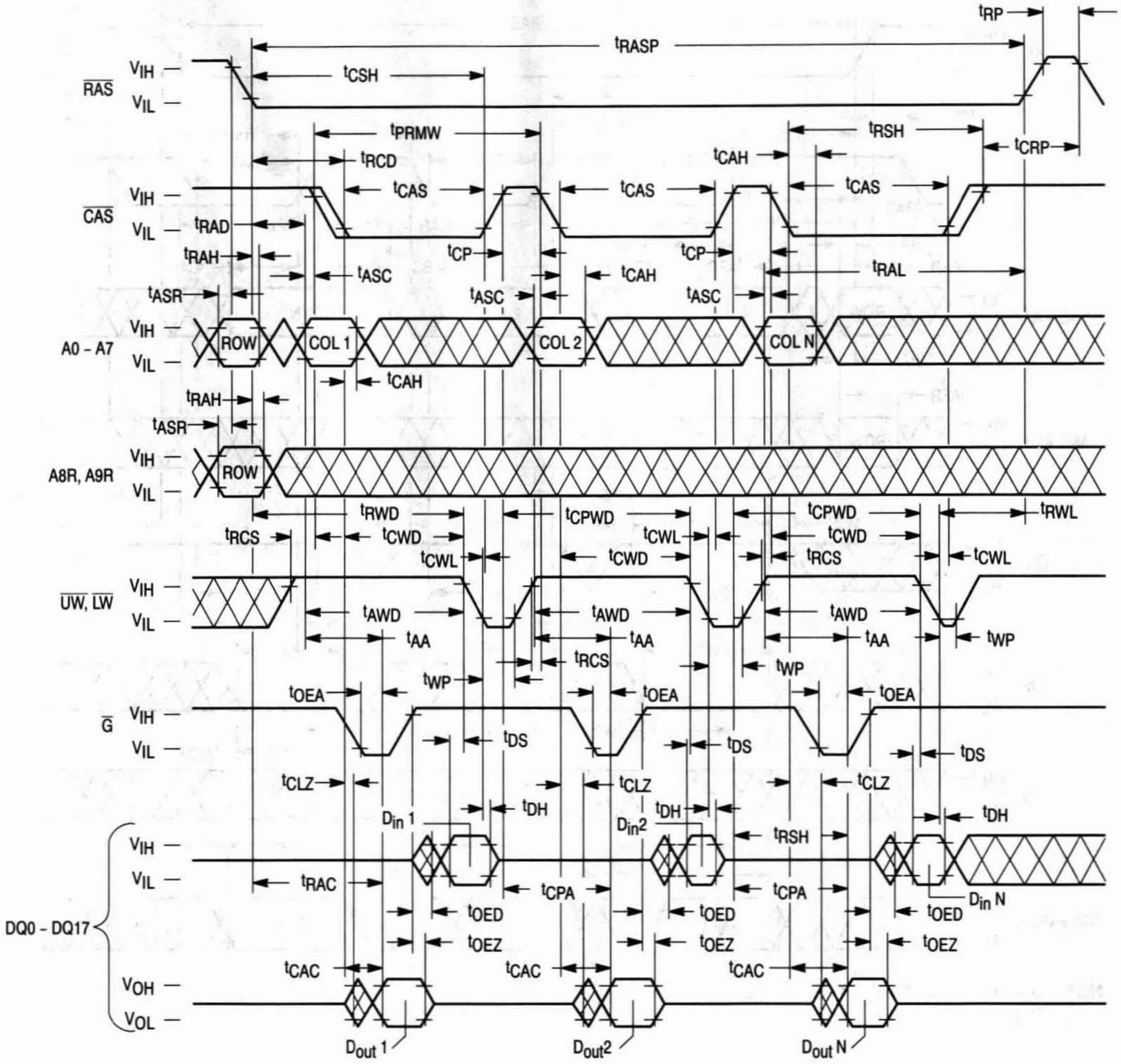
FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)



RAS
CAS
A0 – A7
A8R, A9R
UW
LW
G
DQ0 – DQ8
VIH
VIL
tRASP
tRP
tPC
tCRP
tRCD
tCP
tRSH
tCAS
tRAD
tCSH
tCAH
tRAL
tRAH
tASR
tASC
ROW
COL 1
COL 2
COL N
tMCS
tMCH
tMRH
tCWL
tWCS
tRWL
tWP
tWCH
tDH
tDS
Din 1
Din2
Din N

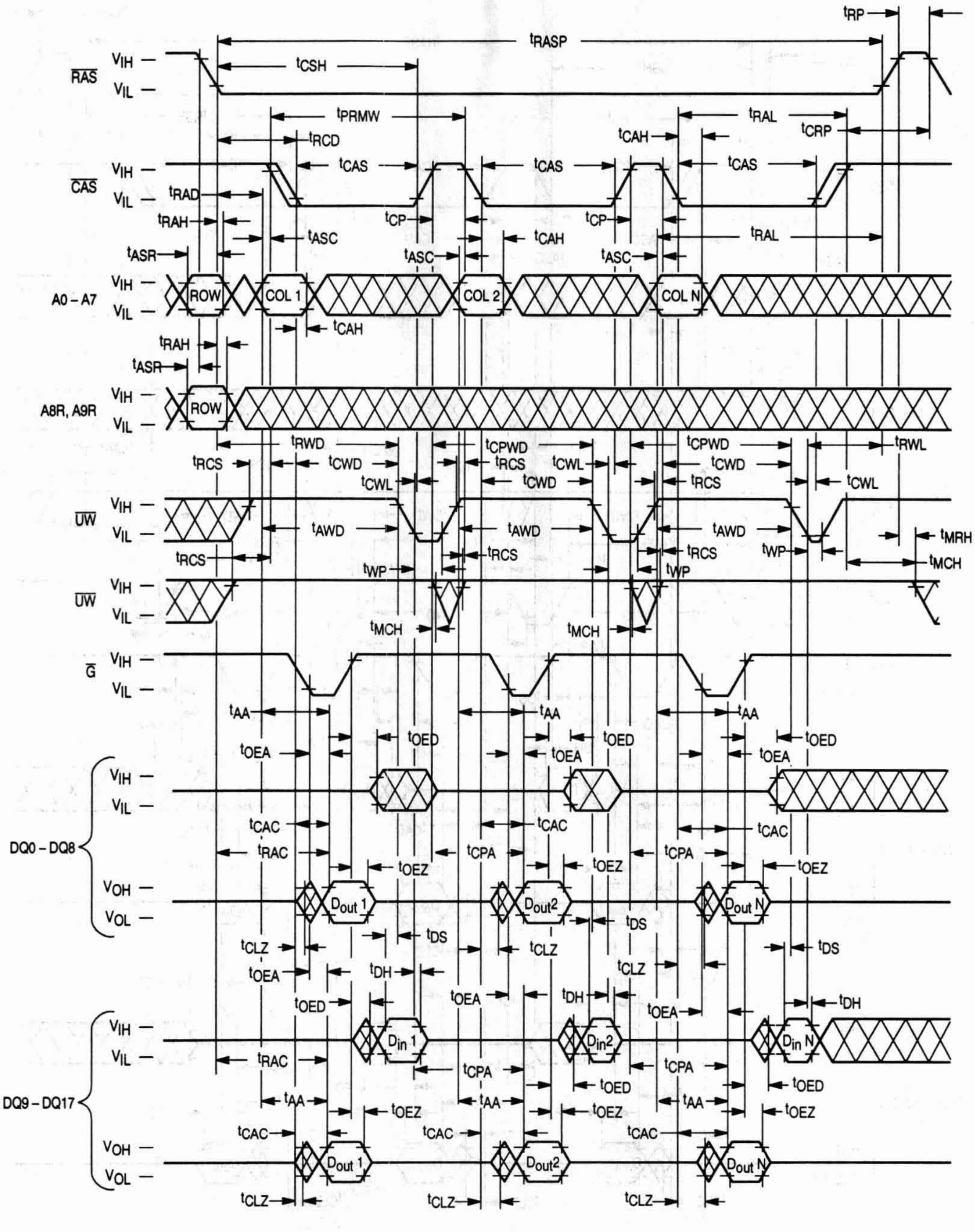
NOTE: D_{in} (DQ9 – DQ17) = Don't Care
D_{out} = Open

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

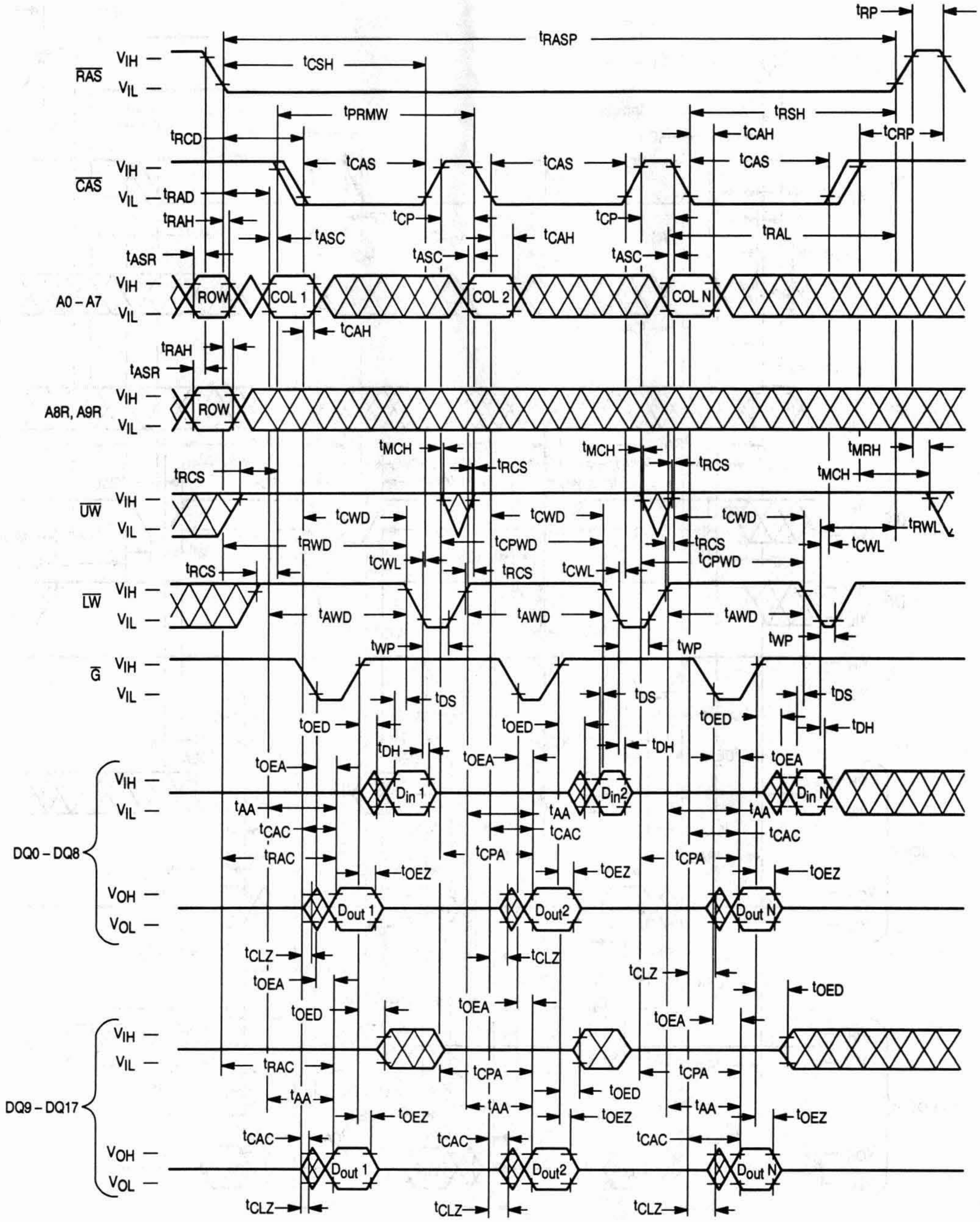


tRP
tRASP
tCSH
tPRMW
tRCD
tRSH
tCRP
tCAH
tCAS
tRAD
tRAH
tASC
tCP
tRAL
tASR
RAS
CAS
VIH
VIL
A0 - A7
ROW
COL 1
COL 2
COL N
A8R, A9R
tRWD
tCPWD
tRWL
tRCS
tCWD
tCWL
UW, LW
tAWD
tAA
tWP
tOEA
G
tDS
tCLZ
tDH
Din 1
Din2
Din N
tRAC
tCPA
tOED
tOEZ
tCAC
DQ0 - DQ17
VOH
VOL
Dout 1
Dout2
Dout N

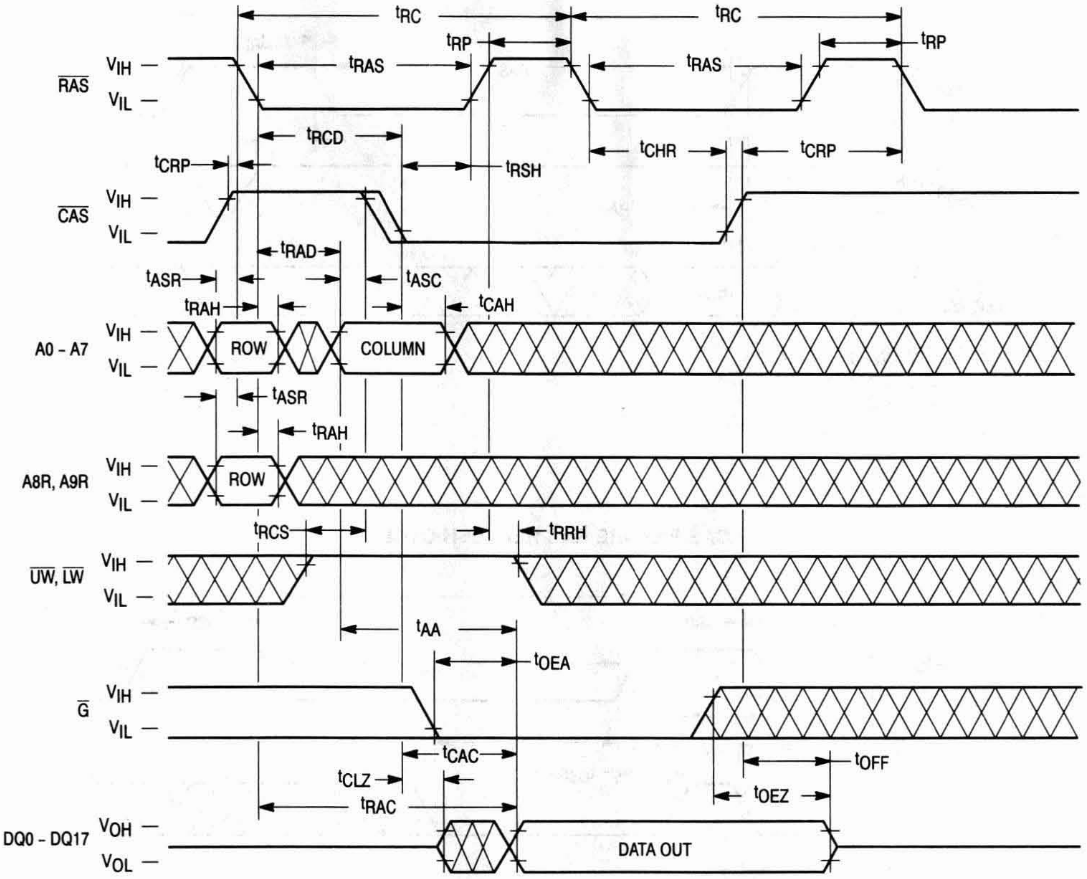
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE


tRP
tRASP
RAS
VIH
VIL
tCSH
tPRMW
tRAL
tCRP
tRCD
tCAH
CAS
tCAS
tRAD
tRAH
tCP
tASC
tCAH
tRAL
tASR
A0 – A7
ROW
COL 1
COL 2
COL N
tCAH
tRAH
tASR
A8R, A9R
ROW
tRWD
tCPWD
tRWL
tRCS
tCWD
tCWL
tWP
UW
tAWD
tMRH
tMCH
tRCS
tWP
UW
tMCH
G
tAA
tOED
tOEA
DQ0 – DQ8
tCAC
tRAC
tCPA
tOEZ
VOH
VOL
Dout 1
Dout2
Dout N
tDS
tCLZ
tDH
tOEA
tOED
DQ9 – DQ17
Din 1
Din2
Din N
tRAC
tCPA
tAA
tOEZ
tCAC
Dout 1
Dout2
Dout N
tCLZ

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE


t_{RP}
t_{RASP}
t_{CSH}
RAS
V_{IH}
V_{IL}
t_{PRMW}
t_{RSH}
t_{RCD}
t_{CAH}
t_{CRP}
t_{CAS}
CAS
t_{RAD}
t_{RAH}
t_{CP}
t_{ASC}
t_{RAL}
t_{ASR}
A0 – A7
ROW
COL 1
COL 2
COL N
A8R, A9R
t_{MCH}
t_{RCS}
t_{MRH}
UW
t_{CWD}
t_{RWL}
t_{RWD}
t_{CPWD}
t_{CWL}
LW
t_{AWD}
t_{WP}
G
t_{DS}
t_{OED}
t_{DH}
t_{OEA}
DQ0 – DQ8
V_{OH}
V_{OL}
D_{in} 1
D_{in}2
D_{in} N
t_{AA}
t_{CAC}
t_{RAC}
t_{CPA}
t_{OEZ}
D_{out} 1
D_{out}2
D_{out} N
t_{CLZ}
DQ9 – DQ17

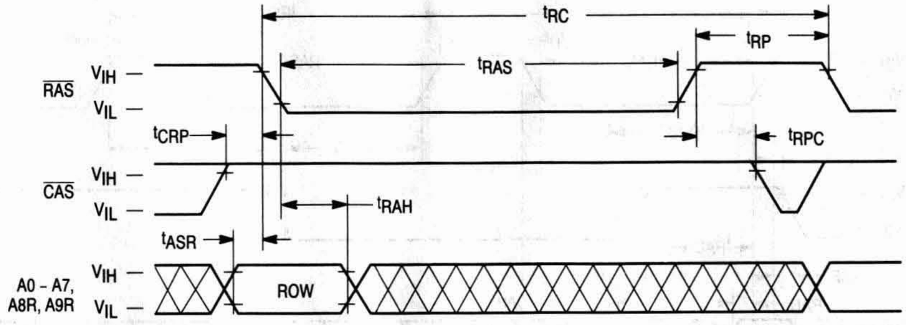
HIDDEN REFRESH CYCLE (READ)



tRC
tRC
tRP
tRP
RAS
VIH
VIL
tRAS
tRAS
tRCD
tCRP
tRSH
tCHR
tCRP
CAS
VIH
VIL
tRAD
tASR
tASC
tRAH
tCAH
A0 - A7
VIH
VIL
ROW
COLUMN
tASR
tRAH
A8R, A9R
VIH
VIL
ROW
tRCS
tRRH
UW, LW
VIH
VIL
tAA
tOEA
G
VIH
VIL
tCAC
tCLZ
tOFF
tOEZ
tRAC
DQ0 - DQ17
VOH
VOL
DATA OUT

NOTE: D_{in} = Open

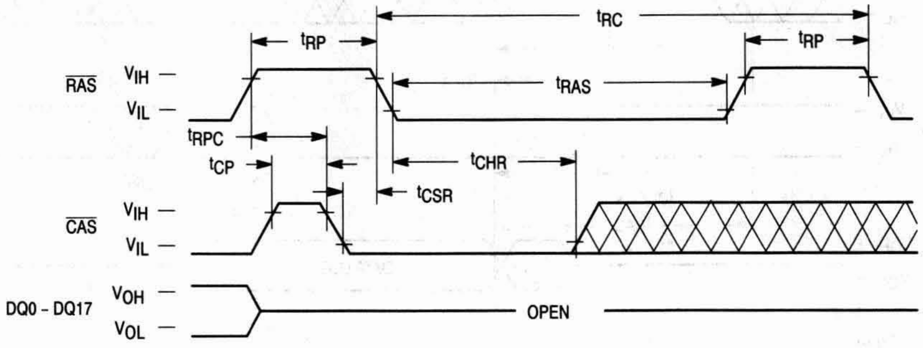
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE



tRC
tRP
tRAS
RAS
VIH
VIL
tCRP
tRPC
CAS
VIH
VIL
tRAH
tASR
A0 - A7,
A8R, A9R
VIH
VIL
ROW

NOTE: $\overline{\text{UW}}$, $\overline{\text{LW}}$, $\overline{\text{G}}$ = "H" or "L"
D_{in} = Don't Care
D_{out} = Open

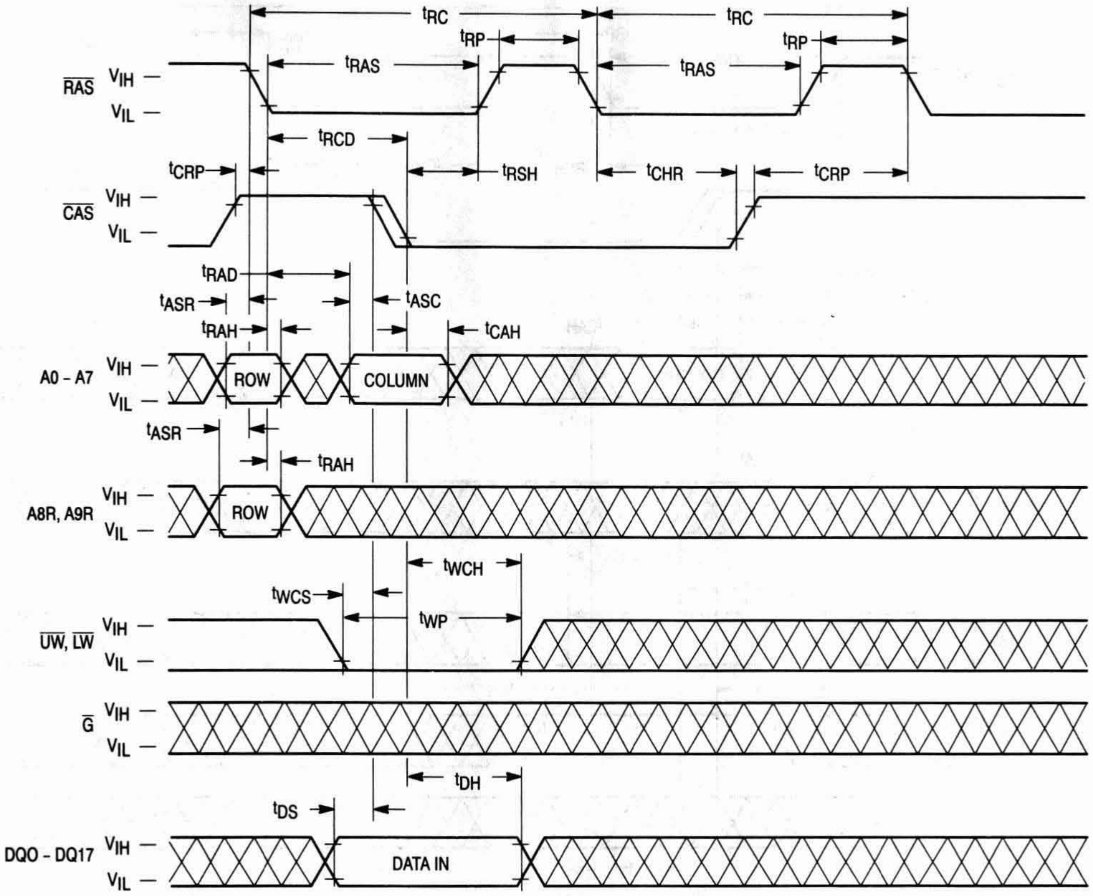
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



tRC
tRP
tRP
RAS
VIH
VIL
tRAS
tRPC
tCP
tCHR
tCSR
CAS
VIH
VIL
DQ0 - DQ17
VOH
VOL
OPEN

NOTE: $\overline{\text{UW}}$, $\overline{\text{LW}}$, $\overline{\text{G}}$, A0 – A7, A8R, A9R = "H" or "L"
D_{in} = Open

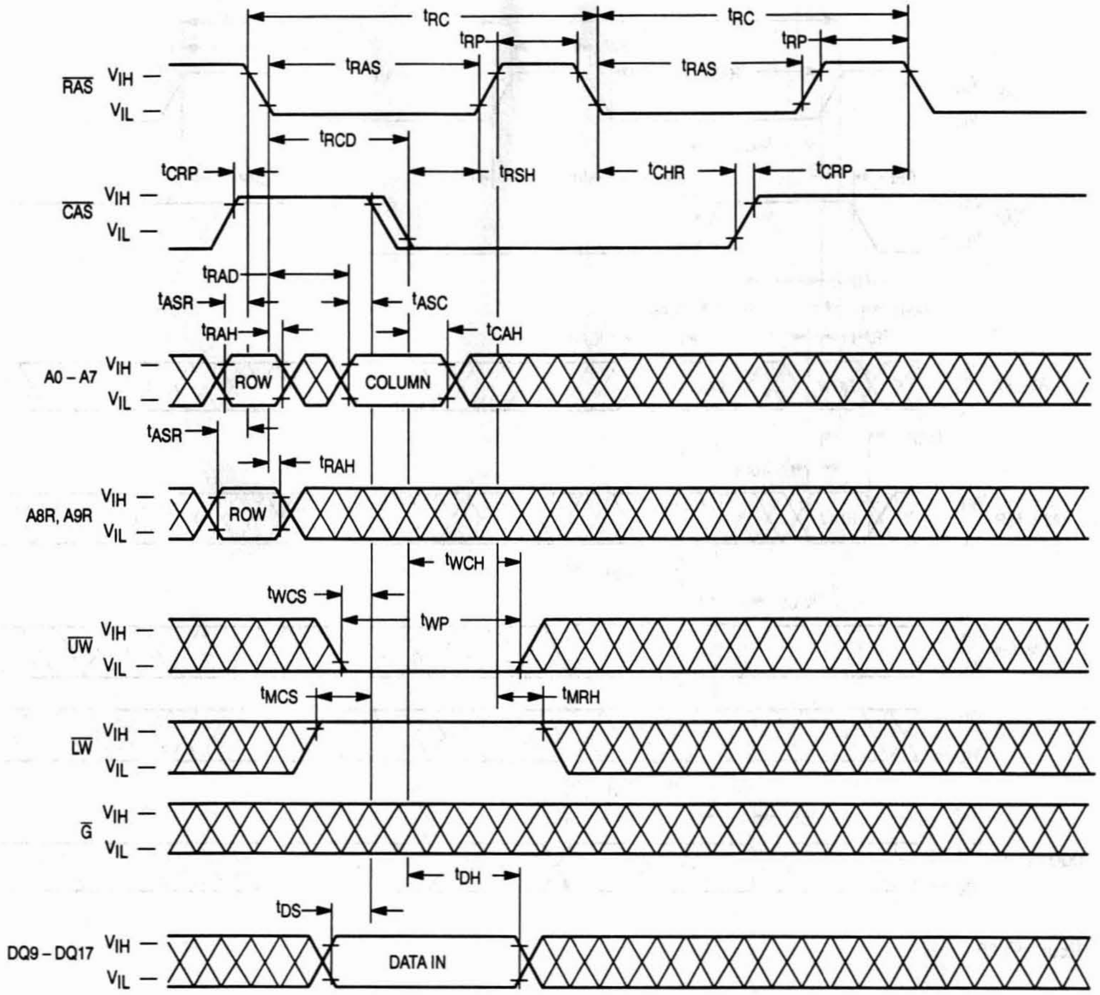
HIDDEN REFRESH CYCLE (WRITE)



t_{RC}
t_{RC}
t_{RP}
t_{RP}
t_{RAS}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RCD}
t_{CRP}
t_{RSH}
t_{CHR}
t_{CRP}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
A0 - A7
ROW
COLUMN
t_{ASR}
t_{RAH}
A8R, A9R
ROW
t_{WCH}
t_{WCS}
t_{WP}
$\overline{UW}$, $\overline{LW}$
$\overline{G}$
t_{DH}
t_{DS}
DQ0 - DQ17
DATA IN

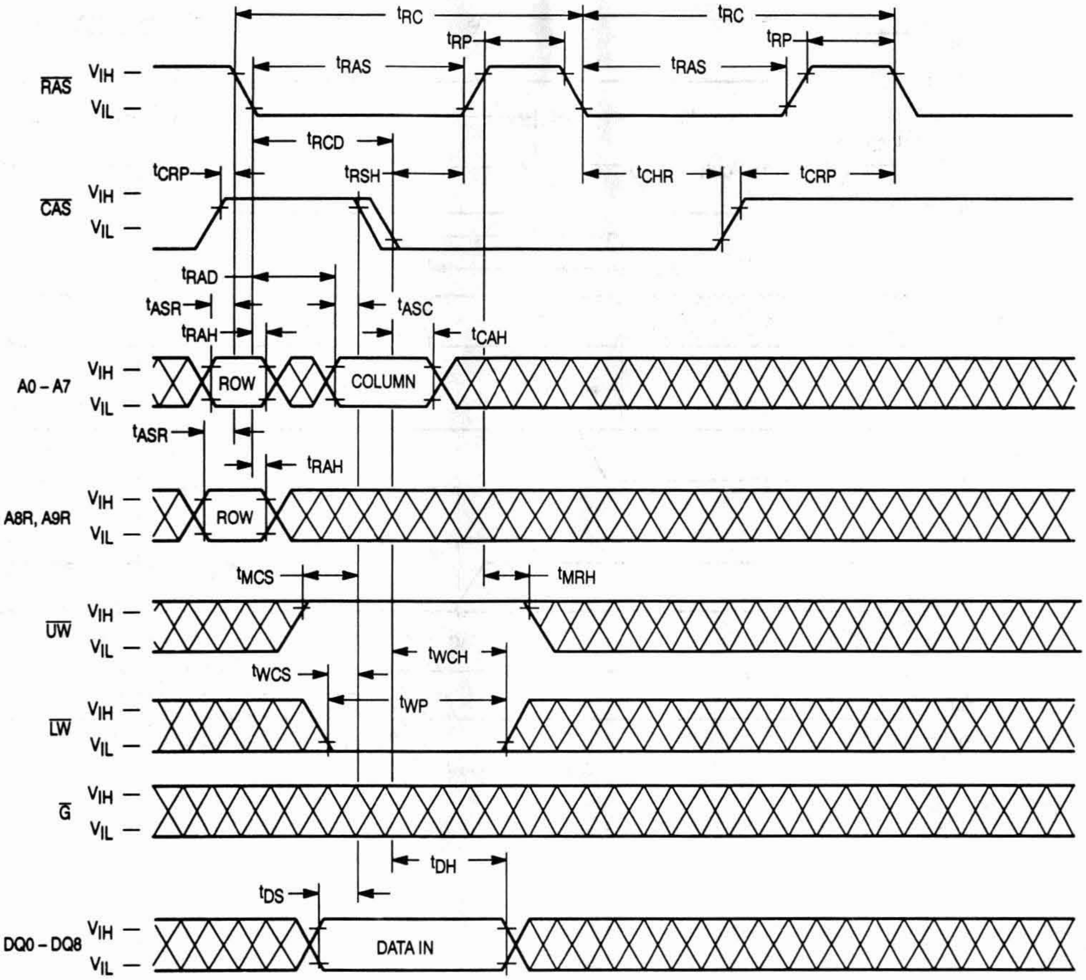
D_{out} = Open

HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)


t_{RC}
t_{RC}
t_{RP}
t_{RP}
t_{RAS}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RCD}
t_{CRP}
t_{RSH}
t_{CHR}
t_{CRP}
$\overline{CAS}$
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
A0 – A7
ROW
COLUMN
t_{ASR}
t_{RAH}
A8R, A9R
ROW
t_{WCH}
t_{WCS}
t_{WP}
$\overline{UW}$
t_{MCS}
t_{MRH}
$\overline{LW}$
$\overline{G}$
t_{DH}
t_{DS}
DQ9 – DQ17
DATA IN

NOTE: D_{in} (DQ0 – DQ8) = Don't Care
D_{out} = Open

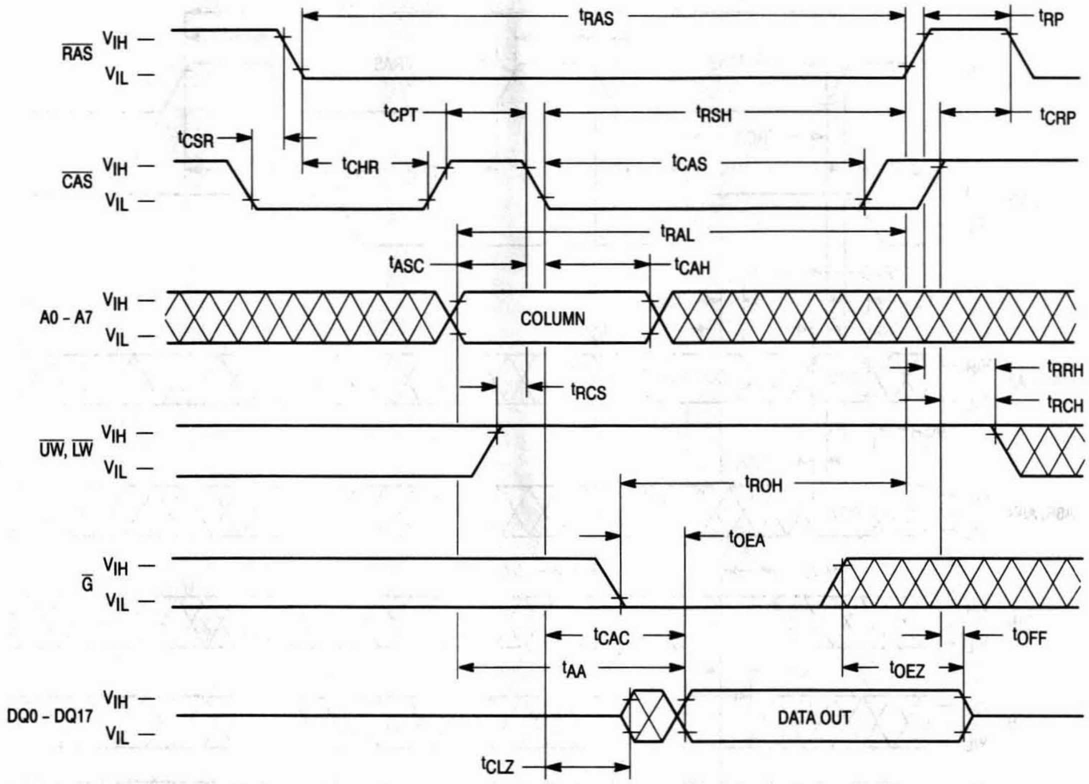
HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



tRC
tRC
tRP
tRP
tRAS
tRAS
RAS
VIH
VIL
tRCD
tCRP
tRSH
tCHR
tCRP
CAS
VIH
VIL
tRAD
tASR
tASC
tRAH
tCAH
A0 – A7
ROW
COLUMN
tASR
tRAH
A8R, A9R
ROW
tMCS
tMRH
UW
tWCH
tWCS
tWP
LW
G
tDH
tDS
DQ0 – DQ8
DATA IN

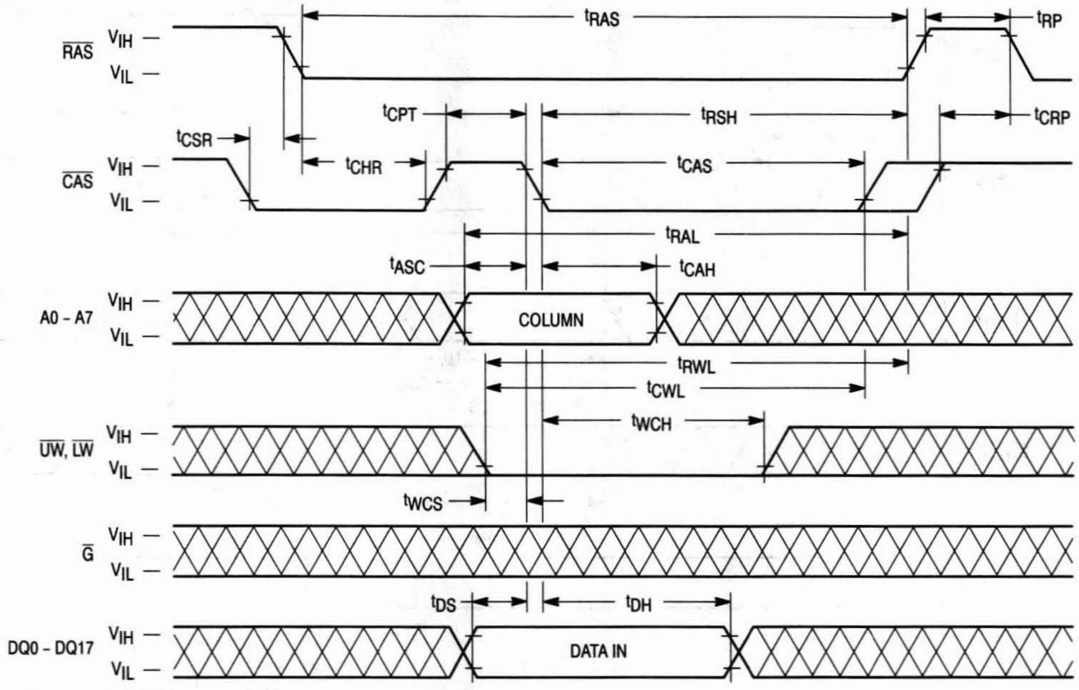
NOTE: D_{in} (DQ9 – DQ17) = Don't Care
D_{out} = Open

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST READ CYCLE


$\overline{\text{RAS}}$
V_{IH} —
V_{IL} —
t_{RAS}
t_{RP}
t_{CPT}
t_{RSH}
t_{CRP}
t_{CSR}
t_{CHR}
t_{CAS}
$\overline{\text{CAS}}$
V_{IH} —
V_{IL} —
t_{RAL}
t_{ASC}
t_{CAH}
A0 - A7
V_{IH} —
V_{IL} —
COLUMN
t_{RRH}
t_{RCS}
t_{RCH}
$\overline{\text{UW}}$, $\overline{\text{LW}}$
V_{IH} —
V_{IL} —
t_{ROH}
t_{OEA}
$\overline{\text{G}}$
V_{IH} —
V_{IL} —
t_{CAC}
t_{OFF}
t_{AA}
t_{OEZ}
DQ0 - DQ17
V_{IH} —
V_{IL} —
DATA OUT
t_{CLZ}

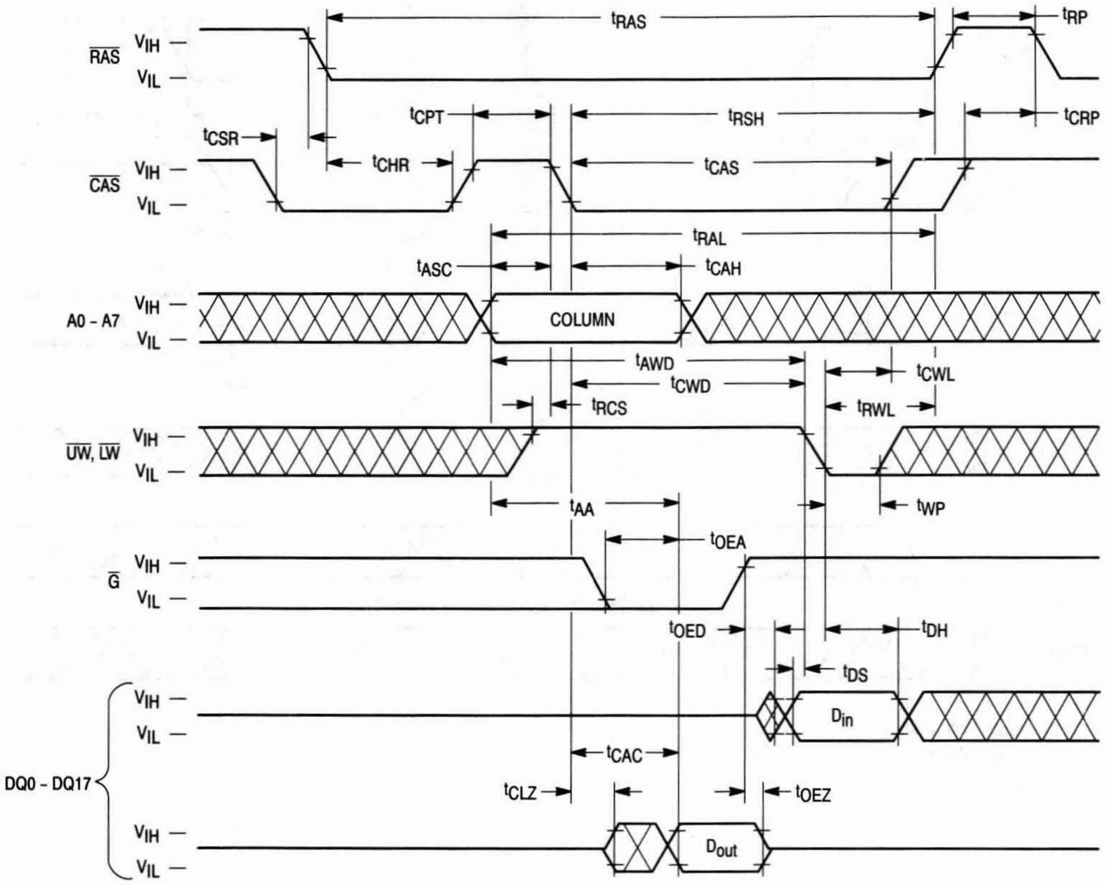
NOTE: A8R, A9R = "H" or "L"
D_{out} = Open

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST WRITE CYCLE


RAS
CAS
A0 - A7
UW, LW
G
DQ0 - DQ17
VIH
VIL
tRAS
tRP
tCPT
tRSH
tCRP
tCSR
tCHR
tCAS
tRAL
tASC
tCAH
COLUMN
tRWL
tCWL
tWCH
tWCS
tDS
tDH
DATA IN

NOTE: A8R, A9R = "H" or "L"
D_{out} = Open

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE


$\overline{RAS}$
V_{IH}
V_{IL}
t_{RAS}
t_{RP}
t_{CPT}
t_{RSH}
t_{CRP}
t_{CSR}
t_{CHR}
t_{CAS}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAL}
t_{ASC}
t_{CAH}
A0 - A7
V_{IH}
V_{IL}
COLUMN
t_{AWD}
t_{CWD}
t_{CWL}
t_{RCS}
t_{RWL}
$\overline{UW}$, $\overline{LW}$
V_{IH}
V_{IL}
t_{AA}
t_{WP}
t_{OEA}
$\overline{G}$
V_{IH}
V_{IL}
t_{OED}
t_{DH}
t_{DS}
V_{IH}
V_{IL}
D_{in}
DQ0 - DQ17
t_{CAC}
t_{CLZ}
t_{OEZ}
V_{IH}
V_{IL}
D_{out}

NOTE: A8R, A9R = "H" or "L"

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight $\overline{\text{RAS}}$-Only refresh cycles or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight $\overline{\text{RAS}}$-Only refresh cycles or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks and will decode one of the 262,144 bit locations in the device. The row address strobe ($\overline{\text{RAS}}$) latches 10 row addresses, and the column access strobe ($\overline{\text{CAS}}$) latches eight column addresses. $\overline{\text{RAS}}$ active transition followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) follows $\overline{\text{RAS}}$ on all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

There are three other variations in addressing the 256K x 18 RAM: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{\text{CAS}}$ and output enable ($\overline{\text{G}}$) control read access time: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum, and $\overline{\text{G}}$ must be active t_{RAC}-t_{GA} (both minimum) to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{\text{G}}$ active transition does not occur in time, read access time is determined by either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ and $\overline{\text{G}}$ clocks are active. When either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers and $\overline{\text{G}}$ disabled.

A late write cycle (referred to as $\overline{\text{G}}$-controlled write) occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but outputs are switched off by $\overline{\text{G}}$ inactive transition, which is required to write to the device. Q may be indeterminate — see note 12 of AC Operating Conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle. $\overline{\text{G}}$ must remain inactive for t_{GH} after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the 256K x 18 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in the prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order.

The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54190B require refresh every 16 milliseconds, while refresh for the MCM5L4190B and MCM5V4190B is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54190B, and 124.8 microseconds for the MCM5L4190B and MCM5V4190B. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54190B, and 128 milliseconds for the MCM5L4190B and MCM5V4190B.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decodes. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh,** and **self refresh** (MCM5V4190B only) are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure that all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order actives an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

Self Refresh (MCM5V4190B Only)

The self refresh is a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh where $\overline{\text{RAS}}$ is held low for a period greater than t_{RASS} (100 microseconds). After this time, an internal timer activates a refresh operation of consecutive row addresses in the dynamic RAM. The self refresh mode is exited when either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ transitions to high (V_{IH}). Because of the long periods involved for this method of refresh, it is recommended that the self refresh mode only be used for long periods of standby, such as a battery backup.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test.** This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

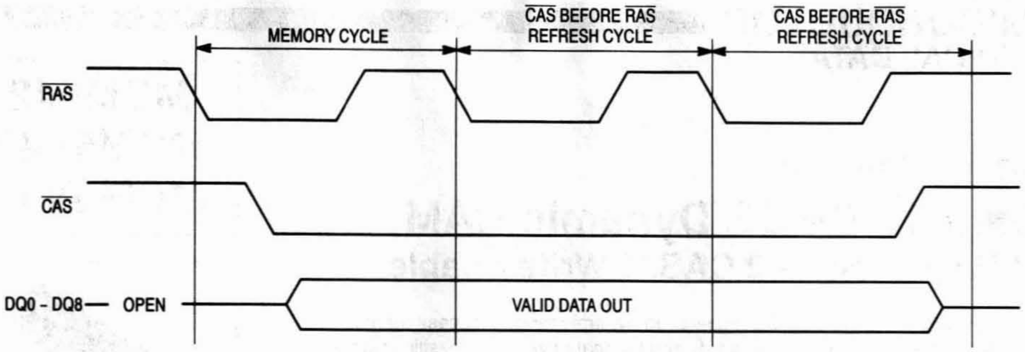

MEMORY CYCLE
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
$\overline{RAS}$
$\overline{CAS}$
DQ0 - DQ8 — OPEN
VALID DATA OUT

Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 54190B / 5L4190B / 5V4190B X XX XX

Motorola Memory Prefix — MCM
Part Number — 54190B, 5L4190B, 5V4190B
Package (J = 400 mil SOJ, T = 400 mil TSOP) — X
Speed (70 = 70 ns, 80 = 80 ns, 10 = 100 ns) — XX
Shipping Method (Blank = Tray, R = Tape and Reel, Blank = Rails) — XX

Full Part Numbers —	MCM54190BJ70	MCM5L4190BJ70	MCM5V4190BJ70
	MCM54190BJ80	MCM5L4190BJ80	MCM5V4190BJ80
	MCM54190BJ10	MCM5L4190BJ10	MCM5V4190BJ10
	MCM54190BT70	MCM5L4190BT70	MCM5V4190BT70
	MCM54190BT80	MCM5L4190BT80	MCM5V4190BT80
	MCM54190BT10	MCM5L4190BT10	MCM5V4190BT10
	MCM54190BJ70R	MCM5L4190BJ70R	MCM5V4190BJ70R
	MCM54190BJ80R	MCM5L4190BJ80R	MCM5V4190BJ80R
	MCM54190BJ10R	MCM5L4190BJ10R	MCM5V4190BJ10R
	MCM54190BT70R	MCM5L4190BT70R	MCM5V4190BT70R
	MCM54190BT80R	MCM5L4190BT80R	MCM5V4190BT80R
	MCM54190BT10R	MCM5L4190BT10R	MCM5V4190BT10R

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM54260B
MCM5L4260B
MCM5V4260B

Product Preview

256K x 16 CMOS Dynamic RAM
Fast Page Mode – 2 CAS, 1 Write Enable

The MCM54260B is a 0.6µ CMOS high-speed dynamic random access memory. It is organized as 262,144 sixteen-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM54260B requires only 9 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 400 mil SOJ plastic package and a 400 mil thin-small-outline package (TSOP).

- Three-State Data Output
- Fast Page Mode
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- Self Refresh (MCM5V4260B only)
- 512 Cycle Refresh:
  - MCM54260B = 8 ms
  - MCM5L4260B and MCM5V4260B = 64 ms
- Fast Access Time (t_{RAC}):
  - MCM54260B-70, MCM5L4260B-70, and MCM5V4260B-70 = 70 ns (Max)
  - MCM54260B-80, MCM5L4260B-80, and MCM5V4260B-80 = 80 ns (Max)
  - MCM54260B-10, MCM5L4260B-10, and MCM5V4260B-10 = 100 ns (Max)
- Low Active Power Dissipation:
  - MCM54260B-70, MCM5L4260B-70, and MCM5V4260B-70 = 550 mW (Max)
  - MCM54260B-80, MCM5L4260B-80, and MCM5V4260B-80 = 468 mW (Max)
  - MCM54260B-10, MCM5L4260B-10, and MCM5V4260B-10 = 413 mW (Max)
- Low Standby Power Dissipation:
  - MCM54260B, MCM5L4260B, and MCM5V4260B = 5.5 mW (Max, TTL Levels)
- Battery Backup Power Dissipation:
  - MCM5L4260B = 1.7 mW (Max, Battery Backup Mode, t_{RC} = 125 µs)
- Self Refresh Power Dissipation:
  - MCM5V4260B = 1.1 mW (Max, Self Refresh Mode)

J PACKAGE
400 MIL SOJ
CASE TBD

T PACKAGE
400 MIL TSOP
CASE 924-01

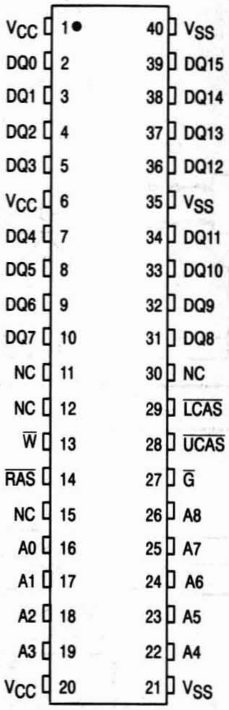
PIN NAMES

A0 – A8	Address Inputs
DQ0 – DQ15	Data Input/Output
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connect
$\overline{\text{G}}$	Output Enable

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

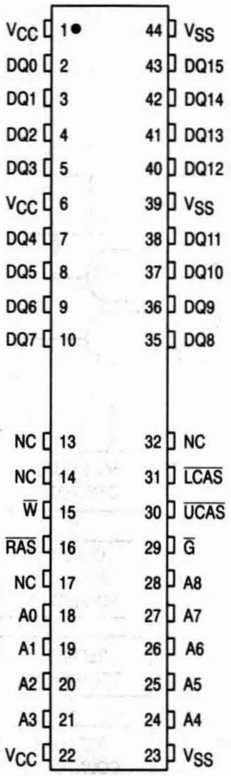
PIN ASSIGNMENTS

400 MIL SOJ



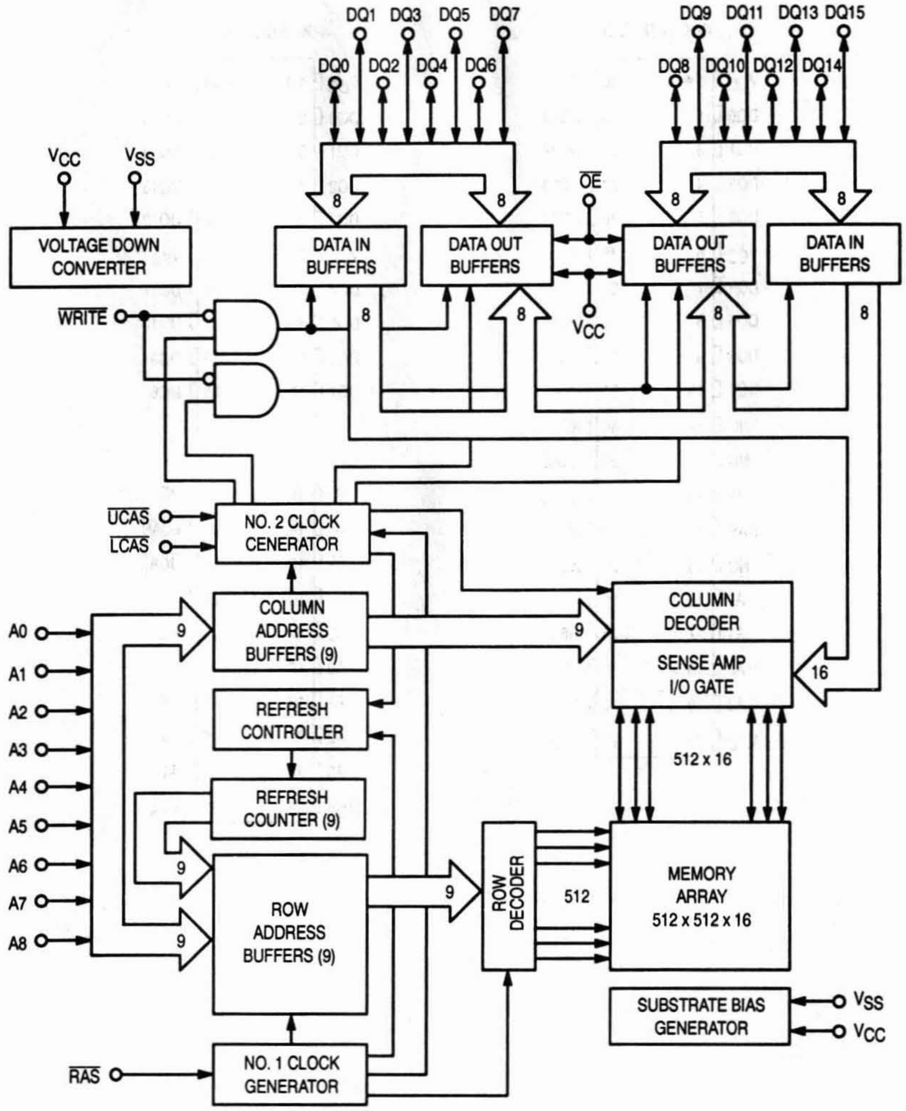
VCC 1 40 VSS
DQ0 2 39 DQ15
DQ1 3 38 DQ14
DQ2 4 37 DQ13
DQ3 5 36 DQ12
VCC 6 35 VSS
DQ4 7 34 DQ11
DQ5 8 33 DQ10
DQ6 9 32 DQ9
DQ7 10 31 DQ8
NC 11 30 NC
NC 12 29 $\overline{LCAS}$
$\overline{W}$ 13 28 $\overline{UCAS}$
$\overline{RAS}$ 14 27 $\overline{G}$
NC 15 26 A8
A0 16 25 A7
A1 17 24 A6
A2 18 23 A5
A3 19 22 A4
VCC 20 21 VSS

400 MIL TSOP



VCC 1 44 VSS
DQ0 2 43 DQ15
DQ1 3 42 DQ14
DQ2 4 41 DQ13
DQ3 5 40 DQ12
VCC 6 39 VSS
DQ4 7 38 DQ11
DQ5 8 37 DQ10
DQ6 9 36 DQ9
DQ7 10 35 DQ8
NC 13 32 NC
NC 14 31 $\overline{LCAS}$
$\overline{W}$ 15 30 $\overline{UCAS}$
$\overline{RAS}$ 16 29 $\overline{G}$
NC 17 28 A8
A0 18 27 A7
A1 19 26 A6
A2 20 25 A5
A3 21 24 A4
VCC 22 23 VSS

BLOCK DIAGRAM


DQ1 DQ3 DQ5 DQ7
DQ0 DQ2 DQ4 DQ6
DQ9 DQ11 DQ13 DQ15
DQ8 DQ10 DQ12 DQ14
VCC
VSS
VOLTAGE DOWN CONVERTER
DATA IN BUFFERS
DATA OUT BUFFERS
OE
DATA OUT BUFFERS
DATA IN BUFFERS
VCC
8
WRITE
UCAS
LCAS
NO. 2 CLOCK CENERATOR
A0
A1
A2
A3
A4
A5
A6
A7
A8
COLUMN ADDRESS BUFFERS (9)
9
COLUMN DECODER
SENSE AMP I/O GATE
16
512 x 16
REFRESH CONTROLLER
REFRESH COUNTER (9)
ROW ADDRESS BUFFERS (9)
ROW DECODER
512
MEMORY ARRAY 512 x 512 x 16
SUBSTRATE BIAS GENERATOR
VSS
VCC
RAS
NO. 1 CLOCK GENERATOR

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.0	V
Logic Low Voltage, All Inputs Except DQ0 – DQ7	V_{IL}	– 0.5*	—	0.8	V
Logic Low Voltage, DQ0 – DQ7	V_{IL}	– 0.5*	—	0.8	V

*– 2.0 V at pulse width ≤ 20 ns

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	1, 2
MCM54260B-70, MCM5L4260B-70, and MCM5V4260B-70, t_{RC} = 130 ns		—	100		
MCM54260B-80, MCM5L4260B-80, and MCM5V4260B-80, t_{RC} = 150 ns		—	85		
MCM54260B-10, MCM5L4260B-10, and MCM5V4260B-10, t_{RC} = 180 ns		—	75		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	1, 2
MCM54260B-70, MCM5L4260B-70, and MCM5V4260B-70, t_{RC} = 130 ns		—	100		
MCM54260B-80, MCM5L4260B-80, and MCM5V4260B-80, t_{RC} = 150 ns		—	85		
MCM54260B-10, MCM5L4260B-10, and MCM5V4260B-10, t_{RC} = 180 ns		—	75		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	1, 2
MCM54260B-70, MCM5L4260B-70, and MCM5V4260B-70, t_{PC} = 45 ns		—	70		
MCM54260B-80, MCM5L4260B-80, and MCM5V4260B-80, t_{PC} = 50 ns		—	60		
MCM54260B-10, MCM5L4260B-10, and MCM5V4260B-10, t_{PC} = 60 ns		—	55		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM54260B	I_{CC5}	—	1.0	mA	
MCM5L4260B and MCM5V4260B		—	200	µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	1
MCM54260B-70, MCM5L4260B-70, and MCM5V4260B-70, t_{RC} = 130 ns		—	100		
MCM54260B-80, MCM5L4260B-80, and MCM5V4260B-80, t_{RC} = 150 ns		—	85		
MCM54260B-10, MCM5L4260B-10, and MCM5V4260B-10, t_{RC} = 180 ns		—	75		
V_{CC} Power Supply Current, Battery Backup Mode — MCM5L4260B Only (t_{RC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0 – A8, $\overline{W}$, D = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	—	300	µA	1, 3
V_{CC} Power Supply Current, Self Refresh Mode — MCM5V4260B Only ($\overline{RAS}$ = $\overline{CAS}$ = V_{IL}; A0 – A8, $\overline{W}$, $\overline{G}$ = V_{CC} – 0.2 V or 0.2 V; DQ0–DQ7 = V_{CC} – 0.2 V, 0.2 V, or Open)	I_{CC8}	—	200	µA	
Input Leakage Current (0 V ≤ V_{in} ≤ 7.0 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ 7.0 V, Output Disable)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading. Maximum currents are at the specified cycle time (min) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery back-up. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, periodically sampled, not 100% tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A8	C_{in}	5	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{G}$		7	
Input/Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0 – DQ15	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM54260B-70 MCM5L4260B-70 MCM5V4260B-70		MCM54260B-80 MCM5L4260B-80 MCM5V4260B-80		MCM54260B-10 MCM5L4260B-10 MCM5V4260B-10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	180	—	ns	5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RWC}	185	—	205	—	245	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	50	—	60	—	ns	
Page Mode Read-Modify-Write Cycle Time	t_{CELCEL}	t_{PRWC}	100	—	105	—	125	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	—	100	ns	6,7,8
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	25	ns	6, 7
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	50	ns	6, 8
Access Time from $\overline{\text{CAS}}$ Precharge	t_{CEHQV}	t_{CPA}	—	40	—	45	—	55	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	15	0	20	ns	9
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	70	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	7
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	8
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Page Mode Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Hold Time From $\overline{\text{CAS}}$ Precharge (Page Mode Only)	t_{CEHREH}	t_{RHCP}	40	—	45	—	55	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	50	—	ns	

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles or 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0 \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greaer than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
9. t_{OFF} (max) and t_{GZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM54260B-70 MCM5L4260B-70 MCM5V4260B-70		MCM54260B-80 MCM5L4260B-80 MCM5V4260B-80		MCM54260B-10 MCM5L4260B-10 MCM5V4260B-10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	10
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{CELWH}	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	11
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	20	—	ns	11
Refresh Period MCM54260B MCM5L4260B and MCM5V4260B	t_{RVRV}	t_{RFSH}	— —	8 128	— —	8 128	— —	8 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	12
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	60	—	ns	12
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	100	—	110	—	135	—	ns	12
Column Address to Write Delay	t_{AVWL}	t_{AWD}	65	—	70	—	85	—	ns	12
$\overline{\text{CAS}}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	70	—	75	—	90	—	ns	12
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle	t_{RELCEH}	t_{CHR}	15	—	15	—	20	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test)	t_{CEHCEL}	t_{CPT}	30	—	30	—	40	—	ns	
$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{G}}$	t_{GLREH}	t_{ROH}	10	—	10	—	20	—	ns	
$\overline{\text{G}}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	20	—	25	ns	6
$\overline{\text{G}}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	25	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{\text{G}}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	25	ns	9
$\overline{\text{G}}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	25	—	ns	
Output Disable Setup Time	t_{GLCEL}	t_{GDS}	0	—	0	—	0	—	ns	

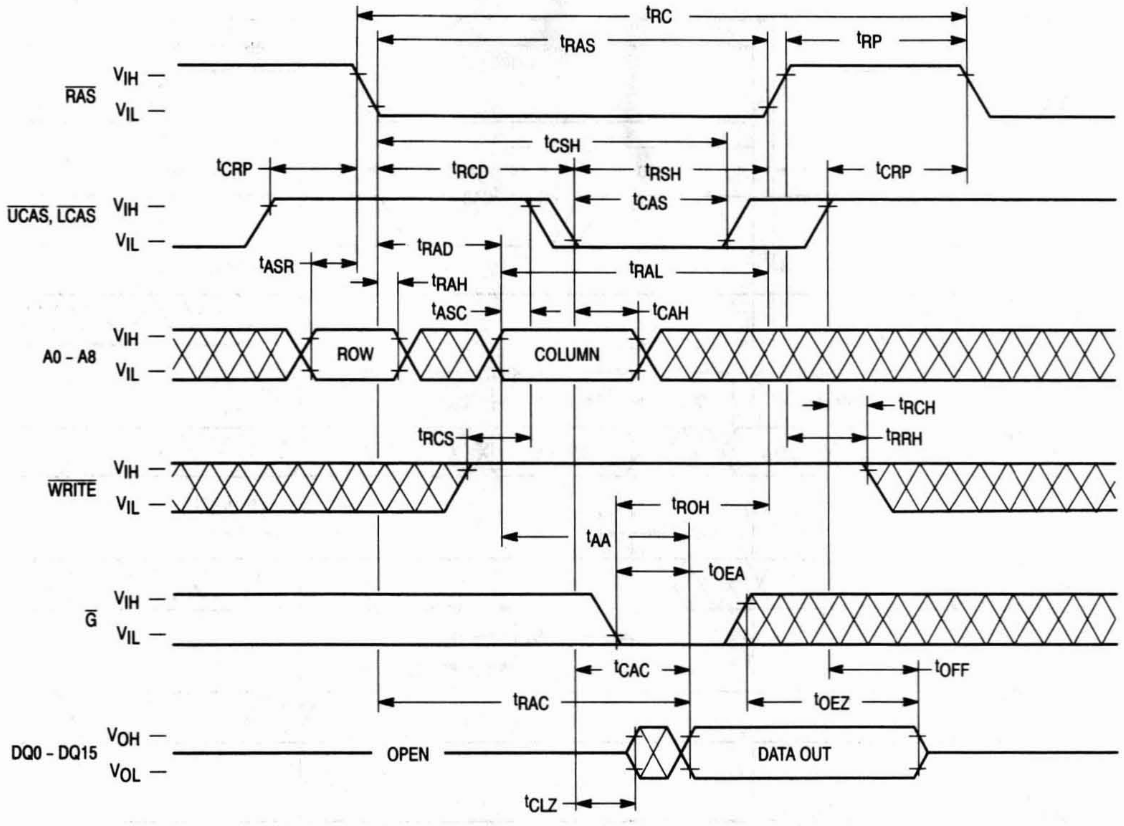
NOTES:

10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in late write or read-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

SELF REFRESH CYCLE

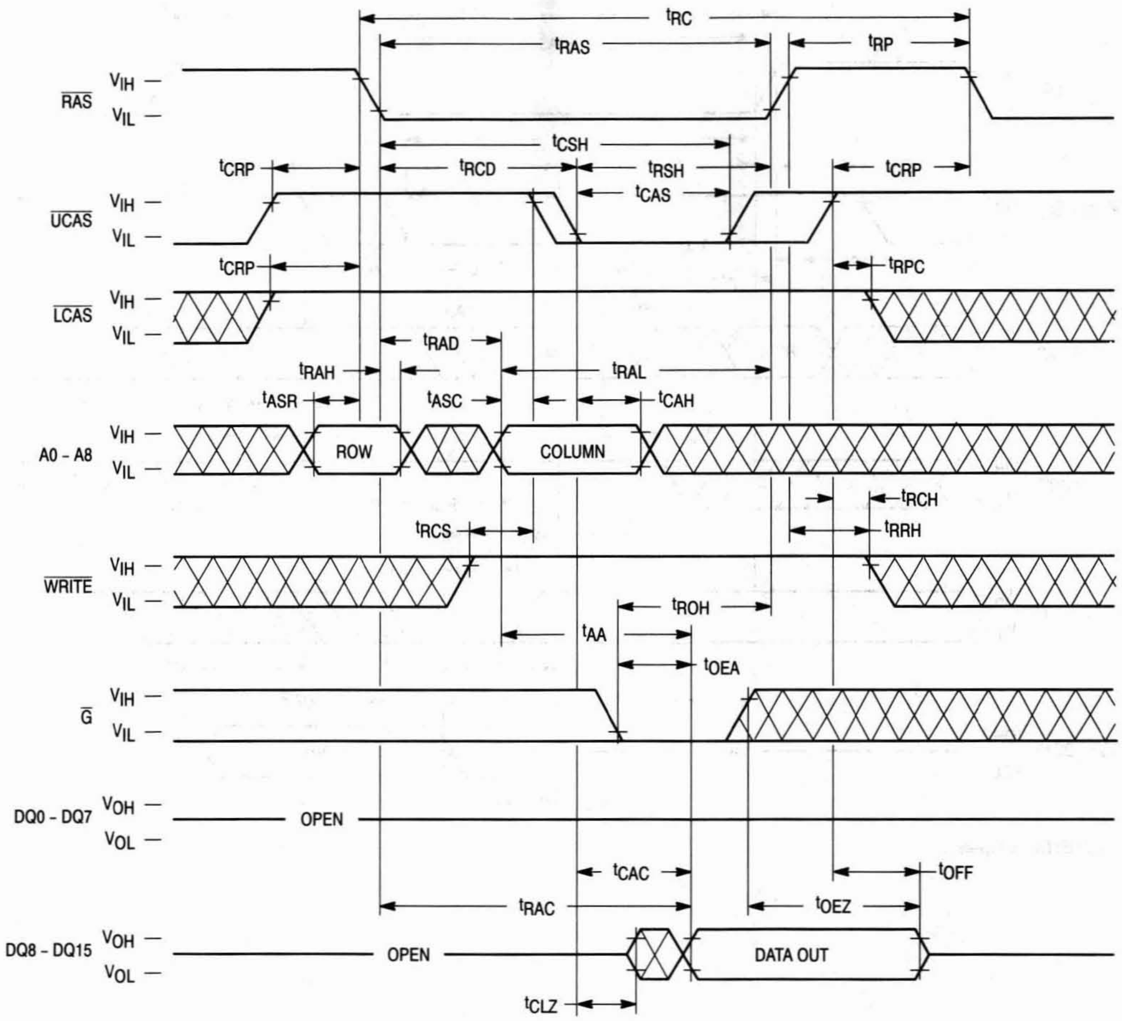
	Symbol		MCM54260B-70 MCM5L4260B-70 MCM5V4260B-70		MCM54260B-80 MCM5L4260B-80 MCM5V4260B-80		MCM54260B-10 MCM5L4260B-10 MCM5V4260B-10			
Parameter	**Std**	**Alt**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh, MCM5V4260B Only)	$t_{RELREHS}$	t_{RASS}	100	—	100	—	100	—	µs	
$\overline{\text{RAS}}$ Prechange Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh, MCM5V4260B Only)	$t_{REHRELS}$	t_{RPS}	130	—	150	—	180	—	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh, MCM5V4260B Only)	t_{REHCEH}	t_{CHS}	–50	—	–60	—	–70	—	ns	

READ CYCLE


tRC
tRAS
tRP
RAS
VIH —
VIL —
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
UCAS, LCAS
VIH —
VIL —
tRAD
tASR
tRAL
tRAH
tASC
tCAH
A0 - A8
VIH —
VIL —
ROW
COLUMN
tRCH
tRCS
tRRH
WRITE
VIH —
VIL —
tROH
tAA
tOEA
G
VIH —
VIL —
tCAC
tOFF
tRAC
tOEZ
DQ0 - DQ15
VOH —
VOL —
OPEN
DATA OUT
tCLZ

NOTE: D_{in} = Open

UPPER BYTE READ CYCLE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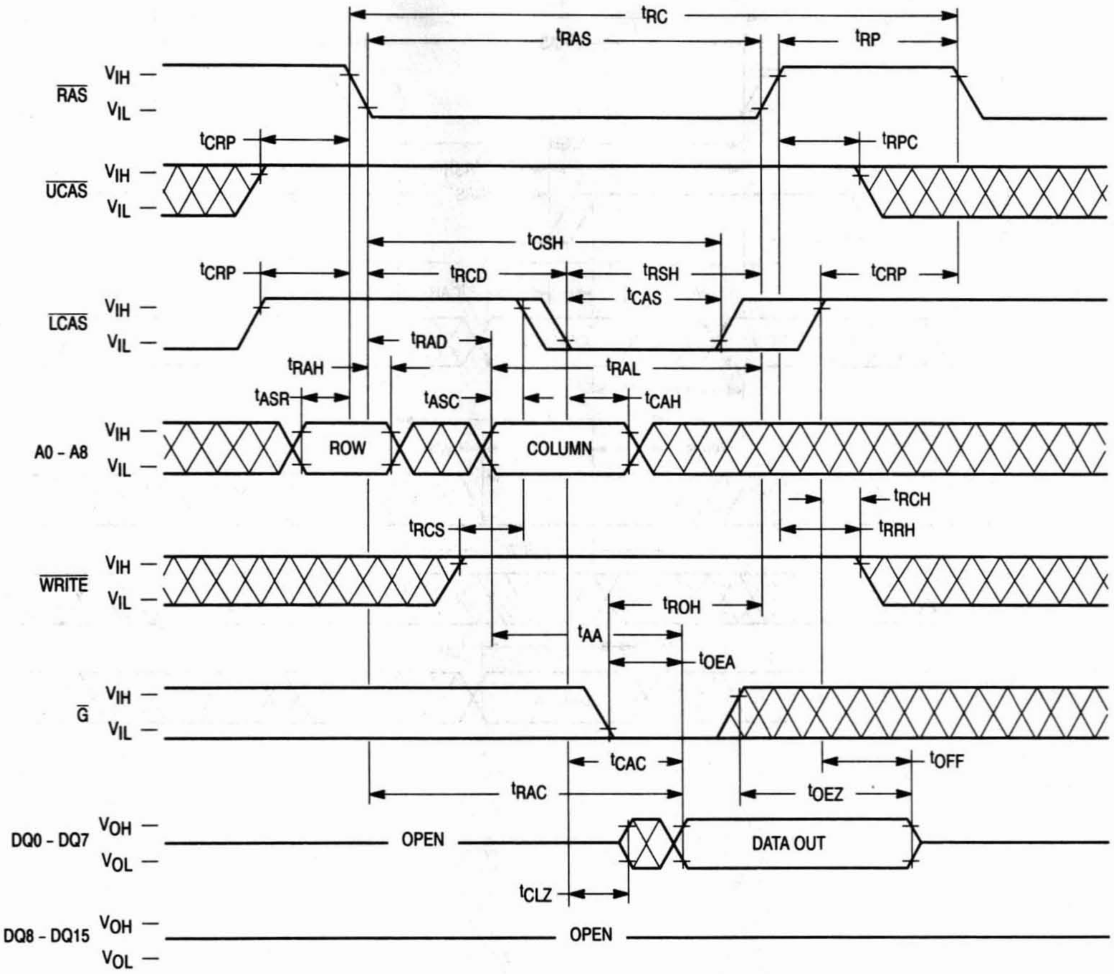
t_{RAS}
t_{RP}
RAS
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
UCAS
t_{CRP}
t_{RPC}
LCAS
t_{RAD}
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 - A8
ROW
COLUMN
t_{RCH}
t_{RCS}
t_{RRH}
WRITE
t_{ROH}
t_{AA}
t_{OEA}
G
DQ0 - DQ7
V_{OH}
V_{OL}
OPEN
t_{CAC}
t_{OFF}
t_{RAC}
t_{OEZ}
DQ8 - DQ15
OPEN
DATA OUT
t_{CLZ}

NOTE: D_{in} (DQ0 – DQ7) = Don't Care
D_{in} (DQ8 – DQ15) = Open

LOWER BYTE READ CYCLE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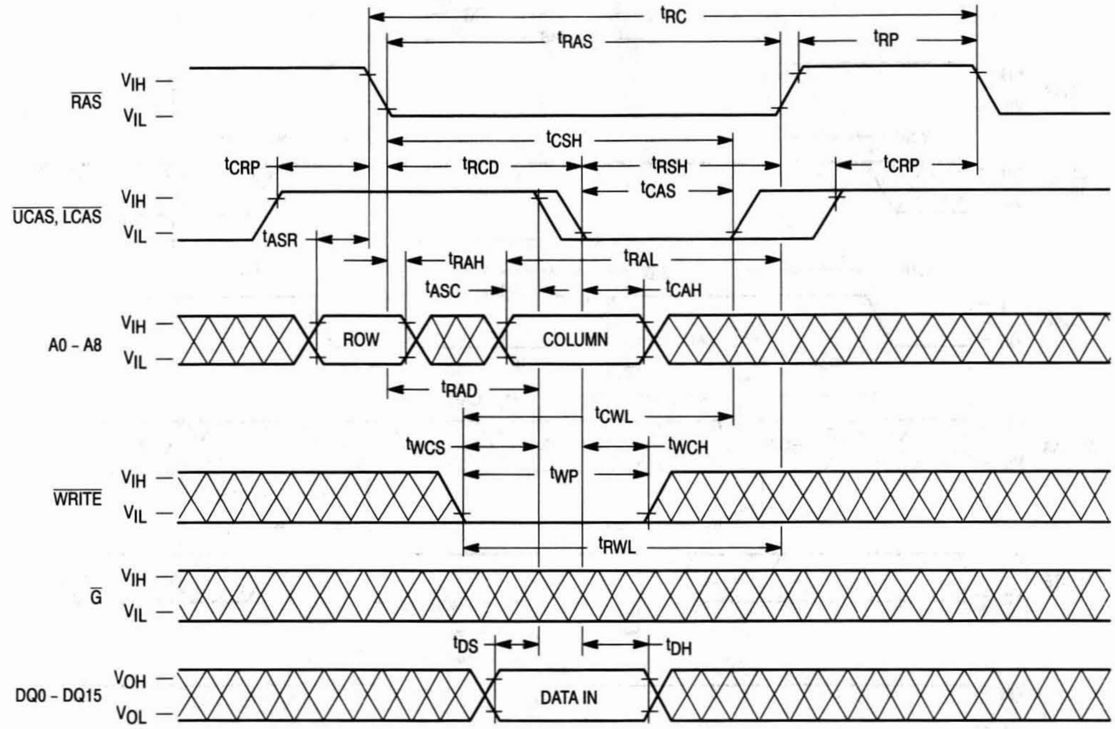
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{UCAS}$
t_{CSH}
t_{RCD}
t_{RSH}
t_{CAS}
$\overline{LCAS}$
t_{RAD}
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 - A8
ROW
COLUMN
t_{RCH}
t_{RRH}
t_{RCS}
$\overline{WRITE}$
t_{ROH}
t_{AA}
t_{OEA}
$\overline{G}$
t_{CAC}
t_{OFF}
t_{RAC}
t_{OEZ}
DQ0 - DQ7
V_{OH}
V_{OL}
OPEN
DATA OUT
t_{CLZ}
DQ8 - DQ15
OPEN

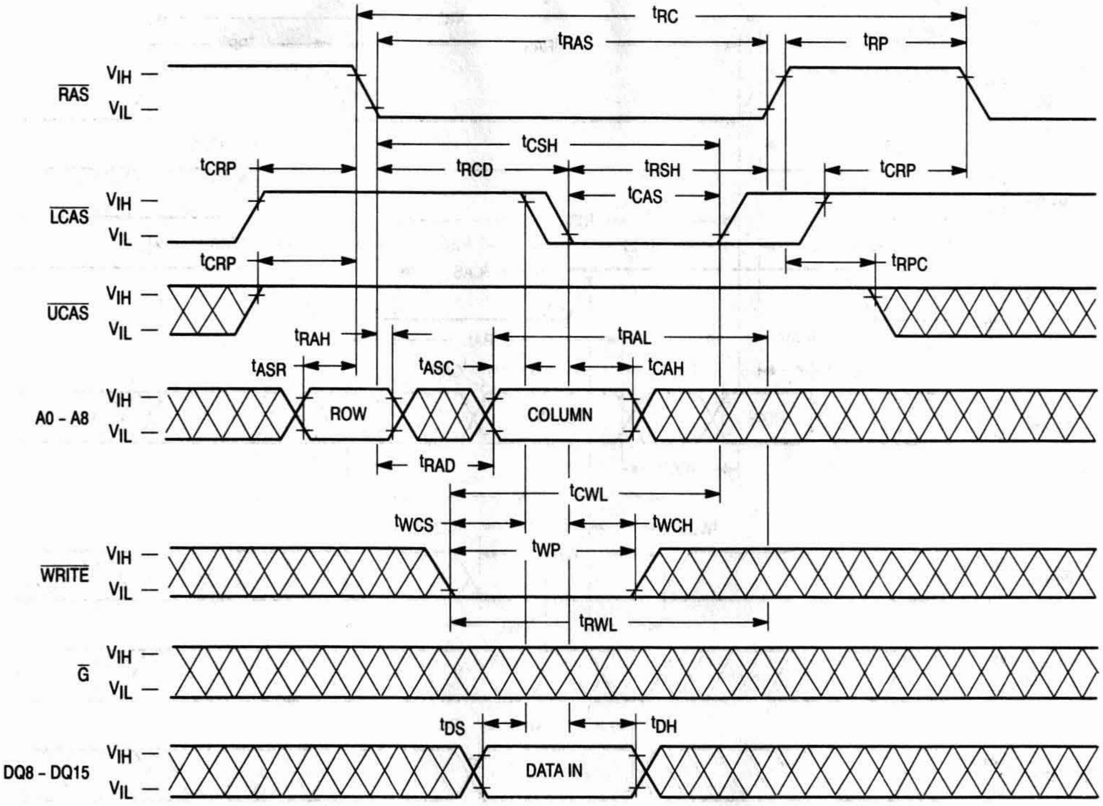
NOTE: D_{in} (DQ0 – DQ7) = Open
D_{in} (DQ8 – DQ15) = Don't Care

WRITE CYCLE (EARLY WRITE)


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
UCAS, LCAS
VIH
VIL
tASR
tRAH
tRAL
tASC
tCAH
A0 - A8
VIH
VIL
ROW
COLUMN
tRAD
tCWL
tWCS
tWCH
tWP
WRITE
VIH
VIL
tRWL
G
VIH
VIL
tDS
tDH
DQ0 - DQ15
VOH
VOL
DATA IN

NOTE: D_{out} = Open

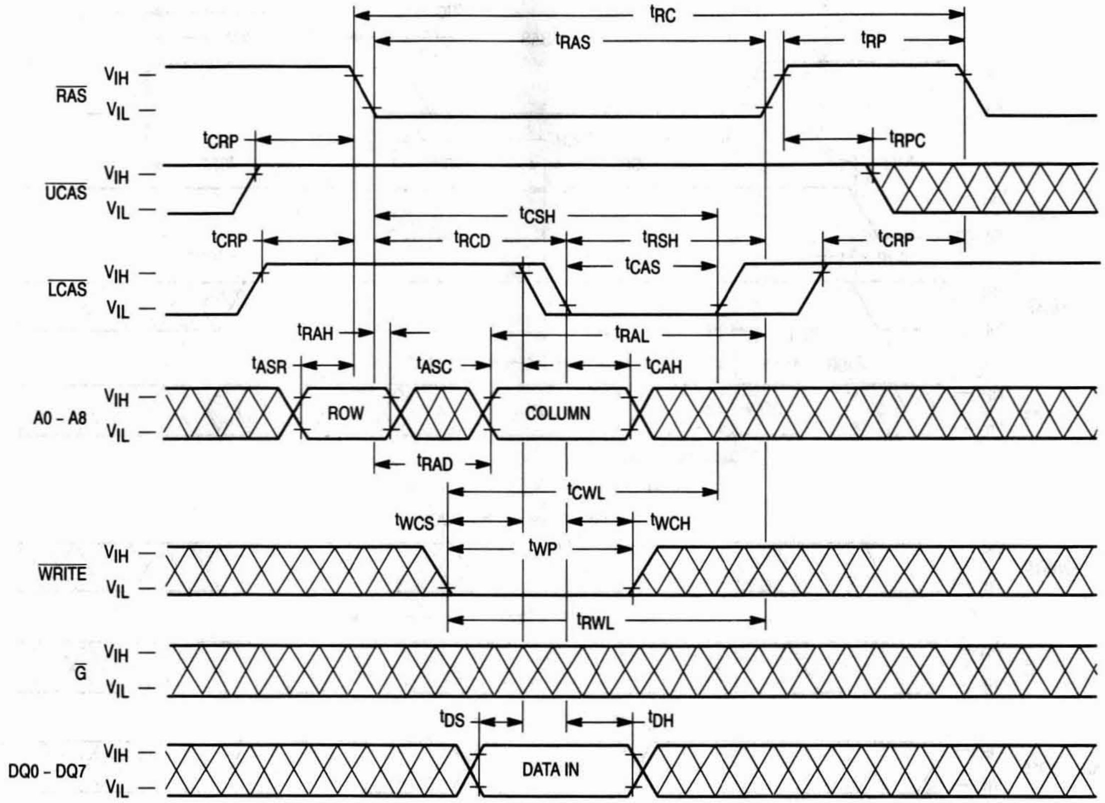
UPPER BYTE WRITE CYCLE (EARLY WRITE)



t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{LCAS}$
t_{CRP}
t_{RPC}
$\overline{UCAS}$
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 - A8
ROW
COLUMN
t_{RAD}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{WRITE}$
t_{RWL}
$\overline{G}$
t_{DS}
t_{DH}
DQ8 - DQ15
DATA IN

NOTE: D_{in} (DQ0 - DQ7) = Don't Care
D_{out} = Open

LOWER BYTE WRITE CYCLE (EARLY WRITE)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t_{RP}
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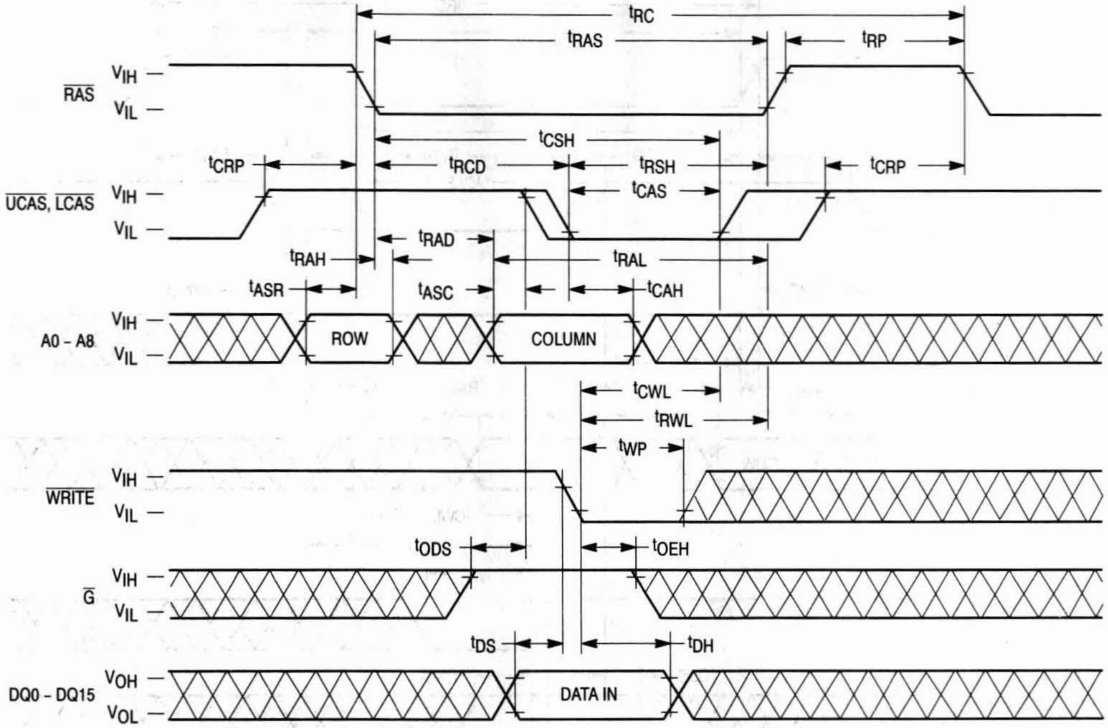
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{UCAS}$
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{LCAS}$
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 – A8
ROW
COLUMN
t_{RAD}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{WRITE}$
t_{RWL}
$\overline{G}$
t_{DS}
t_{DH}
DQ0 – DQ7
DATA IN

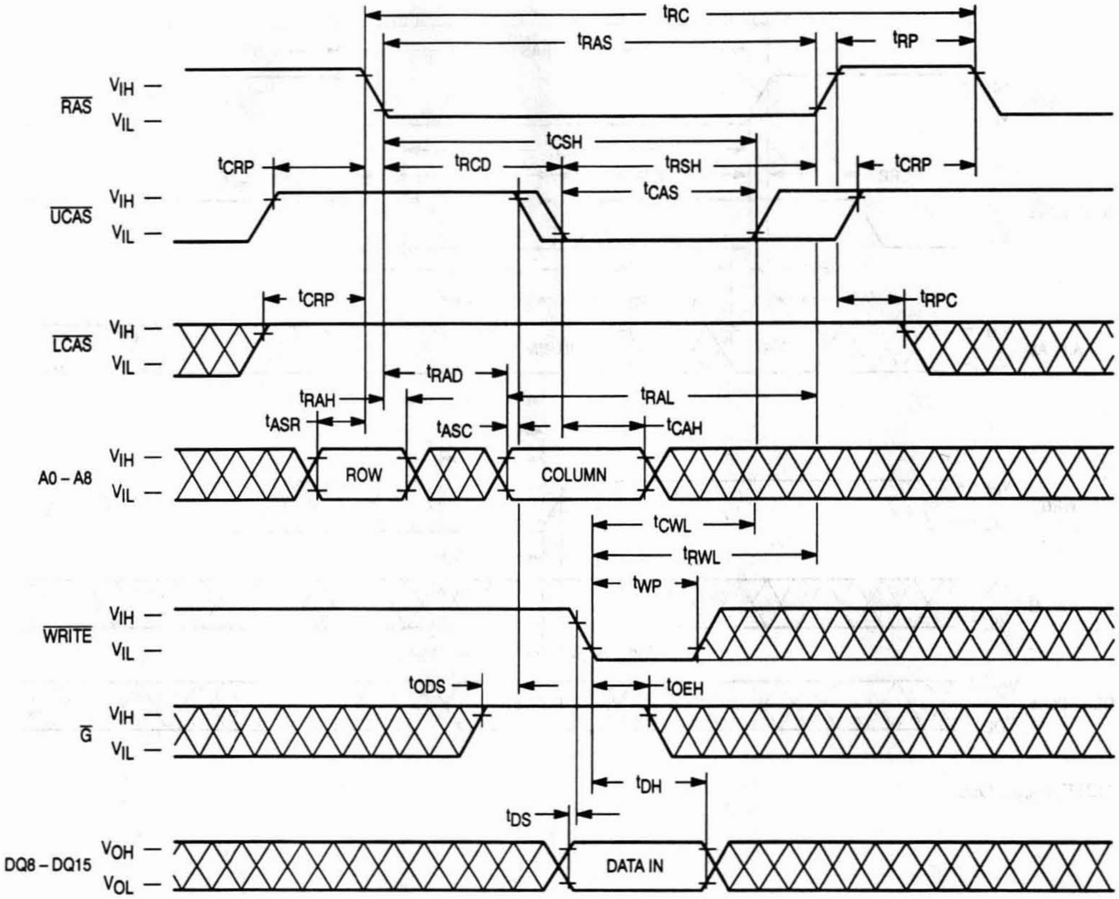
NOTE: D_{in} (DQ8 – DQ15) = Don't Care
D_{out} = Open

WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
UCAS, LCAS
VIH
VIL
tRAD
tRAH
tRAL
tASR
tASC
tCAH
A0 - A8
VIH
VIL
ROW
COLUMN
tCWL
tRWL
tWP
WRITE
VIH
VIL
tODS
tOEH
G
VIH
VIL
tDS
tDH
DQ0 - DQ15
VOH
VOL
DATA IN

NOTE: D_{out} = Open

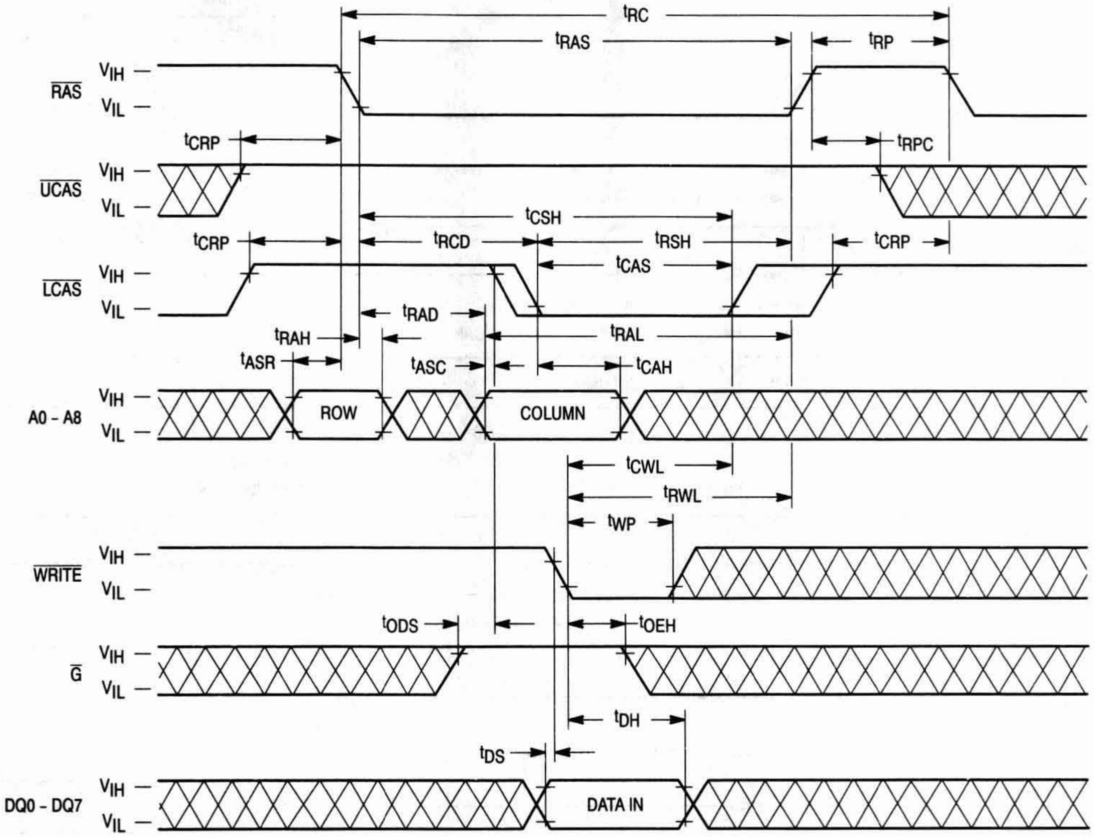
UPPER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{UCAS}$
t_{CRP}
t_{RPC}
$\overline{LCAS}$
t_{RAD}
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 – A8
ROW
COLUMN
t_{CWL}
t_{RWL}
t_{WP}
$\overline{WRITE}$
t_{ODS}
t_{OEH}
$\overline{G}$
t_{DH}
t_{DS}
DQ8 – DQ15
V_{OH}
V_{OL}
DATA IN

NOTE: D_{in} (DQ0 – DQ7) = Don't Care
D_{out} = Open

LOWER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)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tRP
RAS
VIH
VIL
tCRP
tRPC
UCAS
tCSH
tRCD
tRSH
tCAS
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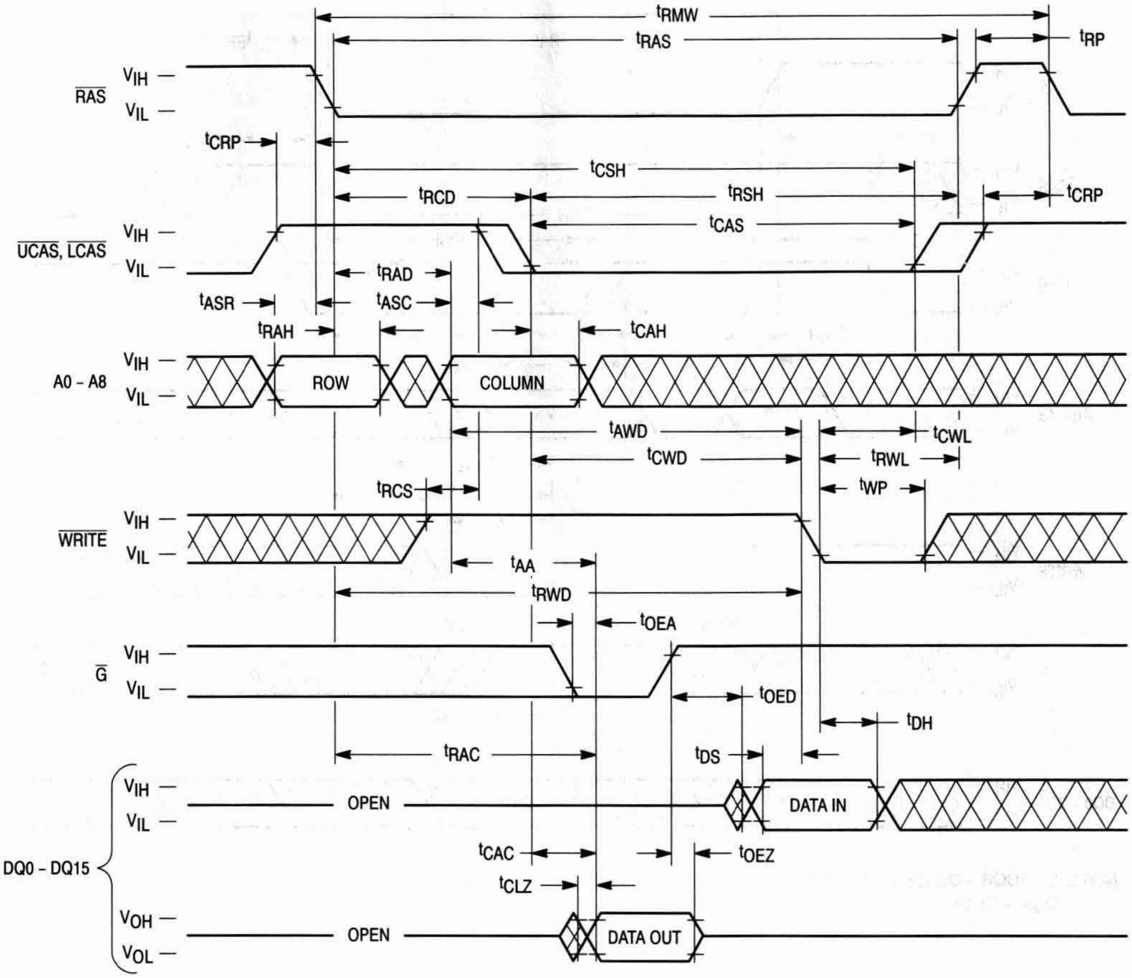
tRAH
tRAL
tASR
tASC
tCAH
A0 - A8
ROW
COLUMN
tCWL
tRWL
tWP
WRITE
tODS
tOEH
G
tDH
tDS
DQ0 - DQ7
DATA IN

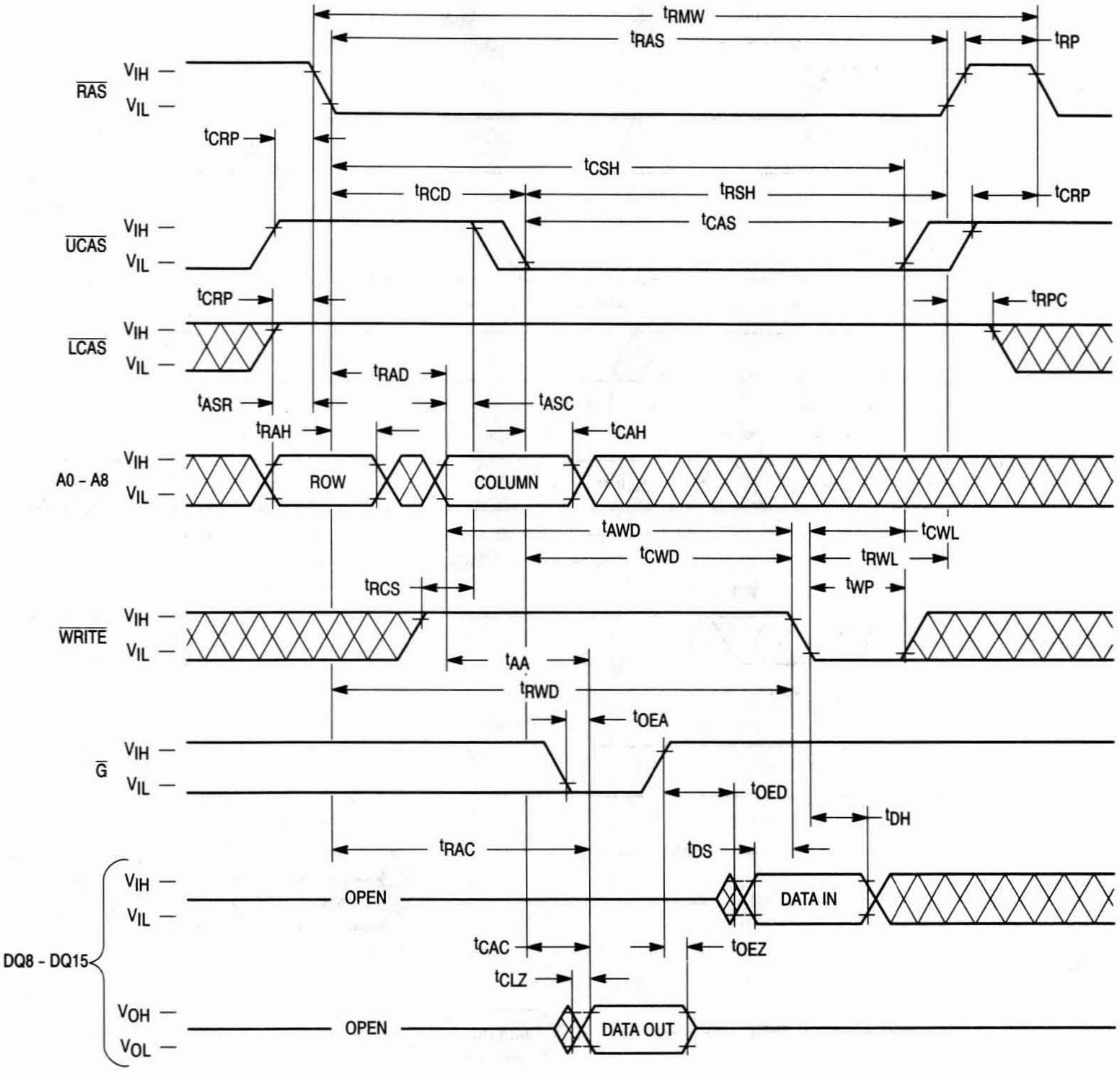
NOTE: D_{in} (DQ8 – DQ15) = Don't Care
D_{out} = Open

READ-MODIFY-WRITE CYCLE



tRMW
tRAS
tRP
RAS
VIH
VIL
tCRP
tCSH
tRCD
tRSH
tCRP
UCAS, LCAS
tCAS
tRAD
tASR
tASC
tRAH
tCAH
A0 - A8
ROW
COLUMN
tAWD
tCWL
tCWD
tRWL
tWP
tRCS
WRITE
tAA
tRWD
tOEA
G
tOED
tDH
tRAC
tDS
DQ0 - DQ15
OPEN
DATA IN
tCAC
tOEZ
tCLZ
VOH
VOL
DATA OUT

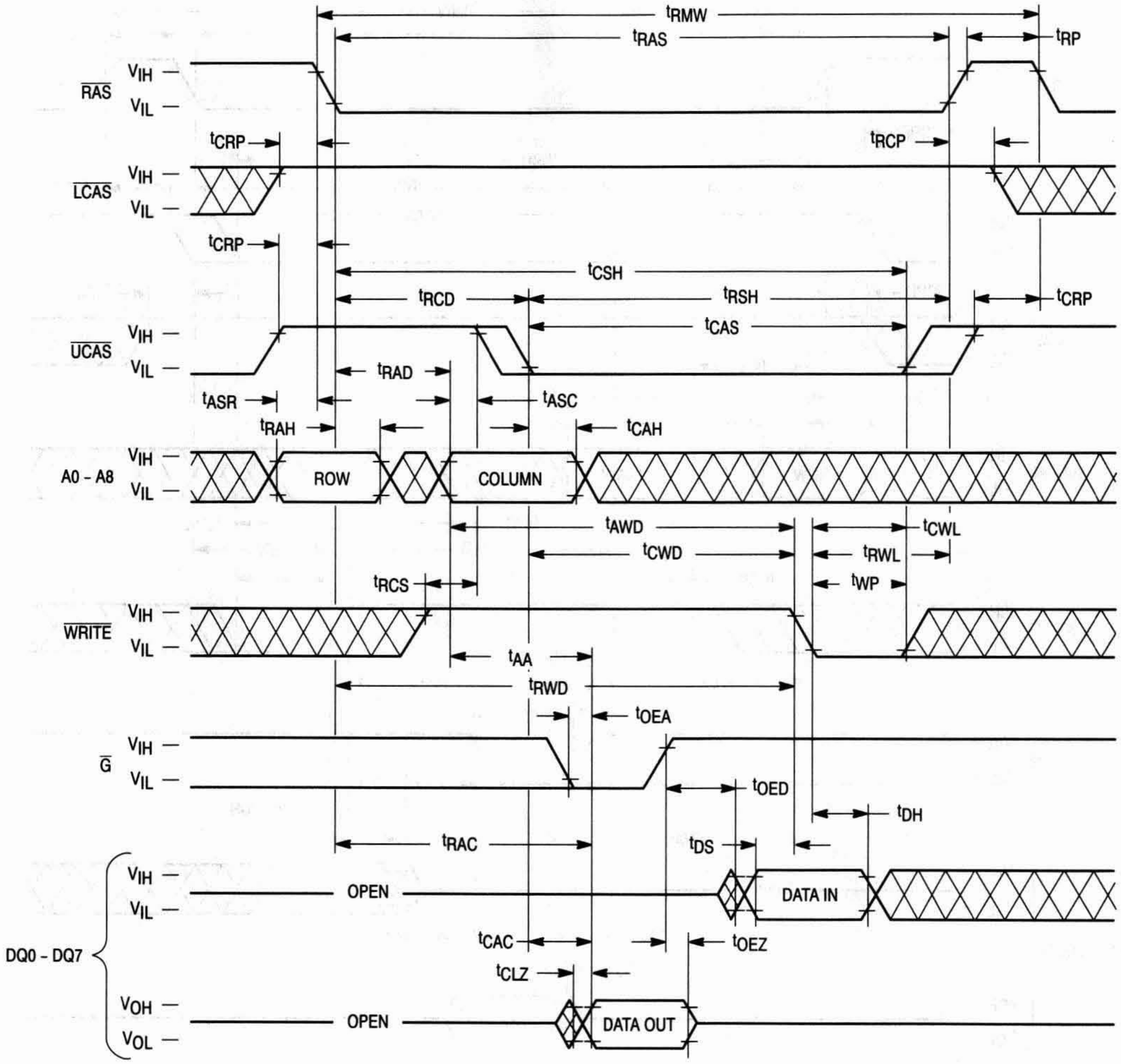
UPPER BYTE READ-MODIFY-WRITE CYCLE



t_{RMW}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{CSH}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{UCAS}$
t_{CRP}
t_{RPC}
$\overline{LCAS}$
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
A0 – A8
ROW
COLUMN
t_{AWD}
t_{CWL}
t_{CWD}
t_{RWL}
t_{RCS}
t_{WP}
$\overline{WRITE}$
t_{AA}
t_{RWD}
t_{OEA}
$\overline{G}$
t_{OED}
t_{DH}
t_{RAC}
t_{DS}
OPEN
DATA IN
DQ8 - DQ15
t_{CAC}
t_{OEZ}
t_{CLZ}
V_{OH}
V_{OL}
OPEN
DATA OUT

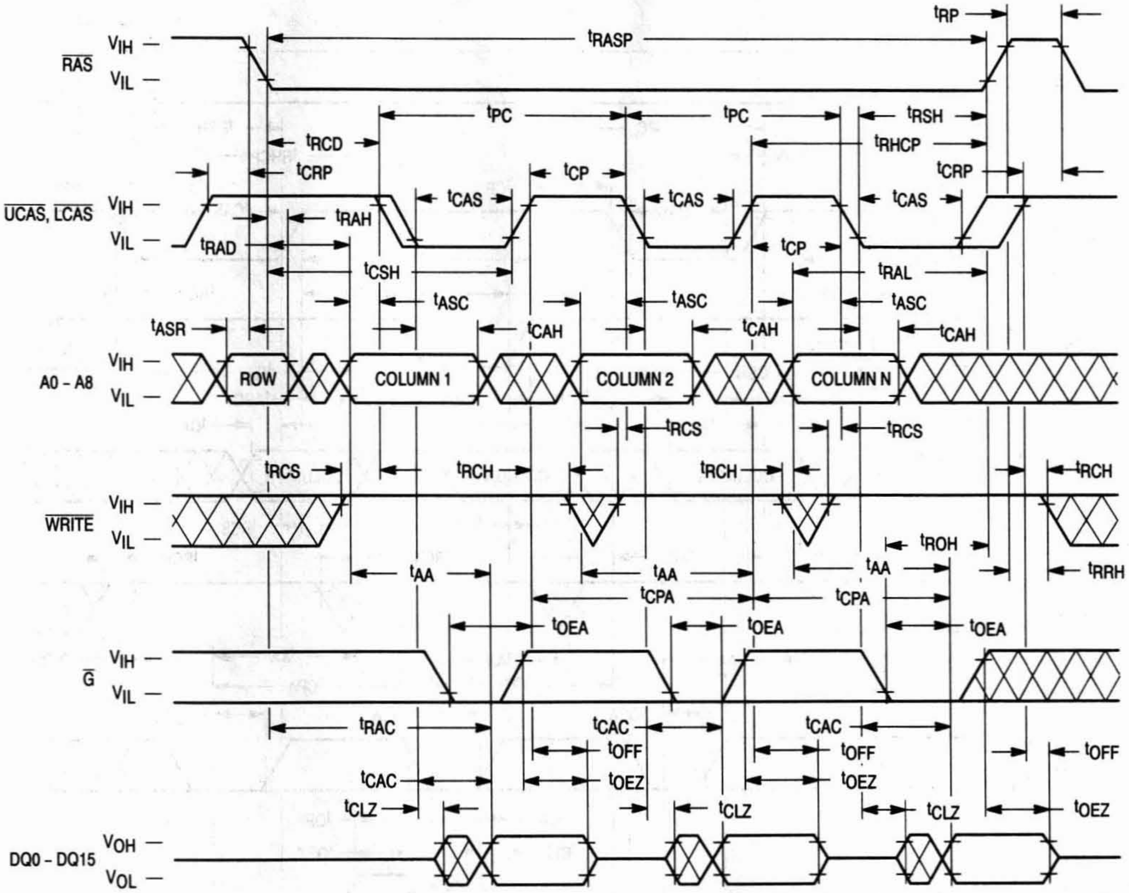
NOTE: D_{in} (DQ0 – DQ7) = Don't Care
D_{out} (DQ0 – DQ7) = Open

LOWER BYTE READ-MODIFY-WRITE CYCLE


t_{RMW}
t_{RAS}
t_{RP}
RAS
V_{IH}
V_{IL}
t_{CRP}
t_{RCP}
LCAS
t_{CSH}
t_{RCD}
t_{RSH}
t_{CAS}
UCAS
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
A0 - A8
ROW
COLUMN
t_{AWD}
t_{CWL}
t_{CWD}
t_{RWL}
t_{RCS}
t_{WP}
WRITE
t_{AA}
t_{RWD}
t_{OEA}
G
t_{OED}
t_{DH}
t_{RAC}
t_{DS}
OPEN
DATA IN
DQ0 - DQ7
t_{CAC}
t_{OEZ}
t_{CLZ}
V_{OH}
V_{OL}
DATA OUT

NOTE: D_{in} (DQ8 – DQ15) = Don't Care
D_{out} (DQ8 – DQ15) = Open

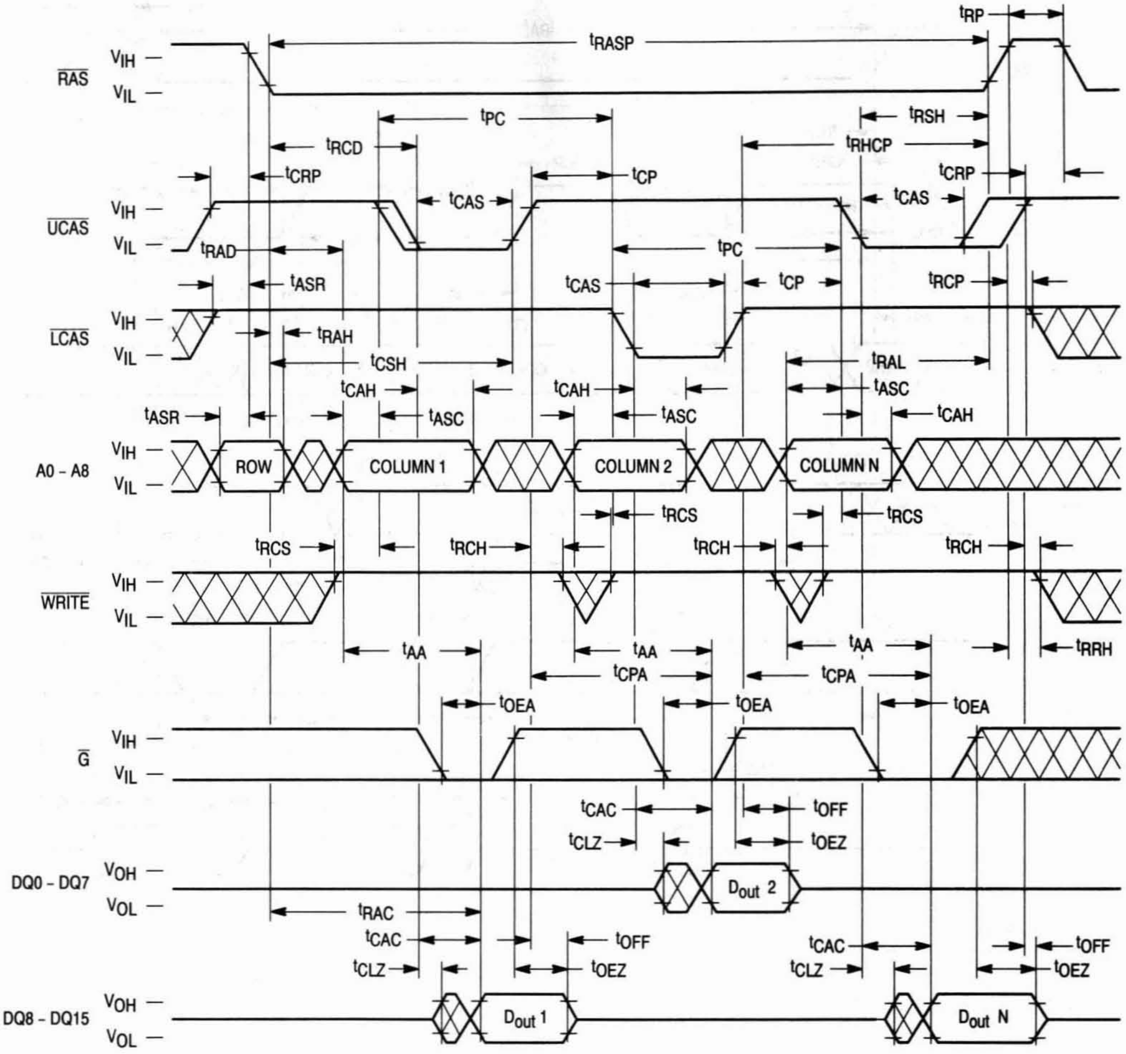
FAST PAGE MODE READ CYCLE



$\overline{RAS}$
V_{IH}
V_{IL}
t_{RP}
t_{RASP}
t_{PC}
t_{PC}
t_{RSH}
t_{RCD}
t_{RHCP}
t_{CRP}
t_{CP}
t_{CRP}
$\overline{UCAS}$, $\overline{LCAS}$
V_{IH}
V_{IL}
t_{CAS}
t_{CAS}
t_{CAS}
t_{RAH}
t_{RAD}
t_{CP}
t_{CSH}
t_{RAL}
t_{ASC}
t_{ASC}
t_{ASC}
t_{ASR}
t_{CAH}
t_{CAH}
t_{CAH}
A0 - A8
V_{IH}
V_{IL}
ROW
COLUMN 1
COLUMN 2
COLUMN N
t_{RCS}
t_{RCS}
t_{RCS}
t_{RCH}
t_{RCH}
t_{RCH}
$\overline{WRITE}$
V_{IH}
V_{IL}
t_{ROH}
t_{AA}
t_{AA}
t_{AA}
t_{RRH}
t_{CPA}
t_{CPA}
t_{OEA}
t_{OEA}
t_{OEA}
$\overline{G}$
V_{IH}
V_{IL}
t_{RAC}
t_{CAC}
t_{CAC}
t_{OFF}
t_{OFF}
t_{OFF}
t_{CAC}
t_{OEZ}
t_{OEZ}
t_{CLZ}
t_{CLZ}
t_{CLZ}
t_{OEZ}
DQ0 - DQ15
V_{OH}
V_{OL}

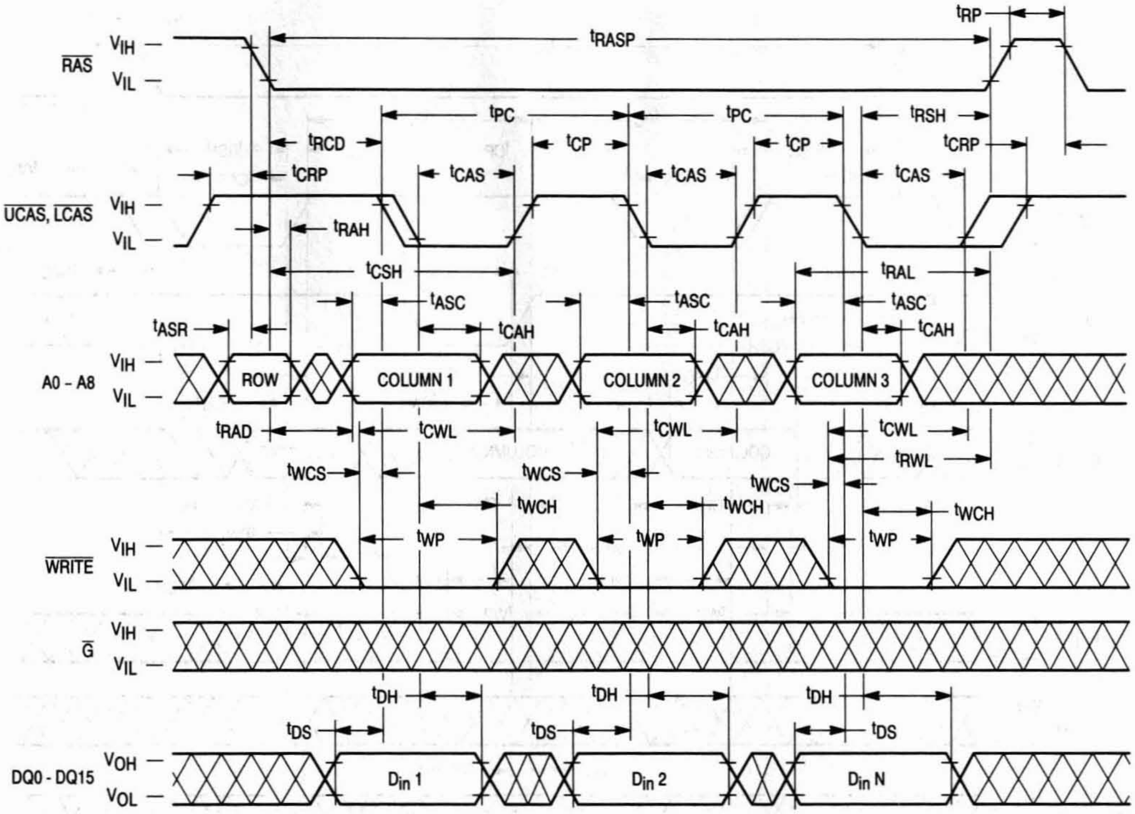
NOTE: D_{in} = Open

FAST PAGE MODE BYTE READ CYCLE


RAS
UCAS
LCAS
A0 - A8
WRITE
G
DQ0 - DQ7
DQ8 - DQ15
VIH
VIL
VOH
VOL
tRASP
tRP
tPC
tRSH
tRCD
tRHCP
tCRP
tCP
tCAS
tRAD
tASR
tRCP
tRAH
tCSH
tRAL
tCAH
tASC
ROW
COLUMN 1
COLUMN 2
COLUMN N
tRCS
tRCH
tAA
tRRH
tCPA
tOEA
tCAC
tOFF
tCLZ
tOEZ
Dout 2
tRAC
Dout 1
Dout N

NOTE: D_{in} Open

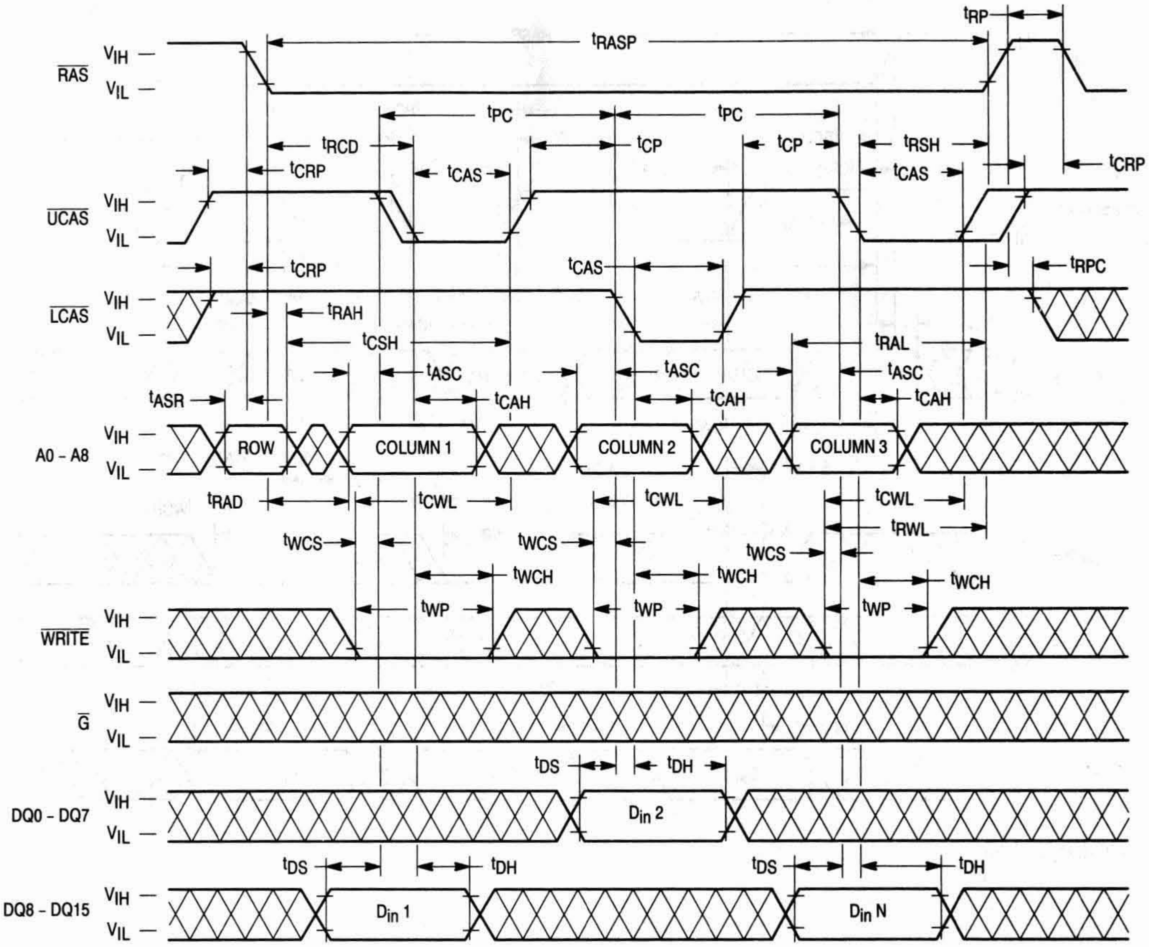
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



tRP
tRASP
RAS
VIH
VIL
tPC
tPC
tRSH
tRCD
tCP
tCP
tCRP
tCRP
tCAS
tCAS
tCAS
UCAS, LCAS
tRAH
tCSH
tRAL
tASC
tASC
tASC
tASR
tCAH
tCAH
tCAH
A0 - A8
ROW
COLUMN 1
COLUMN 2
COLUMN 3
tRAD
tCWL
tCWL
tCWL
tRWL
tWCS
tWCS
tWCS
tWCH
tWCH
tWCH
tWP
tWP
tWP
WRITE
G
tDH
tDH
tDH
tDS
tDS
tDS
DQ0 - DQ15
VOH
VOL
Din 1
Din 2
Din N

NOTE: D_{out} = Open

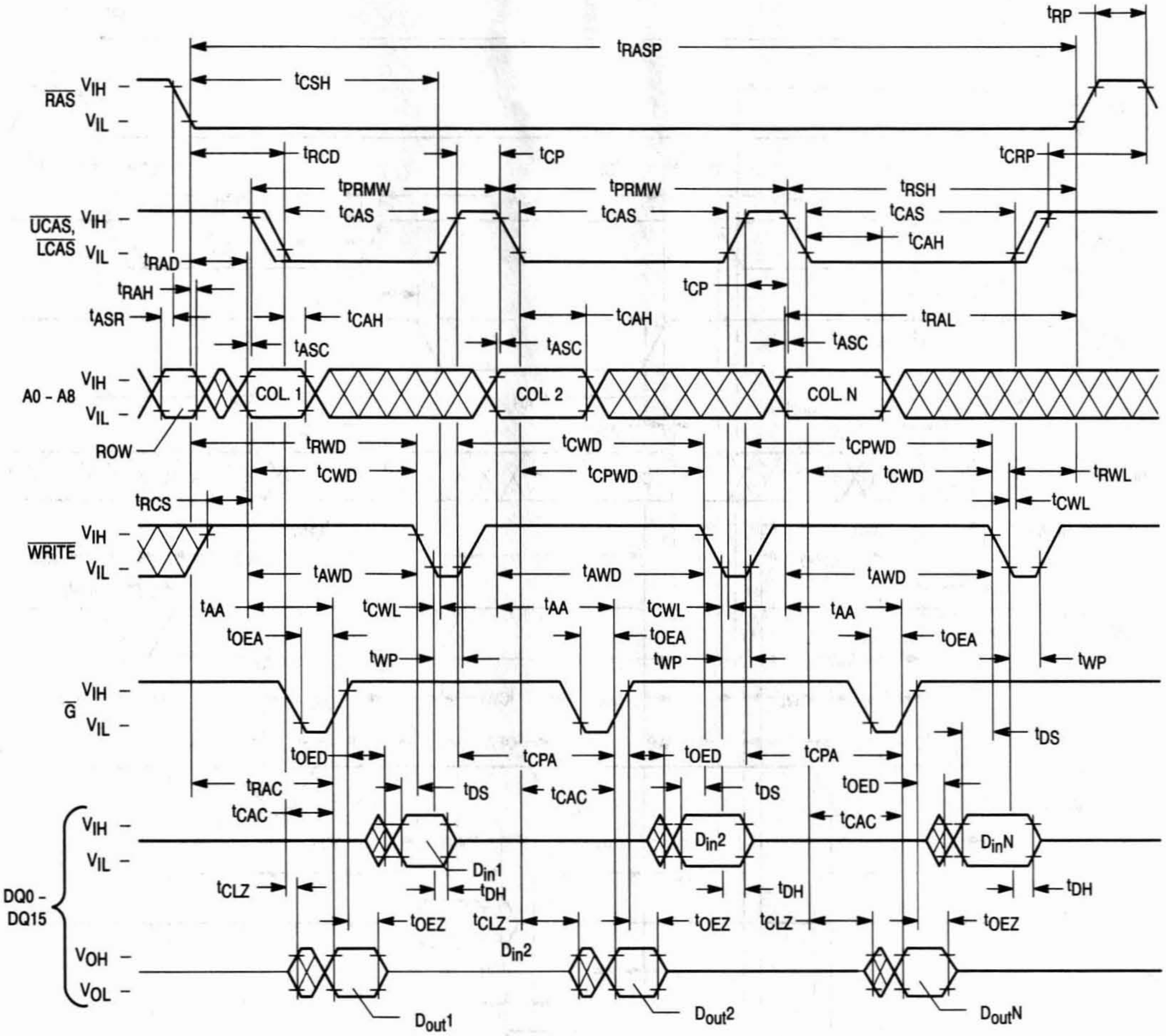
FAST PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



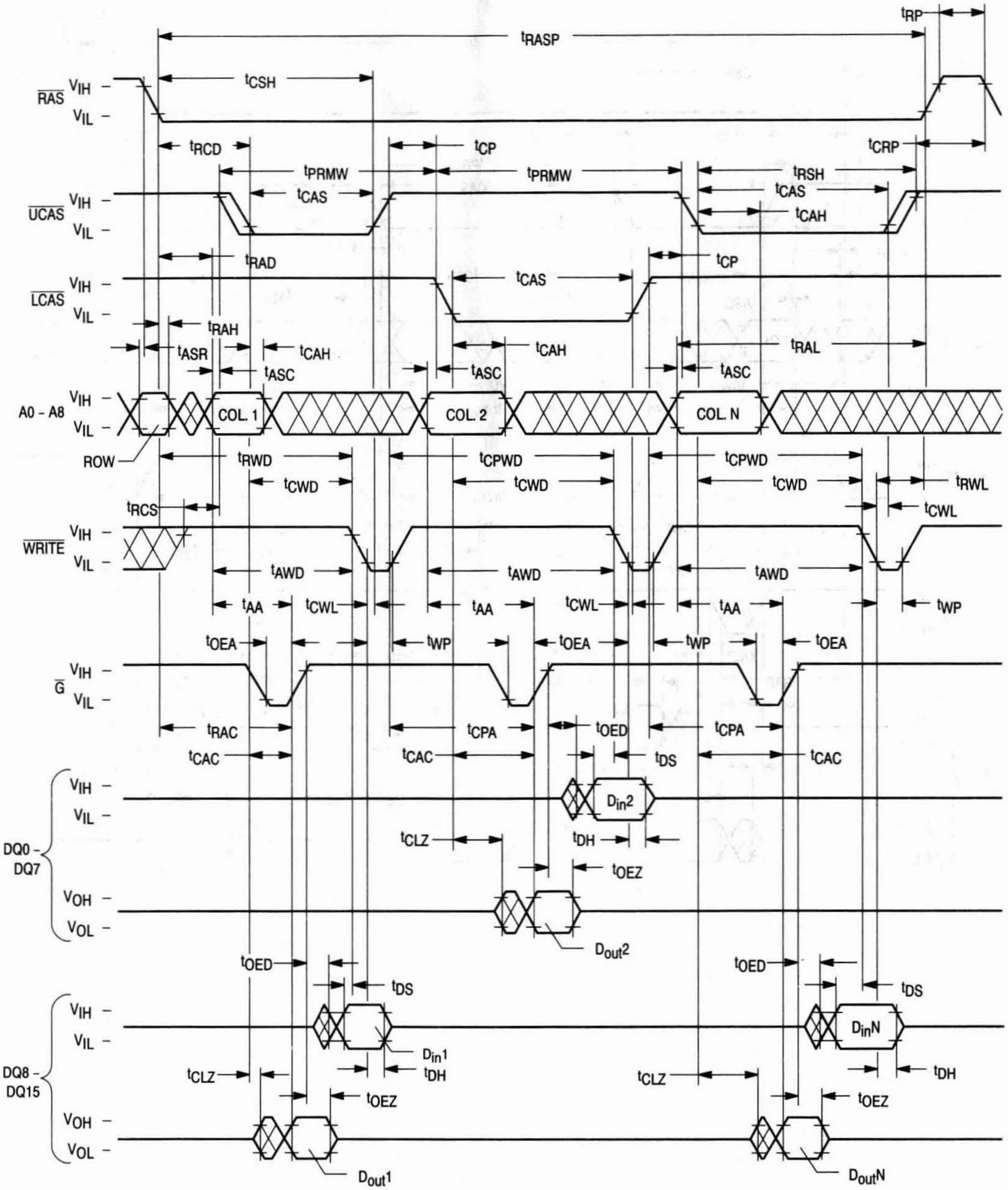
t_{RP}
t_{RASP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{PC}
t_{PC}
t_{RCD}
t_{CP}
t_{CP}
t_{RSH}
t_{CRP}
t_{CAS}
t_{CAS}
t_{CRP}
$\overline{UCAS}$
t_{CRP}
t_{CAS}
t_{RPC}
$\overline{LCAS}$
t_{RAH}
t_{CSH}
t_{RAL}
t_{ASC}
t_{ASC}
t_{ASC}
t_{ASR}
t_{CAH}
t_{CAH}
t_{CAH}
A0 - A8
ROW
COLUMN 1
COLUMN 2
COLUMN 3
t_{RAD}
t_{CWL}
t_{CWL}
t_{CWL}
t_{RWL}
t_{WCS}
t_{WCS}
t_{WCS}
t_{WCH}
t_{WCH}
t_{WCH}
t_{WP}
t_{WP}
t_{WP}
$\overline{WRITE}$
$\overline{G}$
t_{DS}
t_{DH}
DQ0 - DQ7
D_{in} 2
t_{DS}
t_{DH}
t_{DS}
t_{DH}
DQ8 - DQ15
D_{in} 1
D_{in} N

NOTE: D_{out} = Open

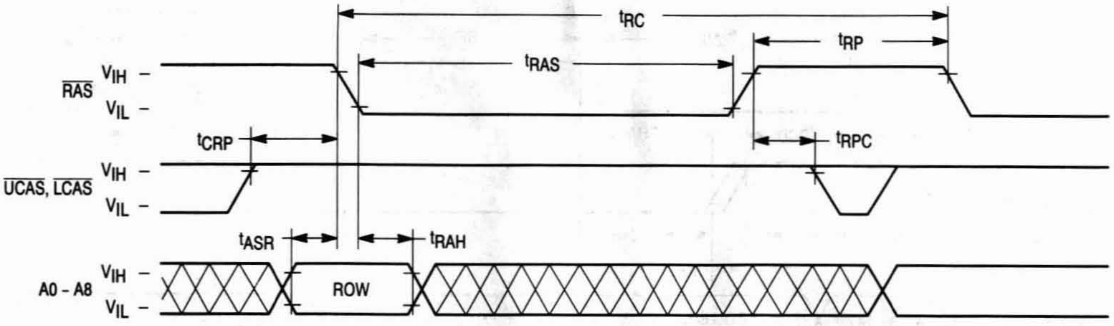
FAST PAGE MODE READ-MODIFY-WRITE CYCLE


tRP
tRASP
tCSH
RAS VIH –
VIL –
tRCD
tCP
tCRP
tPRMW
tPRMW
tRSH
tCAS
tCAS
tCAS
tCAH
UCAS, LCAS VIH –
VIL –
tRAD
tRAH
tCP
tASR
tCAH
tCAH
tRAL
tASC
tASC
tASC
A0 – A8 VIH –
VIL –
COL. 1
COL. 2
COL. N
ROW
tRWD
tCWD
tCPWD
tCWD
tCPWD
tCWD
tRWL
tCWL
tRCS
WRITE VIH –
VIL –
tAWD
tAWD
tAWD
tAA
tCWL
tAA
tCWL
tAA
tOEA
tOEA
tOEA
tWP
tWP
tWP
G VIH –
VIL –
tDS
tOED
tCPA
tOED
tCPA
tRAC
tDS
tCAC
tDS
tOED
tCAC
tCAC
DQ0 – DQ15
VIH –
VIL –
Din1
Din2
DinN
tCLZ
tDH
tDH
tDH
tOEZ
tCLZ
tOEZ
tCLZ
tOEZ
Din2
VOH –
VOL –
Dout1
Dout2
DoutN

FAST PAGE MODE BYTE READ-MODIFY-WRITE CYCLE

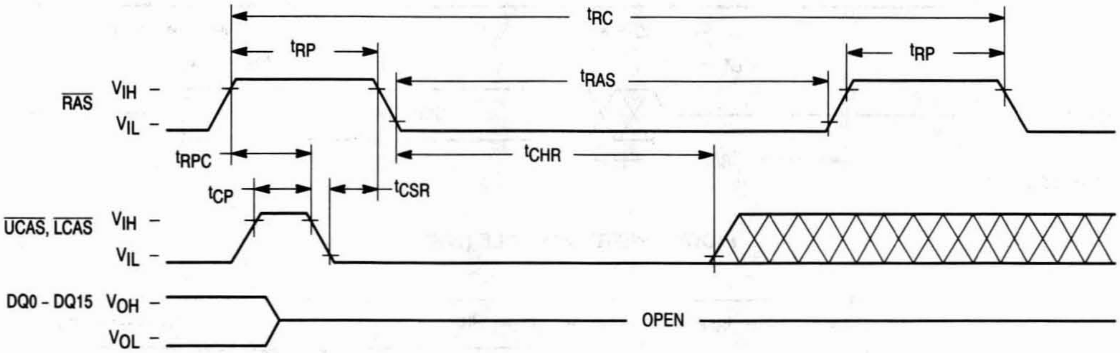

tRASP
tRP
tCSH
RAS
VIH
VIL
tRCD
tCP
tCRP
tPRMW
tPRMW
tRSH
tCAS
tCAS
tCAH
UCAS
tRAD
tCP
LCAS
tCAS
tRAH
tASR
tCAH
tASC
tCAH
tASC
tRAL
tASC
A0 - A8
COL. 1
COL. 2
COL. N
ROW
tRWD
tCPWD
tCPWD
tCWD
tCWD
tCWD
tRWL
tRCS
tCWL
WRITE
tAWD
tAWD
tAWD
tAA
tCWL
tAA
tCWL
tAA
tWP
tOEA
tWP
tOEA
tWP
tOEA
G
tRAC
tCPA
tOED
tCPA
tCAC
tCAC
tDS
tCAC
Din2
tCLZ
tDH
tOEZ
DQ0 - DQ7
VOH
VOL
Dout2
tOED
tDS
tOED
tDS
Din1
DinN
tCLZ
tDH
tCLZ
tDH
DQ8 - DQ15
tOEZ
tOEZ
Dout1
DoutN

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE


t_{RC}
t_{RP}
t_{RAS}
$\overline{\text{RAS}}$
V_{IH} –
V_{IL} –
t_{CRP}
t_{RPC}
$\overline{\text{UCAS}}, \overline{\text{LCAS}}$
t_{ASR}
t_{RAH}
A0 – A8
ROW

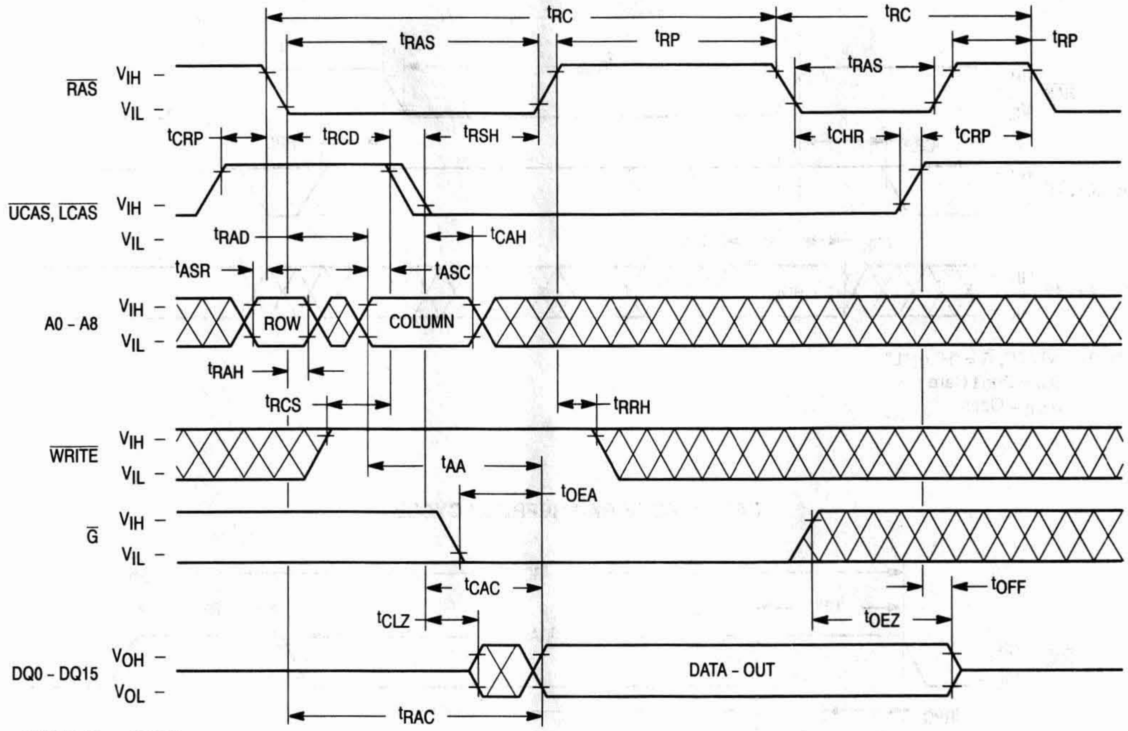
NOTE: $\overline{\text{WRITE}}$, $\overline{\text{G}}$ = "H" or "L"
D_{in} = Don't Care
D_{out} = Open

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE


t_{RC}
t_{RP}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH} –
V_{IL} –
t_{RPC}
t_{CHR}
t_{CP}
t_{CSR}
$\overline{\text{UCAS}}, \overline{\text{LCAS}}$
DQ0 – DQ15
V_{OH} –
V_{OL} –
OPEN

NOTE: $\overline{\text{WRITE}}$, $\overline{\text{G}}$, A0 – A8= "H" or "L"
D_{in} = Don't Care
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is performed when either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ meets this timing.

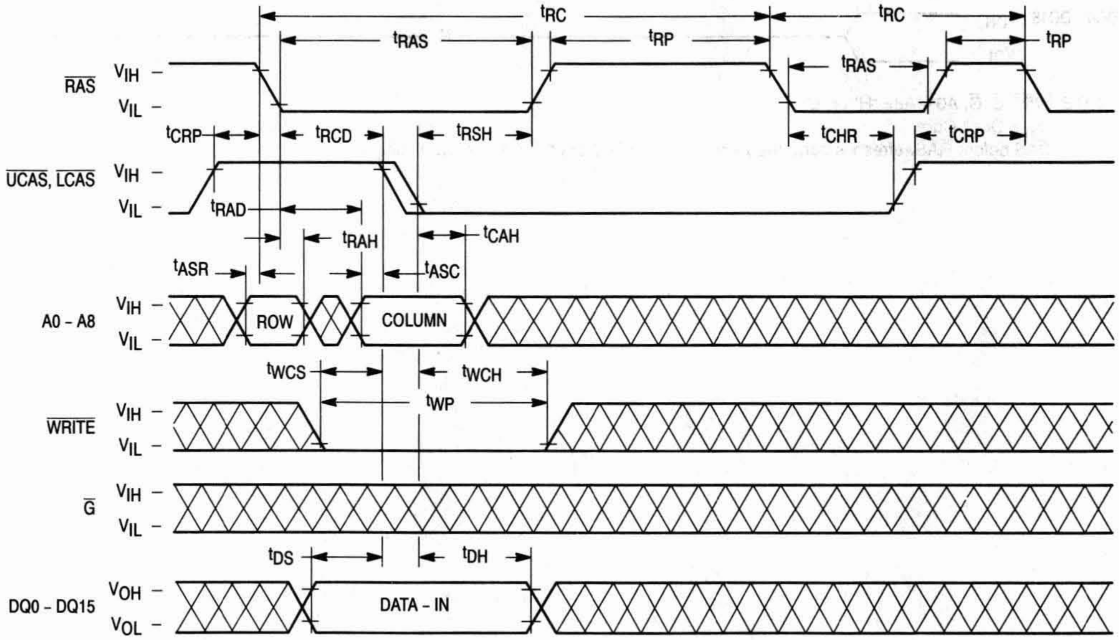
HIDDEN REFRESH CYCLE (READ)



RAS
UCAS, LCAS
A0 – A8
WRITE
G
DQ0 – DQ15
V_{IH}
V_{IL}
V_{OH}
V_{OL}
t_{RC}
t_{RAS}
t_{RP}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{RAD}
t_{CAH}
t_{ASR}
t_{ASC}
ROW
COLUMN
t_{RAH}
t_{RCS}
t_{RRH}
t_{AA}
t_{OEA}
t_{CAC}
t_{OFF}
t_{CLZ}
t_{OEZ}
DATA - OUT
t_{RAC}

NOTE: D_{in} = Open

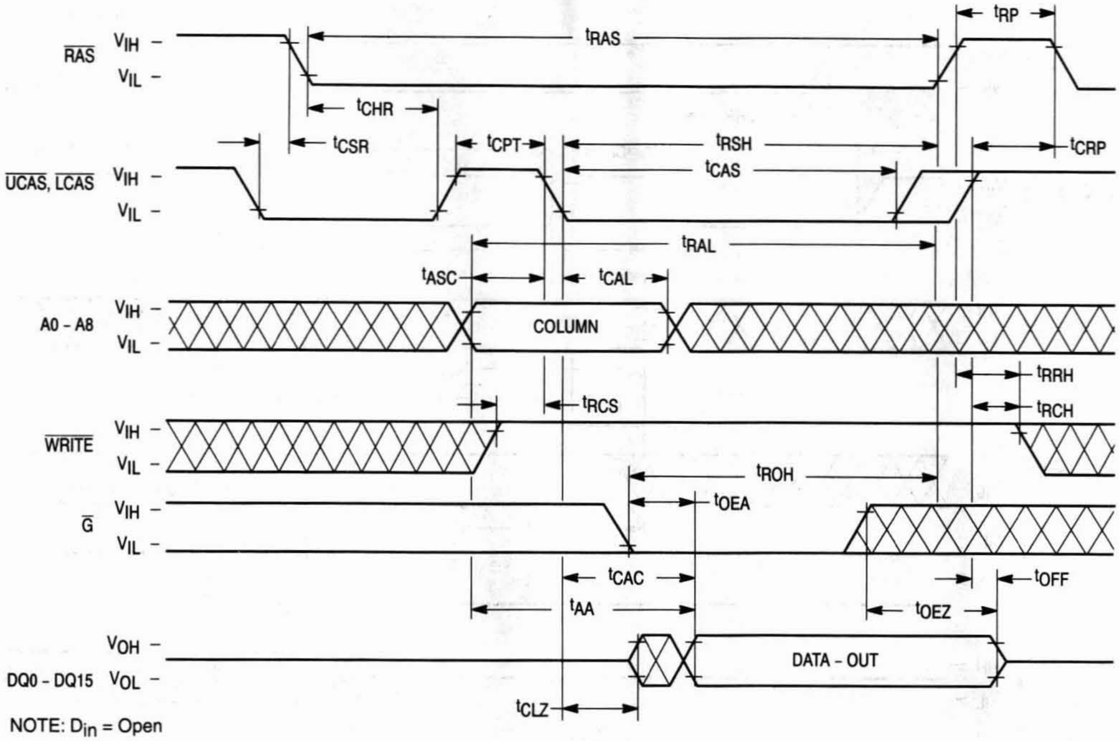
HIDDEN REFRESH CYCLE (WRITE)



RAS
UCAS, LCAS
A0 – A8
WRITE
G
DQ0 – DQ15
V_{IH}
V_{IL}
V_{OH}
V_{OL}
t_{RC}
t_{RAS}
t_{RP}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{RAD}
t_{RAH}
t_{CAH}
t_{ASR}
t_{ASC}
ROW
COLUMN
t_{WCS}
t_{WCH}
t_{WP}
t_{DS}
t_{DH}
DATA - IN

NOTE: D_{out} = Open

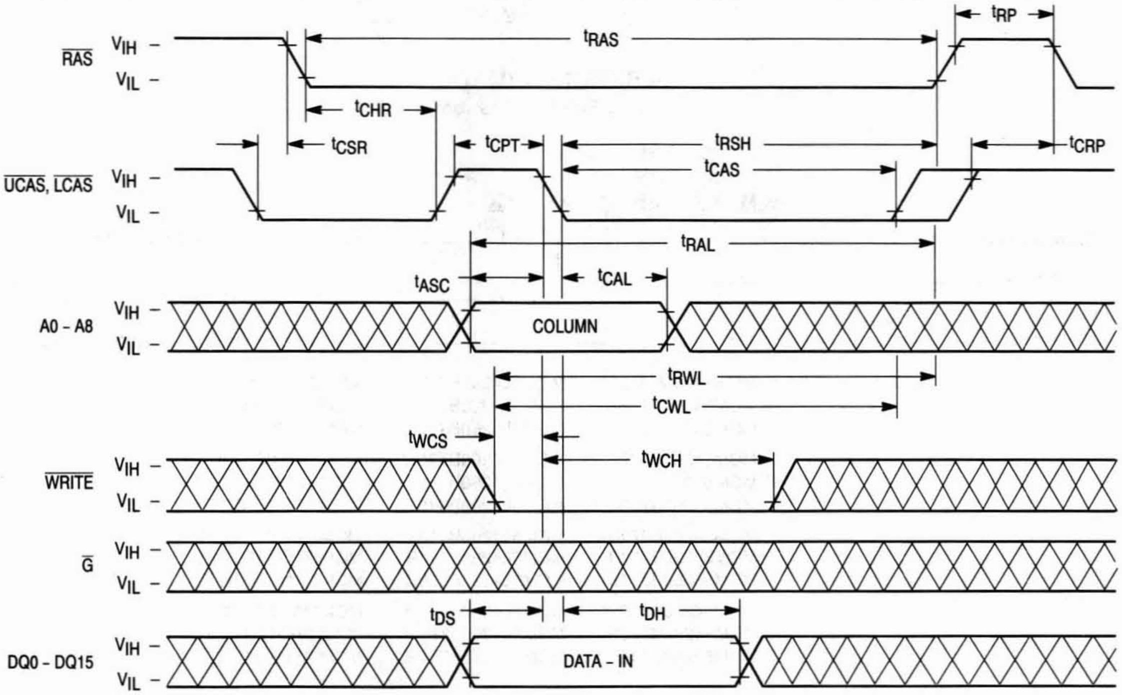
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST READ CYCLE



$\overline{\text{RAS}}$
V_{IH} –
V_{IL} –
t_{RAS}
t_{RP}
t_{CHR}
t_{CSR}
t_{CPT}
t_{RSH}
t_{CAS}
t_{CRP}
$\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$
V_{IH} –
V_{IL} –
t_{RAL}
t_{ASC}
t_{CAL}
A0 – A8
V_{IH} –
V_{IL} –
COLUMN
t_{RRH}
t_{RCS}
t_{RCH}
$\overline{\text{WRITE}}$
V_{IH} –
V_{IL} –
t_{ROH}
t_{OEA}
$\overline{\text{G}}$
V_{IH} –
V_{IL} –
t_{CAC}
t_{OFF}
t_{AA}
t_{OEZ}
V_{OH} –
DQ0 – DQ15
V_{OL} –
DATA – OUT
t_{CLZ}

NOTE: D_{in} = Open

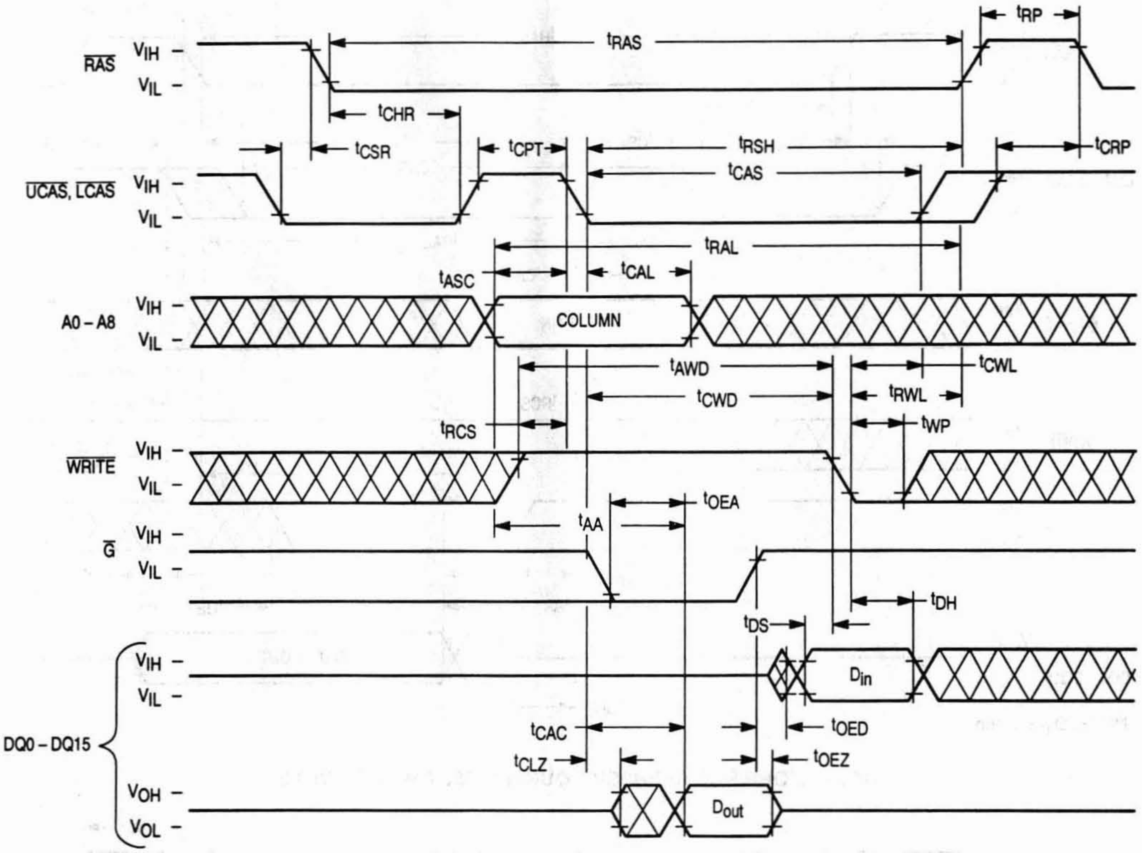
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST WRITE CYCLE



$\overline{\text{RAS}}$
V_{IH} –
V_{IL} –
t_{RAS}
t_{RP}
t_{CHR}
t_{CSR}
t_{CPT}
t_{RSH}
t_{CAS}
t_{CRP}
$\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$
V_{IH} –
V_{IL} –
t_{RAL}
t_{ASC}
t_{CAL}
A0 – A8
V_{IH} –
V_{IL} –
COLUMN
t_{RWL}
t_{CWL}
t_{WCS}
t_{WCH}
$\overline{\text{WRITE}}$
V_{IH} –
V_{IL} –
$\overline{\text{G}}$
V_{IH} –
V_{IL} –
t_{DS}
t_{DH}
DQ0 – DQ15
V_{IH} –
V_{IL} –
DATA – IN

NOTE: D_{out} = Open

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE



$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RAS}
t_{RP}
t_{CHR}
t_{CSR}
t_{CPT}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$
t_{RAL}
t_{ASC}
t_{CAL}
A0 – A8
COLUMN
t_{AWD}
t_{CWL}
t_{CWD}
t_{RWL}
t_{RCS}
t_{WP}
$\overline{\text{WRITE}}$
t_{OEA}
t_{AA}
$\overline{\text{G}}$
t_{DH}
t_{DS}
DQ0 – DQ15
D_{in}
t_{CAC}
t_{OED}
t_{CLZ}
t_{OEZ}
V_{OH}
V_{OL}
D_{out}

ORDERING INFORMATION
(Order by Full Part Number)

54260B
5L4260B
MCM 5V4260B X XX XX

Motorola Memory Prefix — MCM
Part Number — 54260B / 5L4260B / 5V4260B
Package (J = 400 mil SOJ, T = 400 mil TSOP) — X
Speed (70 = 70 ns, 80 = 80 ns, 10 = 100 ns) — XX
Shipping Method (Blank = Rails or Tray, R = Tape and Reel) — XX

Full Part Numbers —	MCM54260BJ70	MCM5L4260BJ70	MCM5V4260BJ70
	MCM54260BJ80	MCM5L4260BJ80	MCM5V4260BJ80
	MCM54260BJ10	MCM5L4260BJ10	MCM5V4260BJ10
	MCM54260BT70	MCM5L4260BT70	MCM5V4260BT70
	MCM54260BT80	MCM5L4260BT80	MCM5V4260BT80
	MCM54260BT10	MCM5L4260BT10	MCM5V4260BT10
	MCM54260BJ70R	MCM5L4260BJ70R	MCM5V4260BJ70R
	MCM54260BJ80R	MCM5L4260BJ80R	MCM5V4260BJ80R
	MCM54260BJ10R	MCM5L4260BJ10R	MCM5V4260BJ10R
	MCM54260BT70R	MCM5L4260BT70R	MCM5V4260BT70R
	MCM54260BT80R	MCM5L4260BT80R	MCM5V4260BT80R
	MCM54260BT10R	MCM5L4260BT10R	MCM5V4260BT10R

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM54280B
MCM5L4280B
MCM5V4280B

Product Preview

256K x 18 CMOS Dynamic RAM
Fast Page Mode – 2 CAS, 1 Write Enable

The MCM54280B is a 0.6µ CMOS high-speed dynamic random access memory. It is organized as 262,144 eighteen-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM54280B requires only 9 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 400 mil SOJ plastic package and a 400 mil thin-small-outline package (TSOP).

- Three-State Data Output
- Fast Page Mode
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- Self Refresh (MCM5V4280B only)
- 512 Cycle Refresh:
  MCM54280B = 8 ms
  MCM5L4280B and MCM5V4280B = 64 ms
- Fast Access Time (t_{RAC}):
  MCM54280B-70, MCM5L4280B-70, and MCM5V4280B-70 = 70 ns (Max)
  MCM54280B-80, MCM5L4280B-80, and MCM5V4280B-80 = 80 ns (Max)
  MCM54280B-10, MCM5L4280B-10, and MCM5V4280B-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM54280B-70, MCM5L4280B-70, and MCM5V4280B-70 = 550 mW (Max)
  MCM54280B-80, MCM5L4280B-80, and MCM5V4280B-80 = 468 mW (Max)
  MCM54280B-10, MCM5L4280B-10, and MCM5V4280B-10 = 413 mW (Max)
- Low Standby Power Dissipation:
  MCM54280B, MCM5L4280B, and MCM5V4280B = 5.5 mW (Max, TTL Levels)
- Battery Backup Power Dissipation:
  MCM5L4280B = 1.7 mW (Max, Battery Backup Mode, t_{RC} = 125 µs)
- Self Refresh Power Dissipation:
  MCM5V4280B = 1.1 mW (Max, Self Refresh Mode)

J PACKAGE
400 MIL SOJ
CASE TBD

T PACKAGE
400 MIL TSOP
CASE TBD

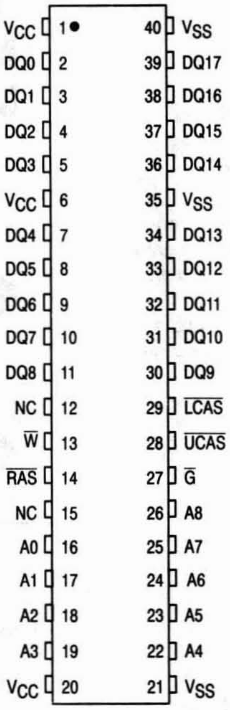
PIN NAMES

A0 – A8	Address Inputs
DQ0 – DQ17	Data Input/Output
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connect
$\overline{\text{G}}$	Output Enable

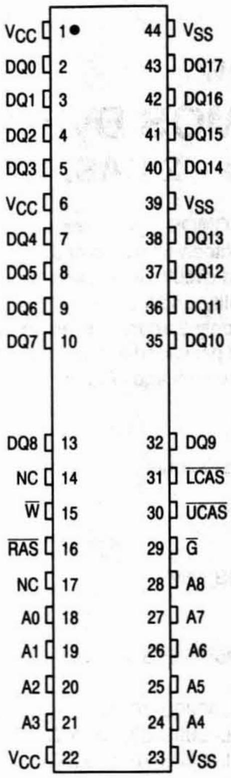
This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

PIN ASSIGNMENTS

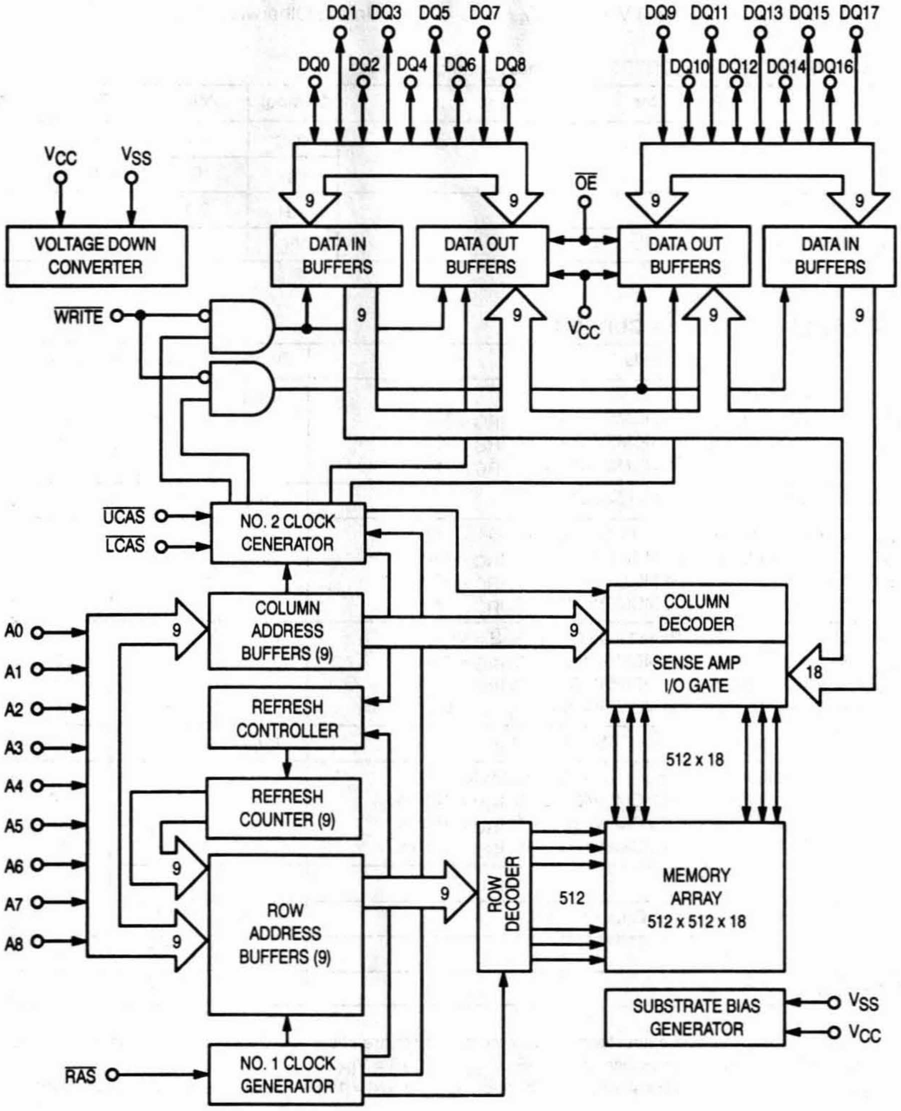
400 MIL SOJ


V_{CC} 1 ● 40 V_{SS}
DQ0 2 39 DQ17
DQ1 3 38 DQ16
DQ2 4 37 DQ15
DQ3 5 36 DQ14
V_{CC} 6 35 V_{SS}
DQ4 7 34 DQ13
DQ5 8 33 DQ12
DQ6 9 32 DQ11
DQ7 10 31 DQ10
DQ8 11 30 DQ9
NC 12 29 $\overline{LCAS}$
$\overline{W}$ 13 28 $\overline{UCAS}$
$\overline{RAS}$ 14 27 $\overline{G}$
NC 15 26 A8
A0 16 25 A7
A1 17 24 A6
A2 18 23 A5
A3 19 22 A4
V_{CC} 20 21 V_{SS}

400 MIL TSOP


V_{CC} 1 ● 44 V_{SS}
DQ0 2 43 DQ17
DQ1 3 42 DQ16
DQ2 4 41 DQ15
DQ3 5 40 DQ14
V_{CC} 6 39 V_{SS}
DQ4 7 38 DQ13
DQ5 8 37 DQ12
DQ6 9 36 DQ11
DQ7 10 35 DQ10
DQ8 13 32 DQ9
NC 14 31 $\overline{LCAS}$
$\overline{W}$ 15 30 $\overline{UCAS}$
$\overline{RAS}$ 16 29 $\overline{G}$
NC 17 28 A8
A0 18 27 A7
A1 19 26 A6
A2 20 25 A5
A3 21 24 A4
V_{CC} 22 23 V_{SS}

BLOCK DIAGRAM



DQ1 DQ3 DQ5 DQ7
DQ0 DQ2 DQ4 DQ6 DQ8
DQ9 DQ11 DQ13 DQ15 DQ17
DQ10 DQ12 DQ14 DQ16
VCC
VSS
VOLTAGE DOWN CONVERTER
DATA IN BUFFERS
DATA OUT BUFFERS
OE
DATA OUT BUFFERS
DATA IN BUFFERS
VCC
9
WRITE
UCAS
LCAS
NO. 2 CLOCK CENERATOR
COLUMN ADDRESS BUFFERS (9)
REFRESH CONTROLLER
REFRESH COUNTER (9)
ROW ADDRESS BUFFERS (9)
NO. 1 CLOCK GENERATOR
RAS
A0
A1
A2
A3
A4
A5
A6
A7
A8
COLUMN DECODER
SENSE AMP I/O GATE
18
512 x 18
ROW DECODER
512
MEMORY ARRAY 512 x 512 x 18
SUBSTRATE BIAS GENERATOR
VSS
VCC

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Data Out Current	I_{out}	50	mA
Soldering Temperature x Time	T_{solder}	260 x 10	°C x s
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	V_{CC} + 0.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 0.5*	—	0.8	V

*– 2.0 V at pulse width ≤ 20 ns

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	1, 2
MCM54280B-70, MCM5L4280B-70, and MCM5V4280B-70, t_{RC} = 130 ns		—	100		
MCM54280B-80, MCM5L4280B-80, and MCM5V4280B-80, t_{RC} = 150 ns		—	95		
MCM54280B-10, MCM5L4280B-10, and MCM5V4280B-10, t_{RC} = 180 ns		—	85		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	1, 2
MCM54280B-70, MCM5L4280B-70, and MCM5V4280B-70, t_{RC} = 130 ns		—	110		
MCM54280B-80, MCM5L4280B-80, and MCM5V4280B-80, t_{RC} = 150 ns		—	95		
MCM54280B-10, MCM5L4280B-10, and MCM5V4280B-10, t_{RC} = 180 ns		—	85		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	1, 2
MCM54280B-70, MCM5L4280B-70, and MCM5V4280B-70, t_{PC} = 45 ns		—	80		
MCM54280B-80, MCM5L4280B-80, and MCM5V4280B-80, t_{PC} = 50 ns		—	70		
MCM54280B-10, MCM5L4280B-10, and MCM5V4280B-10, t_{PC} = 60 ns		—	65		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	1
MCM54280B-70, MCM5L4280B-70, and MCM5V4280B-70, t_{RC} = 130 ns		—	110		
MCM54280B-80, MCM5L4280B-80, and MCM5V4280B-80, t_{RC} = 150 ns		—	95		
MCM54280B-10, MCM5L4280B-10, and MCM5V4280B-10, t_{RC} = 180 ns		—	85		
Input Leakage Current (0 V ≤ V_{in} ≤ 7.0 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ 7.0 V, Output Disable)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading. Maximum currents are at the specified cycle time (min) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery back-up. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, periodically sampled, not 100% tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A8	C_{in}	5	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{G}$		7	
Input/Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0 – DQ15	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

	Symbol		MCM54280B-70 MCM5L4280B-70 MCM5V4280B-70		MCM54280B-80 MCM5L4280B-80 MCM5V4280B-80		MCM54280B-10 MCM5L4280B-10 MCM5V4280B-10			
Parameter	**Std**	**Alt**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	180	—	ns	5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RWC}	185	—	205	—	245	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	50	—	60	—	ns	
Page Mode Read-Modify-Write Cycle Time	t_{CELCEL}	t_{PRWC}	100	—	105	—	125	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	—	100	ns	6,7,8
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	25	ns	6, 7
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	50	ns	6, 8
Access Time from $\overline{\text{CAS}}$ Precharge	t_{CEHQV}	t_{CPA}	—	40	—	45	—	55	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	15	0	20	ns	9
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	70	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	7
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	8
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Hold Time From $\overline{\text{CAS}}$ Precharge (Page Mode Only)	t_{CEHREH}	t_{RHCP}	40	—	45	—	55	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	50	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles or 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0 \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greaer than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
9. t_{OFF} (max) and t_{GZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

	Symbol		MCM54280B-70 MCM5L4280B-70 MCM5V4280B-70		MCM54280B-80 MCM5L4280B-80 MCM5V4280B-80		MCM54280B-10 MCM5L4280B-10 MCM5V4280B-10			
Parameter	**Std**	**Alt**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	10
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{CELWH}	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	11
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	20	—	ns	11
Refresh Period	t_{RVRV}	t_{RFSH}	—	8	— —	8	— —	8	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	12
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	60	—	ns	12
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	100	—	110	—	135	—	ns	12
Column Address to Write Delay	t_{AVWL}	t_{AWD}	65	—	70	—	85	—	ns	12
$\overline{\text{CAS}}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	70	—	75	—	90	—	ns	12
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle	t_{RELCEH}	t_{CHR}	15	—	15	—	20	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test)	t_{CEHCEL}	t_{CPT}	30	—	30	—	40	—	ns	
$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{G}}$	t_{GLREH}	t_{ROH}	10	—	10	—	20	—	ns	
$\overline{\text{G}}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	20	—	25	ns	6
$\overline{\text{G}}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	25	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{\text{G}}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	25	ns	9
$\overline{\text{G}}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	25	—	ns	
Output Disable Setup Time	t_{GLCEL}	t_{GDS}	0	—	0	—	0	—	ns	

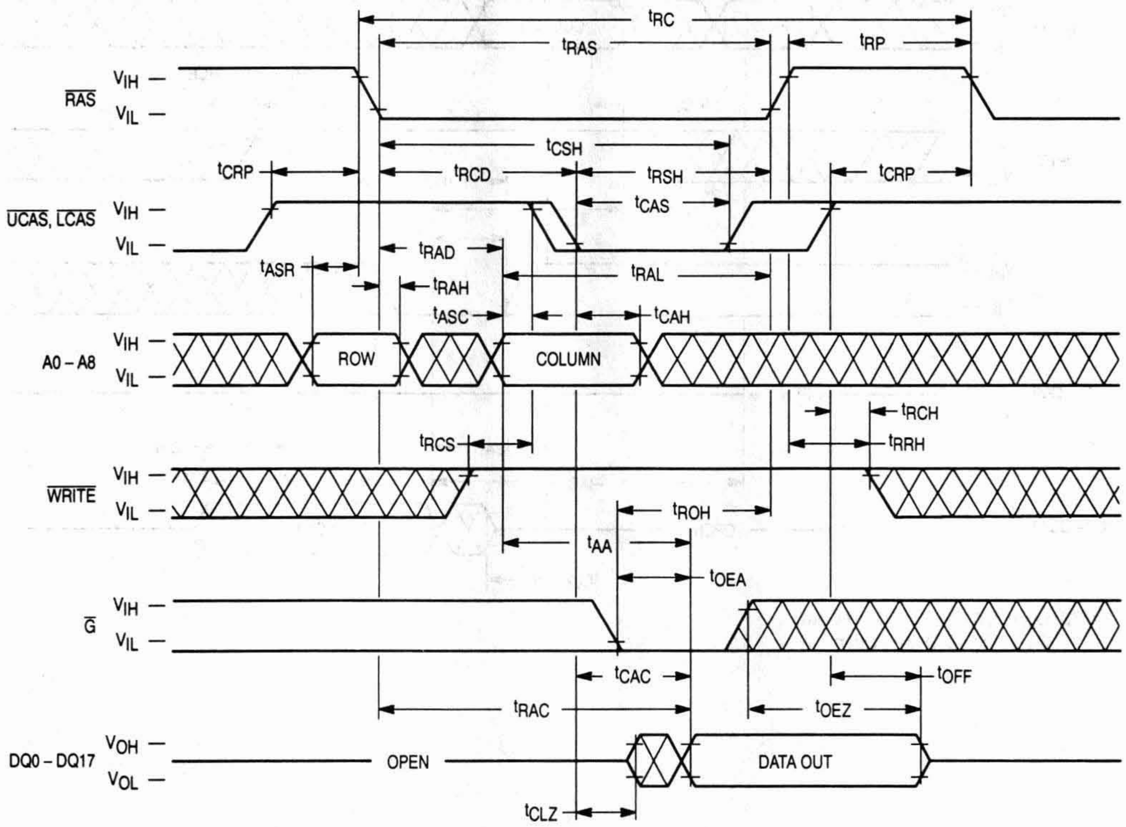
NOTES:

10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in late write or read-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

SELF REFRESH CYCLE

Parameter	Symbol		MCM54280B-70 MCM5L4280B-70 MCM5V4280B-70		MCM54280B-80 MCM5L4280B-80 MCM5V4280B-80		MCM54280B-10 MCM5L4280B-10 MCM5V4280B-10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh, MCM5V4280B Only)	$t_{RELREHS}$	t_{RASS}	100	—	100	—	100	—	µs	
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh, MCM5V4280B Only)	$t_{REHRELS}$	t_{RPS}	130	—	150	—	180	—	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh, MCM5V4280B Only)	t_{REHCEH}	t_{CHS}	–50	—	–60	—	–70	—	ns	

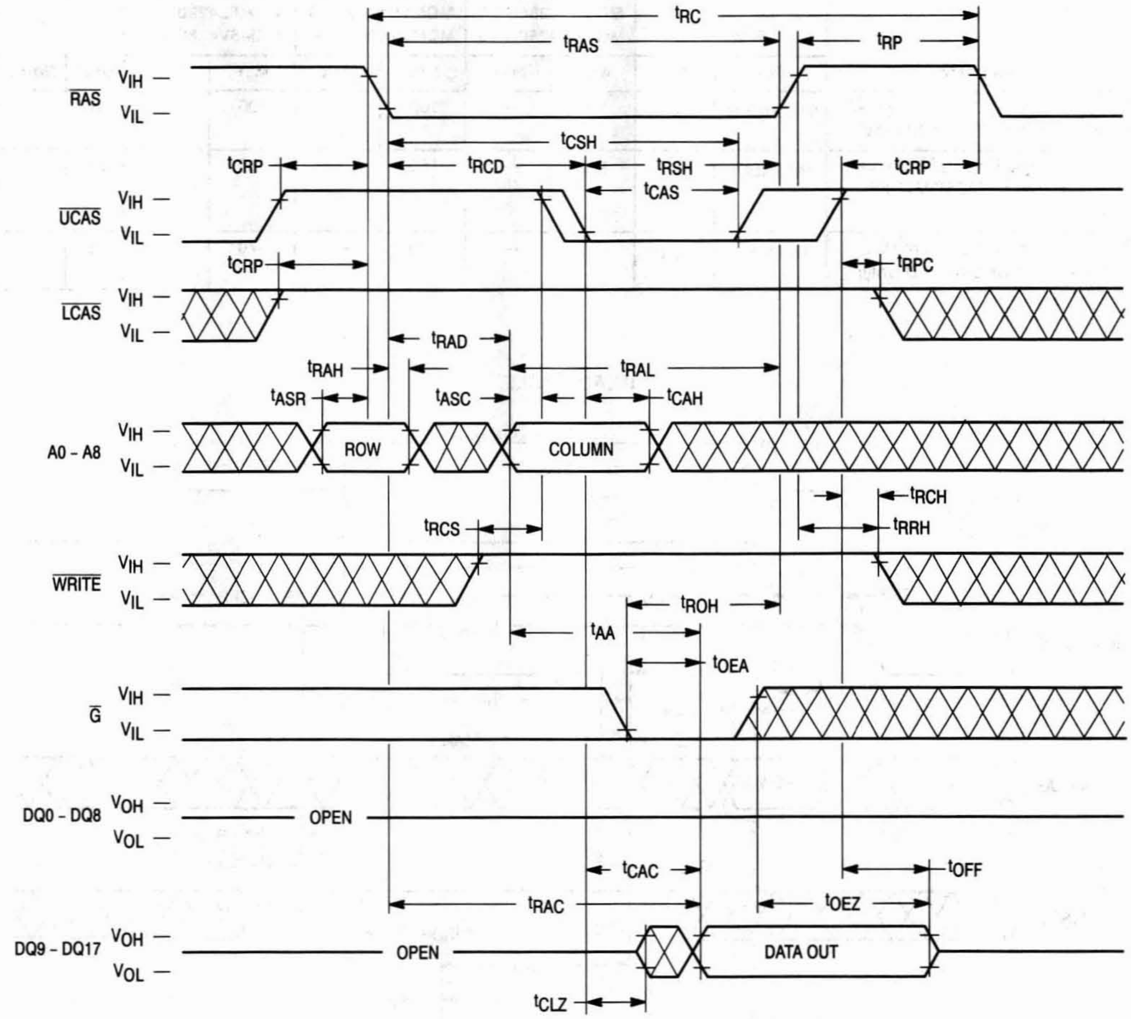
READ CYCLE



tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
UCAS, LCAS
VIH
VIL
tASR
tRAD
tRAL
tRAH
tASC
tCAH
A0 – A8
VIH
VIL
ROW
COLUMN
tRCH
tRRH
tRCS
WRITE
VIH
VIL
tROH
tAA
tOEA
G
VIH
VIL
tCAC
tOFF
tRAC
tOEZ
DQ0 – DQ17
VOH
VOL
OPEN
DATA OUT
tCLZ

NOTE: D_{in} = Open

UPPER BYTE READ CYCLE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t_{RP}
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V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
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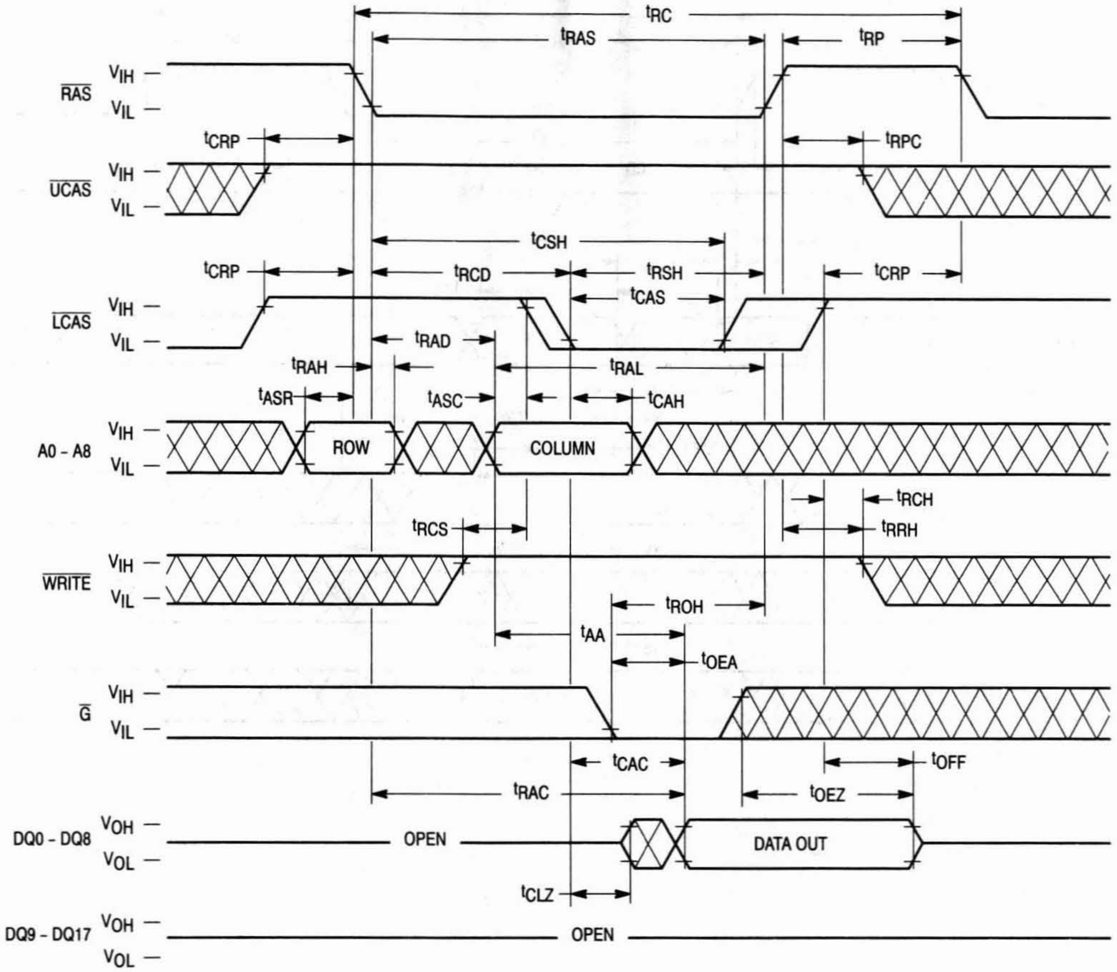
t_{RSH}
t_{CAS}
t_{CRP}
$\overline{UCAS}$
t_{CRP}
t_{RPC}
$\overline{LCAS}$
t_{RAD}
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 – A8
ROW
COLUMN
t_{RCH}
t_{RCS}
t_{RRH}
$\overline{WRITE}$
t_{ROH}
t_{AA}
t_{OEA}
$\overline{G}$
DQ0 – DQ8
V_{OH}
V_{OL}
OPEN
t_{CAC}
t_{OFF}
t_{RAC}
t_{OEZ}
DQ9 – DQ17
OPEN
DATA OUT
t_{CLZ}

NOTE: D_{in} (DQ0 – DQ8) = Don't Care
D_{in} (DQ9 – DQ17) = Open

LOWER BYTE READ CYCLE



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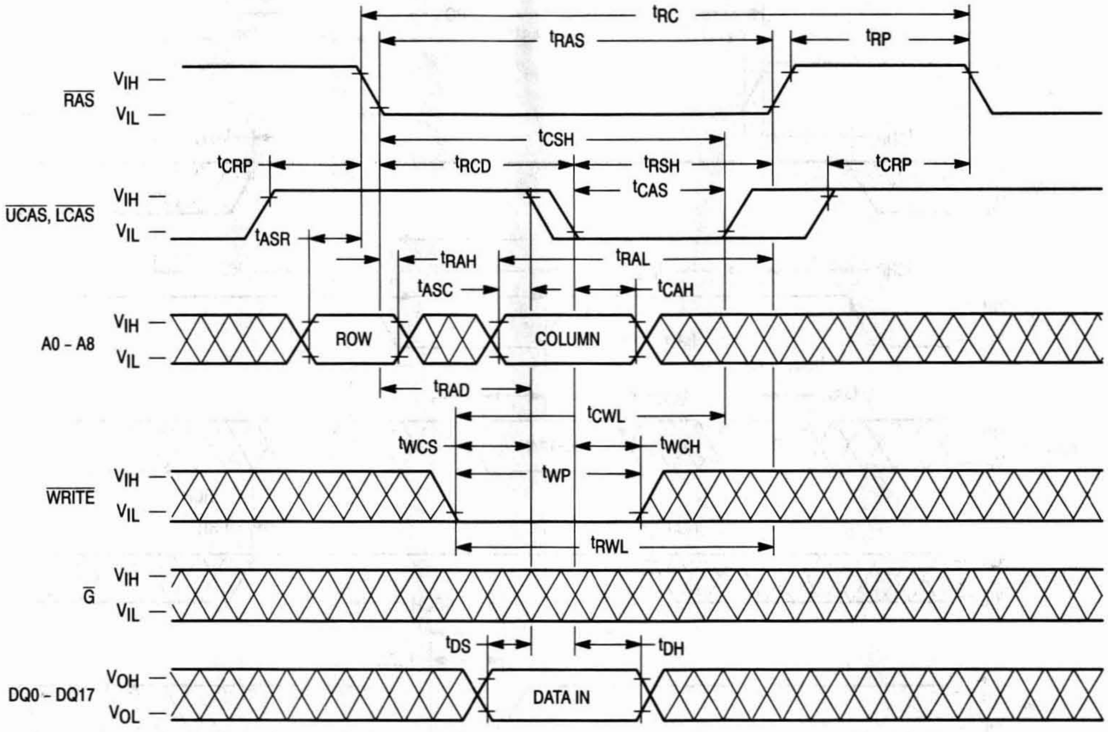
tRP
RAS
VIH
VIL
tCRP
tRPC
UCAS
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
LCAS
tRAD
tRAH
tRAL
tASR
tASC
tCAH
A0 - A8
ROW
COLUMN
tRCH
tRCS
tRRH
WRITE
tROH
tAA
tOEA
G
tCAC
tOFF
tRAC
tOEZ
DQ0 - DQ8
VOH
VOL
OPEN
DATA OUT
tCLZ
DQ9 - DQ17
OPEN

NOTE: D_{in} (DQ0 – DQ8) = Open
D_{in} (DQ9 – DQ17) = Don't Care

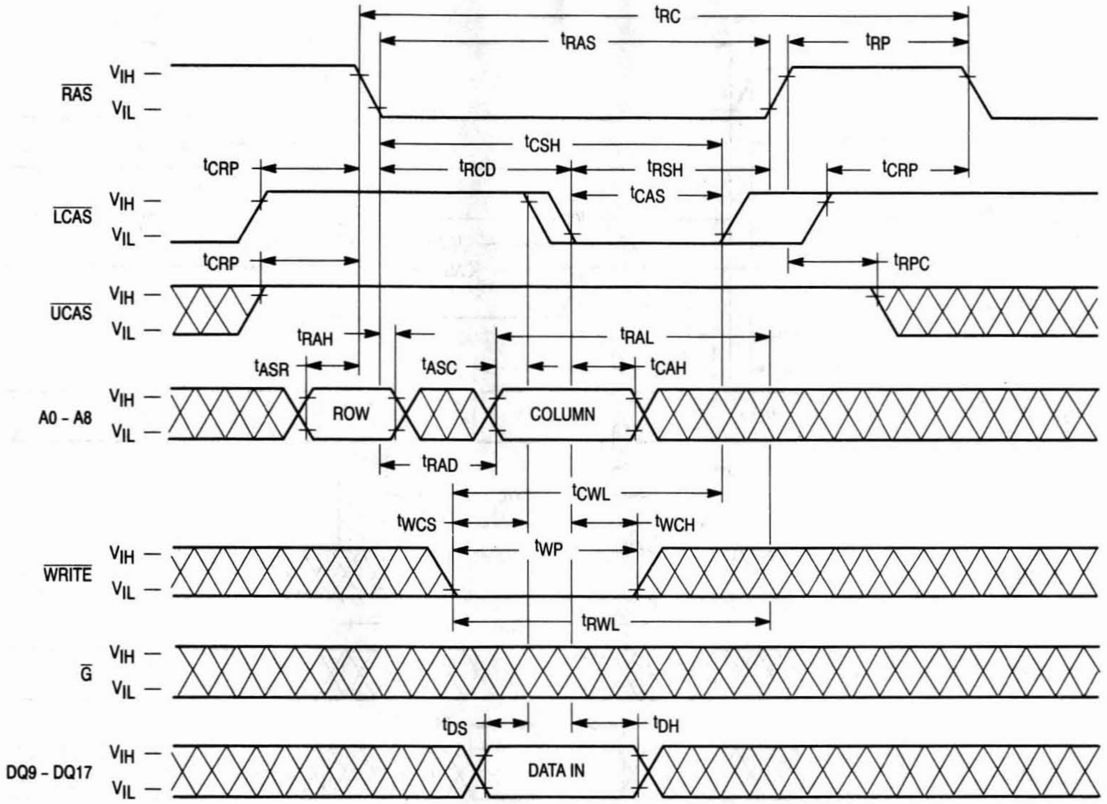
WRITE CYCLE (EARLY WRITE)



t_{RC}
t_{RAS}
t_{RP}
V_{IH}
$\overline{RAS}$
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
V_{IH}
$\overline{UCAS}$, $\overline{LCAS}$
V_{IL}
t_{ASR}
t_{RAH}
t_{RAL}
t_{ASC}
t_{CAH}
V_{IH}
A0 – A8
V_{IL}
ROW
COLUMN
t_{RAD}
t_{CWL}
t_{WCS}
t_{WCH}
V_{IH}
t_{WP}
$\overline{WRITE}$
V_{IL}
t_{RWL}
V_{IH}
$\overline{G}$
V_{IL}
t_{DS}
t_{DH}
V_{OH}
DQ0 – DQ17
V_{OL}
DATA IN

NOTE: D_{out} = Open

UPPER BYTE WRITE CYCLE (EARLY WRITE)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RAS
VIH
VIL
tCSH
tCRP
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tCAS
tCRP
LCAS
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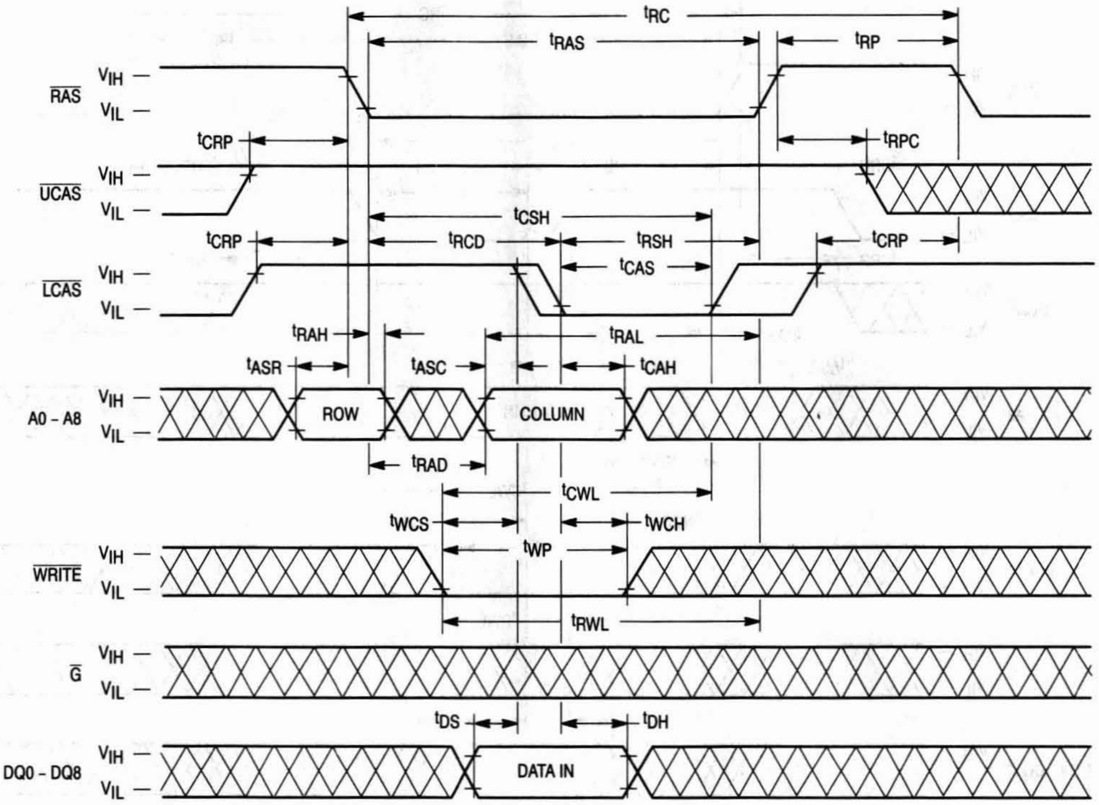
tRPC
UCAS
tRAH
tRAL
tASR
tASC
tCAH
A0 - A8
ROW
COLUMN
tRAD
tCWL
tWCS
tWCH
tWP
WRITE
tRWL
G
tDS
tDH
DQ9 - DQ17
DATA IN

NOTE: D_{in} (DQ0 - DQ8) = Don't Care
D_{out} = Open

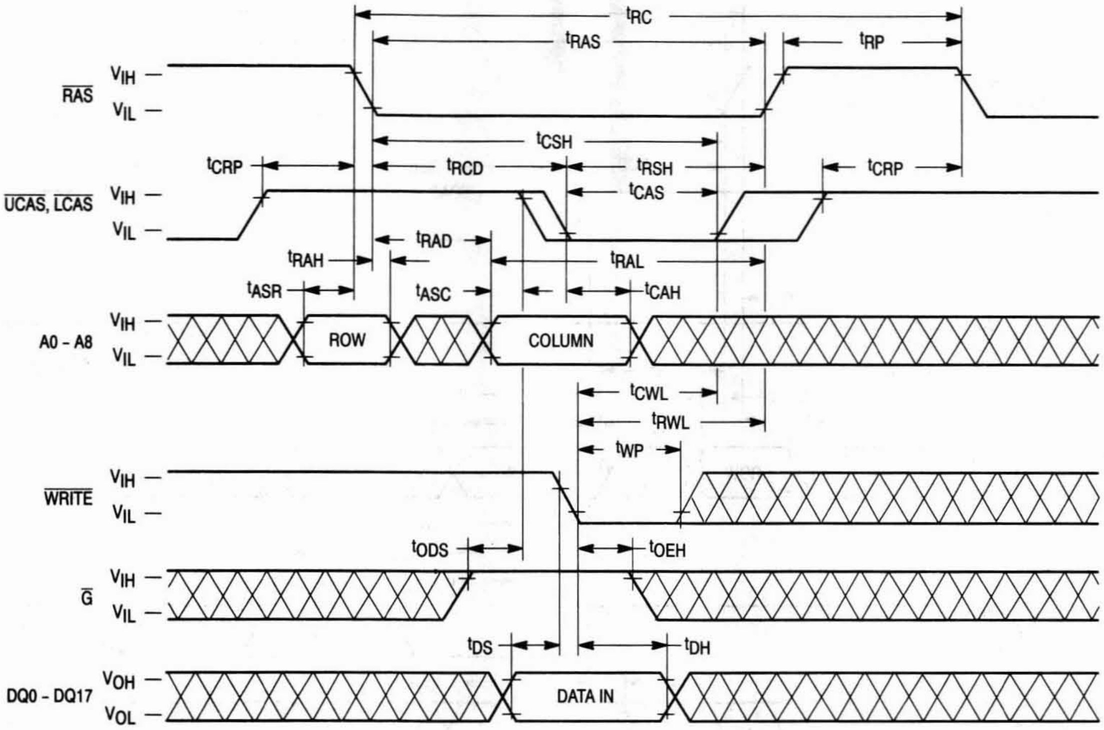
LOWER BYTE WRITE CYCLE (EARLY WRITE)



t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{UCAS}$
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{LCAS}$
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 – A8
ROW
COLUMN
t_{RAD}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{WRITE}$
t_{RWL}
$\overline{G}$
t_{DS}
t_{DH}
DQ0 – DQ8
DATA IN

NOTE: D_{in} (DQ9 – DQ17) = Don't Care
D_{out} = Open

WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)

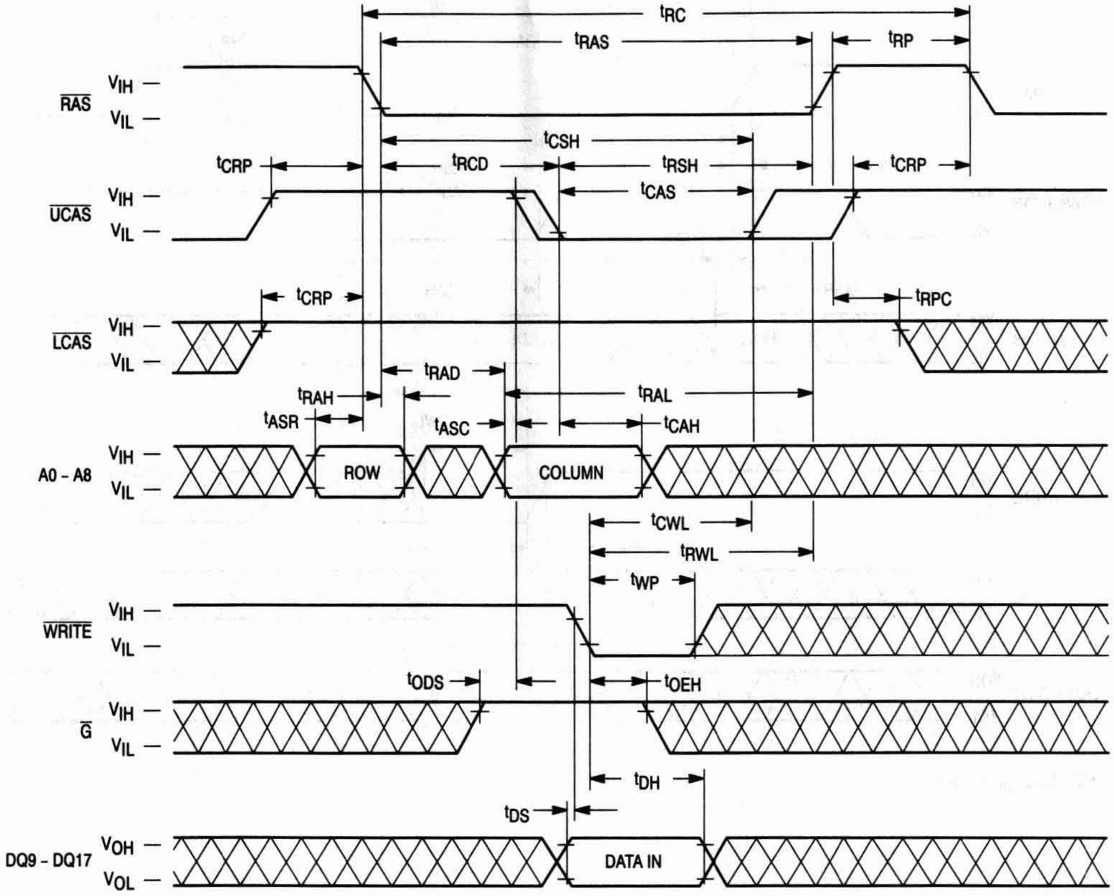


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
UCAS, LCAS
tRAD
tRAH
tRAL
tASR
tASC
tCAH
A0 - A8
ROW
COLUMN
tCWL
tRWL
tWP
WRITE
tODS
tOEH
G
tDS
tDH
DQ0 - DQ17
VOH
VOL
DATA IN

NOTE: D_{out} = Open

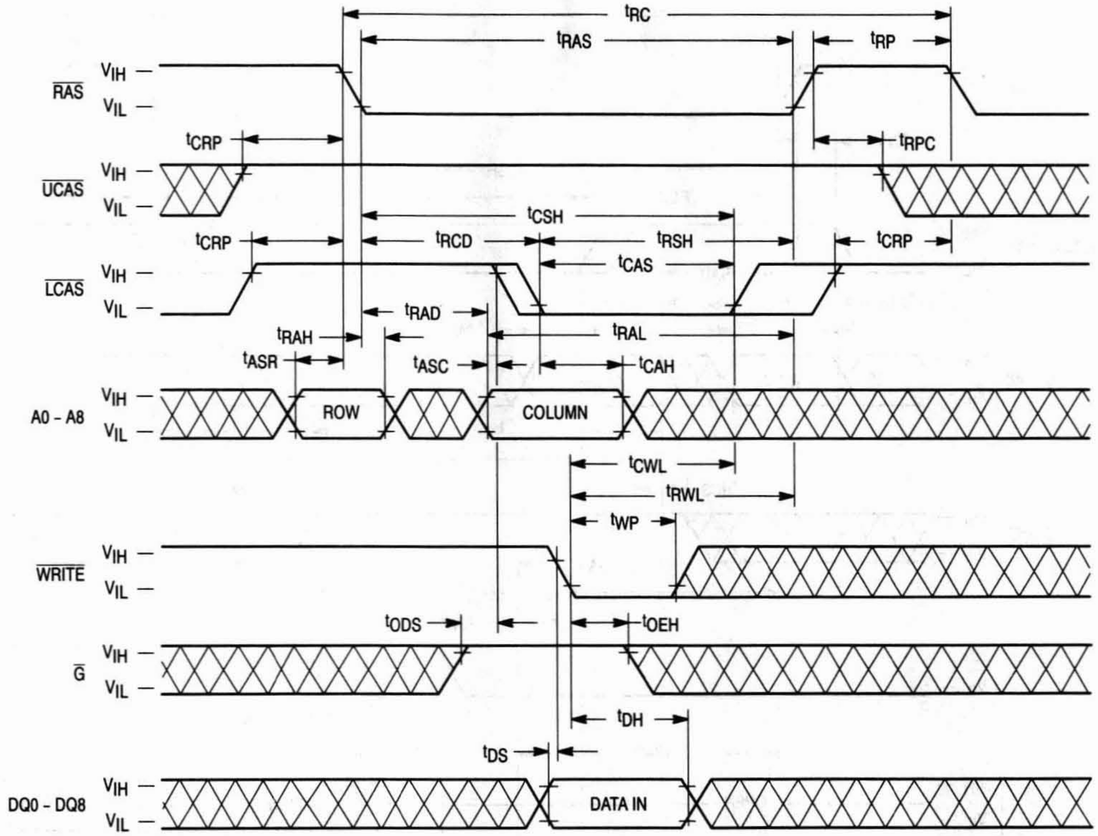
3

UPPER BYTE WRITE CYCLE ($\overline{\text{G}}$ CONTROLLED WRITE)


$\overline{\text{RAS}}$
$\overline{\text{UCAS}}$
$\overline{\text{LCAS}}$
A0 - A8
$\overline{\text{WRITE}}$
$\overline{\text{G}}$
DQ9 - DQ17
V_{IH}
V_{IL}
V_{OH}
V_{OL}
t_{RC}
t_{RAS}
t_{RP}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CAS}
t_{RPC}
t_{RAD}
t_{RAH}
t_{ASR}
t_{ASC}
t_{RAL}
t_{CAH}
ROW
COLUMN
t_{CWL}
t_{RWL}
t_{WP}
t_{ODS}
t_{OEH}
t_{DH}
t_{DS}
DATA IN

NOTE: D_{in} (DQ0 – DQ8) = Don't Care
D_{out} = Open

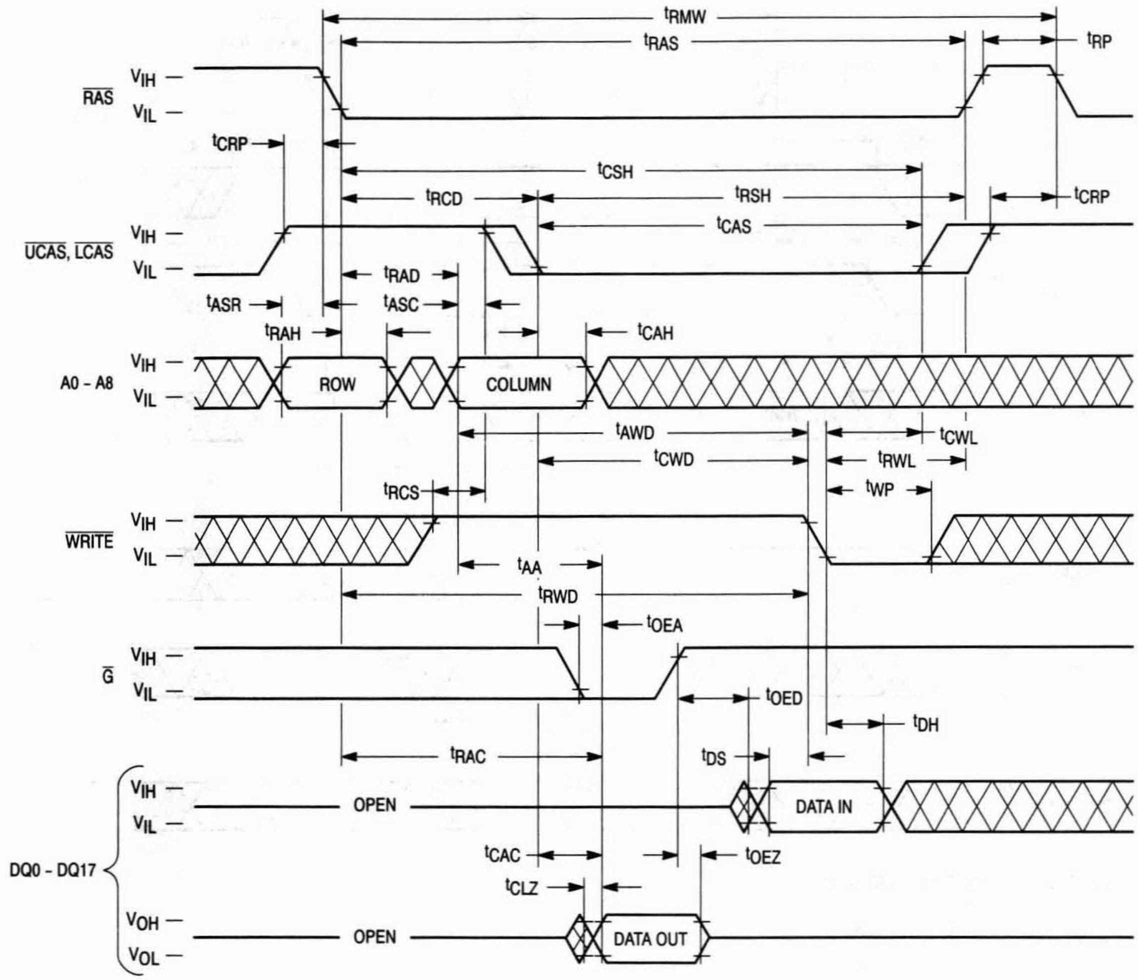
LOWER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



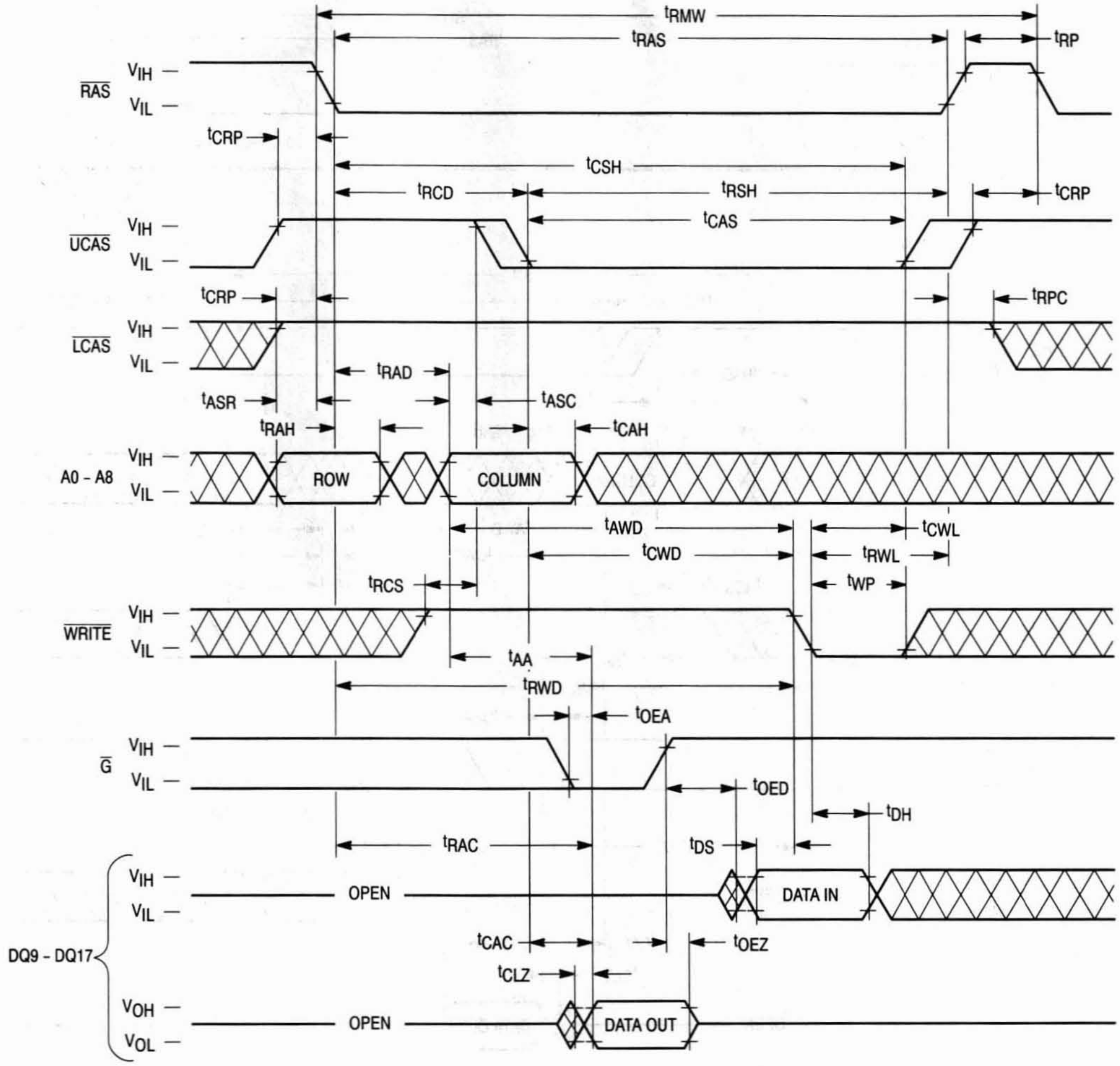
t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{UCAS}$
t_{CSH}
t_{RCD}
t_{RSH}
t_{CAS}
$\overline{LCAS}$
t_{RAD}
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 - A8
ROW
COLUMN
t_{CWL}
t_{RWL}
t_{WP}
$\overline{WRITE}$
t_{ODS}
t_{OEH}
$\overline{G}$
t_{DH}
t_{DS}
DQ0 - DQ8
DATA IN

NOTE: D_{in} (DQ9 – DQ17) = Don't Care
D_{out} = Open

READ-MODIFY-WRITE CYCLE


tRMW
tRAS
tRP
RAS
VIH —
VIL —
tCRP
tCSH
tRCD
tRSH
tCRP
tCAS
UCAS, LCAS
VIH —
VIL —
tRAD
tASR
tASC
tRAH
tCAH
A0 – A8
VIH —
VIL —
ROW
COLUMN
tAWD
tCWL
tCWD
tRWL
tRCS
tWP
WRITE
VIH —
VIL —
tAA
tRWD
tOEA
G
VIH —
VIL —
tOED
tDH
tRAC
tDS
VIH —
VIL —
OPEN
DATA IN
DQ0 – DQ17
tCAC
tOEZ
tCLZ
VOH —
VOL —
OPEN
DATA OUT

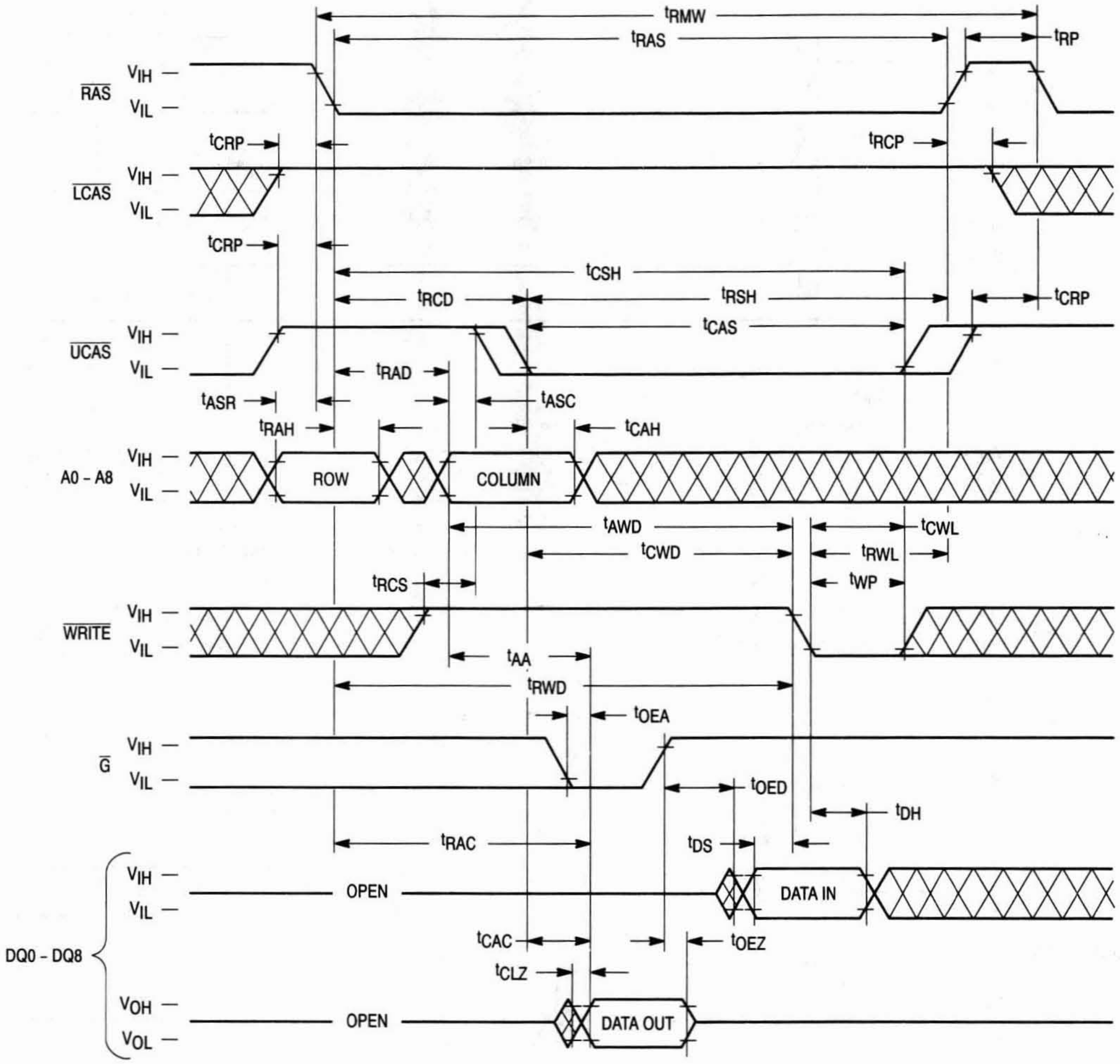
UPPER BYTE READ-MODIFY-WRITE CYCLE



t_RMW
t_RAS
t_RP
RAS
V_IH
V_IL
t_CRP
t_CSH
t_RCD
t_RSH
t_CRP
t_CAS
UCAS
V_IH
V_IL
t_CRP
t_RPC
LCAS
V_IH
V_IL
t_RAD
t_ASR
t_ASC
t_RAH
t_CAH
A0 - A8
V_IH
V_IL
ROW
COLUMN
t_AWD
t_CWL
t_CWD
t_RWL
t_RCS
t_WP
WRITE
V_IH
V_IL
t_AA
t_RWD
t_OEA
G
V_IH
V_IL
t_OED
t_DH
t_RAC
t_DS
V_IH
V_IL
OPEN
DATA IN
DQ9 - DQ17
t_CAC
t_OEZ
t_CLZ
V_OH
V_OL
OPEN
DATA OUT

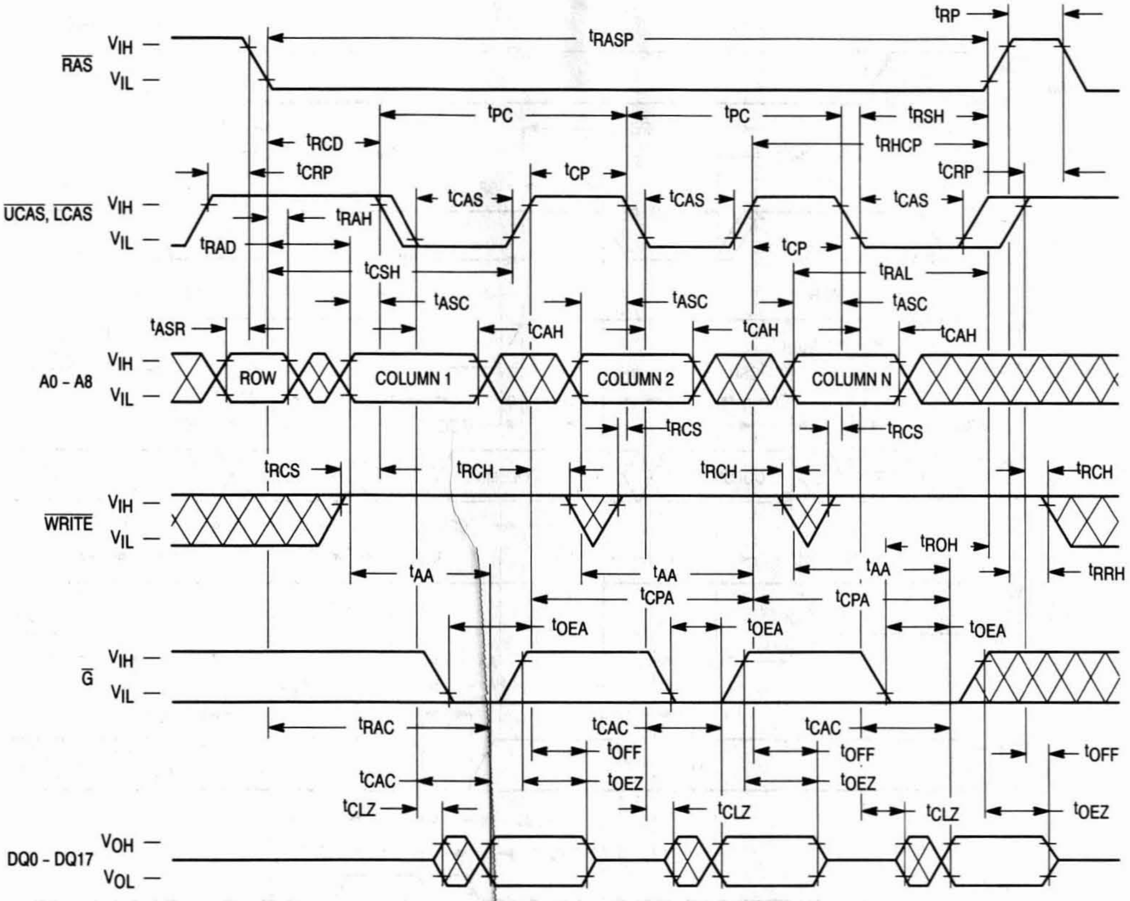
NOTE: D_{in} (DQ0 – DQ8) = Don't Care
D_{out} (DQ0 – DQ8) = Open

LOWER BYTE READ-MODIFY-WRITE CYCLE


t_RMW
t_RAS
t_RP
RAS
V_IH
V_IL
t_CRP
t_RCP
LCAS
t_CRP
t_CSH
t_RCD
t_RSH
t_CRP
UCAS
t_CAS
t_RAD
t_ASR
t_ASC
t_RAH
t_CAH
A0 - A8
ROW
COLUMN
t_AWD
t_CWL
t_CWD
t_RWL
t_WP
t_RCS
WRITE
t_AA
t_RWD
t_OEA
G
t_OED
t_DH
t_RAC
t_DS
OPEN
DATA IN
DQ0 - DQ8
t_CAC
t_OEZ
t_CLZ
V_OH
V_OL
OPEN
DATA OUT

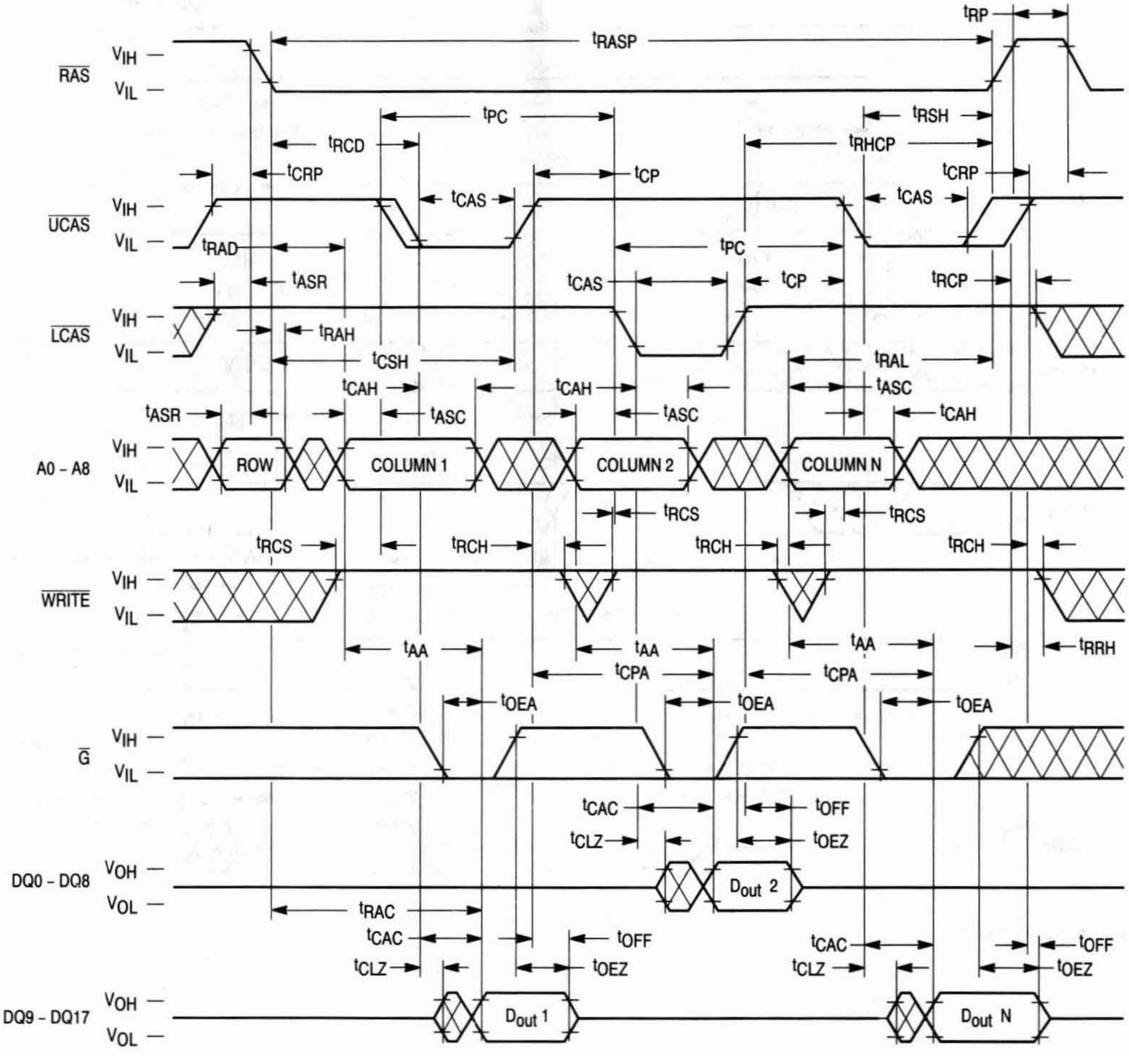
NOTE: D_{in} (DQ9 – DQ17) = Don't Care
D_{out} (DQ9 – DQ17) = Open

FAST PAGE MODE READ CYCLE


RAS
UCAS, LCAS
A0 - A8
WRITE
G
DQ0 - DQ17
V_IH
V_IL
V_OH
V_OL
tRASP
tRP
tPC
tRSH
tRHCP
tRCD
tCRP
tCP
tCAS
tRAH
tRAD
tCSH
tRAL
tASC
tASR
tCAH
ROW
COLUMN 1
COLUMN 2
COLUMN N
tRCS
tRCH
tROH
tRRH
tAA
tCPA
tOEA
tRAC
tCAC
tOFF
tOEZ
tCLZ

NOTE: D_{in} = Open

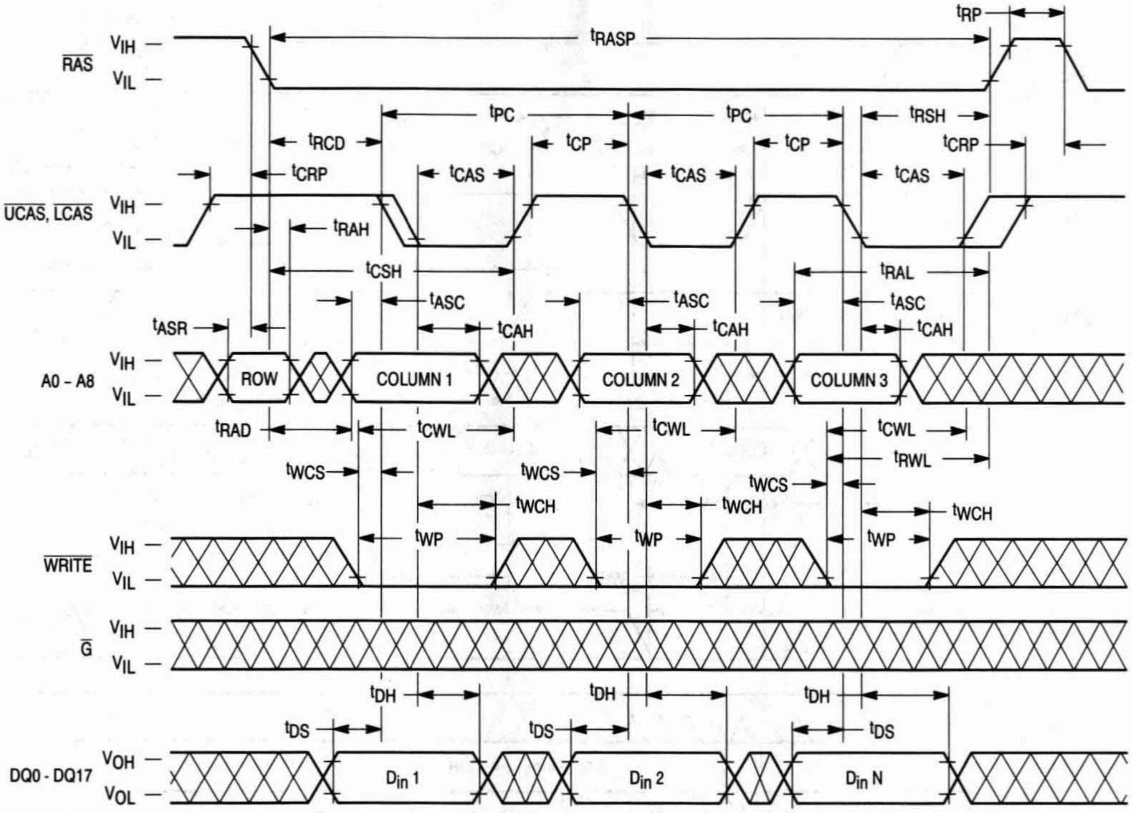
FAST PAGE MODE BYTE READ CYCLE



RAS
UCAS
LCAS
A0 – A8
WRITE
G
DQ0 – DQ8
DQ9 – DQ17
VIH
VIL
VOH
VOL
tRASP
tRP
tPC
tRSH
tRCD
tRHCP
tCRP
tCP
tCAS
tRAD
tASR
tRCP
tRAH
tCSH
tRAL
tCAH
tASC
ROW
COLUMN 1
COLUMN 2
COLUMN N
tRCS
tRCH
tAA
tRRH
tCPA
tOEA
tCAC
tOFF
tCLZ
tOEZ
tRAC
Dout 1
Dout 2
Dout N

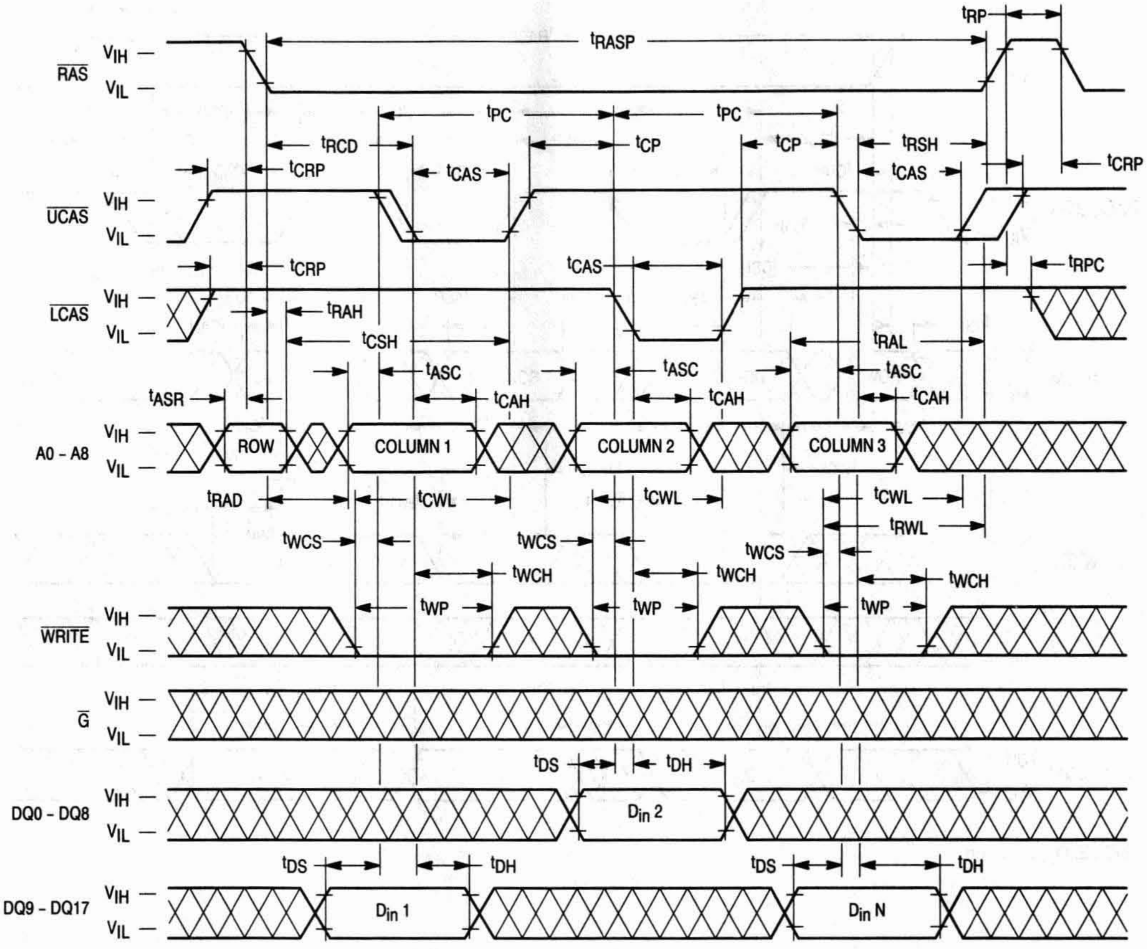
NOTE: D_{in} Open

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)


$\overline{RAS}$
V_{IH}
V_{IL}
t_{RP}
t_{RASP}
t_{PC}
t_{PC}
t_{RSH}
t_{RCD}
t_{CP}
t_{CP}
t_{CRP}
t_{CRP}
t_{CAS}
t_{CAS}
t_{CAS}
$\overline{UCAS}, \overline{LCAS}$
t_{RAH}
t_{CSH}
t_{RAL}
t_{ASC}
t_{ASC}
t_{ASC}
t_{ASR}
t_{CAH}
t_{CAH}
t_{CAH}
A0 - A8
ROW
COLUMN 1
COLUMN 2
COLUMN 3
t_{RAD}
t_{CWL}
t_{CWL}
t_{CWL}
t_{RWL}
t_{WCS}
t_{WCS}
t_{WCS}
t_{WCH}
t_{WCH}
t_{WCH}
t_{WP}
t_{WP}
t_{WP}
$\overline{WRITE}$
$\overline{G}$
t_{DH}
t_{DH}
t_{DH}
t_{DS}
t_{DS}
t_{DS}
DQ0 - DQ17
V_{OH}
V_{OL}
D_{in} 1
D_{in} 2
D_{in} N

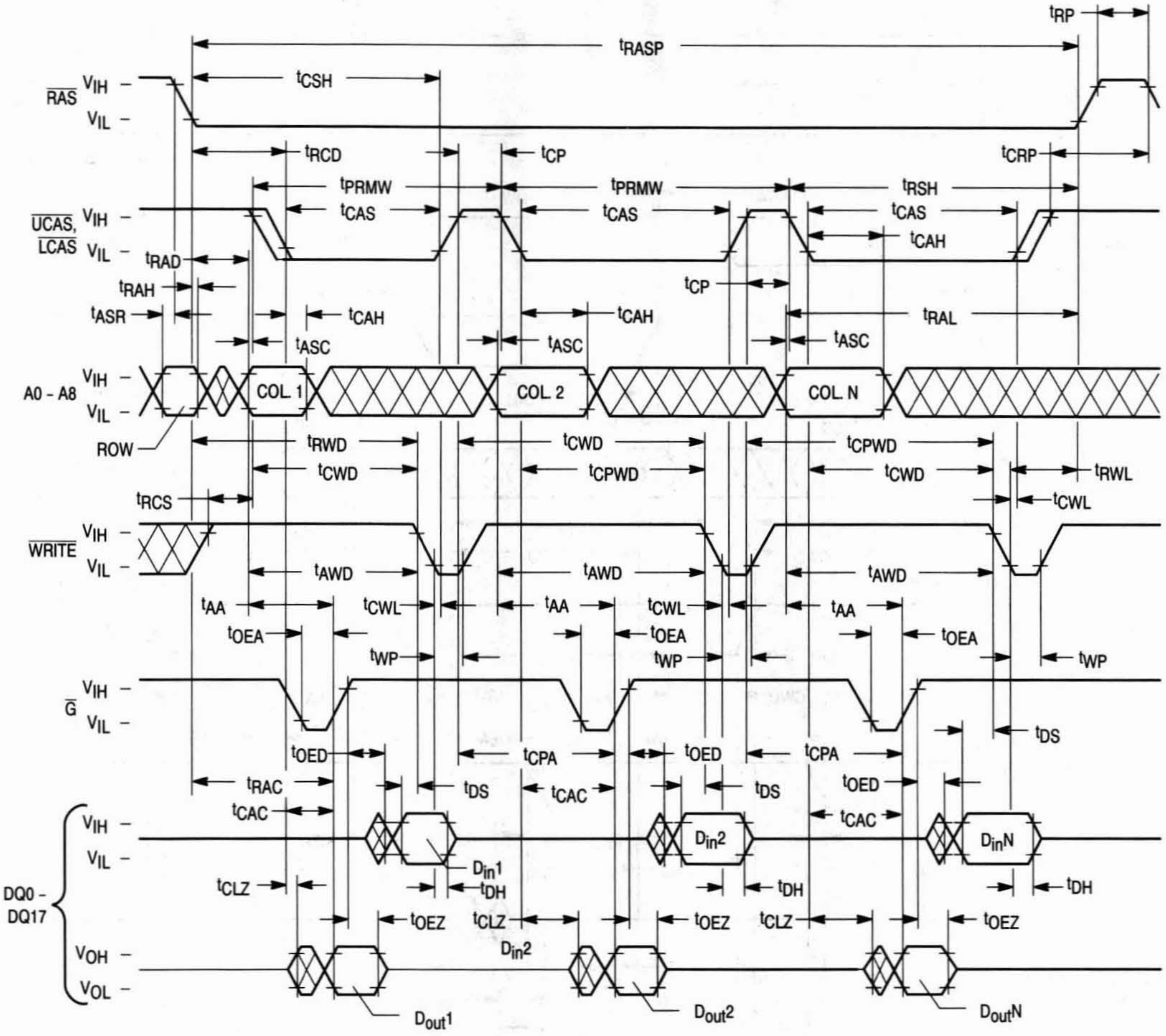
NOTE: D_{out} = Open

FAST PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)

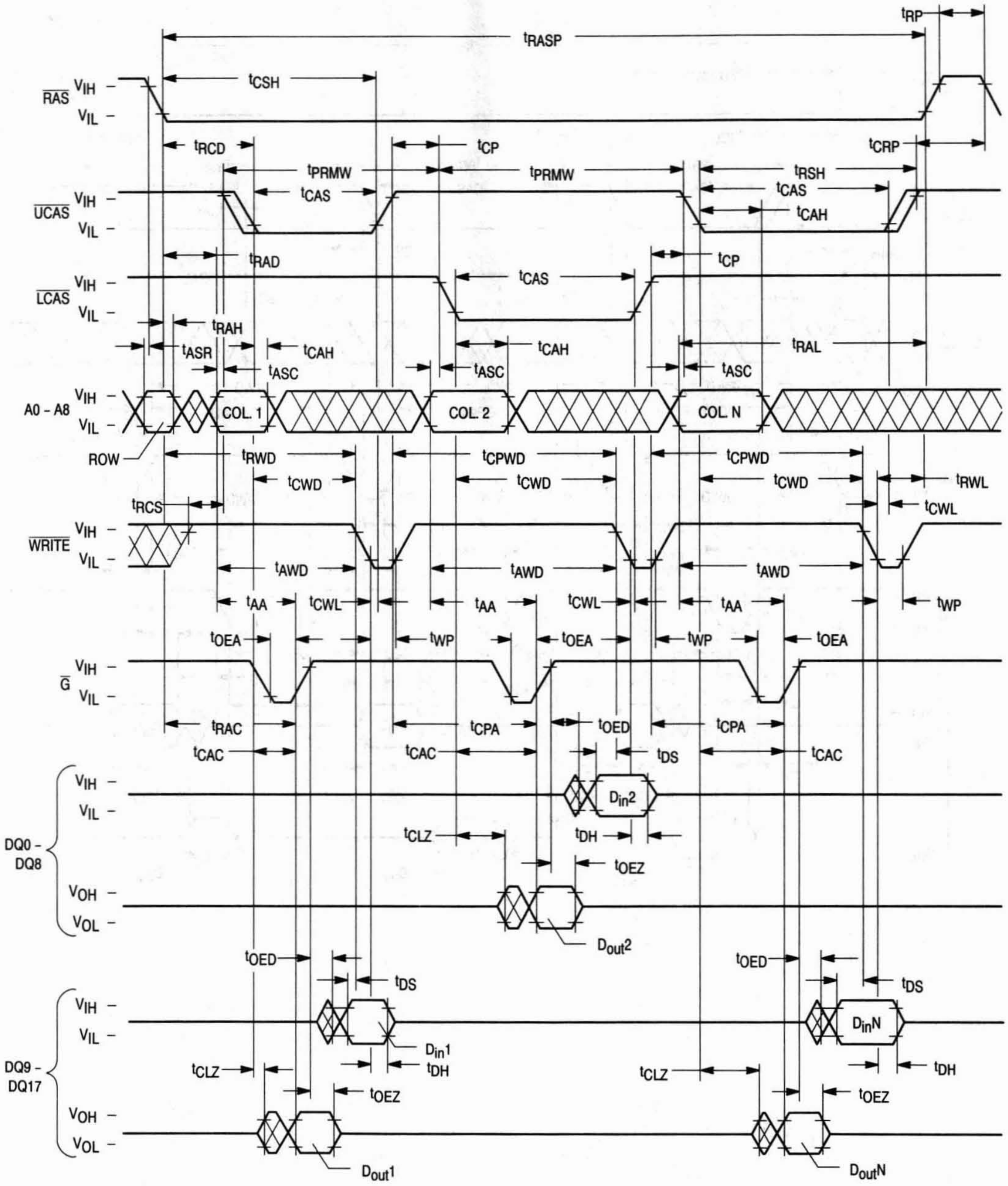

$\overline{RAS}$
$\overline{UCAS}$
$\overline{LCAS}$
A0 - A8
$\overline{WRITE}$
$\overline{G}$
DQ0 - DQ8
DQ9 - DQ17
V_{IH}
V_{IL}
t_{RP}
t_{RASP}
t_{PC}
t_{PC}
t_{RCD}
t_{CP}
t_{CP}
t_{RSH}
t_{CRP}
t_{CAS}
t_{CAS}
t_{CRP}
t_{CRP}
t_{CAS}
t_{RPC}
t_{RAH}
t_{CSH}
t_{RAL}
t_{ASC}
t_{ASC}
t_{ASC}
t_{ASR}
t_{CAH}
t_{CAH}
t_{CAH}
ROW
COLUMN 1
COLUMN 2
COLUMN 3
t_{RAD}
t_{CWL}
t_{CWL}
t_{CWL}
t_{RWL}
t_{WCS}
t_{WCS}
t_{WCS}
t_{WCH}
t_{WCH}
t_{WCH}
t_{WP}
t_{WP}
t_{WP}
t_{DS}
t_{DH}
D_{in} 2
t_{DS}
t_{DH}
t_{DS}
t_{DH}
D_{in} 1
D_{in} N

NOTE: D_{out} = Open

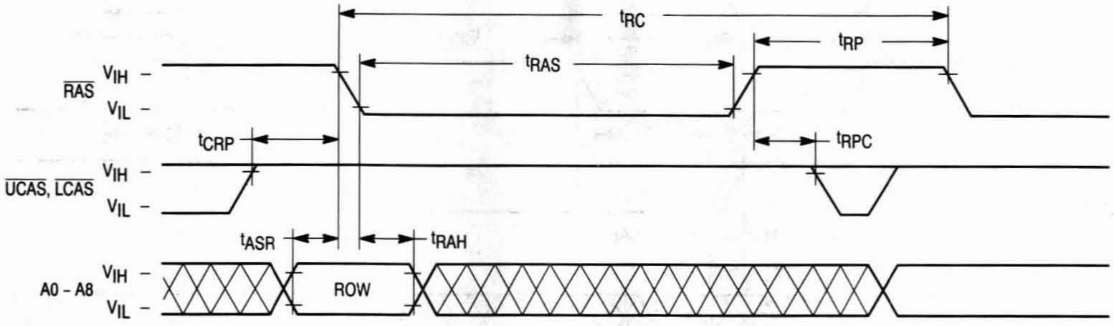
FAST PAGE MODE READ-MODIFY-WRITE CYCLE


t_{RP}
t_{RASP}
$\overline{RAS}$ V_{IH} – V_{IL} –
t_{CSH}
t_{RCD}
t_{CP}
t_{CRP}
t_{PRMW}
t_{PRMW}
t_{RSH}
t_{CAS}
t_{CAS}
t_{CAS}
t_{CAH}
$\overline{UCAS}$, $\overline{LCAS}$ V_{IH} – V_{IL} –
t_{RAD}
t_{RAH}
t_{ASR}
t_{CAH}
t_{CAH}
t_{CP}
t_{RAL}
t_{ASC}
t_{ASC}
t_{ASC}
A0 - A8 V_{IH} – V_{IL} –
COL. 1
COL. 2
COL. N
ROW
t_{RWD}
t_{CWD}
t_{CPWD}
t_{CWD}
t_{CPWD}
t_{CWD}
t_{RWL}
t_{CWL}
t_{RCS}
$\overline{WRITE}$ V_{IH} – V_{IL} –
t_{AWD}
t_{AWD}
t_{AWD}
t_{AA}
t_{CWL}
t_{AA}
t_{CWL}
t_{AA}
t_{OEA}
t_{OEA}
t_{OEA}
t_{WP}
t_{WP}
t_{WP}
$\overline{G}$ V_{IH} – V_{IL} –
t_{DS}
t_{OED}
t_{CPA}
t_{OED}
t_{CPA}
t_{RAC}
t_{DS}
t_{CAC}
t_{DS}
t_{OED}
t_{CAC}
t_{CAC}
DQ0 - DQ17 V_{IH} – V_{IL} – V_{OH} – V_{OL} –
$D_{in}1$
$D_{in}2$
$D_{in}N$
t_{CLZ}
t_{DH}
t_{DH}
t_{DH}
t_{OEZ}
t_{CLZ}
t_{OEZ}
t_{CLZ}
t_{OEZ}
$D_{in}2$
$D_{out}1$
$D_{out}2$
$D_{out}N$

FAST PAGE MODE BYTE READ-MODIFY-WRITE CYCLE

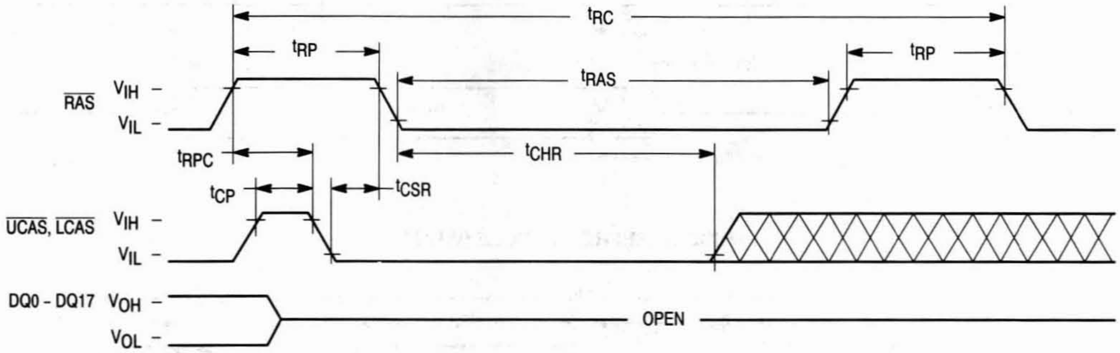

tRP
tRASP
RAS
VIH
VIL
tCSH
tRCD
tCP
tCRP
tPRMW
tPRMW
tRSH
tCAS
tCAS
tCAH
UCAS
VIH
VIL
tRAD
tCP
LCAS
VIH
VIL
tCAS
tRAH
tASR
tCAH
tCAH
tRAL
tASC
tASC
tASC
A0 - A8
VIH
VIL
ROW
COL. 1
COL. 2
COL. N
tRWD
tCPWD
tCPWD
tCWD
tCWD
tCWD
tRWL
tCWL
tRCS
WRITE
VIH
VIL
tAWD
tAWD
tAWD
tAA
tCWL
tAA
tCWL
tAA
tWP
tOEA
tWP
tOEA
tWP
tOEA
G
VIH
VIL
tRAC
tCPA
tOED
tCPA
tCAC
tCAC
tDS
tCAC
DQ0 - DQ8
VIH
VIL
Din2
tCLZ
tDH
tOEZ
VOH
VOL
Dout2
tOED
tDS
tOED
tDS
DQ9 - DQ17
VIH
VIL
Din1
DinN
tCLZ
tDH
tCLZ
tDH
tOEZ
tOEZ
VOH
VOL
Dout1
DoutN

$\overline{\text{RAS}}$-ONLY REFRESH CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCRP
tRPC
UCAS, LCAS
VIH
VIL
tASR
tRAH
A0 - A8
VIH
VIL
ROW

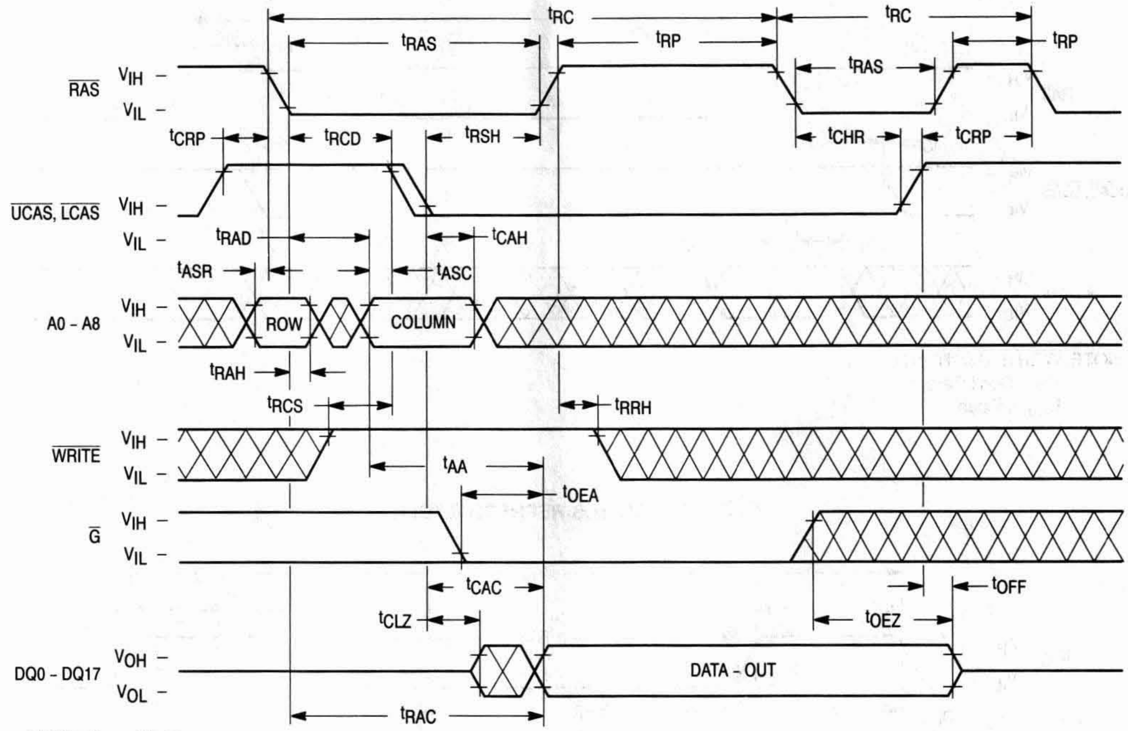
NOTE: $\overline{\text{WRITE}}$, $\overline{\text{G}}$ = “H” or “L”
D_{in} = Don’t Care
D_{out} = Open

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE


tRC
tRP
tRP
tRAS
RAS
VIH
VIL
tRPC
tCHR
tCP
tCSR
UCAS, LCAS
VIH
VIL
DQ0 - DQ17
VOH
VOL
OPEN

NOTE: $\overline{\text{WRITE}}$, $\overline{\text{G}}$, A0 – A8= “H” or “L”
D_{in} = Don’t Care
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is performed when either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ meets this timing.

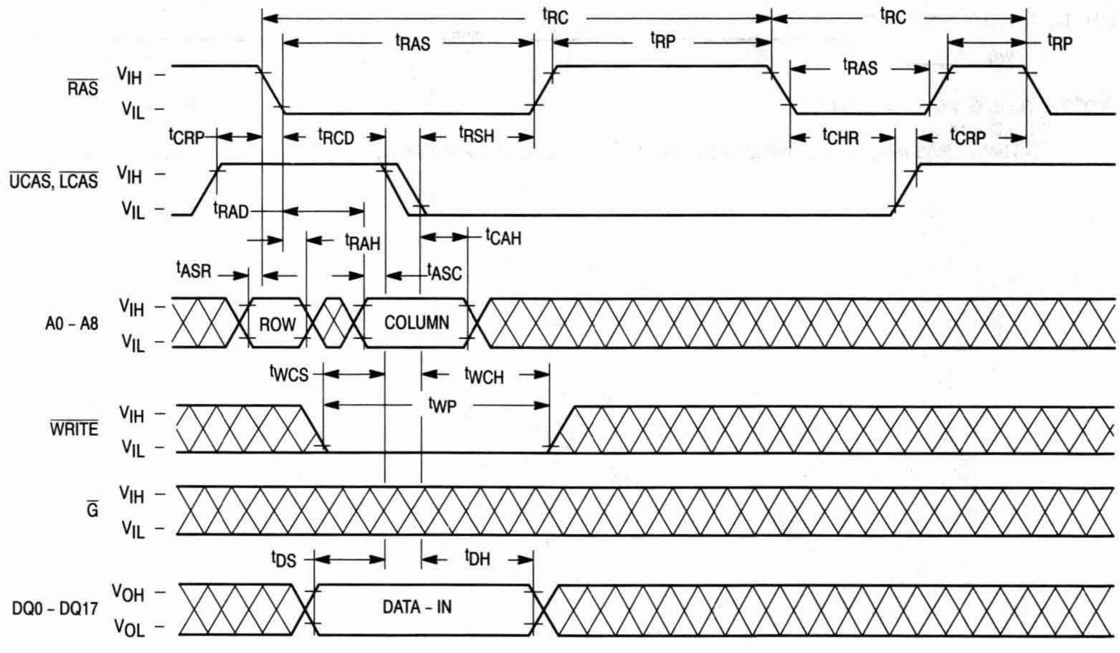
HIDDEN REFRESH CYCLE (READ)



t_{RC}
t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
t_{RP}
RAS
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CRP}
UCAS, LCAS
V_{IH}
V_{IL}
t_{RAD}
t_{CAH}
t_{ASR}
t_{ASC}
A0 - A8
V_{IH}
V_{IL}
ROW
COLUMN
t_{RAH}
t_{RCS}
t_{RRH}
WRITE
V_{IH}
V_{IL}
t_{AA}
t_{OEA}
G
V_{IH}
V_{IL}
t_{CAC}
t_{OFF}
t_{CLZ}
t_{OEZ}
DQ0 - DQ17
V_{OH}
V_{OL}
DATA - OUT
t_{RAC}

NOTE: D_{in} = Open

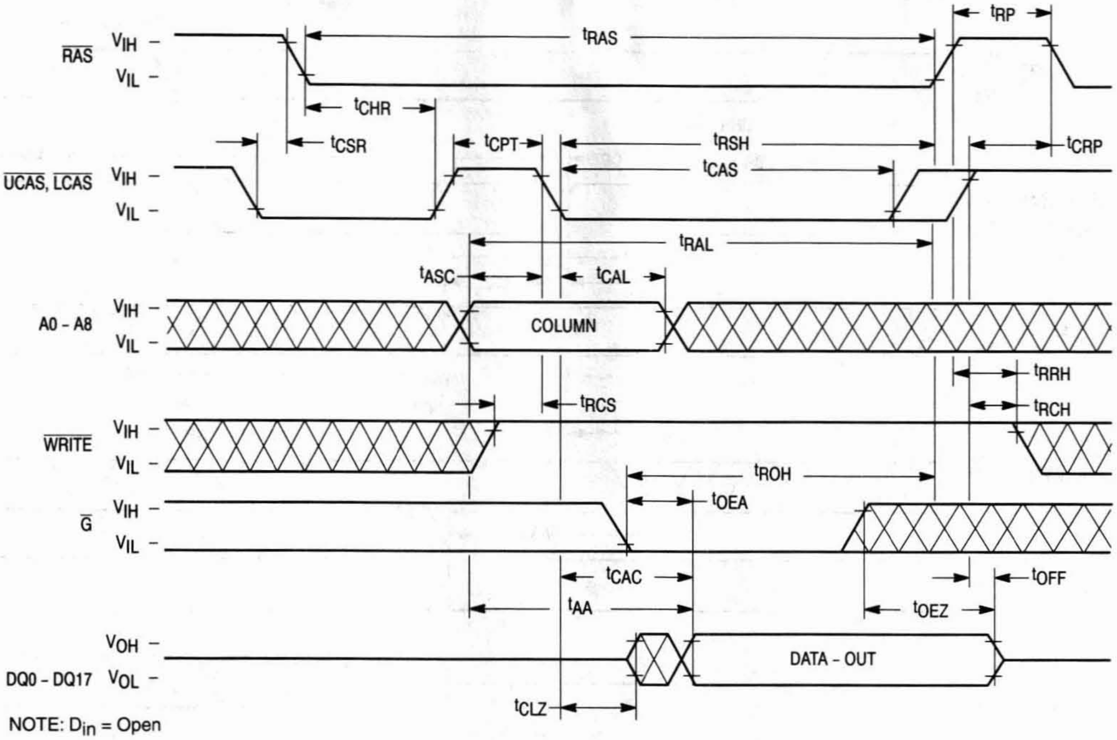
HIDDEN REFRESH CYCLE (WRITE)



t_{RC}
t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
t_{RP}
RAS
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CRP}
UCAS, LCAS
V_{IH}
V_{IL}
t_{RAD}
t_{RAH}
t_{CAH}
t_{ASR}
t_{ASC}
A0 - A8
V_{IH}
V_{IL}
ROW
COLUMN
t_{WCS}
t_{WCH}
t_{WP}
WRITE
V_{IH}
V_{IL}
G
V_{IH}
V_{IL}
t_{DS}
t_{DH}
DQ0 - DQ17
V_{OH}
V_{OL}
DATA - IN

NOTE: D_{out} = Open

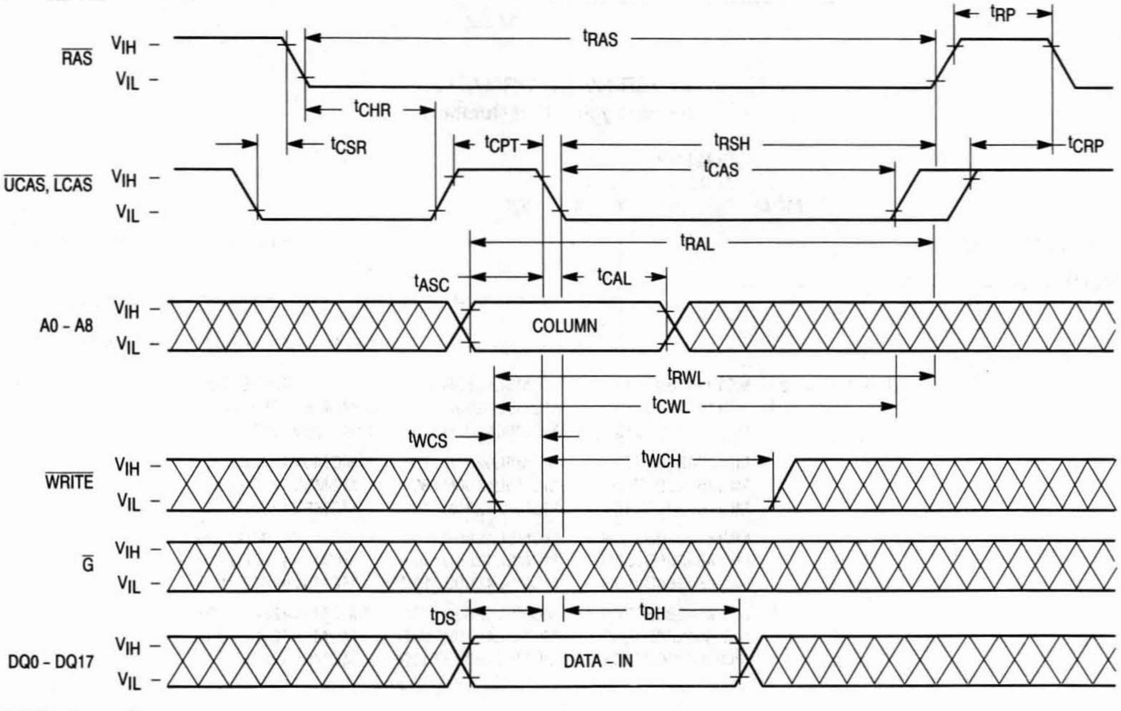
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST READ CYCLE



RAS
VIH
VIL
tRAS
tRP
tCHR
tCSR
tCPT
tRSH
tCRP
UCAS, LCAS
tCAS
tRAL
tASC
tCAL
A0 - A8
COLUMN
tRRH
tRCS
tRCH
WRITE
tROH
G
tOEA
tCAC
tOFF
tAA
tOEZ
VOH
VOL
DQ0 - DQ17
DATA - OUT
tCLZ

NOTE: D_{in} = Open

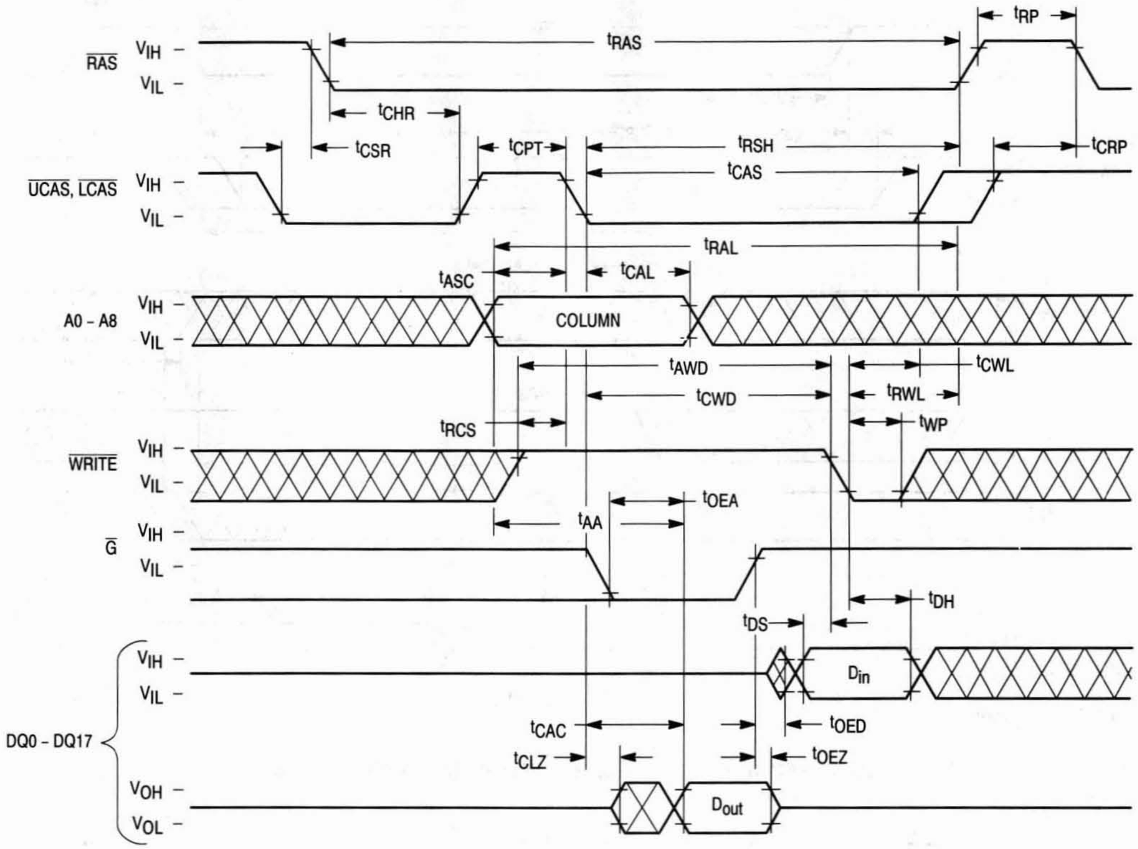
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST WRITE CYCLE



RAS
VIH
VIL
tRAS
tRP
tCHR
tCSR
tCPT
tRSH
tCRP
UCAS, LCAS
tCAS
tRAL
tASC
tCAL
A0 - A8
COLUMN
tRWL
tCWL
tWCS
tWCH
WRITE
G
tDS
tDH
DQ0 - DQ17
DATA - IN

NOTE: D_{out} = Open

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE


$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RP}
t_{RAS}
t_{CHR}
t_{CSR}
t_{CPT}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$
t_{RAL}
t_{ASC}
t_{CAL}
A0 – A8
COLUMN
t_{AWD}
t_{CWL}
t_{CWD}
t_{RWL}
t_{RCS}
t_{WP}
$\overline{\text{WRITE}}$
t_{OEA}
t_{AA}
$\overline{\text{G}}$
t_{DH}
t_{DS}
D_{in}
DQ0 – DQ17
t_{CAC}
t_{OED}
t_{CLZ}
t_{OEZ}
V_{OH}
V_{OL}
D_{out}

ORDERING INFORMATION

(Order by Full Part Number)

54280B
5L4280B
MCM 5V4280B X XX XX

Motorola Memory Prefix
Part Number
Shipping Method (Blank = Tray, R = Tape and Reel, Blank = Rails)
Speed (70 = 70 ns, 80 = 80 ns, 10 = 100 ns)
Package (J = 400 mil SOJ, T = 400 mil TSOP)

Full Part Numbers —			
	MCM54280BJ70	MCM5L4280BJ70	MCM5V4280BJ70
	MCM54280BJ80	MCM5L4280BJ80	MCM5V4280BJ80
	MCM54280BJ10	MCM5L4280BJ10	MCM5V4280BJ10
	MCM54280BT70	MCM5L4280BT70	MCM5V4280BT70
	MCM54280BT80	MCM5L4280BT80	MCM5V4280BT80
	MCM54280BT10	MCM5L4280BT10	MCM5V4280BT10
	MCM54280BJ70R	MCM5L4280BJ70R	MCM5V4280BJ70R
	MCM54280BJ80R	MCM5L4280BJ80R	MCM5V4280BJ80R
	MCM54280BJ10R	MCM5L4280BJ10R	MCM5V4280BJ10R
	MCM54280BT70R	MCM5L4280BT70R	MCM5V4280BT70R
	MCM54280BT80R	MCM5L4280BT80R	MCM5V4280BT80R
	MCM54280BT10R	MCM5L4280BT10R	MCM5V4280BT10R

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM54400A
MCM5L4400A

1M x 4 CMOS Dynamic RAM
Fast Page Mode

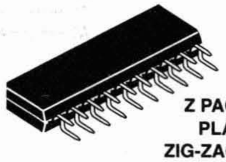
The MCM54400A is a 0.7µ CMOS high-speed dynamic random access memory. It is organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM54400A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil J-lead small outline package (SOJ), a 100 mil zig-zag in-line package (ZIP), and a 300 mil thin-small-outline package (TSOP).

- Three-State Data Output
- Fast Page Mode
- Test Mode
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM54400A = 16 ms
  MCM5L4400A = 128 ms
- Fast Access Time (t_{RAC}):
  - MCM54400A-60 and MCM5L4400A-60 = 60 ns (Max)
  - MCM54400A-70 and MCM5L4400A-70 = 70 ns (Max)
  - MCM54400A-80 and MCM5L4400A-80 = 80 ns (Max)
- Low Active Power Dissipation:
  - MCM54400A-60 and MCM5L4400A-60 = 660 mW (Max)
  - MCM54400A-80 and MCM5L4400A-80 = 550 mW (Max)
  - MCM54400A-80 and MCM5L4400A-80 = 468 mW (Max)
- Low Standby Power Dissipation:
  - MCM54400A and MCM5L400A = 11 mW (Max, TTL Levels)
  - MCM54400A = 5.5 mW (Max, CMOS Levels)
  - MCM5L4400A = 1.1 mW (Max, CMOS Levels)

N PACKAGE
300 MIL SOJ
CASE 822-03

T PACKAGE
300 MIL TSOP
CASE 892-01



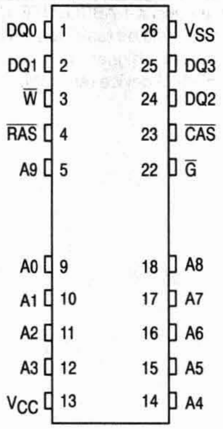
Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836-02

PIN NAMES

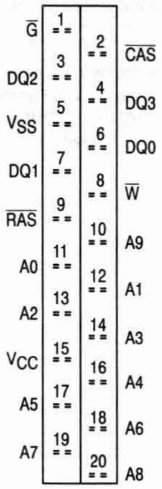
A0 – A9	Address Input
DQ0 – DQ3	Data Input
$\overline{\text{G}}$	Output Enable
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

PIN ASSIGNMENTS

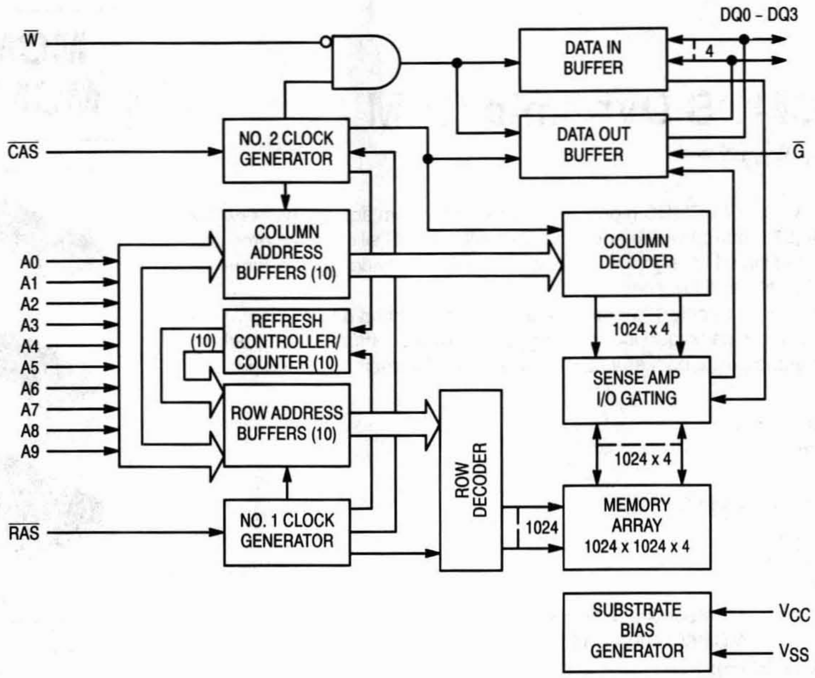
300 MIL SOJ/TSOP



100 MIL ZIP



BLOCK DIAGRAM


DQ0 – DQ3
W̄
DATA IN BUFFER
4
DATA OUT BUFFER
Ḡ
CAS̄
NO. 2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (10)
COLUMN DECODER
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
REFRESH CONTROLLER/ COUNTER (10)
(10)
1024 x 4
SENSE AMP I/O GATING
ROW ADDRESS BUFFERS (10)
1024 x 4
ROW DECODER
MEMORY ARRAY 1024 x 1024 x 4
1024
RAS̄
NO. 1 CLOCK GENERATOR
SUBSTRATE BIAS GENERATOR
VCC
VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current	I_{out}	50	mA
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.0	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	1, 2
MCM54400A-60 and MCM5L4400A-60, t_{RC} = 110 ns		—	120		
MCM54400A-70 and MCM5L4400A-70, t_{RC} = 130 ns		—	100		
MCM54400A-80 and MCM5L4400A-80, t_{RC} = 150 ns		—	85		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	1, 2
MCM54400A-60 and MCM5L4400A-60, t_{RC} = 110 ns		—	120		
MCM54400A-70 and MCM5L4400A-70, t_{RC} = 130 ns		—	100		
MCM54400A-80 and MCM5L4400A-80, t_{RC} = 150 ns		—	85		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	1, 2
MCM54400A-60 and MCM5L4400A-60, t_{PC} = 45 ns		—	70		
MCM54400A-70 and MCM5L4400A-70, t_{PC} = 45 ns		—	70		
MCM54400A-80 and MCM5L4400A-80, t_{PC} = 50 ns		—	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} – 0.2 V)	I_{CC5}				
MCM54400A		—	1.0	mA	
MCM5L4400A		—	200	µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	1
MCM54400A-60 and MCM5L4400A-60, t_{RC} = 110 ns		—	120		
MCM54400A-70 and MCM5L4400A-70, t_{RC} = 130 ns		—	100		
MCM54400A-80 and MCM5L4400A-80, t_{RC} = 150 ns		—	85		
V_{CC} Power Supply Current, Battery Backup Mode — MCM5L4400A Only (t_{RC} = 125 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2 V; $\overline{G}$, $\overline{W}$ = V_{CC} – 0.2 V; A0 – A9 = V_{CC} – 0.2 V or 0.2 V; DQ0 – DQ3 = V_{CC} – 0.2 V or 0.2 V or OPEN; t_{RAS} = Min to 300 ns)	I_{CC7}	—	300	µA	1, 3
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery-back up. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A9	C_{in}	5	pF
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0 – DQ3	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM54400A-60 MCM5L4400A-60		MCM54400A-70 MCM5L4400A-70		MCM54400A-80 MCM5L4400A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	165	—	185	—	205	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	50	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	95	—	100	—	105	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	40	—	40	—	45	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	200 k	70	200 k	80	200 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	20	10 k	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) and/or t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

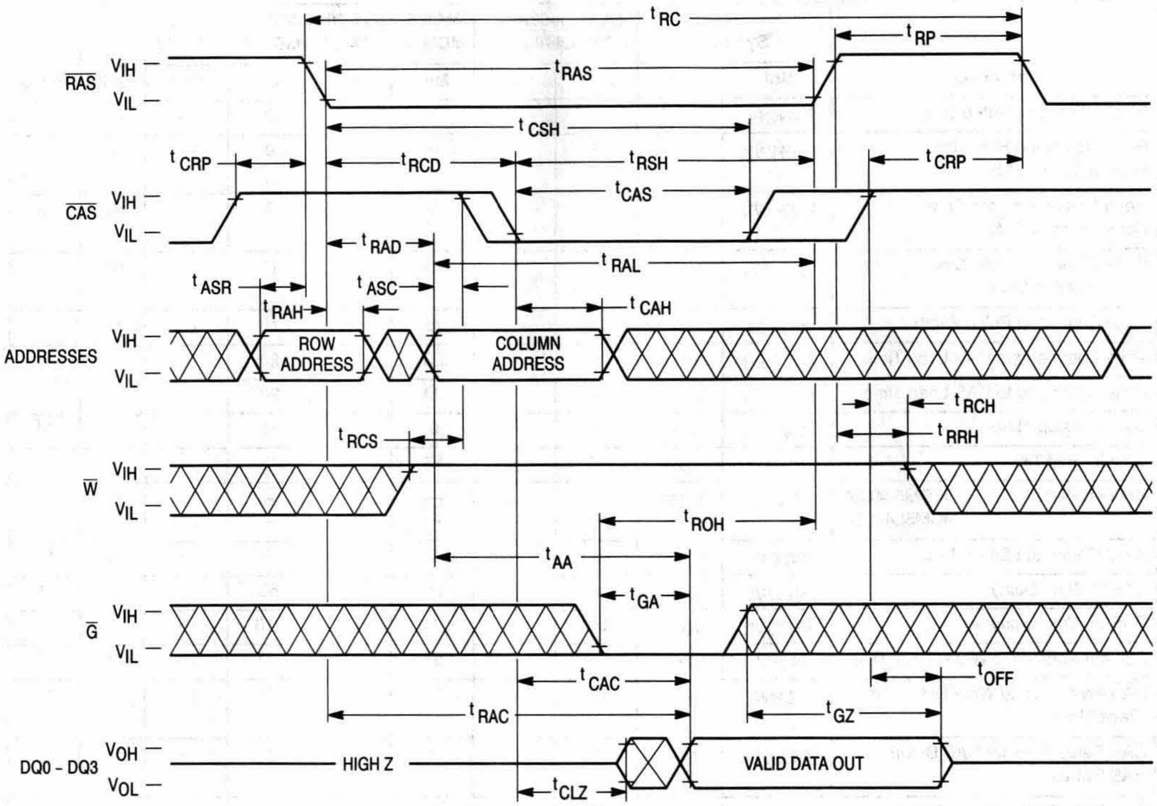
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM54400A-60 MCM5L4400A-60		MCM54400A-70 MCM5L4400A-70		MCM54400A-80 MCM5L4400A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	14
Refresh Period MCM54400A MCM5L4400A	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	50	—	ns	15
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	90	—	100	—	110	—	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	60	—	65	—	70	—	ns	15
$\overline{\text{CAS}}$ Precharge to Write Delay Time (Page Mode)	t_{CEHWL}	t_{CPWD}	70	—	70	—	75	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Time	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{G}}$	t_{GLREH}	t_{ROH}	10	—	10	—	10	—	ns	
$\overline{\text{G}}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	20	—	20	ns	
$\overline{\text{G}}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	20	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{\text{G}}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	20	ns	10
$\overline{\text{G}}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	20	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	

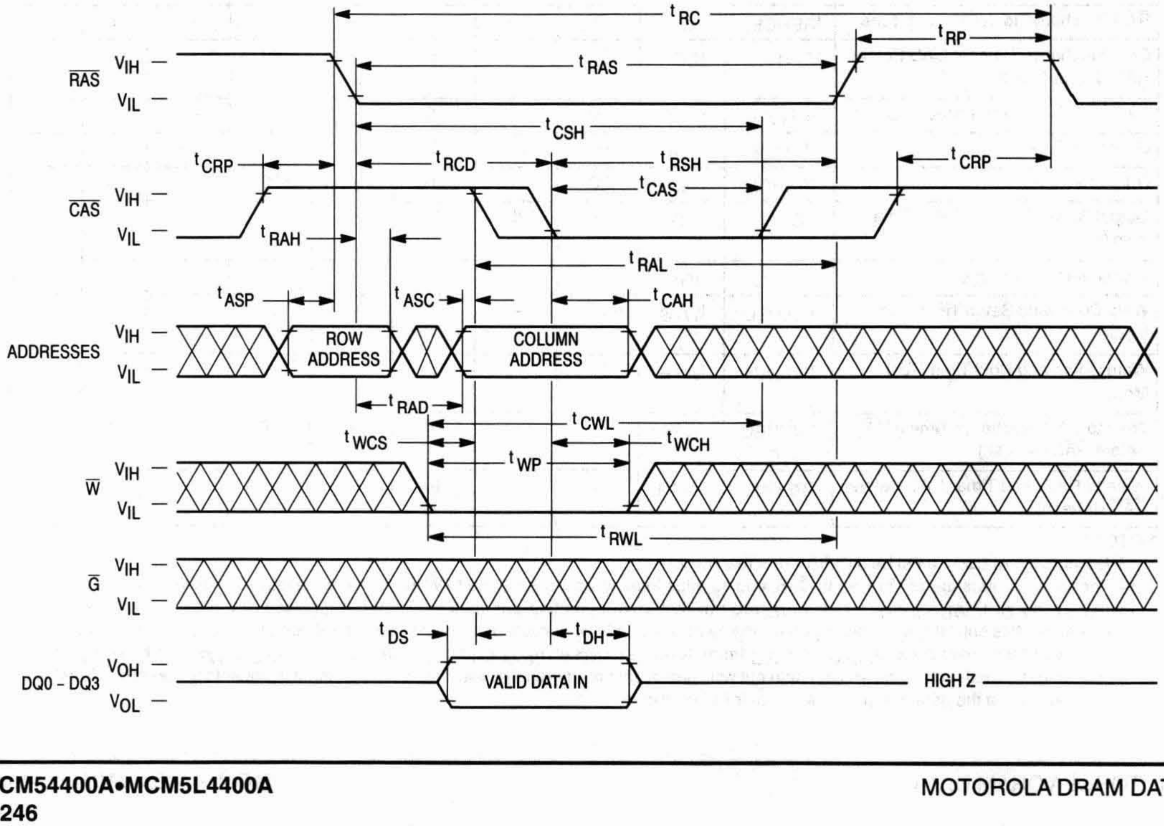
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in late write or read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE


t_{RC}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RAS}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
$\overline{CAS}$
t_{CAS}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{RCH}
t_{RRH}
t_{RCS}
$\overline{W}$
t_{ROH}
t_{AA}
t_{GA}
$\overline{G}$
t_{OFF}
t_{CAC}
t_{RAC}
t_{GZ}
DQ0 – DQ3
V_{OH}
V_{OL}
HIGH Z
VALID DATA OUT
t_{CLZ}

EARLY WRITE CYCLE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t_{RP}
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V_{IH}
V_{IL}
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t_{CRP}
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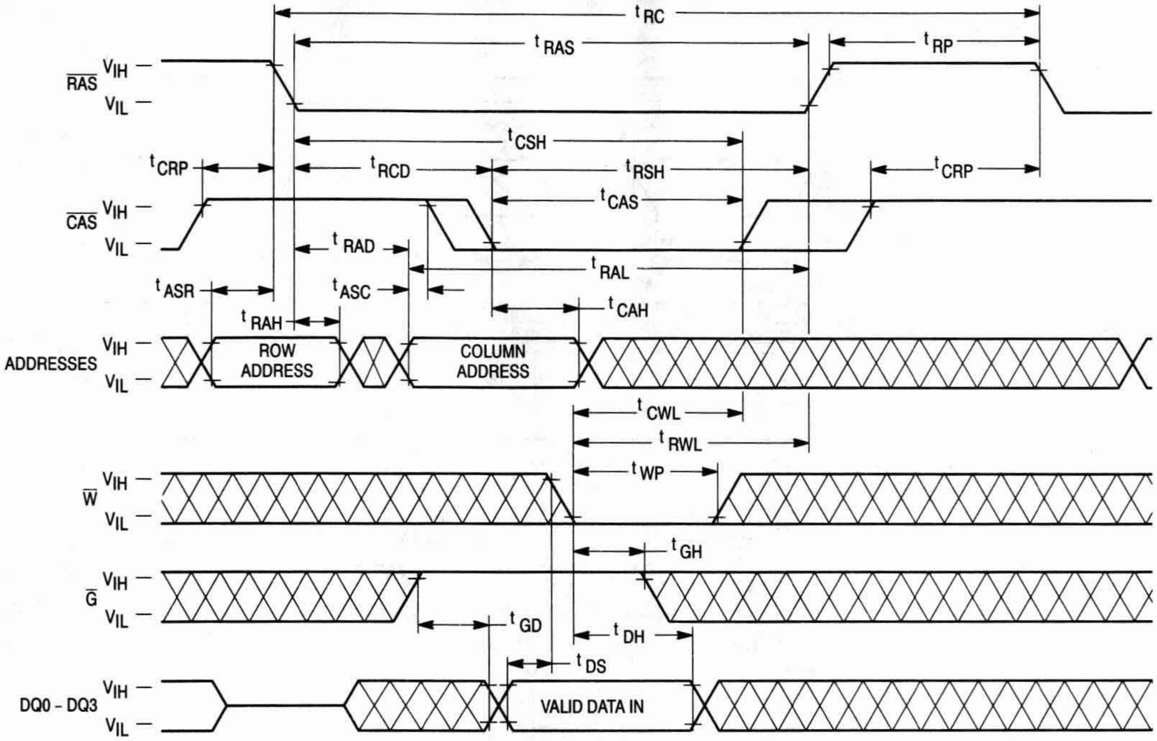
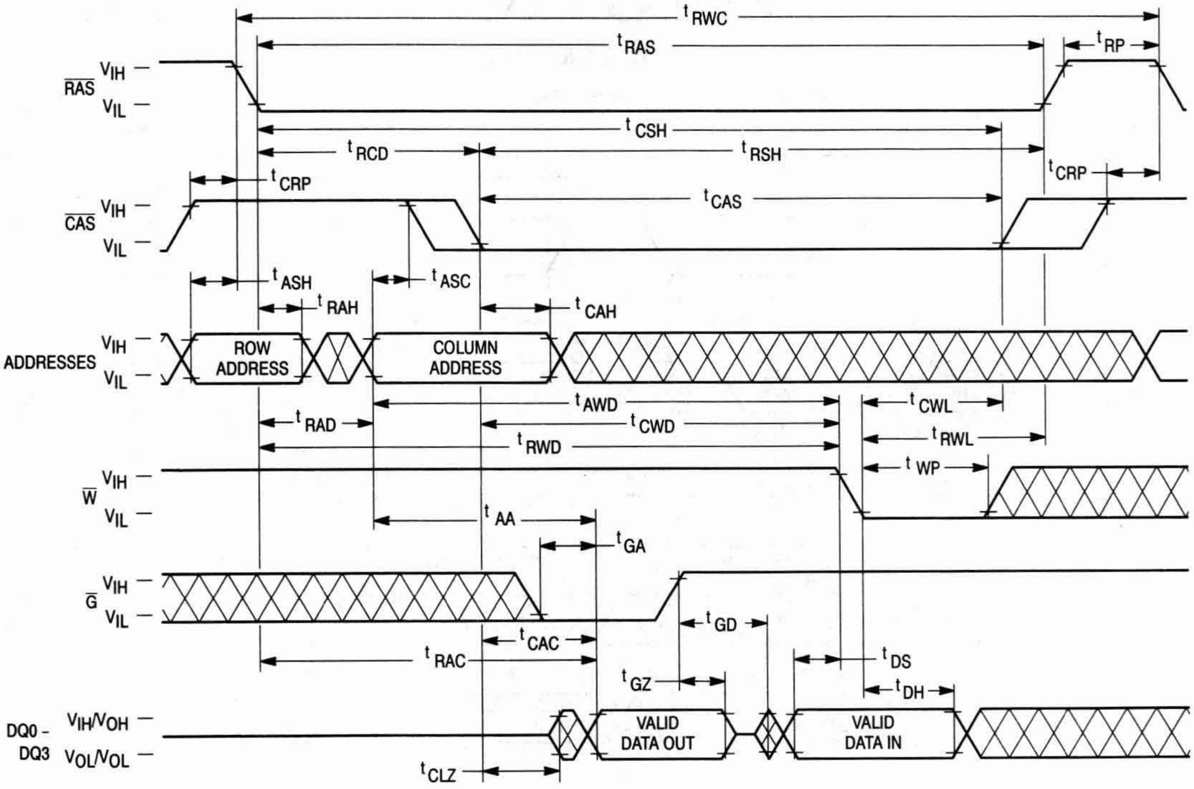
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
t_{RAH}
t_{RAL}
t_{ASP}
t_{ASC}
t_{CAH}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{RAD}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{W}$
t_{RWL}
$\overline{G}$
t_{DS}
t_{DH}
DQ0 – DQ3
V_{OH}
V_{OL}
VALID DATA IN
HIGH Z

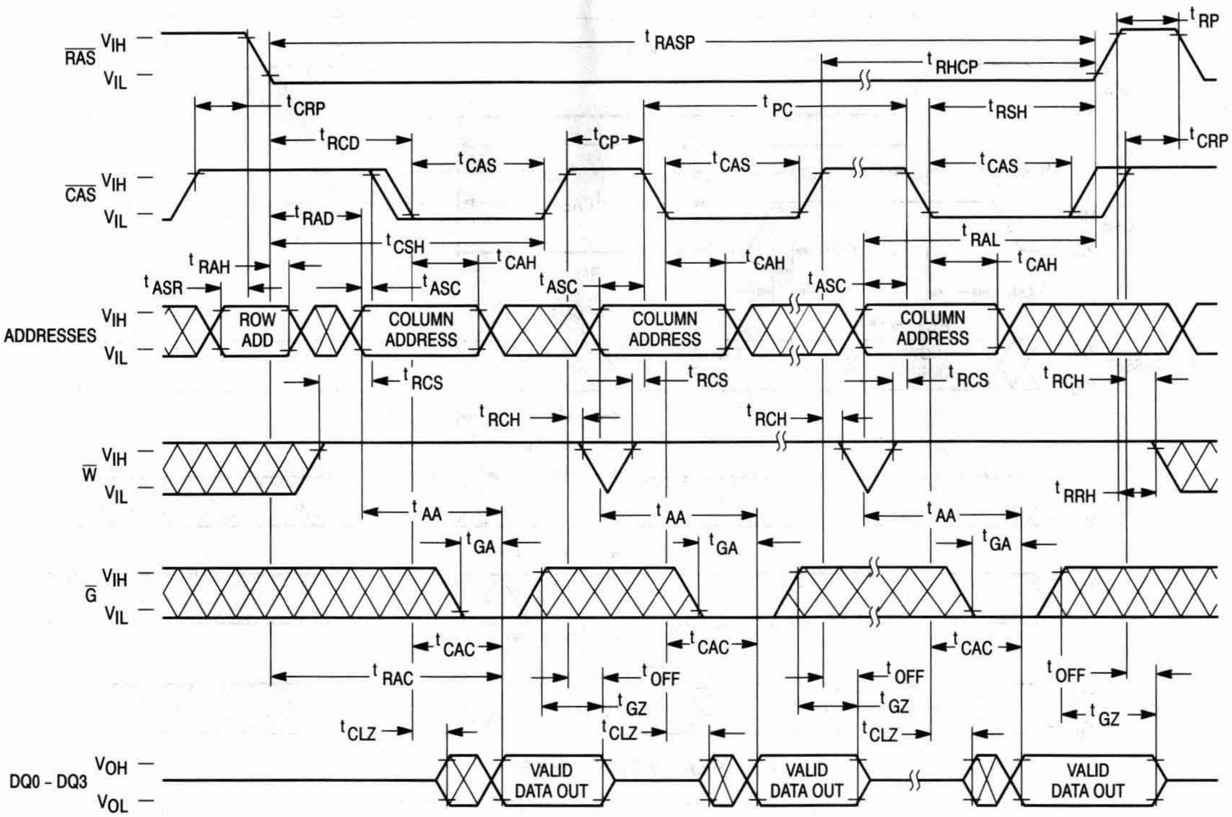
$\overline{\text{G}}$ CONTROLLED WRITE CYCLE


t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$ V_{IH} V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$ V_{IH} V_{IL}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
t_{RAH}
ADDRESSES V_{IH} V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{CWL}
t_{RWL}
t_{WP}
$\overline{W}$ V_{IH} V_{IL}
t_{GH}
$\overline{G}$ V_{IH} V_{IL}
t_{GD}
t_{DH}
t_{DS}
DQ0 – DQ3 V_{IH} V_{IL}
VALID DATA IN

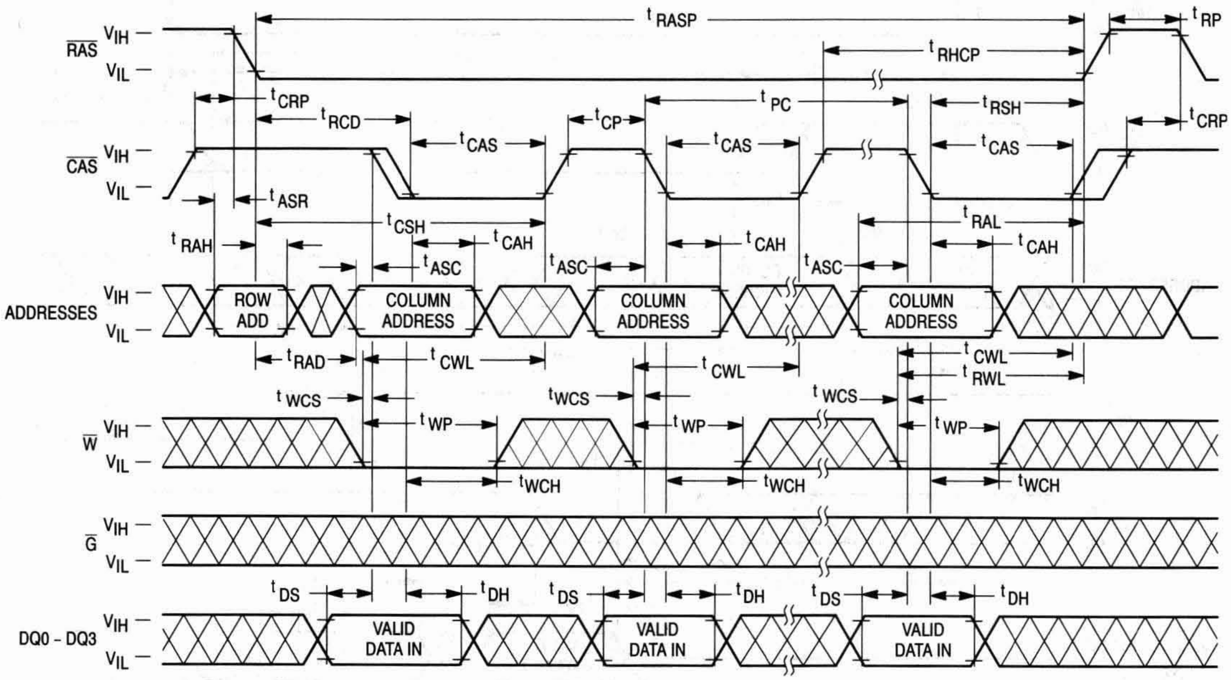
READ-WRITE CYCLE


t_{RWC}
t_{RAS}
t_{RP}
$\overline{RAS}$ V_{IH} V_{IL}
t_{CSH}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CRP}
t_{CAS}
$\overline{CAS}$ V_{IH} V_{IL}
t_{ASH}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES V_{IH} V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{AWD}
t_{CWL}
t_{RAD}
t_{CWD}
t_{RWL}
t_{RWD}
t_{WP}
$\overline{W}$ V_{IH} V_{IL}
t_{AA}
t_{GA}
$\overline{G}$ V_{IH} V_{IL}
t_{GD}
t_{CAC}
t_{RAC}
t_{DS}
t_{GZ}
t_{DH}
DQ0 - DQ3 V_{IH}/V_{OH} V_{OL}/V_{OL}
VALID DATA OUT
VALID DATA IN
t_{CLZ}

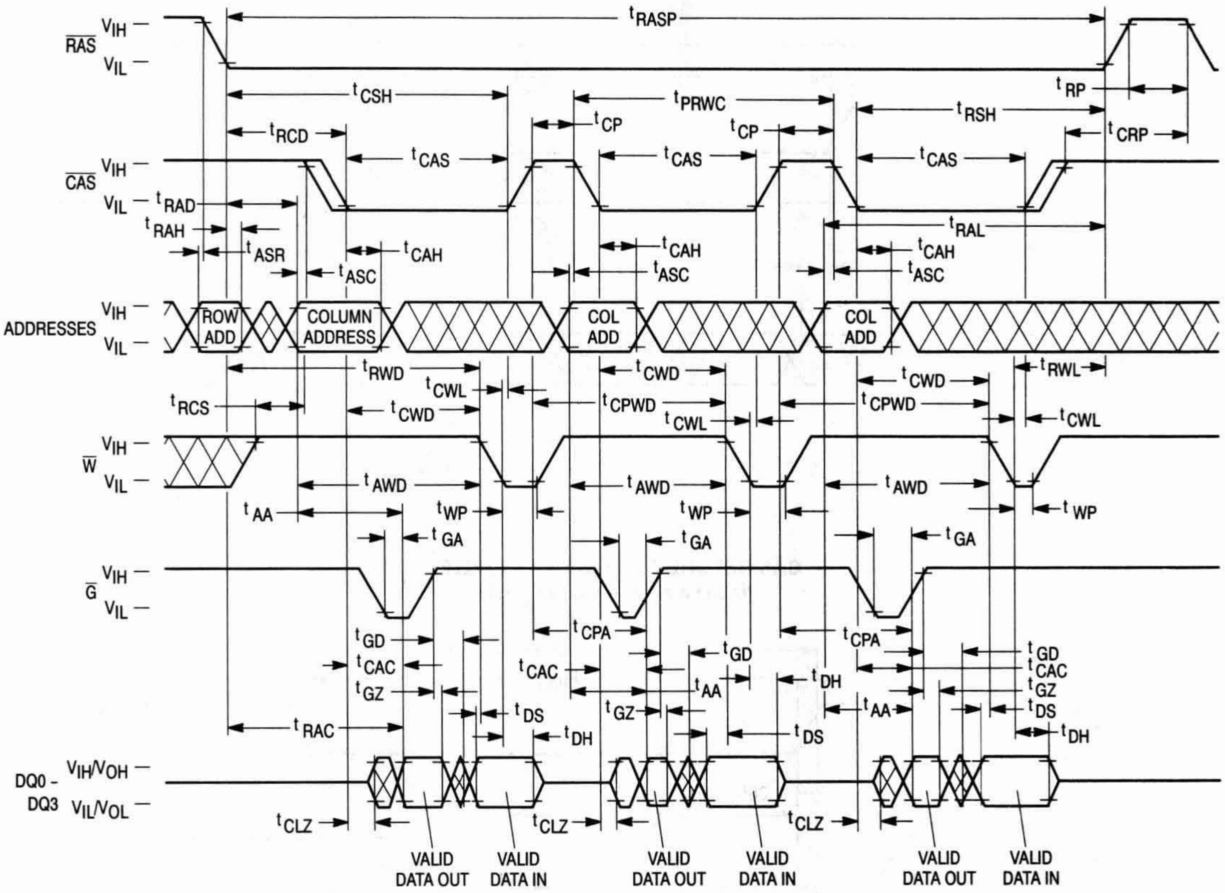
FAST PAGE MODE READ CYCLE


RAS VIH VIL
CAS VIH VIL
ADDRESSES VIH VIL
W VIH VIL
G VIH VIL
DQ0 – DQ3 VOH VOL
tRASP
tRP
tRHCP
tCRP
tPC
tRSH
tRCD
tCP
tCAS
tRAD
tCSH
tRAL
tRAH
tCAH
tASR
tASC
ROW ADD
COLUMN ADDRESS
tRCS
tRCH
tRRH
tAA
tGA
tCAC
tRAC
tOFF
tGZ
tCLZ
VALID DATA OUT

FAST PAGE MODE EARLY WRITE CYCLE

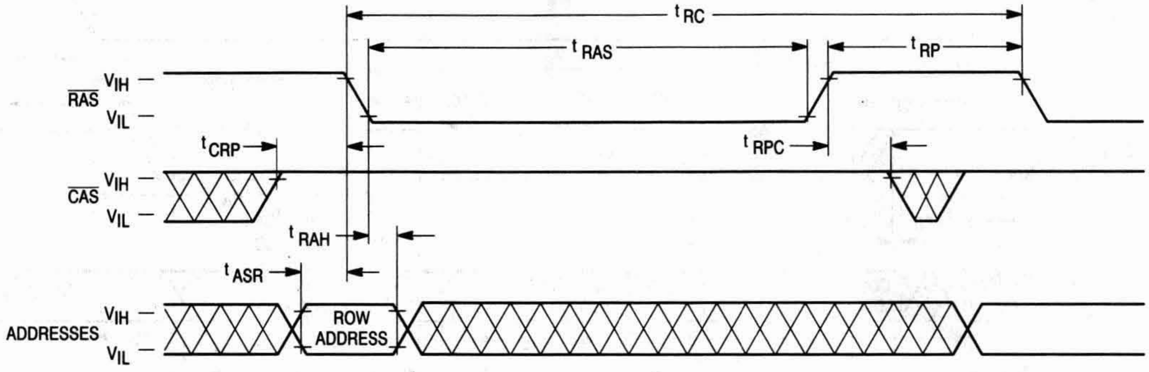

RAS VIH VIL
CAS VIH VIL
ADDRESSES VIH VIL
W VIH VIL
G VIH VIL
DQ0 – DQ3 VIH VIL
tRASP
tRP
tRHCP
tCRP
tPC
tRSH
tRCD
tCP
tCAS
tASR
tCSH
tRAL
tRAH
tCAH
tASC
ROW ADD
COLUMN ADDRESS
tRAD
tCWL
tRWL
tWCS
tWP
tWCH
tDS
tDH
VALID DATA IN

FAST PAGE MODE READ-WRITE CYCLE


RAS VIH
RAS VIL
CAS VIH
CAS VIL
ADDRESSES VIH
ADDRESSES VIL
W VIH
W VIL
G VIH
G VIL
DQ0 - DQ3 VIH/VOH
VIL/VOL
tRASP
tRP
tCRP
tCSH
tPRWC
tRSH
tRCD
tCP
tCAS
tRAD
tRAH
tASR
tCAH
tASC
tRAL
ROW ADD
COLUMN ADDRESS
COL ADD
tRWD
tCWL
tCWD
tCPWD
tRWL
tRCS
tAWD
tAA
tWP
tGA
tGD
tCAC
tGZ
tCPA
tDH
tDS
tRAC
tCLZ
VALID DATA OUT
VALID DATA IN

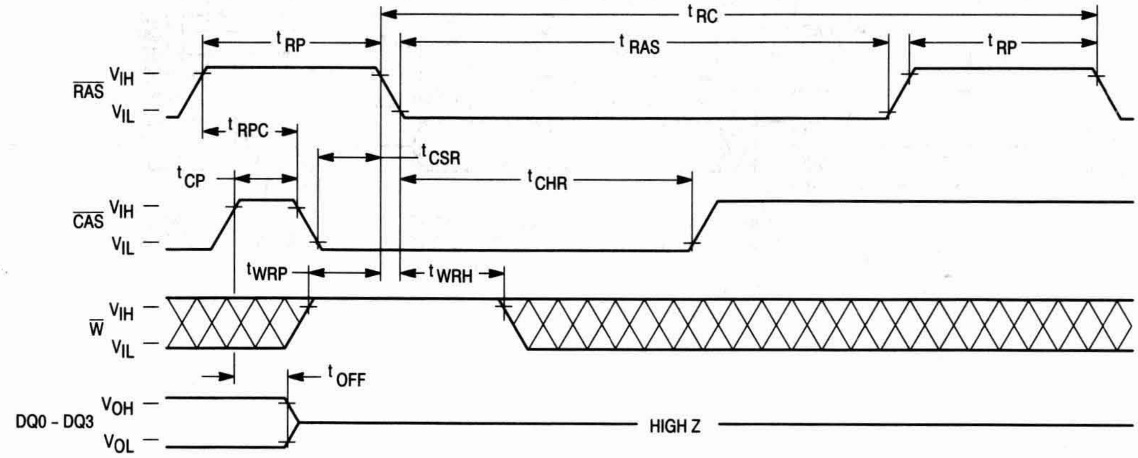
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

($\overline{\text{W}}$ and $\overline{\text{G}}$ are Don't Care)

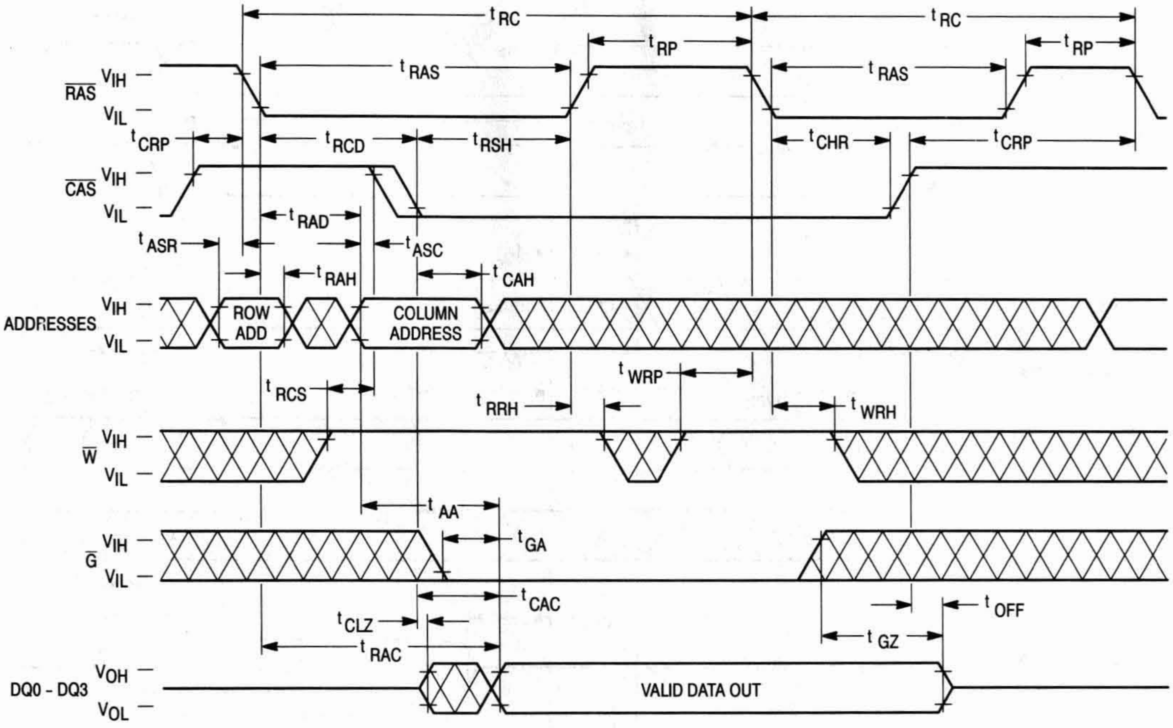

t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$
t_{RAH}
t_{ASR}
ADDRESSES
ROW ADDRESS

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

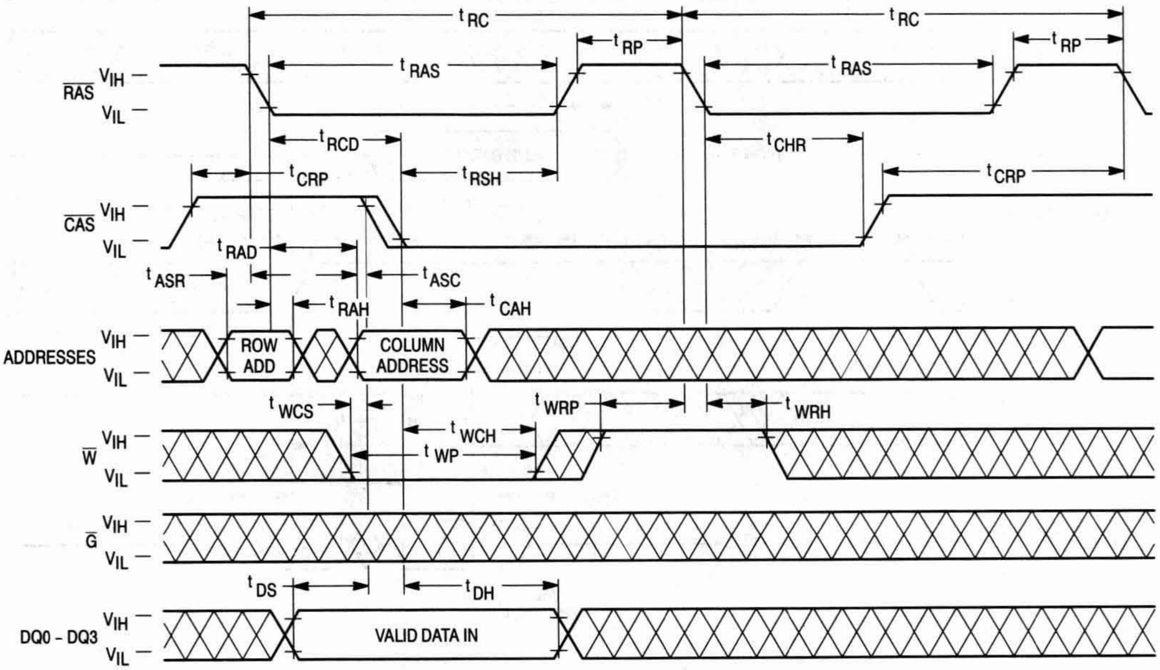
($\overline{\text{G}}$ and A0 – A9 are Don't Care)


t_{RC}
t_{RP}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RPC}
t_{CSR}
t_{CP}
t_{CHR}
$\overline{\text{CAS}}$
t_{WRP}
t_{WRH}
$\overline{\text{W}}$
t_{OFF}
DQ0 - DQ3
V_{OH}
V_{OL}
HIGH Z

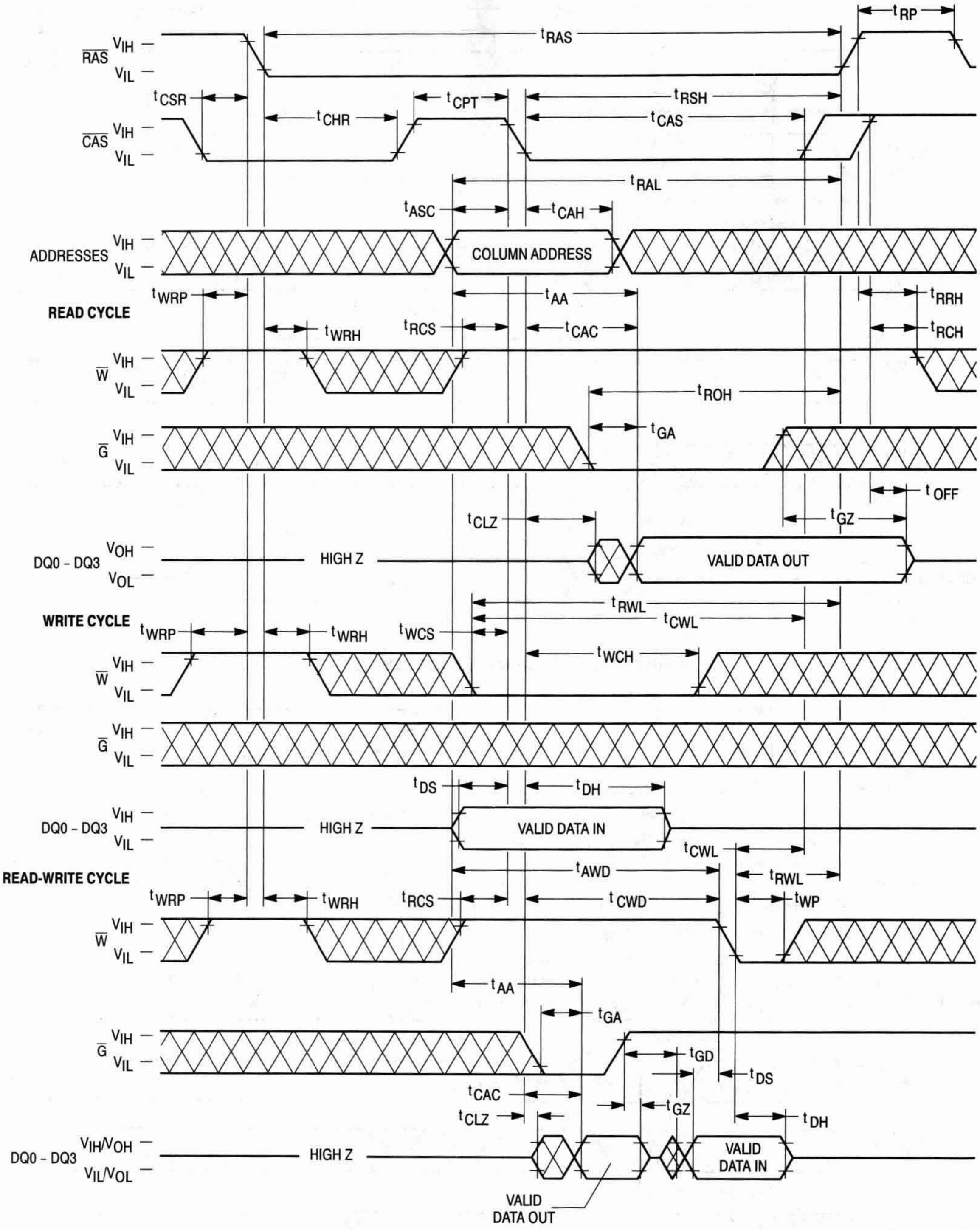
HIDDEN REFRESH CYCLE (READ)


t RC
t RC
t RP
t RP
t RAS
t RAS
RAS
VIH
VIL
t CRP
t RCD
t RSH
t CHR
t CRP
CAS
VIH
VIL
t RAD
t ASR
t ASC
t RAH
t CAH
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
t RCS
t WRP
t RRH
t WRH
W
VIH
VIL
t AA
t GA
G
VIH
VIL
t CAC
t OFF
t CLZ
t GZ
t RAC
DQ0 - DQ3
VOH
VOL
VALID DATA OUT

HIDDEN REFRESH CYCLE (EARLY WRITE)


t RC
t RC
t RP
t RP
t RAS
t RAS
RAS
VIH
VIL
t RCD
t CHR
t CRP
t RSH
t CRP
CAS
VIH
VIL
t RAD
t ASR
t ASC
t RAH
t CAH
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
t WCS
t WRP
t WRH
t WCH
t WP
W
VIH
VIL
G
VIH
VIL
t DS
t DH
DQ0 - DQ3
VIH
VIL
VALID DATA IN

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



tRP
tRAS
RAS VIH
VIL
tCSR
tCPT
tRSH
tCHR
tCAS
CAS VIH
VIL
tRAL
tASC
tCAH
ADDRESSES VIH
VIL
COLUMN ADDRESS
READ CYCLE
tWRP
tAA
tRRH
tWRH
tRCS
tCAC
tRCH
W VIH
VIL
tROH
G VIH
VIL
tGA
tOFF
tCLZ
tGZ
DQ0 - DQ3 VOH
VOL
HIGH Z
VALID DATA OUT
WRITE CYCLE
tRWL
tCWL
tWRP
tWRH
tWCS
tWCH
W VIH
VIL
G VIH
VIL
tDS
tDH
DQ0 - DQ3 VIH
VIL
HIGH Z
VALID DATA IN
tCWL
tAWD
tRWL
READ-WRITE CYCLE
tWRP
tWRH
tRCS
tCWD
tWP
W VIH
VIL
tAA
tGA
G VIH
VIL
tGD
tDS
tCAC
tGZ
tCLZ
tDH
DQ0 - DQ3 VIH/VOH
VIL/VOL
HIGH Z
VALID DATA IN
VALID DATA OUT

3

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds or 128 milliseconds in case of low power device with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the 1M x 4 RAM: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{\text{CAS}}$ and output enable ($\overline{\text{G}}$) control read access time: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum and $\overline{\text{G}}$ must be active t_{RAC}-t_{GA} (both minimum) after $\overline{\text{RAS}}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{\text{G}}$ active transition does not occur in time, read access time is determined by either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ and $\overline{\text{G}}$ clocks are active. When either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers and $\overline{\text{G}}$ disabled.

A late write cycle (referred to as $\overline{\text{G}}$-controlled write) occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but outputs are switched off by $\overline{\text{G}}$ inactive transition, which is required to write to the device. Q may be indeterminate — see note 15 of AC Operating Conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle. $\overline{\text{G}}$ must remain inactive for t_{GH} after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the 1M x 4 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54400A require refresh every 16 milliseconds, while refresh time for the MCM5L4400A is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54400A, and 124.8 microseconds for the MCM5L4400A. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54400A and 128 milliseconds on the MCM5L4400A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decodes. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{\text{RAS}}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode entry) as in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0" into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

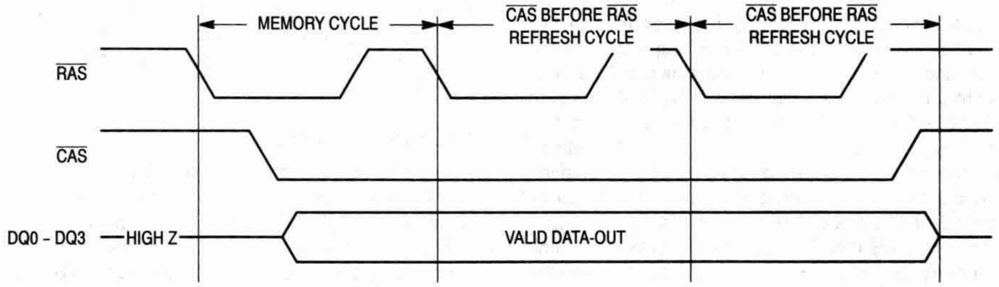


Figure 1. Hidden Refresh Cycle

TEST MODE

The internal organization of this device (512K x 8) allows it to be tested as if it were a 512K x 4 DRAM. Nineteen of the twenty addresses are used when operating the device in test mode. Column address A0 is ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0 – B7) in parallel. External data out is determined by the internal test mode logic of the device. See following truth table and test mode block diagram.

$\overline{\text{W}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ timing puts the device in **Test Mode** as shown in the test mode timing diagram. A **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** or a **$\overline{\text{RAS}}$-only refresh cycle** puts the device back into normal mode. Refresh is performed in test mode by using a **$\overline{\text{W}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle** which uses internal refresh address counter.

TEST MODE TRUTH TABLE

D	B0, B1	B2, B3	B4, B5	B6, B7	Q
0	0	0	0	0	1
1	1	1	1	1	1
—	Any Other				0

TEST MODE
AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

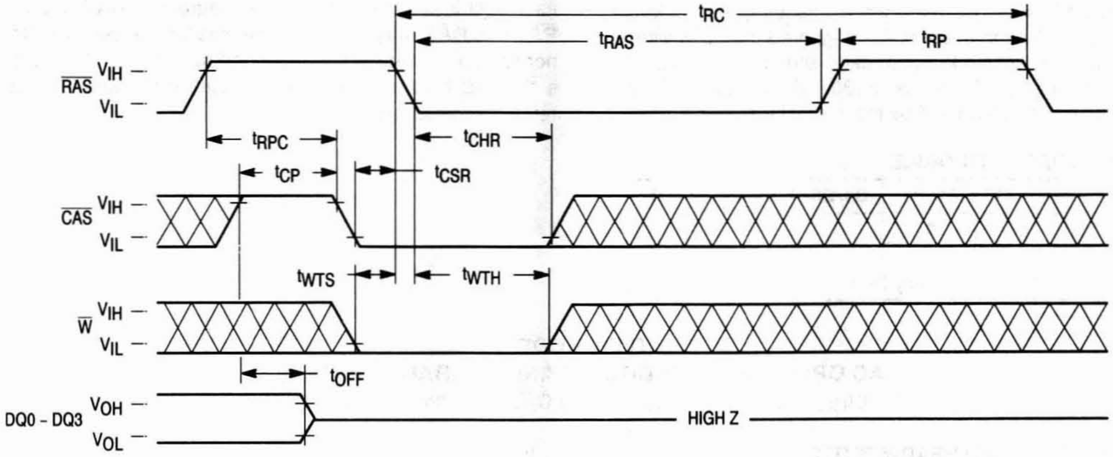
Parameter	Symbol		54400A-60 5L4400A-60		54400A-70 5L4400A-70		54400A-80 5L4400A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	115	—	135	—	155	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	—	50	—	55	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	65	—	75	—	85	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	25	—	25	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	45	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	45	—	45	—	50	ns	6
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	65	10 k	75	10 k	85	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	65	200 k	75	200 k	85	200 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	25	—	25	—	25	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	65	—	75	—	85	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	45	—	45	—	50	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	25	10 k	25	10 k	25	10 k	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	45	—	ns	

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).

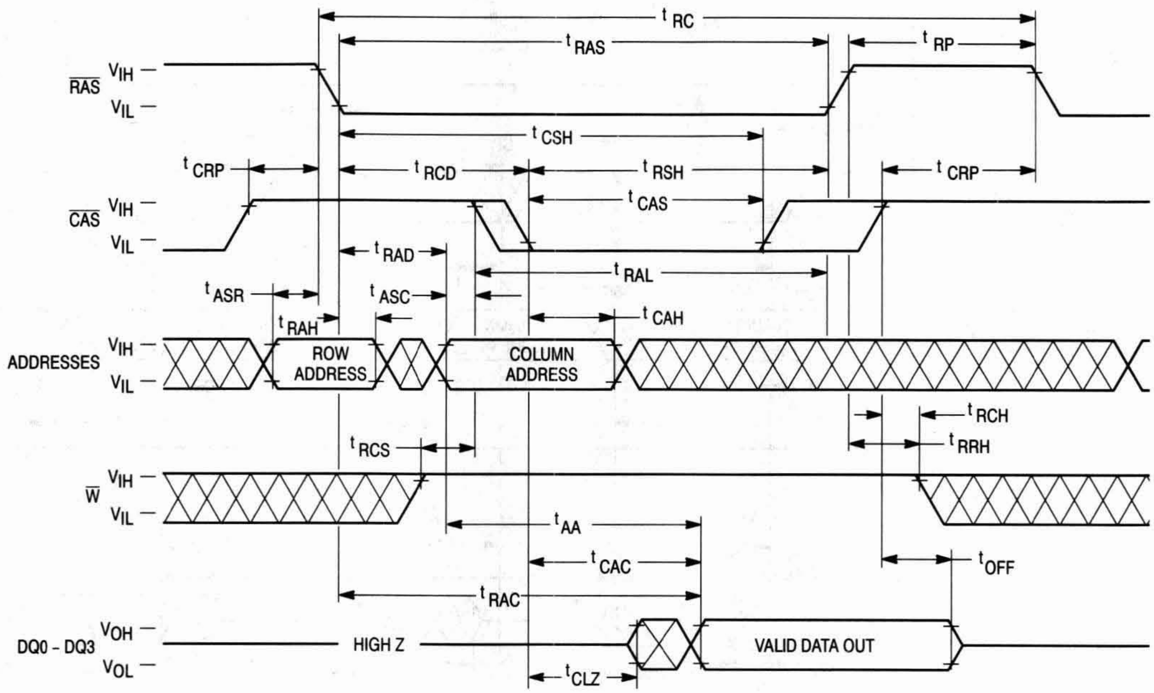
$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE (TEST MODE ENTRY)

($\overline{\text{G}}$ and A0 – A9 are Don't Care)

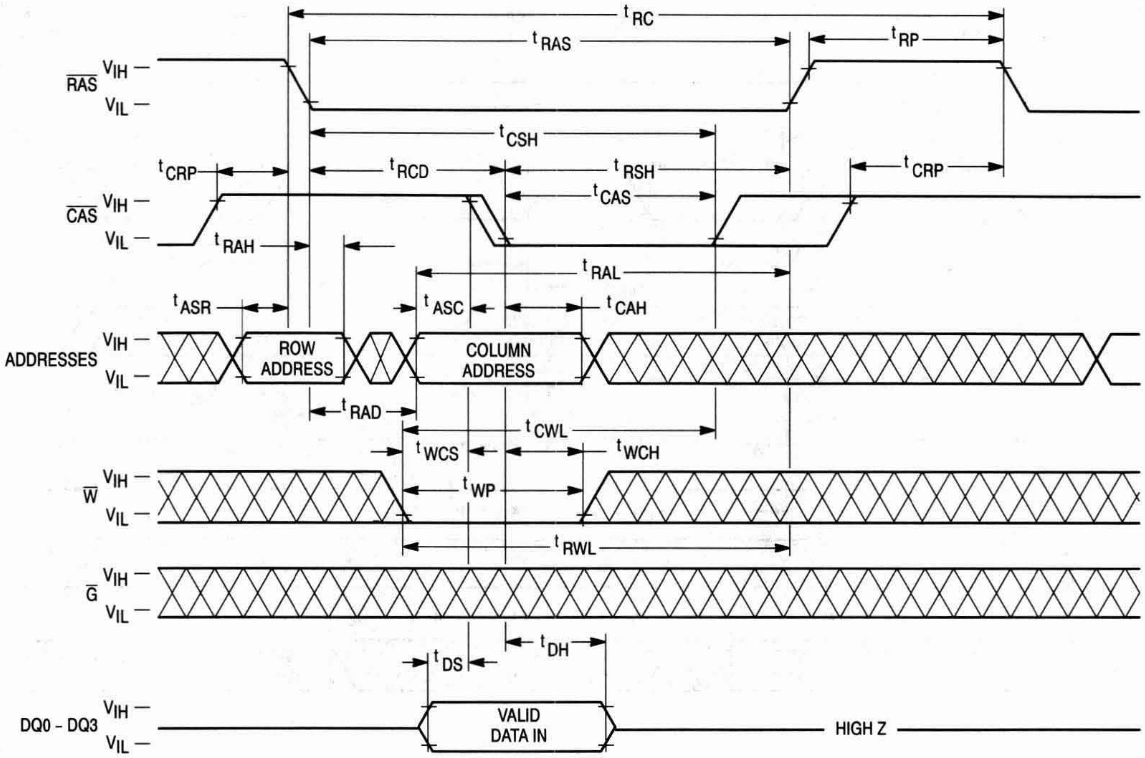

t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RPC}
t_{CHR}
t_{CP}
t_{CSR}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{WTS}
t_{WTH}
$\overline{W}$
V_{IH}
V_{IL}
t_{OFF}
DQ0 - DQ3
V_{OH}
V_{OL}
HIGH Z

TEST MODE — READ CYCLE

($\overline{G}$ = Low)

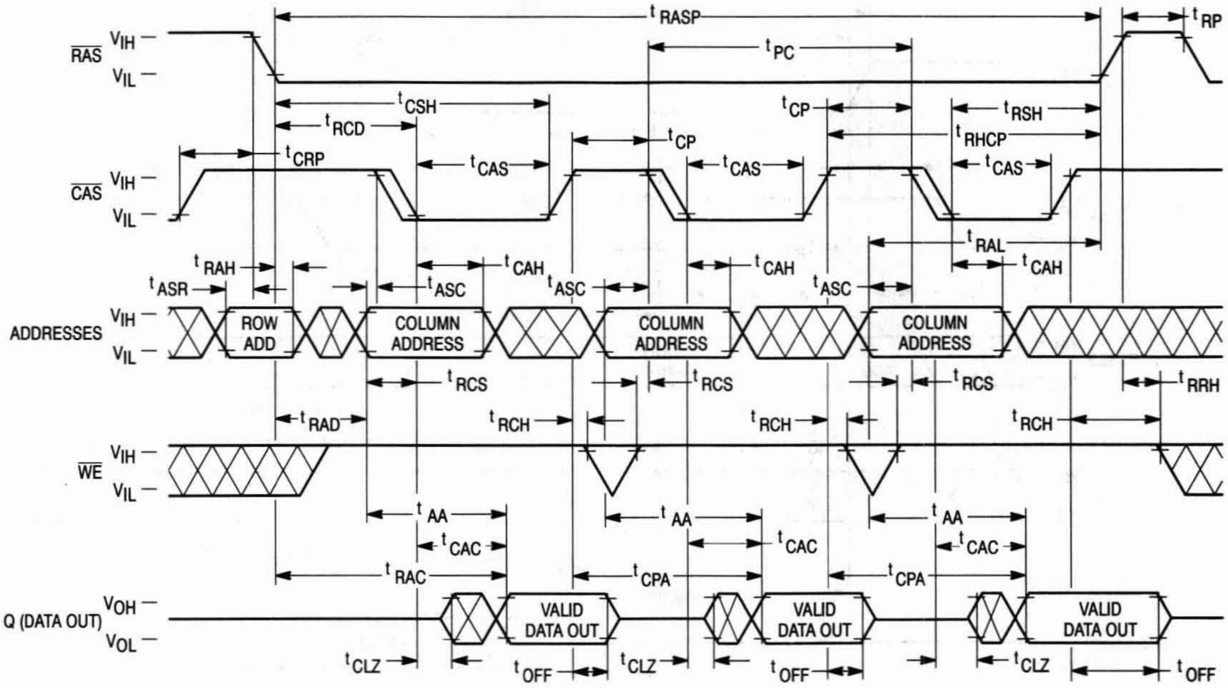

t RC
t RAS
t RP
RAS
VIH
VIL
t CSH
t CRP
t RCD
t RSH
t CRP
t CAS
CAS
VIH
VIL
t RAD
t RAL
t ASR
t ASC
t RAH
t CAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
t RCH
t RRH
t RCS
W
VIH
VIL
t AA
t CAC
t OFF
t RAC
DQ0 - DQ3
VOH
VOL
HIGH Z
VALID DATA OUT
t CLZ

TEST MODE — EARLY WRITE CYCLE


t RC
t RAS
t RP
RAS
VIH
VIL
t CSH
t CRP
t RCD
t RSH
t CRP
t CAS
CAS
VIH
VIL
t RAH
t RAL
t ASR
t ASC
t CAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
t RAD
t CWL
t WCS
t WCH
t WP
W
VIH
VIL
t RWL
G
VIH
VIL
t DH
t DS
DQ0 - DQ3
VIH
VIL
VALID DATA IN
HIGH Z

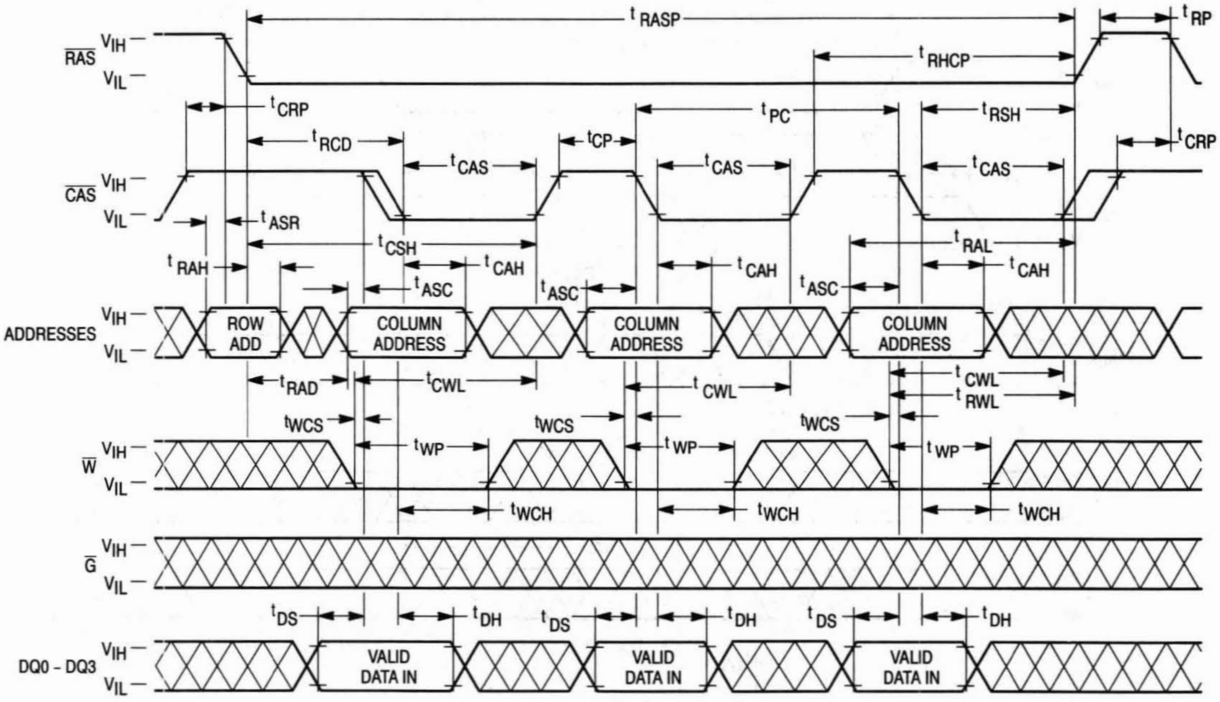
TEST MODE — FAST PAGE MODE READ CYCLE

($\overline{G}$ = Low)



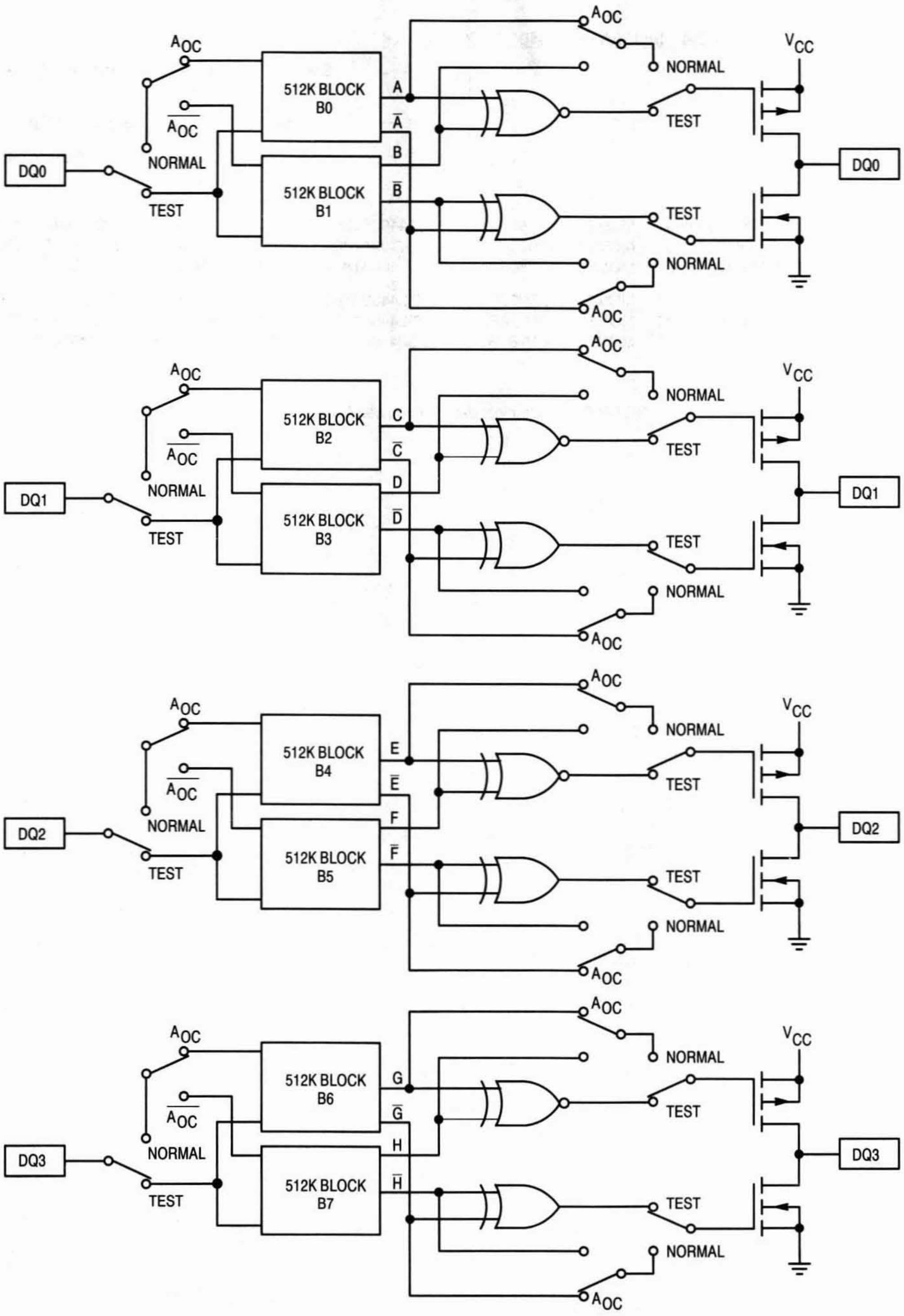
RAS
VIH
VIL
CAS
ADDRESSES
WE
Q (DATA OUT)
VOH
VOL
ROW ADD
COLUMN ADDRESS
VALID DATA OUT
tRASP
tRP
tPC
tCSH
tRCD
tCRP
tCP
tRSH
tRHCP
tCAS
tRAL
tRAH
tASR
tCAH
tASC
tRCS
tRRH
tRAD
tRCH
tAA
tCAC
tRAC
tCPA
tCLZ
tOFF

TEST MODE — FAST PAGE MODE EARLY WRITE CYCLE



RAS
VIH
VIL
CAS
ADDRESSES
W
G
DQ0 - DQ3
ROW ADD
COLUMN ADDRESS
VALID DATA IN
tRASP
tRP
tRHCP
tCRP
tPC
tRSH
tRCD
tCP
tCAS
tASR
tCSH
tRAL
tRAH
tCAH
tASC
tRAD
tCWL
tRWL
tWCS
tWP
tWCH
tDS
tDH

TEST MODE BLOCK DIAGRAM



A_{OC}
$\overline{A_{OC}}$
NORMAL
TEST
DQ0
512K BLOCK B0
512K BLOCK B1
A
$\overline{A}$
B
$\overline{B}$
V_{CC}
DQ1
512K BLOCK B2
512K BLOCK B3
C
$\overline{C}$
D
$\overline{D}$
DQ2
512K BLOCK B4
512K BLOCK B5
E
$\overline{E}$
F
$\overline{F}$
DQ3
512K BLOCK B6
512K BLOCK B7
G
$\overline{G}$
H
$\overline{H}$

ORDERING INFORMATION

(Order by Full Part Number)

MCM 54400A or 5L4400A X XX XX

Motorola Memory Prefix

Part Number

Shipping Method (R2 = Tape and Reel, Blank = Rails for SOJ, ZIP, and Trays for TSOP)

Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns)

Package (N = 300 mil SOJ, Z = 100 mil Plastic ZIP, T = 300 mil TSOP)

Full Part Numbers —	MCM54400AN60	MCM54400AN60R2	MCM54400AT60	MCM54400AT60R2	MCM54400AZ60
	MCM54400AN70	MCM54400AN70R2	MCM54400AT70	MCM54400AT70R2	MCM54400AZ70
	MCM54400AN80	MCM54400AN80R2	MCM54400AT80	MCM54400AT80R2	MCM54400AZ80
	MCM5L4400AN60	MCM5L4400AN60R2	MCM5L4400AT60	MCM5L4400AT60R2	MCM5L4400AZ60
	MCM5L4400AN70	MCM5L4400AN70R2	MCM5L4400AT70	MCM5L4400AT70R2	MCM5L4400AZ70
	MCM5L4400AN80	MCM5L4400AN80R2	MCM5L4400AT80	MCM5L4400AT80R2	MCM5L4400AZ80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM54400A-C

Advance Information

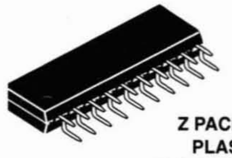
1M x 4 CMOS Dynamic RAM
Fast Page Mode
Operating Temperature – 40°C to + 85°C

The MCM54400A is a 0.7µ CMOS high-speed dynamic random access memory. It is organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM54400A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in standard 300 mil small outline J-lead (SOJ) and 100 mil zig-zag in-line (ZIP) package.

- Three-State Data Output
- Fast Page Mode
- Test Mode
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM54400A-C = 16 ms
- Fast Access Time (t_{RAC}): MCM54400A-C70 = 70 ns (Max)
  MCM54400A-C80 = 80 ns (Max)
- Low Active Power: MCM54400A-C70 = 550 mW (Max)
  MCM54400A-C80 = 468 mW (Max)
- Low Standby Power Dissipation:
  MCM54400A-C = 11 mW (Max, TTL Levels)
  = 5.5 mW (Max, CMOS Levels)

N PACKAGE
300 MIL SOJ
CASE 822-03



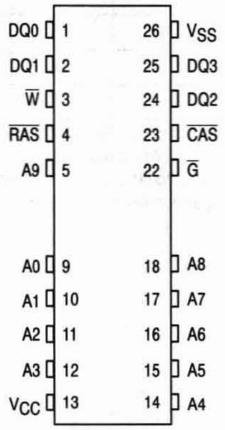
Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836-02

PIN NAMES

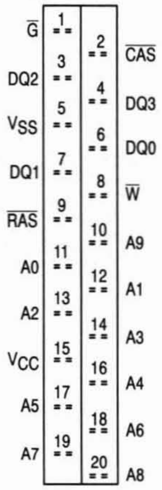
A0 – A9	Address Input
DQ0 – DQ3	Data Input/Output
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

PIN ASSIGNMENTS

300 MIL SOJ

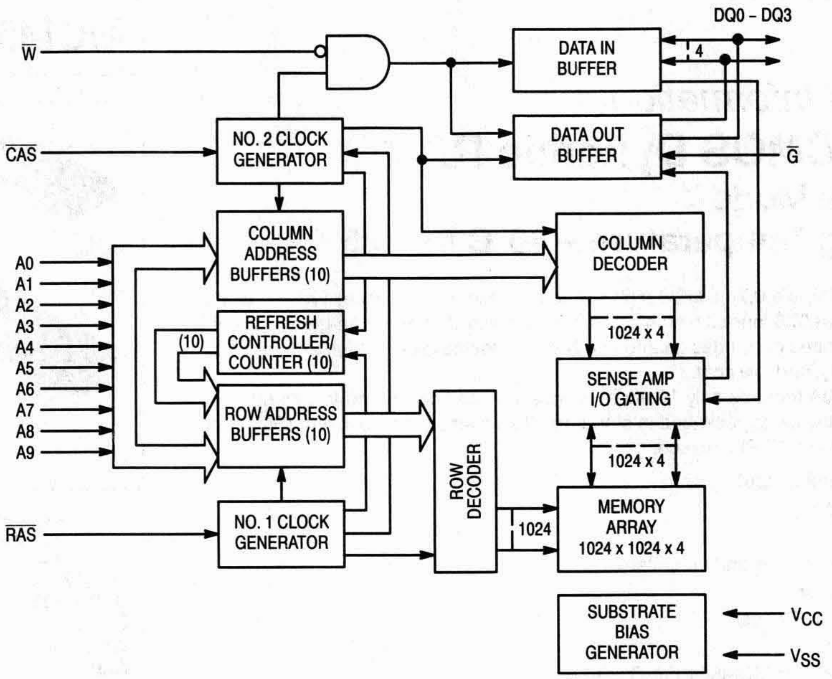

DQ0 1
DQ1 2
W 3
RAS 4
A9 5
A0 9
A1 10
A2 11
A3 12
VCC 13
26 VSS
25 DQ3
24 DQ2
23 CAS
22 G
18 A8
17 A7
16 A6
15 A5
14 A4

100 MIL ZIP


G 1
2 CAS
DQ2 3
4 DQ3
VSS 5
6 DQ0
DQ1 7
8 W
RAS 9
10 A9
A0 11
12 A1
A2 13
14 A3
VCC 15
16 A4
A5 17
18 A6
A7 19
20 A8

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM


DQ0 - DQ3
$\overline{W}$
DATA IN BUFFER
4
DATA OUT BUFFER
$\overline{G}$
$\overline{CAS}$
NO. 2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (10)
COLUMN DECODER
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
(10)
REFRESH CONTROLLER/ COUNTER (10)
ROW ADDRESS BUFFERS (10)
1024 x 4
SENSE AMP I/O GATING
1024 x 4
ROW DECODER
$\overline{RAS}$
NO. 1 CLOCK GENERATOR
1024
MEMORY ARRAY 1024 x 1024 x 4
SUBSTRATE BIAS GENERATOR
V_{CC}
V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM54400A-C70, t_{RC} = 130 ns MCM54400A-C80, t_{RC} = 150 ns	I_{CC1}	— —	100 85	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles ($\overline{CAS}$ = V_{IH}) MCM54400A-C70, t_{RC} = 130 ns MCM54400A-C80, t_{RC} = 150 ns	I_{CC3}	— —	100 85	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL}) MCM54400A-C70, t_{PC} = 45 ns MCM54400A-C80, t_{PC} = 50 ns	I_{CC4}	— —	70 60	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} – 0.2 V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM54400A-C70, t_{RC} = 130 ns MCM54400A-C80, t_{RC} = 150 ns	I_{CC6}	— —	100 85	mA	3
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery-back up. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A9	C_{in}	5	pF
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0 – DQ3	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM54400A-C70		MCM54400A-C80		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	185	—	205	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	50	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	100	—	105	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	40	—	45	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	200,000	80	200,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	45	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) and/or t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

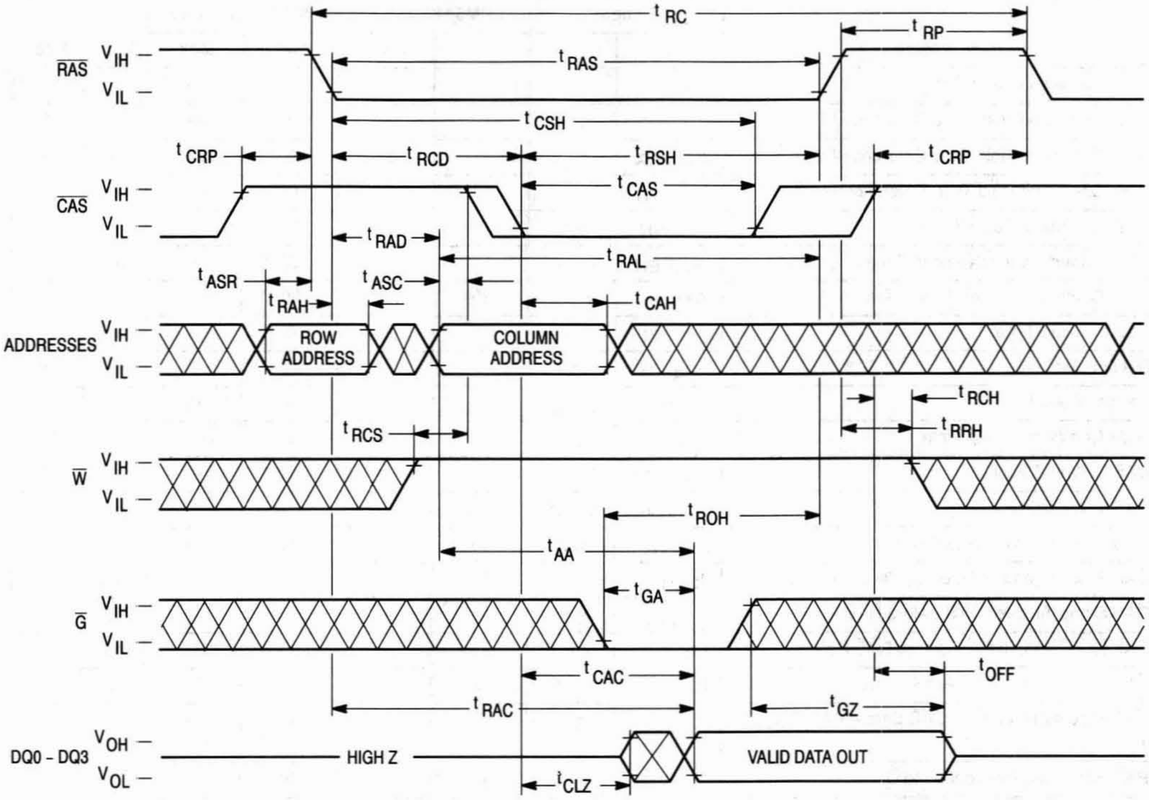
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM54400A-C70		MCM54400A-C80		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14
Refresh Period	t_{RVRV}	t_{RFSH}	—	16	—	16	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	ns	15
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	100	—	110	—	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	65	—	70	—	ns	15
$\overline{\text{CAS}}$ Precharge to Write Delay Time (Page Mode)	t_{CEHWL}	t_{CPWD}	70	—	75	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	ns	
$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{G}}$	t_{GLREH}	t_{ROH}	10	—	10	—	ns	
$\overline{\text{G}}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	20	ns	
$\overline{\text{G}}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{\text{G}}$	t_{GHQZ}	t_{GZ}	0	20	0	20	ns	10
$\overline{\text{G}}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	ns	

NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in late write or read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE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RAS
VIH
VIL
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tCRP
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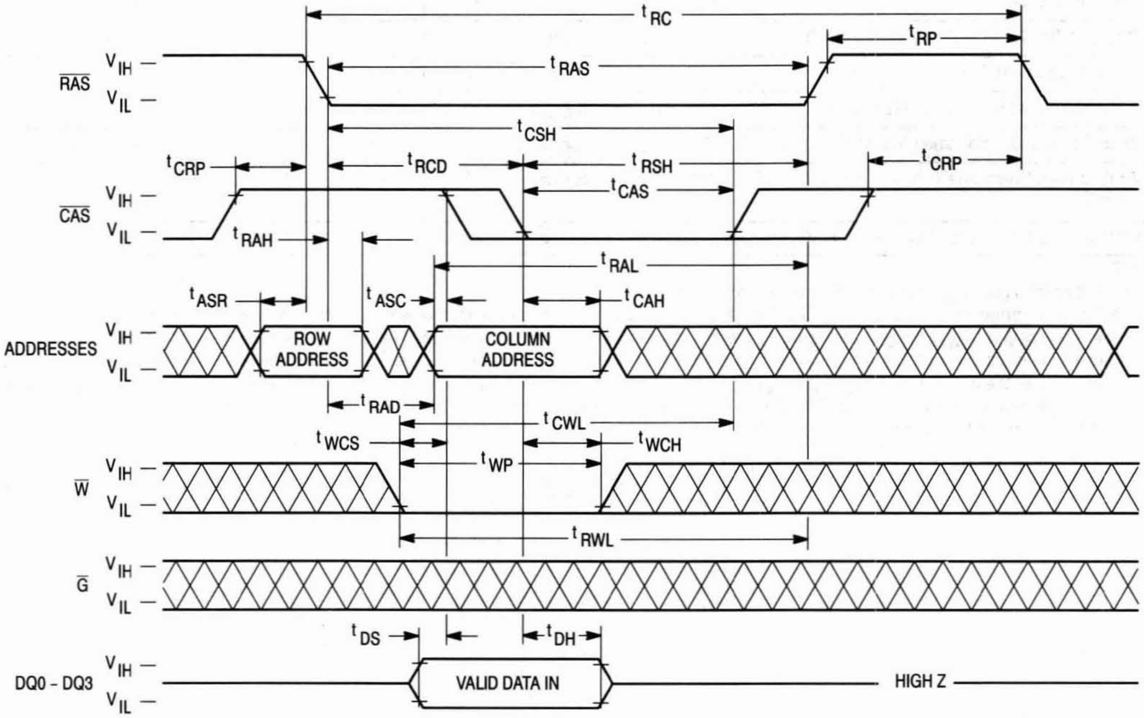
tCRP
CAS
VIH
VIL
tCAS
tRAD
tRAL
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRCH
tRCS
tRRH
W
VIH
VIL
tROH
tAA
G
VIH
VIL
tGA
tCAC
tOFF
tRAC
tGZ
DQ0 – DQ3
VOH
VOL
HIGH Z
VALID DATA OUT
tCLZ

EARLY WRITE CYCLE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tCRP
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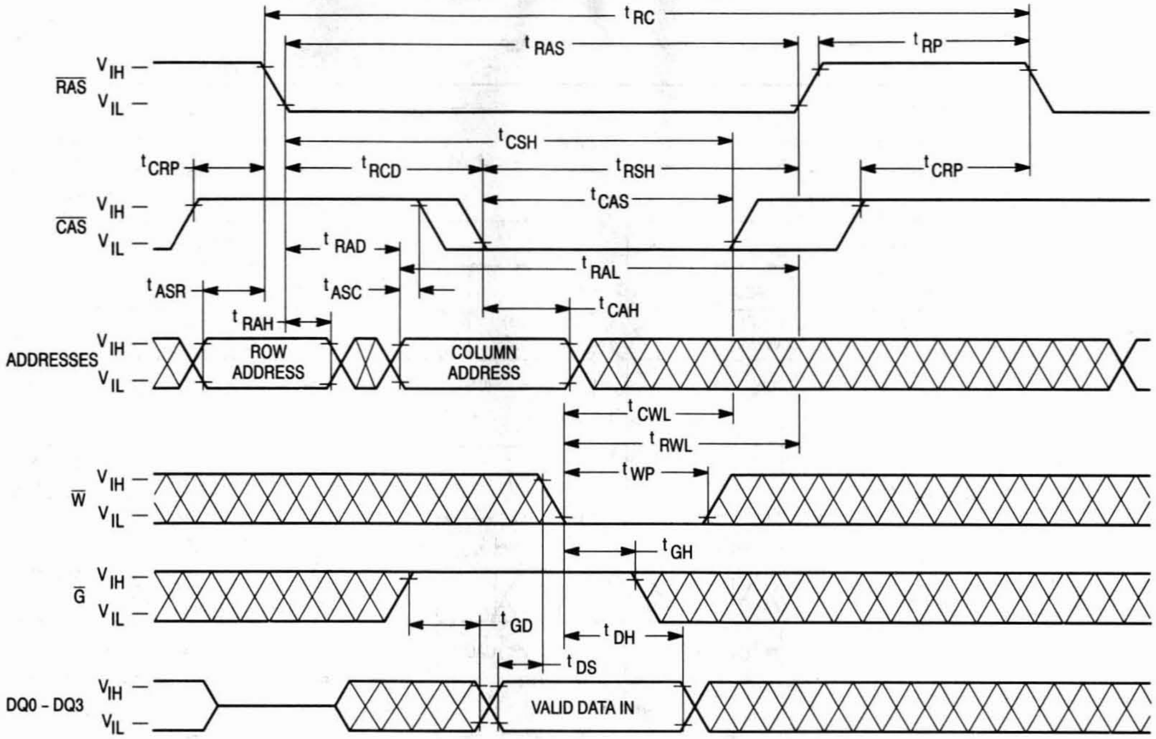
VIH
VIL
tCAS
tRAH
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAD
tCWL
tWCS
tWCH
tWP
W
VIH
VIL
tRWL
G
VIH
VIL
tDS
tDH
DQ0 – DQ3
VIH
VIL
VALID DATA IN
HIGH Z

$\overline{G}$ CONTROLLED WRITE CYCLE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VIH
VIL
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tCRP
tCAS
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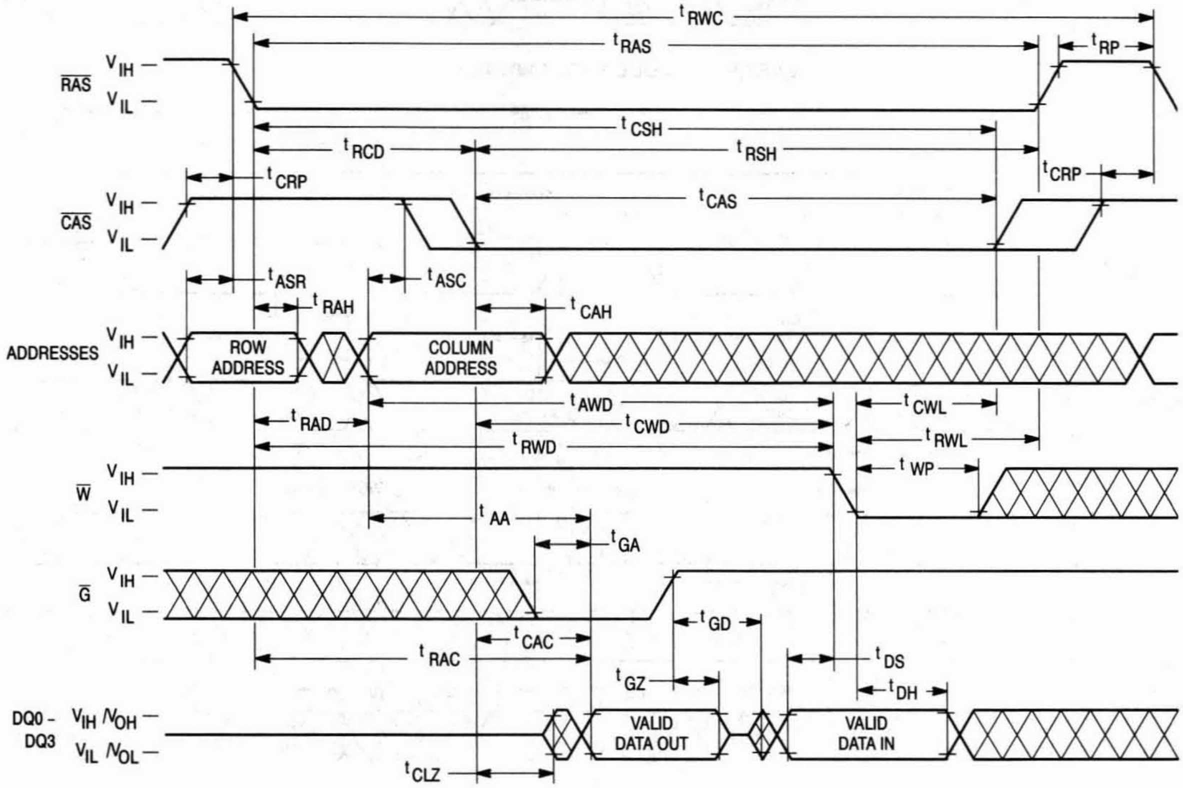
VIH
VIL
tRAD
tRAL
tASR
tASC
tCAH
tRAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tCWL
tRWL
tWP
$\overline{W}$
VIH
VIL
tGH
$\overline{G}$
VIH
VIL
tGD
tDH
tDS
DQ0 - DQ3
VIH
VIL
VALID DATA IN

READ-WRITE CYCLE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VIH
VIL
tCSH
tRCD
tRSH
tCRP
tCRP
tCAS
$\overline{CAS}$
VIH
VIL
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tAWD
tRAD
tCWD
tCWL
tRWD
tRWL
tWP
$\overline{W}$
VIH
VIL
tAA
tGA
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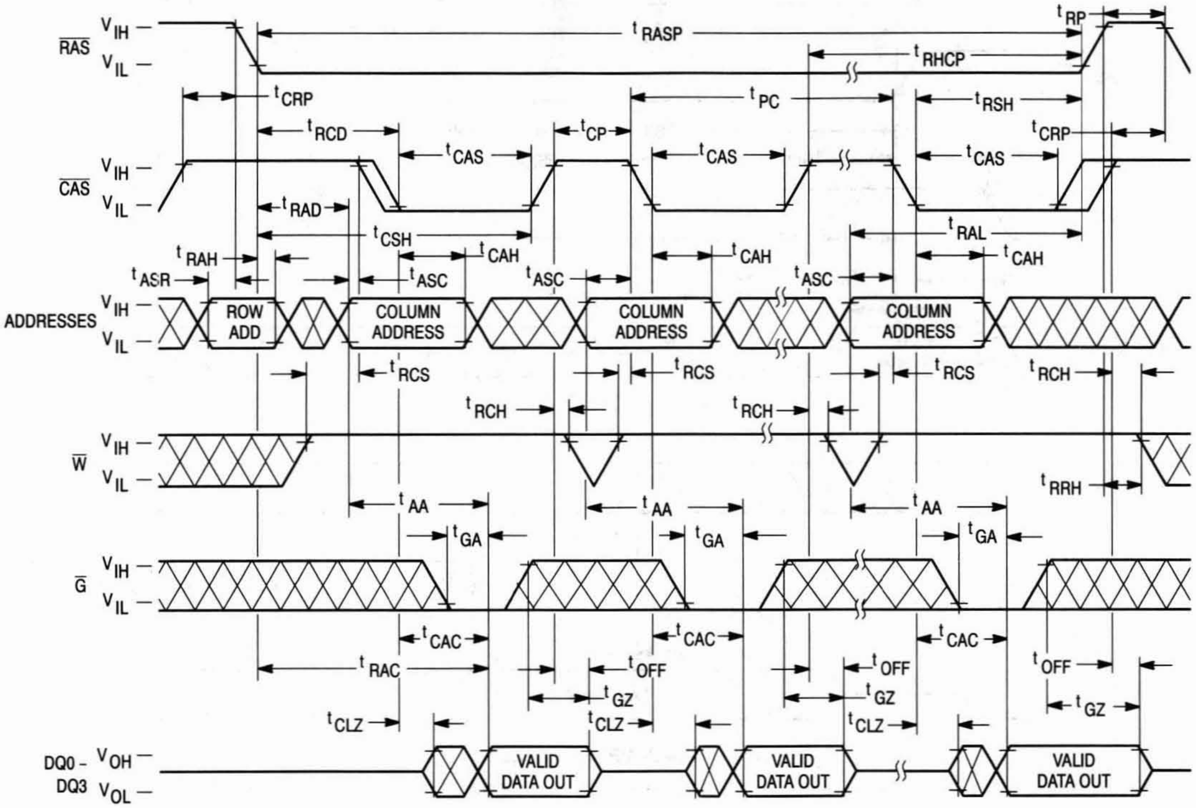
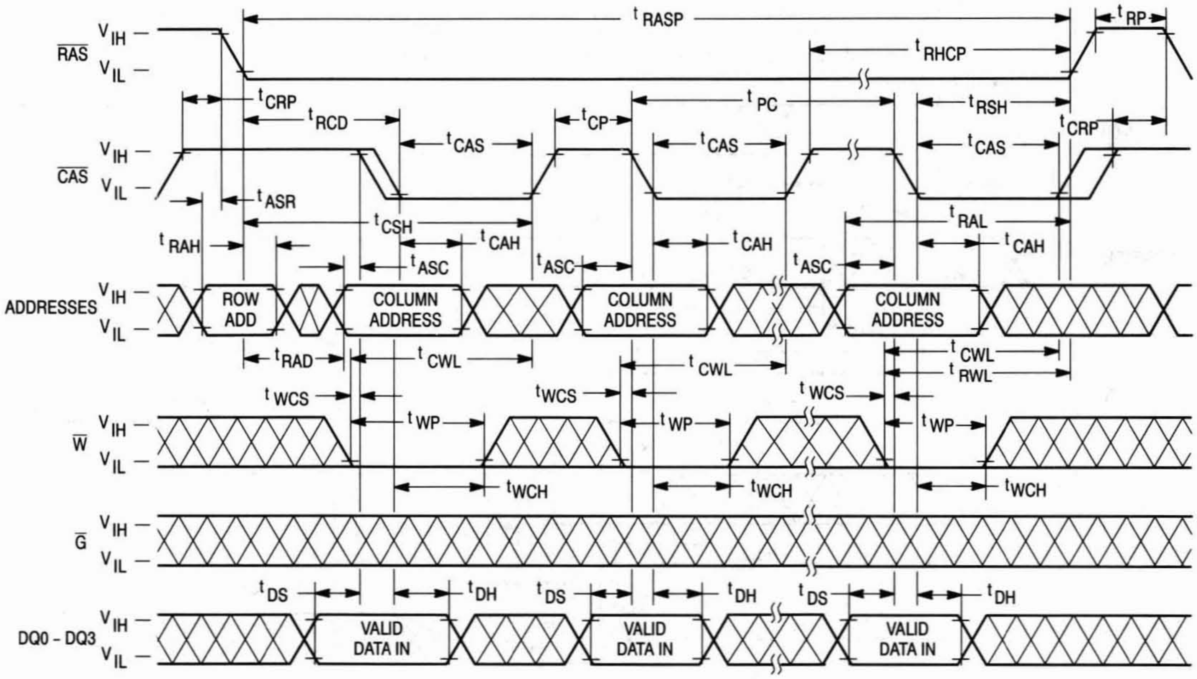
VIH
VIL
tGD
tCAC
tRAC
tDS
tGZ
tDH
DQ0 - DQ3
VIH /VOH
VIL /VOL
VALID DATA OUT
VALID DATA IN
tCLZ

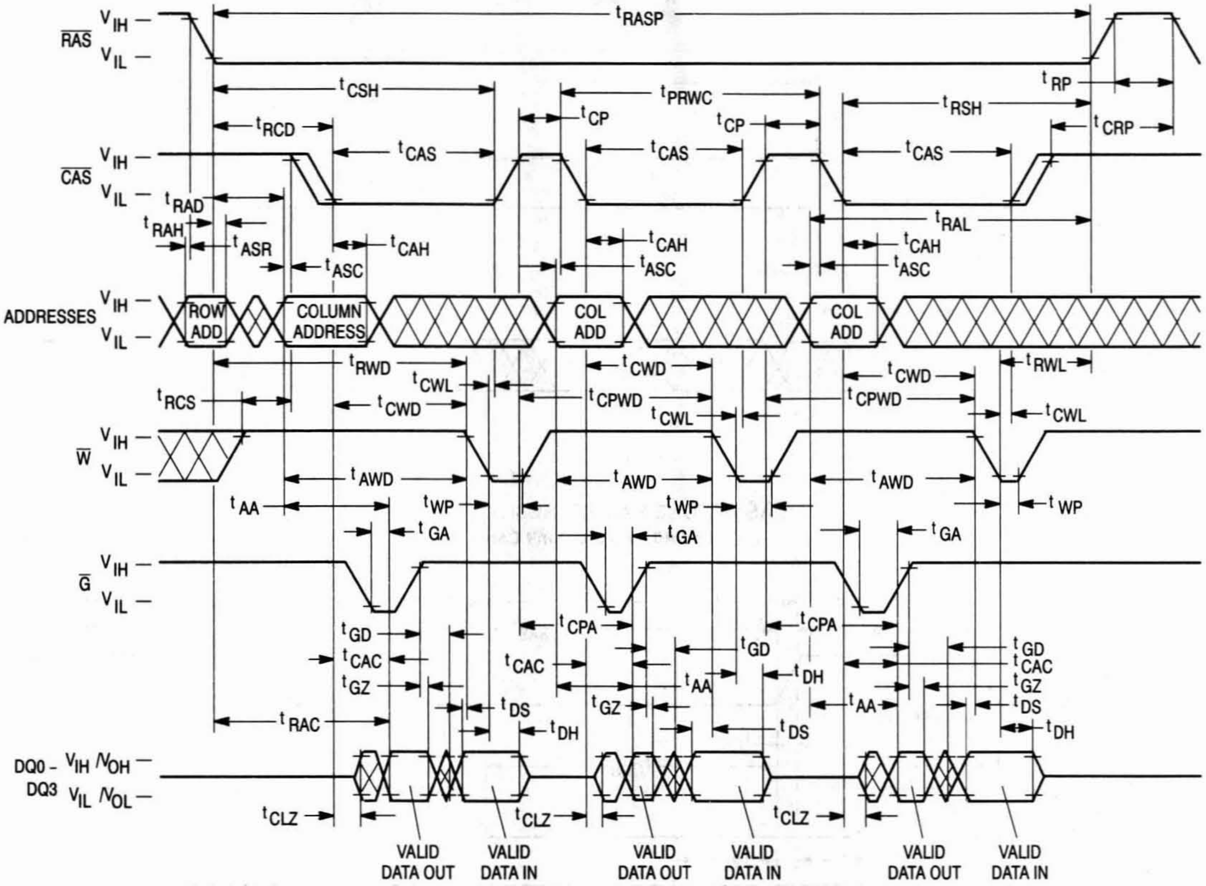
FAST PAGE MODE READ CYCLE


RAS
CAS
ADDRESSES
W
G
DQ0 – DQ3
VIH
VIL
VOH
VOL
tRASP
tRP
tRHCP
tCRP
tRCD
tPC
tRSH
tCP
tCAS
tRAD
tCSH
tRAL
tRAH
tASR
tASC
tCAH
ROW ADD
COLUMN ADDRESS
tRCS
tRCH
tRRH
tAA
tGA
tCAC
tRAC
tOFF
tGZ
tCLZ
VALID DATA OUT

FAST PAGE MODE EARLY WRITE CYCLE

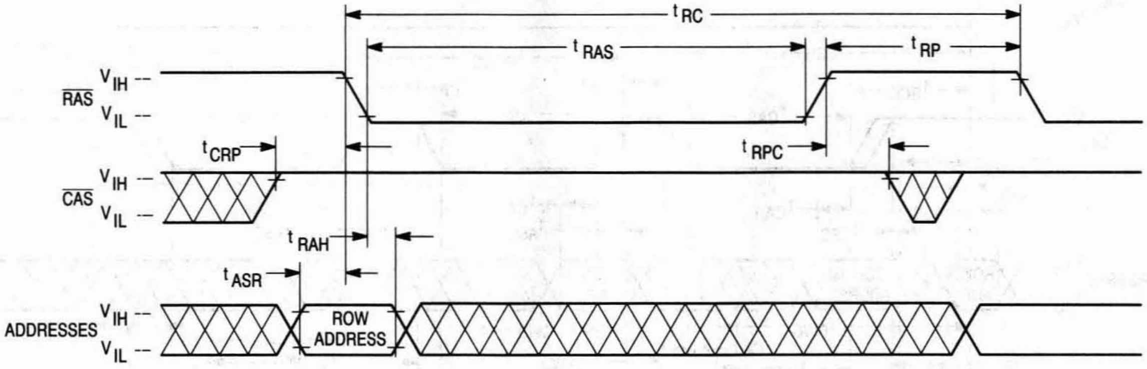

RAS
CAS
ADDRESSES
W
G
DQ0 – DQ3
VIH
VIL
tRASP
tRP
tRHCP
tCRP
tRCD
tPC
tRSH
tCP
tCAS
tASR
tCSH
tRAH
tCAH
tASC
tRAL
ROW ADD
COLUMN ADDRESS
tRAD
tCWL
tRWL
tWCS
tWP
tWCH
tDS
tDH
VALID DATA IN

FAST PAGE MODE READ-WRITE CYCLE


RAS
VIH
VIL
CAS
ADDRESSES
W
G
DQ0 - DQ3
VIH /VOH
VIL /VOL
tRASP
tCSH
tPRWC
tRSH
tRP
tRCD
tCP
tCRP
tCAS
tRAD
tRAH
tASR
tASC
tCAH
tRAL
ROW ADD
COLUMN ADDRESS
COL ADD
tRWD
tCWL
tCWD
tCPWD
tRWL
tRCS
tAWD
tAA
tWP
tGA
tCPA
tGD
tCAC
tGZ
tDS
tDH
tRAC
tCLZ
VALID DATA OUT
VALID DATA IN

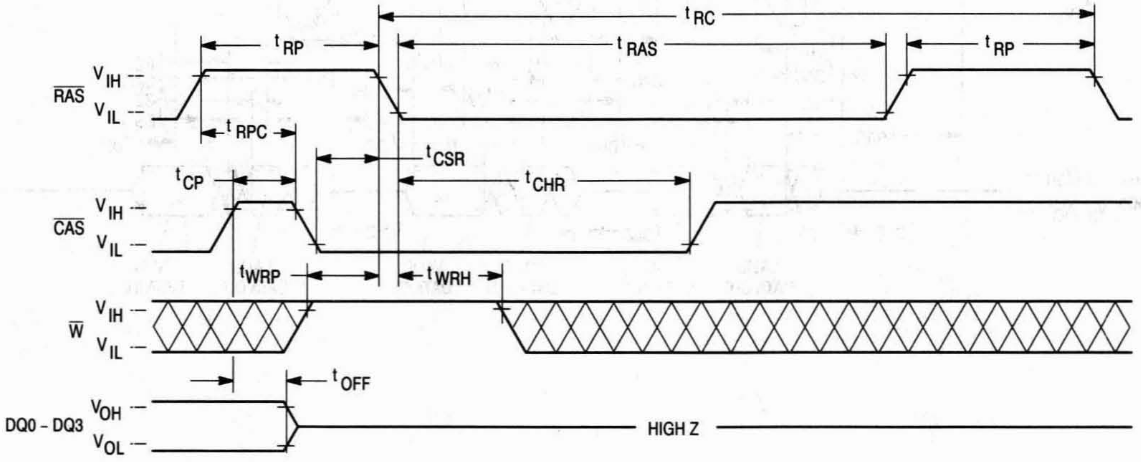
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

($\overline{\text{W}}$ and $\overline{\text{G}}$ are Don't Care)

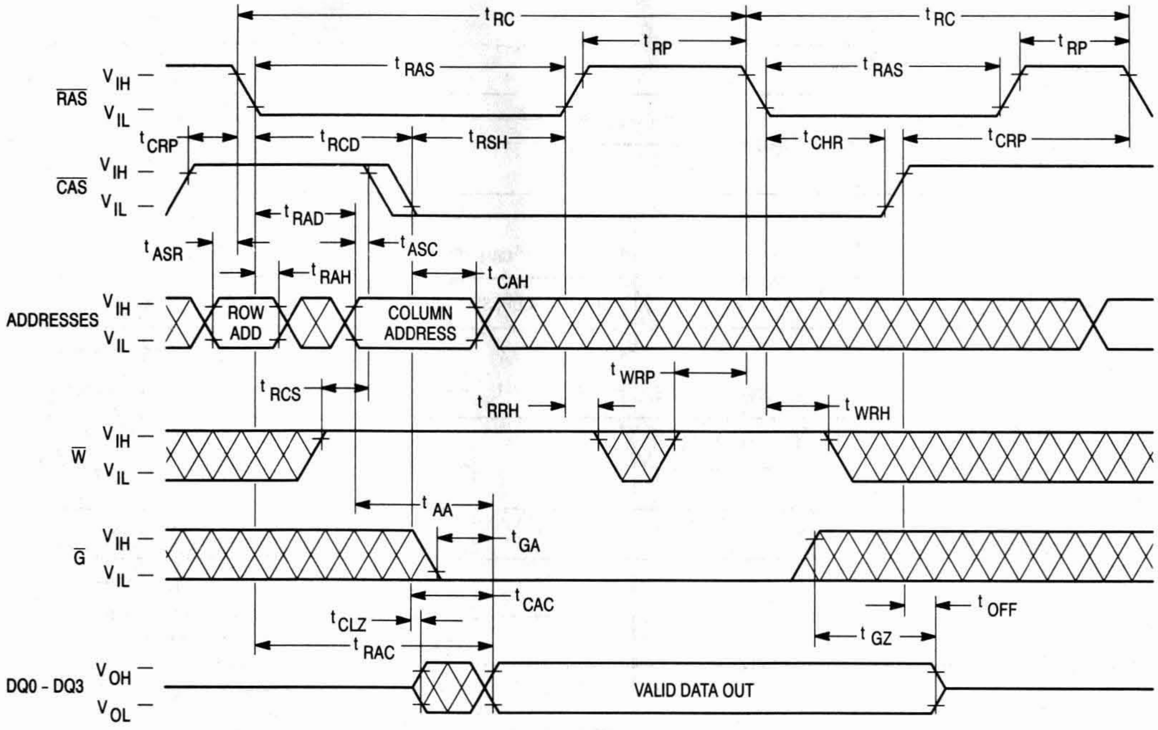

t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

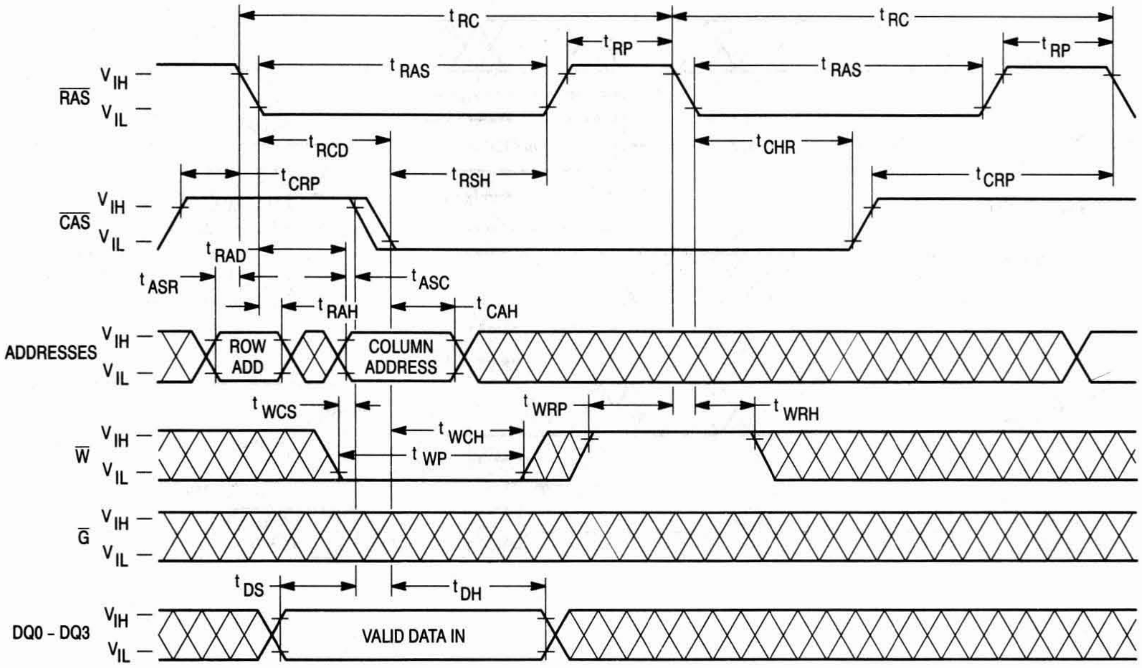
($\overline{\text{G}}$ and A0 – A9 are Don't Care)


t_{RC}
t_{RP}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RPC}
t_{CSR}
t_{CP}
t_{CHR}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{WRP}
t_{WRH}
$\overline{\text{W}}$
V_{IH}
V_{IL}
t_{OFF}
DQ0 – DQ3
V_{OH}
V_{OL}
HIGH Z

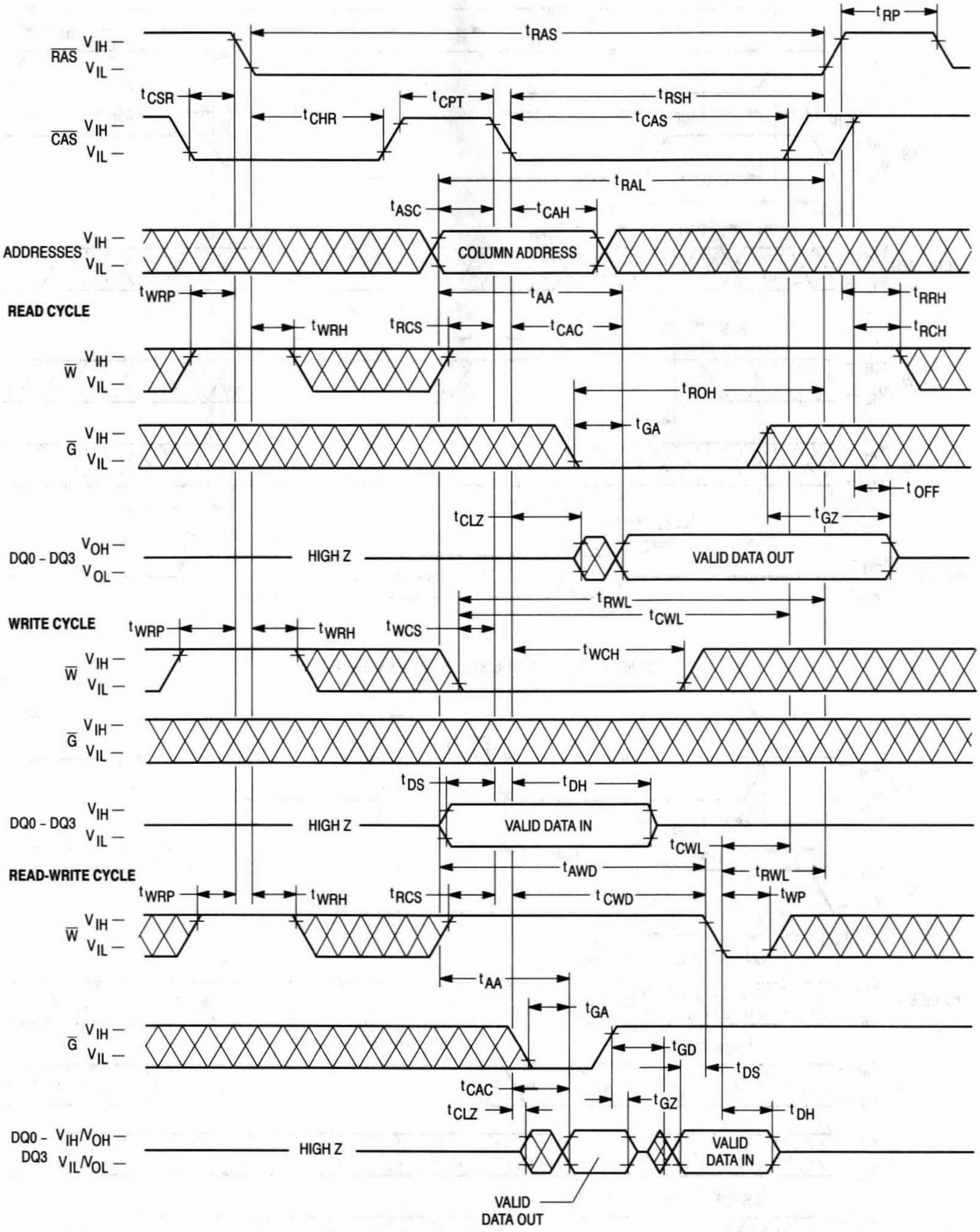
HIDDEN REFRESH CYCLE (READ)


t RC
t RC
t RP
t RP
RAS
V IH
V IL
t RAS
t RAS
t CRP
t RCD
t RSH
t CHR
t CRP
CAS
V IH
V IL
t RAD
t ASR
t ASC
t RAH
t CAH
ADDRESSES
V IH
V IL
ROW ADD
COLUMN ADDRESS
t WRP
t RCS
t RRH
t WRH
W
V IH
V IL
t AA
G
V IH
V IL
t GA
t CAC
t OFF
t CLZ
t GZ
t RAC
DQ0 - DQ3
V OH
V OL
VALID DATA OUT

HIDDEN REFRESH CYCLE (EARLY WRITE)


t RC
t RC
t RP
t RP
RAS
V IH
V IL
t RAS
t RAS
t RCD
t CHR
t CRP
t RSH
t CRP
CAS
V IH
V IL
t RAD
t ASR
t ASC
t RAH
t CAH
ADDRESSES
V IH
V IL
ROW ADD
COLUMN ADDRESS
t WCS
t WRP
t WRH
t WCH
t WP
W
V IH
V IL
G
V IH
V IL
t DS
t DH
DQ0 - DQ3
V IH
V IL
VALID DATA IN

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE


RAS V_IH V_IL
t_RAS
t_RP
CAS V_IH V_IL
t_CSR
t_CHR
t_CPT
t_RSH
t_CAS
t_RAL
t_ASC
t_CAH
ADDRESSES V_IH V_IL
COLUMN ADDRESS
READ CYCLE
t_WRP
t_AA
t_RRH
t_WRH
t_RCS
t_CAC
t_RCH
W V_IH V_IL
t_ROH
t_GA
G V_IH V_IL
t_OFF
t_CLZ
t_GZ
DQ0 - DQ3 V_OH V_OL
HIGH Z
VALID DATA OUT
WRITE CYCLE
t_RWL
t_CWL
t_WRP
t_WRH
t_WCS
t_WCH
W V_IH V_IL
G V_IH V_IL
t_DS
t_DH
DQ0 - DQ3 V_IH V_IL
HIGH Z
VALID DATA IN
t_CWL
READ-WRITE CYCLE
t_AWD
t_RWL
t_WRP
t_WRH
t_RCS
t_CWD
t_WP
W V_IH V_IL
t_AA
t_GA
G V_IH V_IL
t_GD
t_DS
t_CAC
t_CLZ
t_GZ
t_DH
DQ0 - DQ3 V_IH/V_OH V_IL/V_OL
HIGH Z
VALID DATA IN
VALID DATA OUT

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the 1M x 4 RAM: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{\text{CAS}}$ and output enable ($\overline{\text{G}}$) control read access time: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum and $\overline{\text{G}}$ must be active t_{RAC}-t_{GA} (both minimum) after $\overline{\text{RAS}}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{\text{G}}$ active transition does not occur in time, read access time is determined by either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ and $\overline{\text{G}}$ clocks are active. When either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers and $\overline{\text{G}}$ disabled.

A late write cycle (referred to as $\overline{\text{G}}$-controlled write) occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but outputs are switched off by $\overline{\text{G}}$ inactive transition, which is required to write to the device. Q may be indeterminate — see note 15 of AC Operating Conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle. $\overline{\text{G}}$ must remain inactive for t_{GH} after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the 1M x 4 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54400A-C require refresh every 16 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54400A-C. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54400A-C.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decoder. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{\text{RAS}}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode cycle) as in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

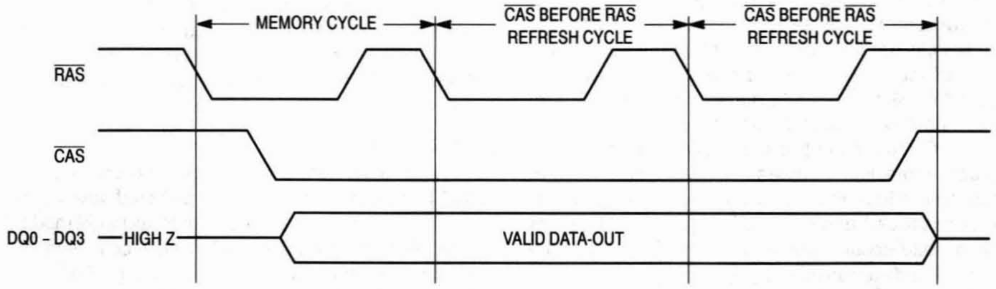

MEMORY CYCLE
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
DQ0 – DQ3
HIGH Z
VALID DATA-OUT

Figure 1. Hidden Refresh Cycle

TEST MODE

The internal organization of this device (512K x 8) allows it to be tested as if it were a 512K x 4 DRAM. Nineteen of the twenty addresses are used when operating the device in test mode. Column address A0 is ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0 – B7) in parallel. External data out is determined by the internal test mode logic of the device. See following truth table and test mode block diagram.

$\overline{\text{W}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ timing puts the device in **Test Mode** as shown in the test mode timing diagram. A **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** or a **$\overline{\text{RAS}}$-only refresh cycle** puts the device back in normal mode. Refresh is performed in test mode by using a **$\overline{\text{W}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle** which uses internal refresh address counter.

TEST MODE TRUTH TABLE

D	B0, B1	B2, B3	B4, B5	B6, B7	Q
0	0	0	0	0	1
1	1	1	1	1	1
—	Any Other				0

TEST MODE
AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 40 to 85°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

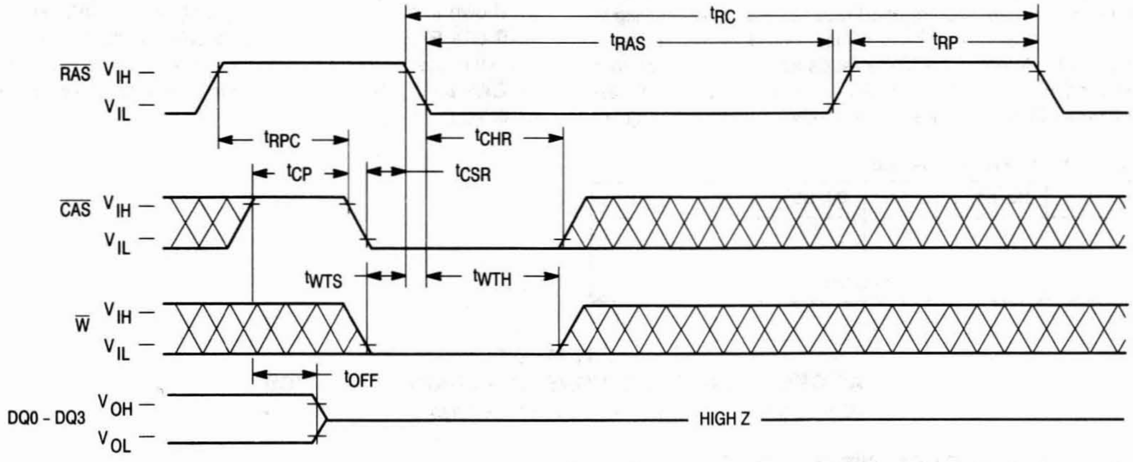
Parameter	Symbol		MCM54400A-C70		MCM54400A-C80		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	135	—	155	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	—	55	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	75	—	85	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	25	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	40	—	45	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	45	—	50	ns	6
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	75	10 k	85	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	75	200 k	85	200 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	25	—	25	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	75	—	85	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	45	—	50	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	25	10 k	25	10 k	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	40	—	45	—	ns	

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($-40°C \le T_A \le 85°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).

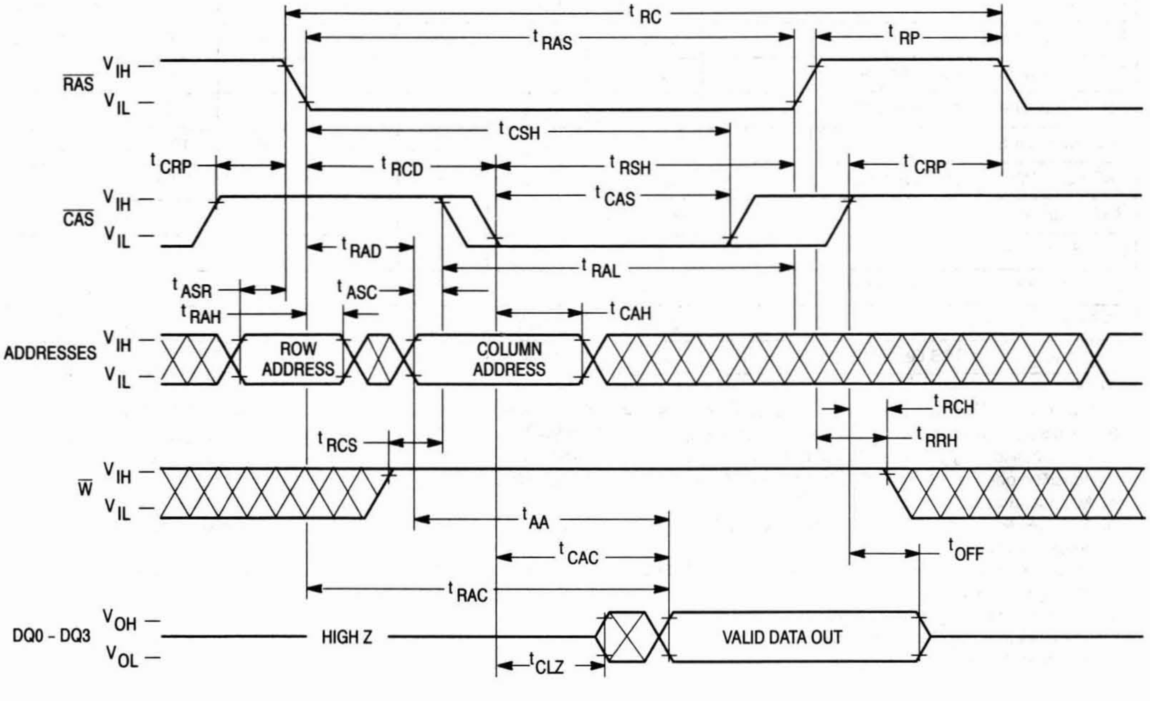
$\overline{W}$, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE (TEST MODE ENTRY)

($\overline{G}$ and A0 – A9 are Don't Care)

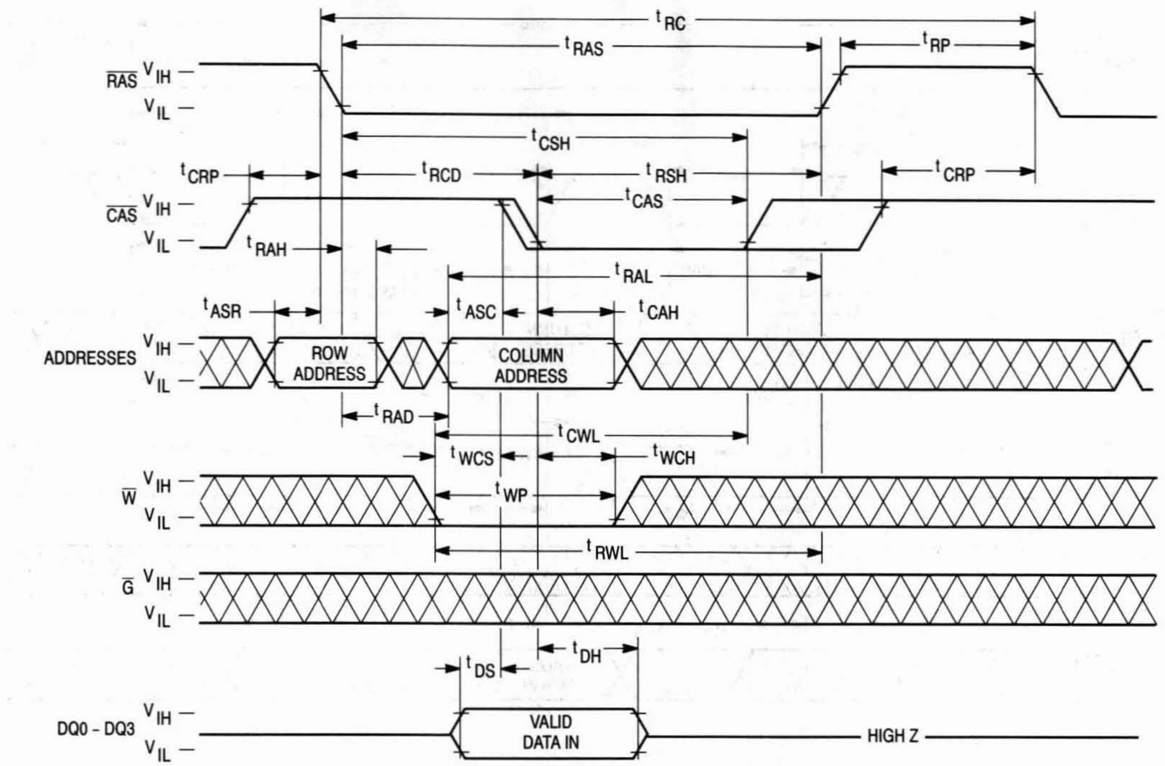

t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$ V_{IH} —
V_{IL} —
t_{RPC}
t_{CHR}
t_{CP}
t_{CSR}
$\overline{CAS}$ V_{IH} —
V_{IL} —
t_{WTS}
t_{WTH}
$\overline{W}$ V_{IH} —
V_{IL} —
t_{OFF}
DQ0 - DQ3 V_{OH} —
V_{OL} —
HIGH Z

TEST MODE — READ CYCLE

($\overline{G}$ = Low)

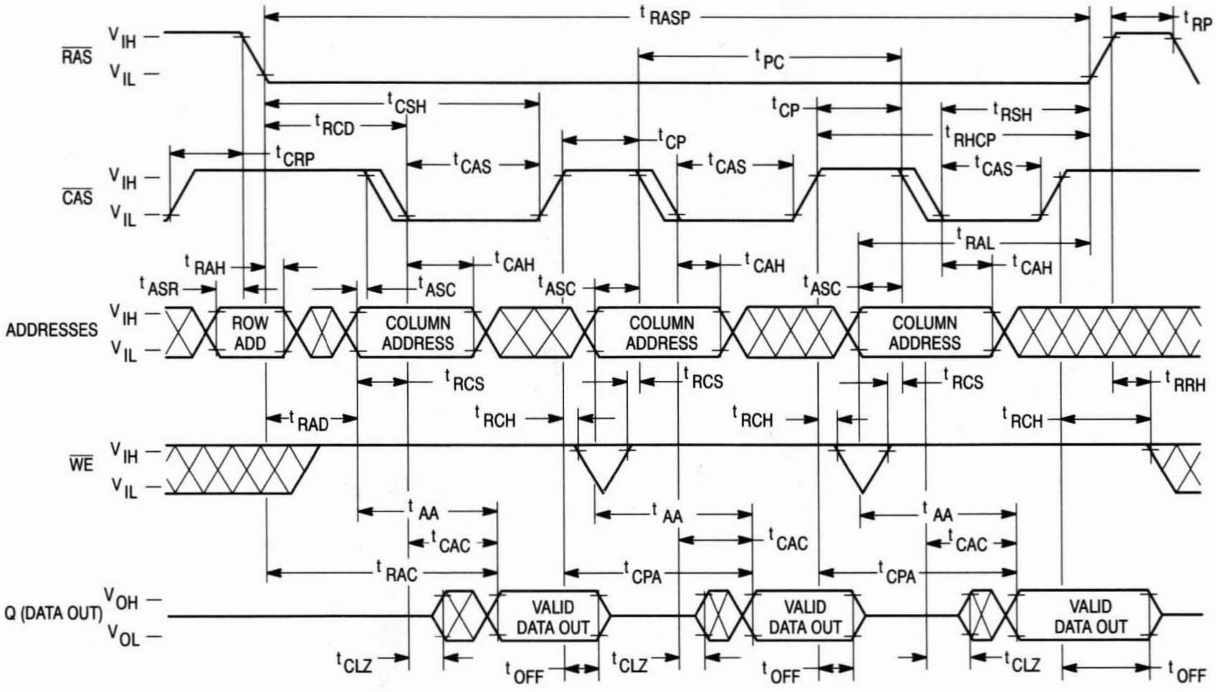

t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$ V_{IH} —
V_{IL} —
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$ V_{IH} —
V_{IL} —
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES V_{IH} —
V_{IL} —
ROW ADDRESS
COLUMN ADDRESS
t_{RCH}
t_{RRH}
t_{RCS}
$\overline{W}$ V_{IH} —
V_{IL} —
t_{AA}
t_{CAC}
t_{OFF}
t_{RAC}
DQ0 - DQ3 V_{OH} —
V_{OL} —
HIGH Z
VALID DATA OUT
t_{CLZ}

TEST MODE — EARLY WRITE CYCLE

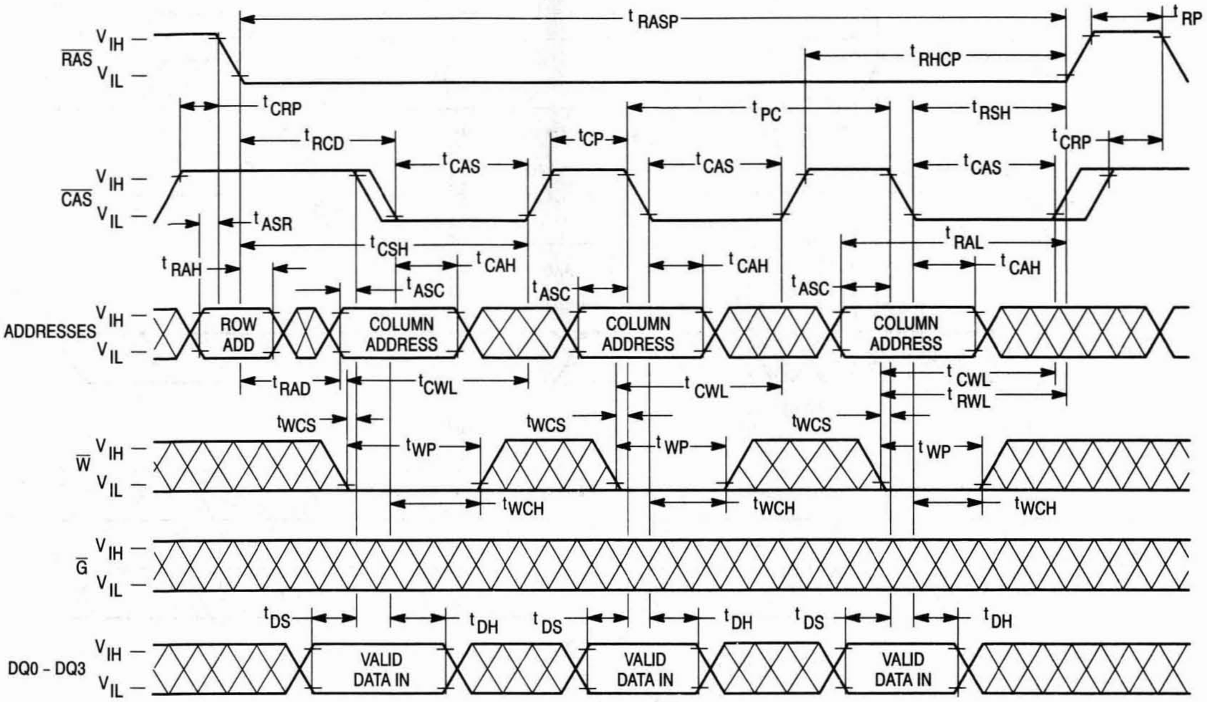

t RC
t RAS
t RP
RAS
V IH
V IL
t CSH
t CRP
t RCD
t RSH
t CAS
CAS
t RAH
t RAL
t ASR
t ASC
t CAH
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t RAD
t CWL
t WCS
t WCH
t WP
W
t RWL
G
t DS
t DH
DQ0 – DQ3
VALID DATA IN
HIGH Z

TEST MODE — FAST PAGE MODE READ CYCLE

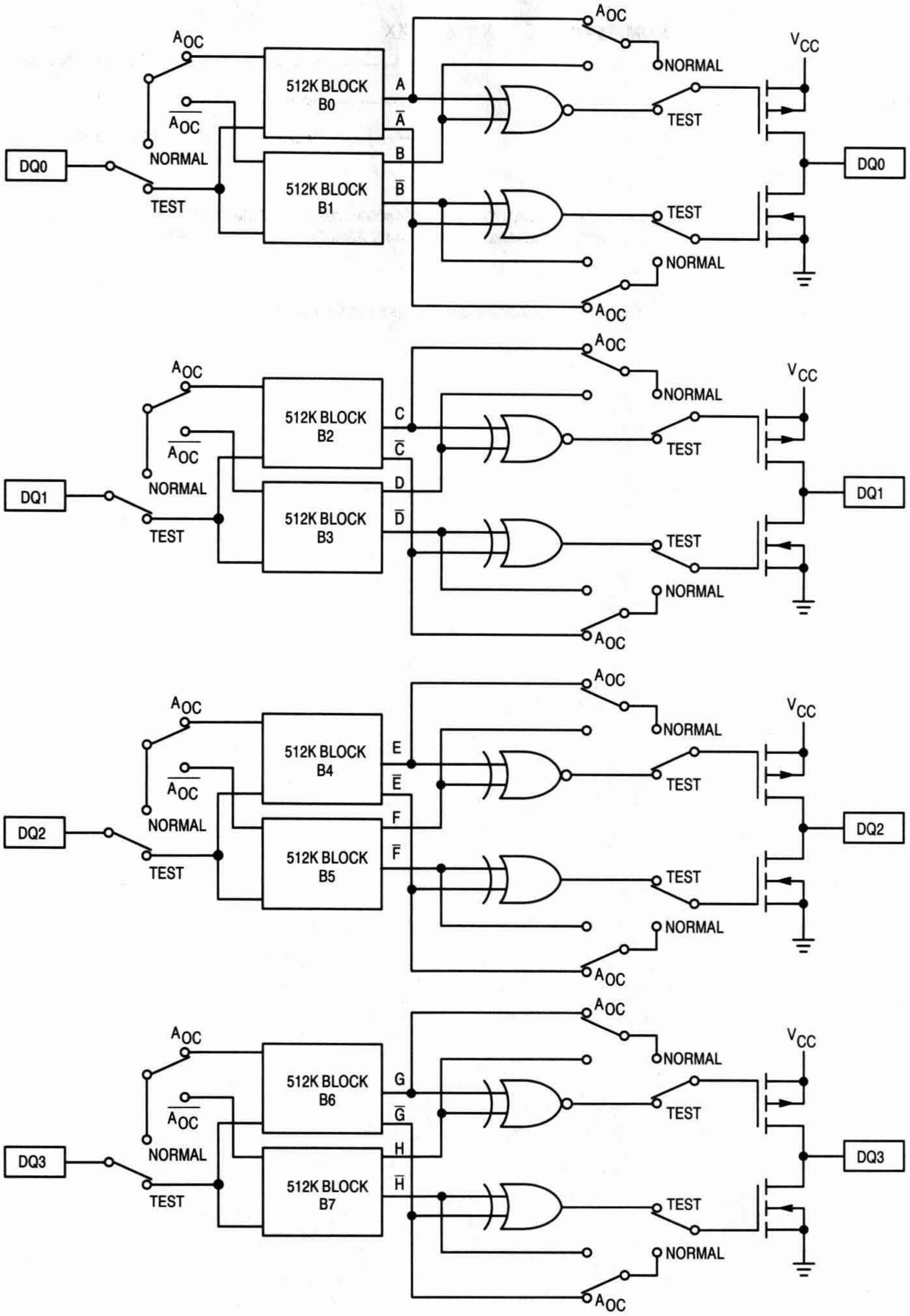
(G = Low)


t RASP
t RP
RAS
V IH
V IL
t PC
t CSH
t CP
t RSH
t RCD
t RHCP
t CRP
t CAS
CAS
t RAL
t RAH
t CAH
t ASR
t ASC
ADDRESSES
ROW ADD
COLUMN ADDRESS
t RCS
t RRH
t RAD
t RCH
WE
t AA
t CAC
t RAC
t CPA
Q (DATA OUT)
V OH
V OL
VALID DATA OUT
t CLZ
t OFF

TEST MODE — FAST PAGE MODE EARLY WRITE CYCLE


RAS
CAS
ADDRESSES
W
G
DQ0 - DQ3
V IH
V IL
t RASP
t RP
t RHCP
t CRP
t PC
t RSH
t RCD
t CP
t CAS
t ASR
t RAH
t CSH
t CAH
t RAL
t ASC
ROW ADD
COLUMN ADDRESS
t RAD
t CWL
t RWL
t WCS
t WP
t WCH
t DS
t DH
VALID DATA IN

TEST MODE BLOCK DIAGRAM


DQ0
DQ1
DQ2
DQ3
A_{OC}
$\overline{A_{OC}}$
NORMAL
TEST
512K BLOCK B0
512K BLOCK B1
512K BLOCK B2
512K BLOCK B3
512K BLOCK B4
512K BLOCK B5
512K BLOCK B6
512K BLOCK B7
A
$\overline{A}$
B
$\overline{B}$
C
$\overline{C}$
D
$\overline{D}$
E
$\overline{E}$
F
$\overline{F}$
G
$\overline{G}$
H
$\overline{H}$
V_{CC}

ORDERING INFORMATION
(Order by Full Part Number)

MCM 54400A-C X XX XX

Motorola Memory Prefix — MCM

Part Number — 54400A-C

Shipping Method (R2 = Tape and Reel, Blank = Rails)

Speed (70 = 70 ns, 80 = 80 ns)

Package (N = 300 mil SOJ, Z = 100 mil Plastic ZIP)

Full Part Numbers — MCM54400AN70 MCM54400AN70R2 MCM54400AZ70
MCM54400AN80 MCM54400AN80R2 MCM54400AZ80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM54402A

Advance Information

4M x 1 CMOS Dynamic RAM

Static Column

N PACKAGE
300 MIL SOJ
CASE 822-03

T PACKAGE
300 MIL TSOP
CASE 892-01

Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836-02

The MCM54402A is a 0.7μ CMOS high-speed dynamic random access memory. It is organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The static column mode feature allows column data to be accessed upon the column address transition when $\overline{RAS}$ and $\overline{CS}$ are held low, similar to static RAM operation.

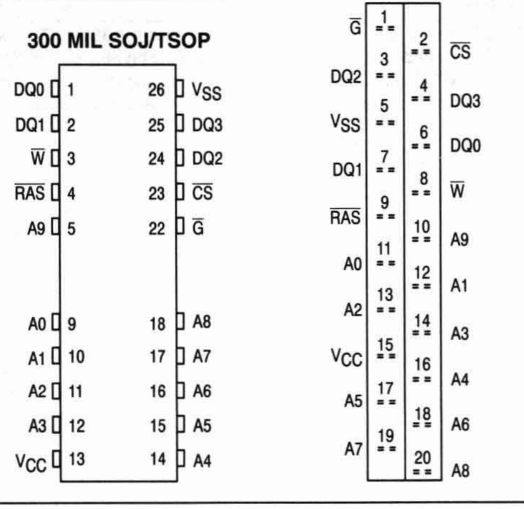
The MCM54402A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil J-lead small outline package, a 300 mil thin-small-outline package (TSOP), and a 100 mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Static Column Mode
- Test Mode
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM54402A = 16 ms
- Fast Access Time (t_{RAC}):
  - MCM54402A-60 = 60 ns (Max)
  - MCM54402A-70 = 70 ns (Max)
  - MCM54402A-80 = 80 ns (Max)
- Low Active Power:
  - MCM54402A-60 = 660 mW (Max)
  - MCM54402A-70 = 550 mW (Max)
  - MCM54402A-80 = 468 mW (Max)
- Low Standby Power Dissipation:
  - MCM54402A = 11 mW (Max, TTL Levels)
  - = 5.5 mW (Max, CMOS Levels)

PIN NAMES

Pin	Function
A0 – A9	Address Input
DQ0 – DQ3	Data Input
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

PIN ASSIGNMENTS

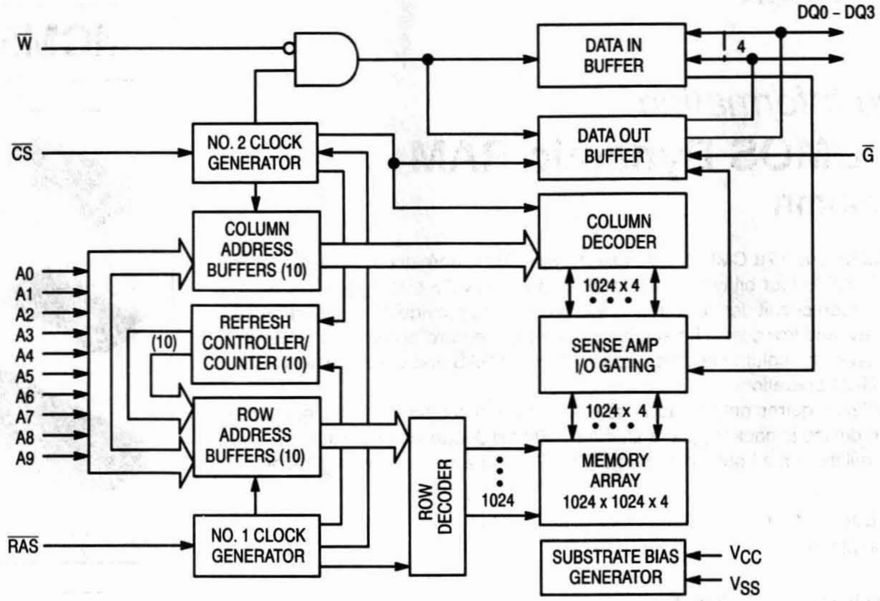


300 MIL SOJ/TSOP

100 MIL ZIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM


DQ0 – DQ3
W
DATA IN BUFFER
4
DATA OUT BUFFER
G
CS
NO. 2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (10)
COLUMN DECODER
1024 x 4
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
REFRESH CONTROLLER/ COUNTER (10)
(10)
SENSE AMP I/O GATING
1024 x 4
ROW ADDRESS BUFFERS (10)
ROW DECODER
MEMORY ARRAY 1024 x 1024 x 4
1024
RAS
NO. 1 CLOCK GENERATOR
SUBSTRATE BIAS GENERATOR
VCC
VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM54402A-60, t_{RC} = 110 ns MCM54402A-70, t_{RC} = 130 ns MCM54402A-80, t_{RC} = 150 ns	I_{CC1}	— — —	120 100 85	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles ($\overline{CS}$ = V_{IH}) MCM54402A-60, t_{RC} = 110 ns MCM54402A-70, t_{RC} = 130 ns MCM54402A-80, t_{RC} = 150 ns	I_{CC3}	— — —	120 100 85	mA	1, 2
V_{CC} Power Supply Current During Static Column Mode Cycle ($\overline{RAS}$ = $\overline{CS}$ =V_{IL}) MCM54402A-60, t_{SC} = 35 ns MCM54402A-70, t_{SC} = 40 ns MCM54402A-80, t_{SC} = 45 ns	I_{CC4}	— — —	95 85 75	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle MCM54402A-60, t_{RC} = 110 ns MCM54402A-70, t_{RC} = 130 ns MCM54402A-80, t_{RC} = 150 ns	I_{CC6}	— — —	120 100 85	mA	1
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current ($\overline{CS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CS}$ = V_{IH}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A9	C_{in}	5	pF
	$\overline{G}$, $\overline{RAS}$, $\overline{CS}$, $\overline{W}$		7	
I/O Capacitance ($\overline{CS}$ = V_{IH} to Disable Output)	DQ0 – DQ3	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\,\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM54402A-60		MCM54402A-70		MCM54402A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	165	—	185	—	205	—	ns	5
Static Column Mode Cycle Time	t_{AVAV}	t_{SC}	35	—	40	—	45	—	ns	
Static Column Mode Read-Write Cycle Time	t_{AVAV}	t_{SRWC}	90	—	100	—	110	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{CS}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6, 9
Access Time from Last Write	t_{WLQV}	t_{ALW}	—	55	—	65	—	75	ns	6, 10
$\overline{CS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	11
Data Out Hold from Address Change	t_{AXQX}	t_{AOH}	5	—	5	—	5	—	ns	
Data Out Enable from Write	t_{WHQV}	t_{OW}	—	20	—	20	—	20	ns	
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{RAS}$ Pulse Width (Static Column Mode)	t_{RELREH}	t_{RASC}	60	200 k	70	200 k	80	200 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{CS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CS}$ Pulse Width	t_{CELCEH}	t_{CS}	20	10 k	20	10 k	20	10 k	ns	
$\overline{CS}$ Pulse Width (Static Column Mode)	t_{CELCEH}	t_{CSC}	20	200 k	20	200 k	20	200 k	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	13
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{CS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. Assumes that $t_{LWAD} \ge t_{LWAD}$ (max).
11. t_{OFF} (max) and/or t_{GZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM54402A-60		MCM54402A-70		MCM54402A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$ (Read Cycle)	t_{RELAX}	t_{AR}	70	—	80	—	90	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Column Address Hold Time Reference to $\overline{RAS}$ High	t_{REHAX}	t_{AH}	5	—	5	—	5	—	ns	14
Last Write to Column Address Delay Time	t_{WLAV}	t_{LWAD}	20	25	20	30	20	35	ns	15
Last Write to Column Address Hold Time	t_{WLAX}	t_{AHLW}	55	—	65	—	75	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	16
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	16
Write Command Hold Time Referenced to $\overline{CS}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command Inactive Time	t_{WHWL}	t_{WI}	10	—	10	—	10	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{CS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	17
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	17
Refresh Period	t_{RVRV}	t_{RFSH}	—	16	—	16	—	16	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	18
$\overline{CS}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	50	—	ns	18
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	90	—	100	—	110	—	ns	18
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	60	—	65	—	70	—	ns	18
$\overline{CS}$ Setup Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CS}$ Hold Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{CS}$ Precharge Time for $\overline{CS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	—	10	—	10	—	ns	

NOTES:

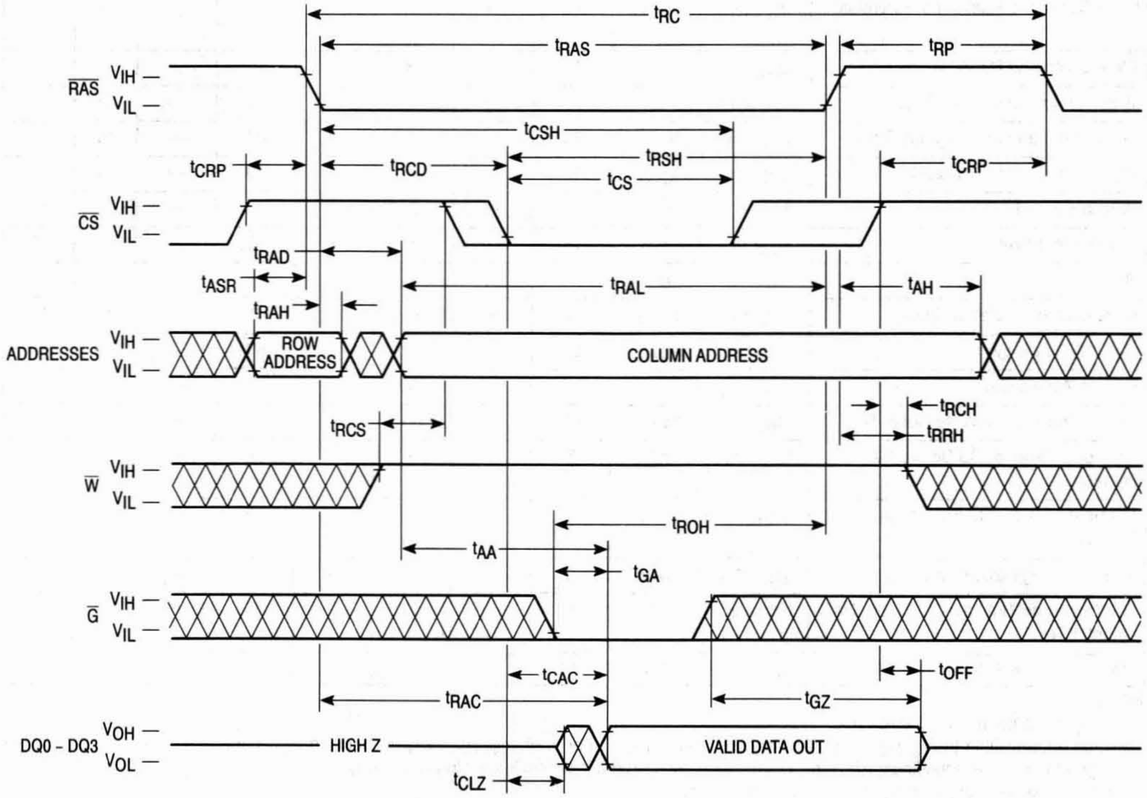
(continued)

14. t_{AH} must be met for a read cycle.
15. Operation within the t_{LWAD} (max) limit ensures that t_{ALW} can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
17. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in read-write cycles.
18. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM54402A-60		MCM54402A-70		MCM54402A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	20	—	20	ns	
$\overline{G}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	20	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	20	ns	11
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	20	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	ns	
Write to $\overline{RAS}$ Precharge Time ($\overline{CS}$ Before $\overline{RAS}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	10	—	ns	
Write to $\overline{RAS}$ Hold Time ($\overline{CS}$ Before $\overline{RAS}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	

READ CYCLE



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VIH
VIL
tCSH
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CS
VIH
VIL
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tRAL
tAH
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ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
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W
VIH
VIL
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tAA
tGA
G
VIH
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DQ0 - DQ3
VOH
VOL
HIGH Z
VALID DATA OUT
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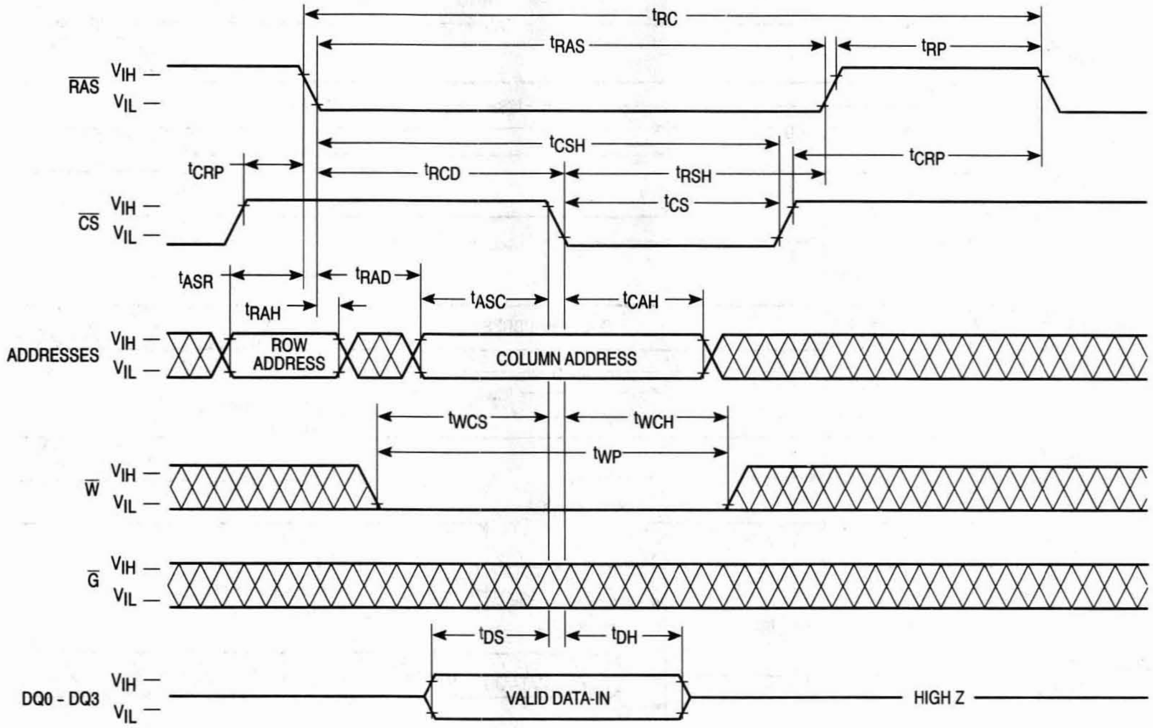
EARLY WRITE CYCLE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ROW ADDRESS
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VIH
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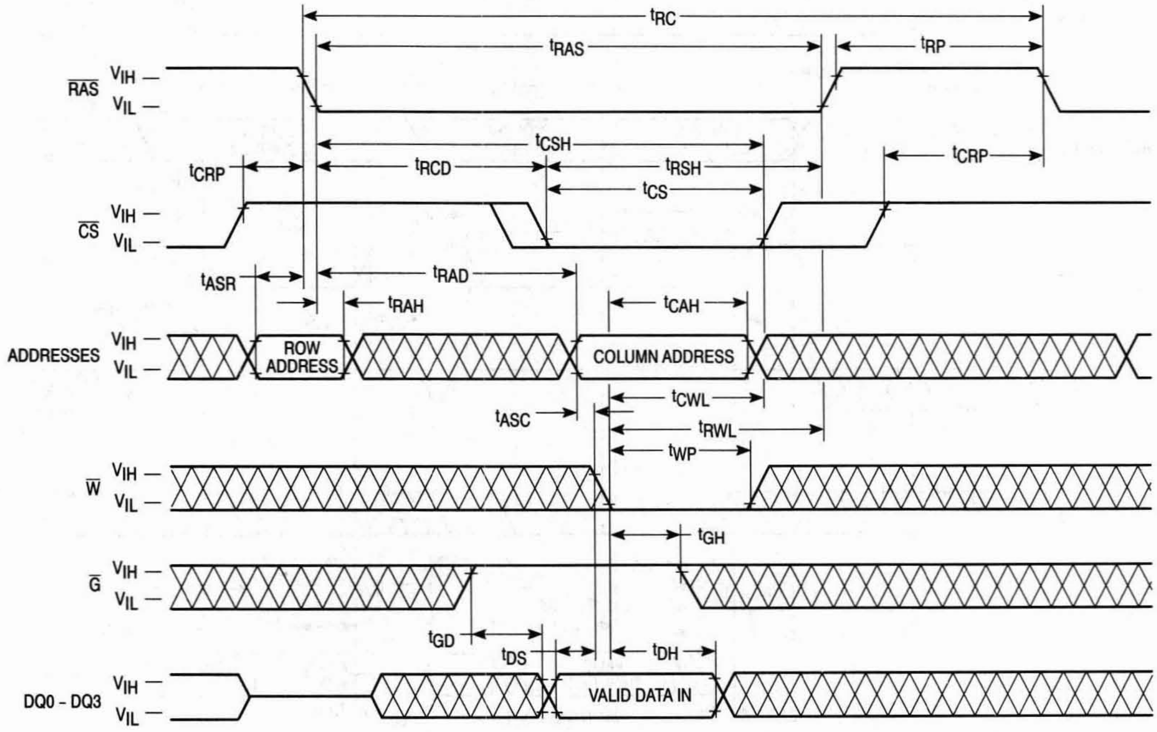
DQ0 - DQ3
VIH
VIL
VALID DATA-IN
HIGH Z

G CONTROLLED LATE WRITE CYCLE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ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
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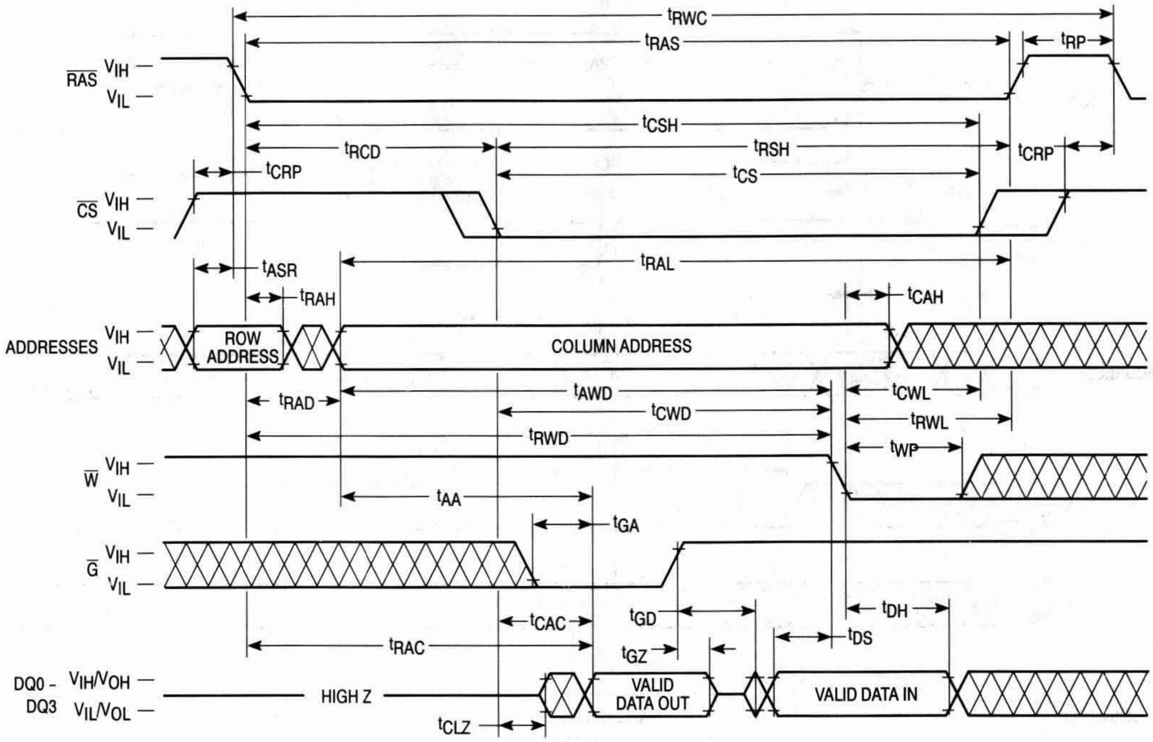
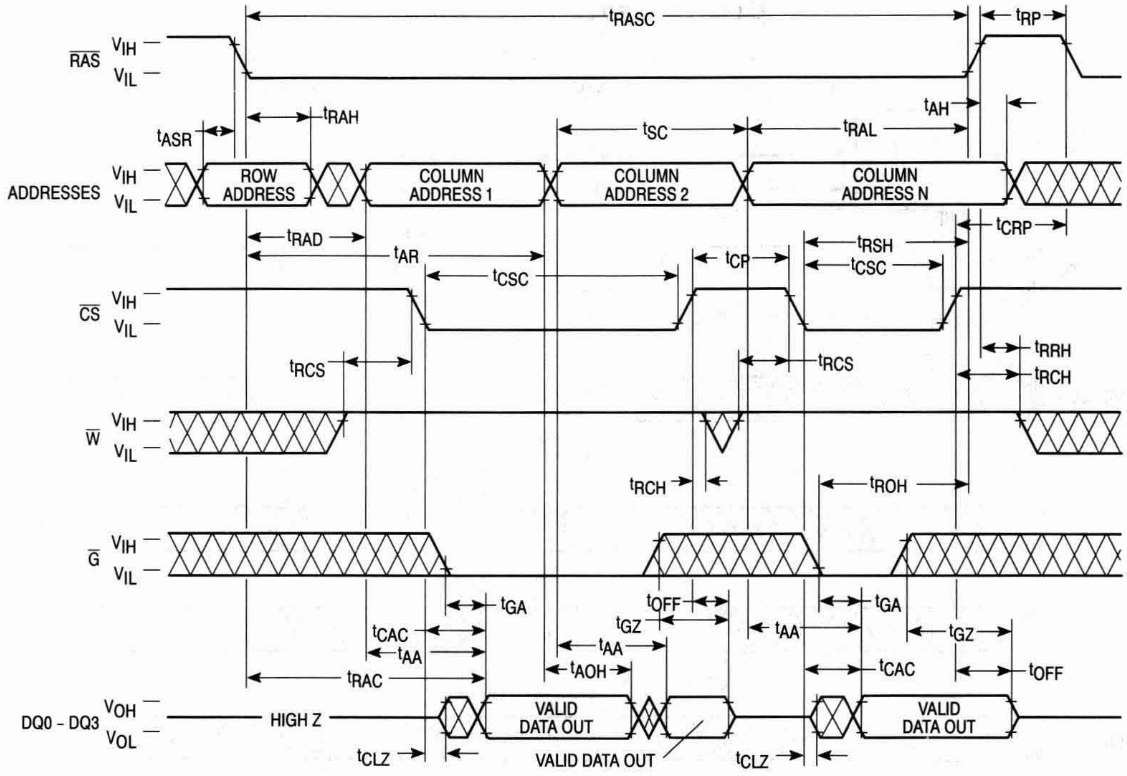
tWP
W
VIH
VIL
tGH
G
VIH
VIL
tGD
tDS
tDH
DQ0 - DQ3
VIH
VIL
VALID DATA IN

READ-WRITE CYCLE



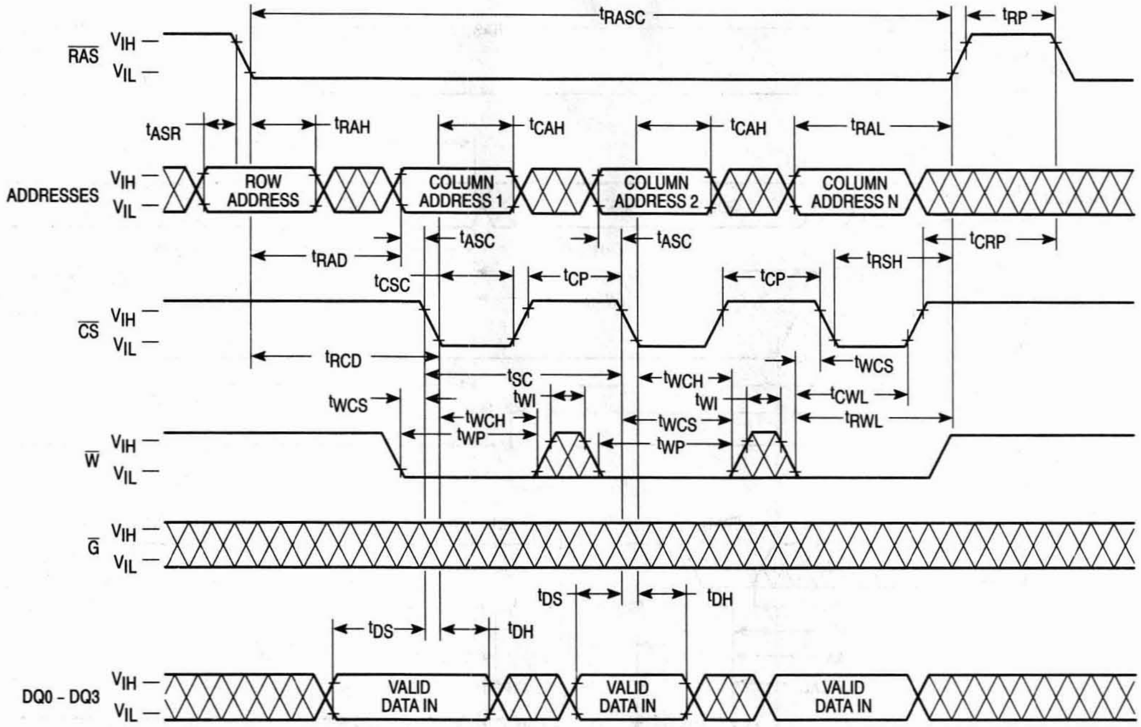
t_{RWC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CRP}
t_{CS}
$\overline{CS}$
t_{ASR}
t_{RAL}
t_{RAH}
t_{CAH}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{RAD}
t_{AWD}
t_{CWL}
t_{CWD}
t_{RWL}
t_{RWD}
t_{WP}
$\overline{W}$
t_{AA}
t_{GA}
$\overline{G}$
t_{GD}
t_{DH}
t_{CAC}
t_{DS}
t_{RAC}
t_{GZ}
DQ0 - DQ3
V_{IH}/V_{OH}
V_{IL}/V_{OL}
HIGH Z
VALID DATA OUT
VALID DATA IN
t_{CLZ}

STATIC COLUMN MODE READ CYCLE

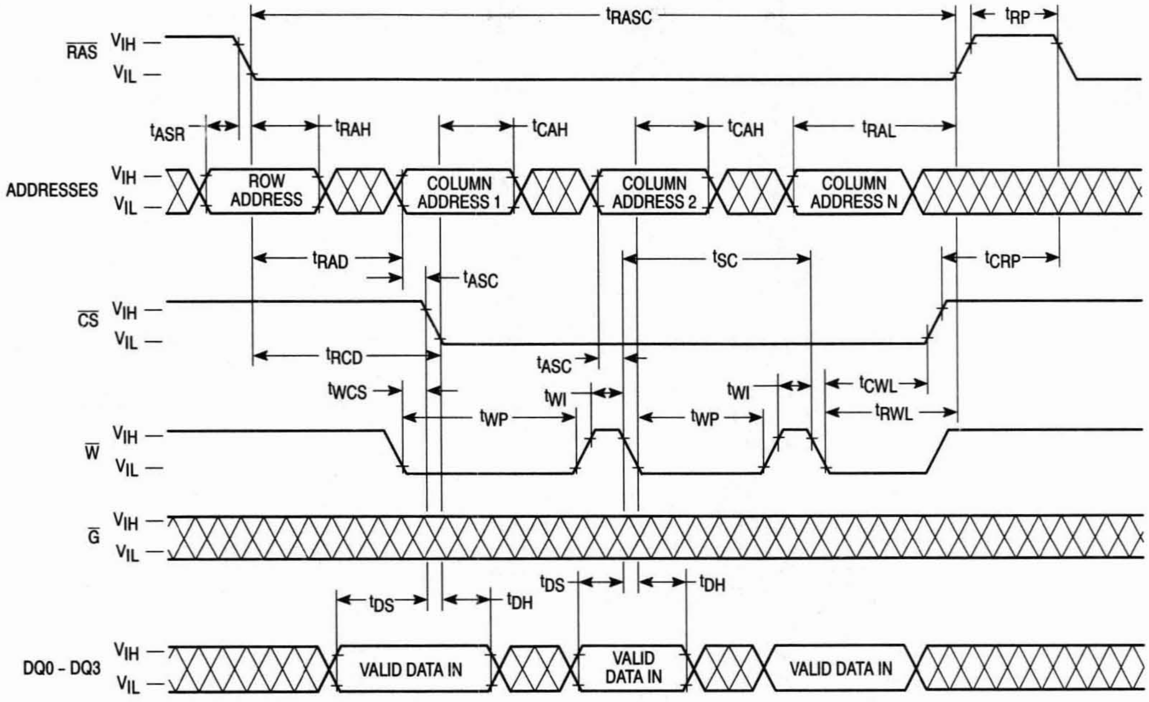


t_{RASC}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{AH}
t_{RAH}
t_{ASR}
t_{SC}
t_{RAL}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS N
t_{RAD}
t_{CRP}
t_{AR}
t_{RSH}
t_{CP}
t_{CSC}
t_{CSC}
$\overline{CS}$
t_{RCS}
t_{RCS}
t_{RRH}
t_{RCH}
$\overline{W}$
t_{RCH}
t_{ROH}
$\overline{G}$
t_{OFF}
t_{GA}
t_{GA}
t_{CAC}
t_{GZ}
t_{AA}
t_{GZ}
t_{AA}
t_{AA}
t_{AOH}
t_{CAC}
t_{RAC}
t_{OFF}
DQ0 - DQ3
V_{OH}
V_{OL}
HIGH Z
VALID DATA OUT
VALID DATA OUT
VALID DATA OUT
t_{CLZ}
t_{CLZ}

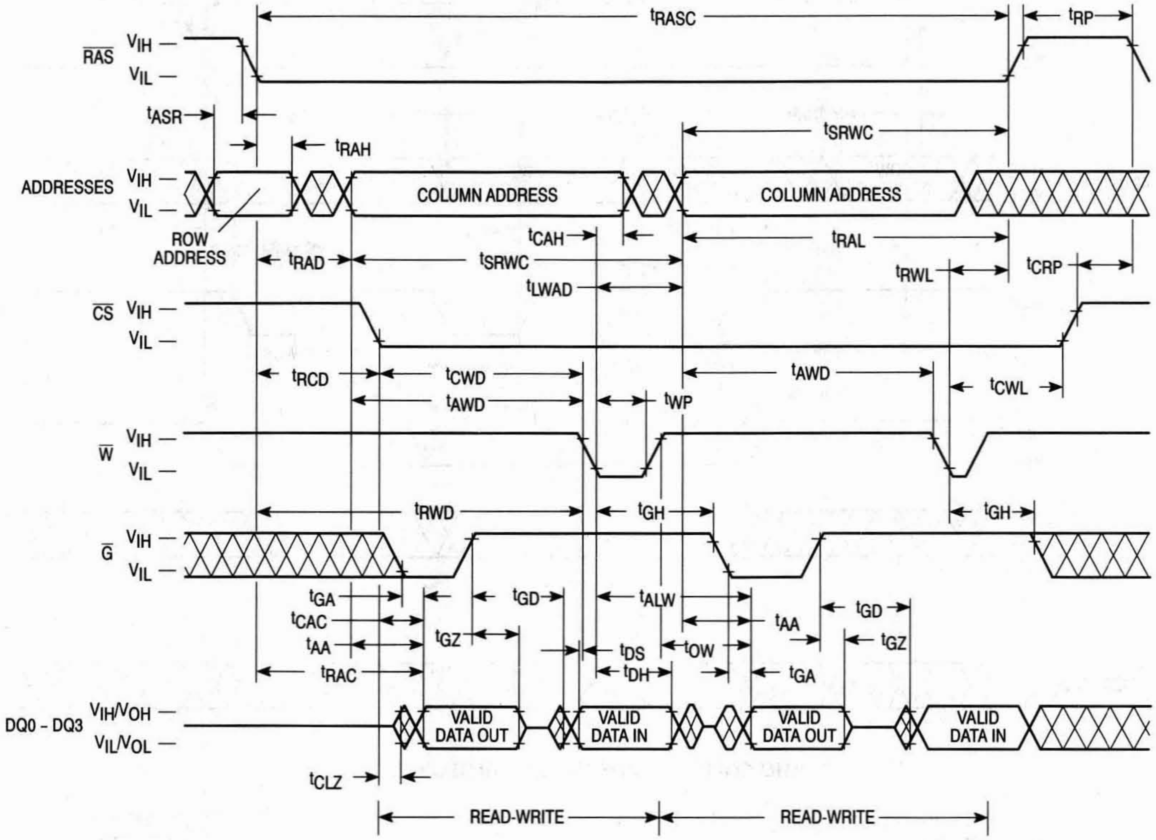
STATIC COLUMN MODE EARLY WRITE CYCLE (A)


tRASC
tRP
RAS
VIH
VIL
tASR
tRAH
tCAH
tCAH
tRAL
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS N
tASC
tASC
tCRP
tRAD
tCSC
tCP
tCP
tRSH
CS
tRCD
tWCS
tSC
tWCH
tWI
tWI
tCWL
tWCS
tWCH
tWP
tWCS
tWP
tRWL
W
G
tDS
tDH
tDS
tDH
DQ0 - DQ3
VALID DATA IN
VALID DATA IN
VALID DATA IN

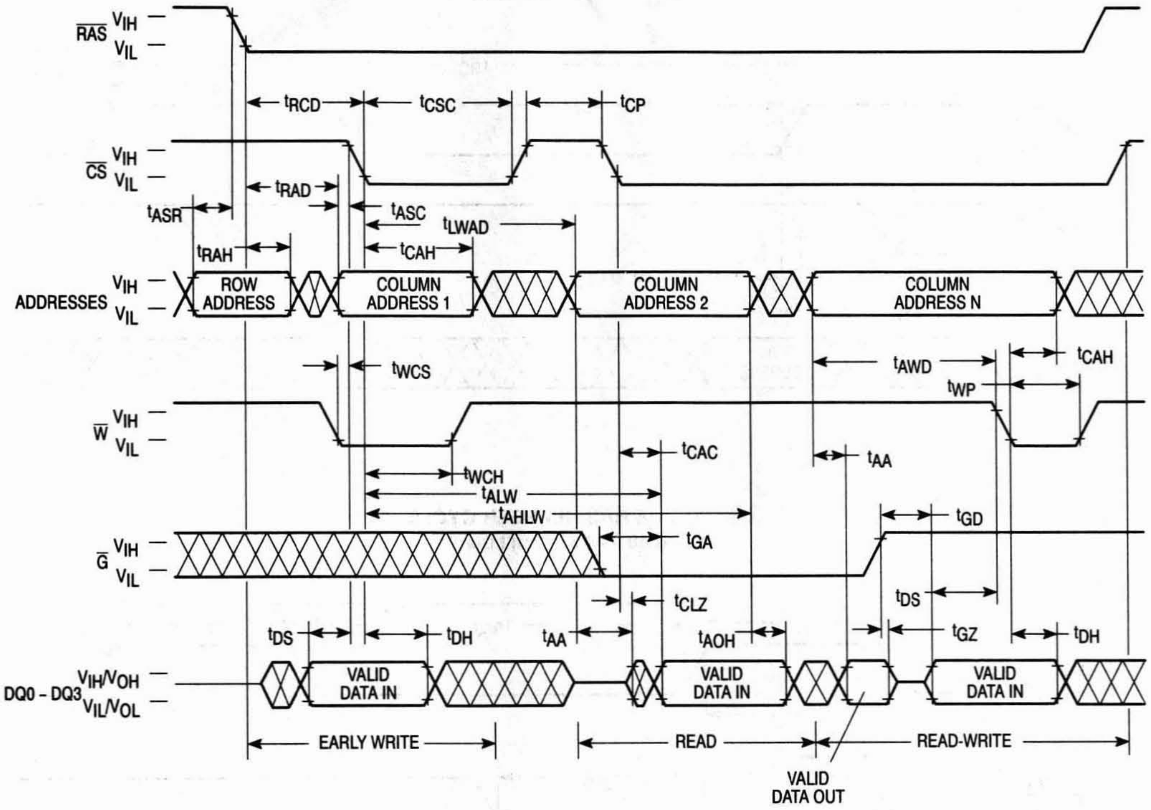
STATIC COLUMN MODE EARLY WRITE CYCLE (B)


tRASC
tRP
RAS
VIH
VIL
tASR
tRAH
tCAH
tCAH
tRAL
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS N
tRAD
tSC
tCRP
tASC
CS
tRCD
tASC
tWCS
tWI
tWI
tCWL
tWP
tWP
tRWL
W
G
tDS
tDH
tDS
tDH
DQ0 - DQ3
VALID DATA IN
VALID DATA IN
VALID DATA IN

STATIC COLUMN MODE READ-WRITE CYCLE

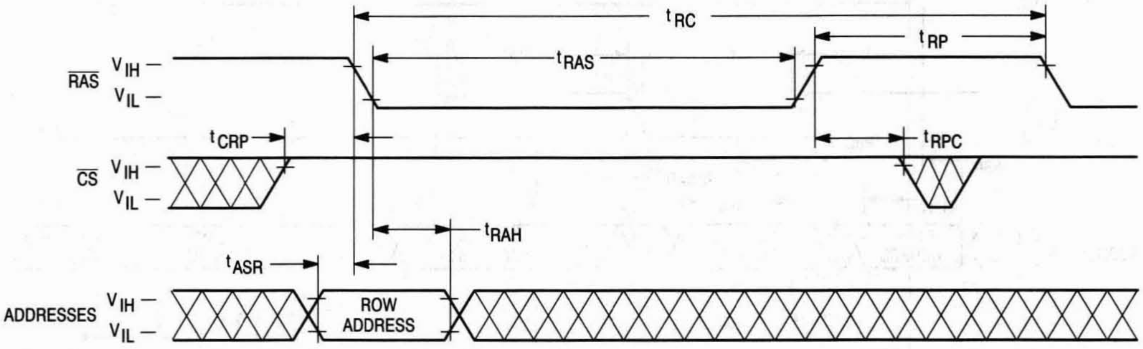

tRASC
tRP
RAS
VIH
VIL
tASR
tSRWC
tRAH
ADDRESSES
COLUMN ADDRESS
COLUMN ADDRESS
ROW ADDRESS
tCAH
tRAL
tRAD
tSRWC
tRWL
tCRP
tLWAD
CS
tRCD
tCWD
tAWD
tCWL
tAWD
tWP
W
tRWD
tGH
tGH
G
tGA
tGD
tALW
tGD
tCAC
tAA
tGZ
tAA
tGZ
tDS
tOW
tRAC
tDH
tGA
DQ0 – DQ3
VIH/VOH
VIL/VOL
VALID DATA OUT
VALID DATA IN
VALID DATA OUT
VALID DATA IN
tCLZ
READ-WRITE
READ-WRITE

STATIC COLUMN MODE READ/WRITE MIXED CYCLE


$\overline{RAS}$ V_{IH} V_{IL}
t_{RCD}
t_{CSC}
t_{CP}
$\overline{CS}$ V_{IH} V_{IL}
t_{RAD}
t_{ASR}
t_{ASC}
t_{LWAD}
t_{RAH}
t_{CAH}
ADDRESSES V_{IH} V_{IL}
ROW ADDRESS
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS N
t_{WCS}
t_{AWD}
t_{CAH}
t_{WP}
$\overline{W}$ V_{IH} V_{IL}
t_{CAC}
t_{AA}
t_{WCH}
t_{ALW}
t_{AHLW}
t_{GD}
$\overline{G}$ V_{IH} V_{IL}
t_{GA}
t_{DS}
t_{CLZ}
t_{DS}
t_{DH}
t_{AA}
t_{AOH}
t_{GZ}
t_{DH}
DQ0 – DQ3 V_{IH}/V_{OH} V_{IL}/V_{OL}
VALID DATA IN
VALID DATA IN
VALID DATA IN
EARLY WRITE
READ
READ-WRITE
VALID DATA OUT

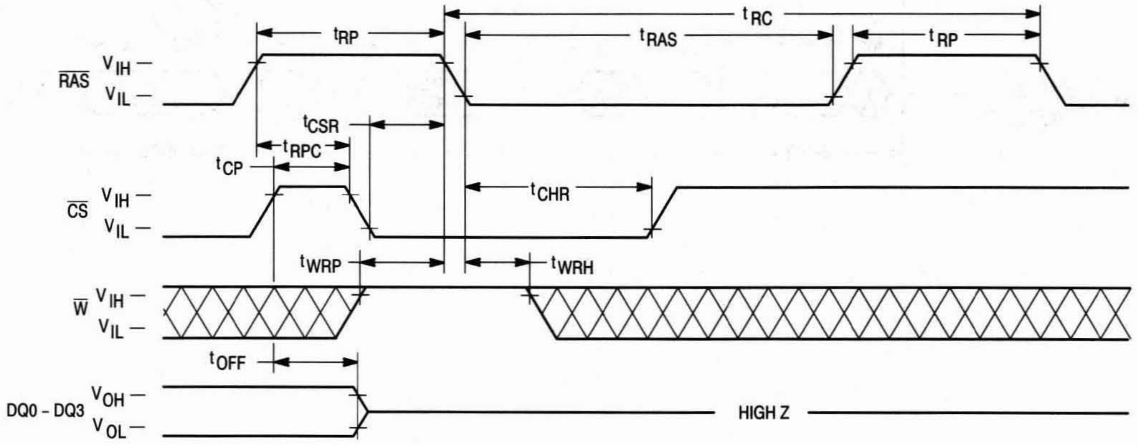
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

($\overline{\text{W}}$ and $\overline{\text{G}}$ are Don't Care)

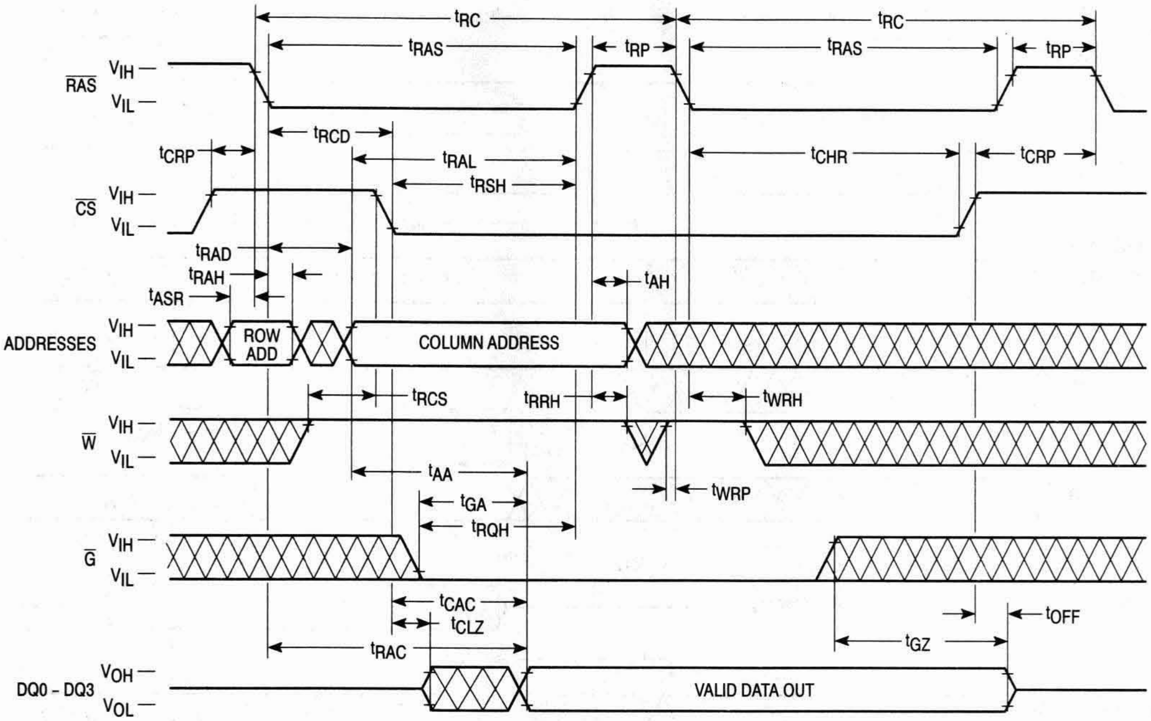

t RC
t RP
t RAS
RAS
V IH
V IL
t CRP
t RPC
CS
V IH
V IL
t RAH
t ASR
ADDRESSES
V IH
V IL
ROW ADDRESS

$\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

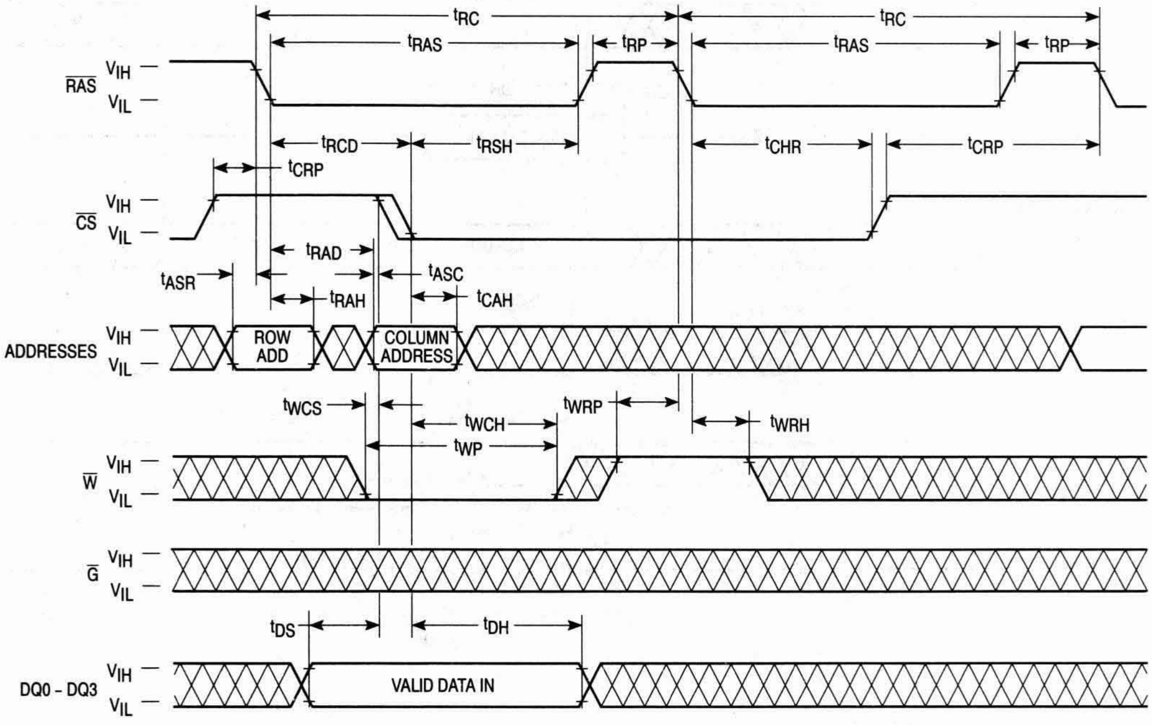
($\overline{\text{G}}$ and A0 – A9 are Don't Care)


t RC
t RP
t RAS
t RP
RAS
V IH
V IL
t CSR
t RPC
t CP
t CHR
CS
V IH
V IL
t WRP
t WRH
W
V IH
V IL
t OFF
DQ0 - DQ3
V OH
V OL
HIGH Z

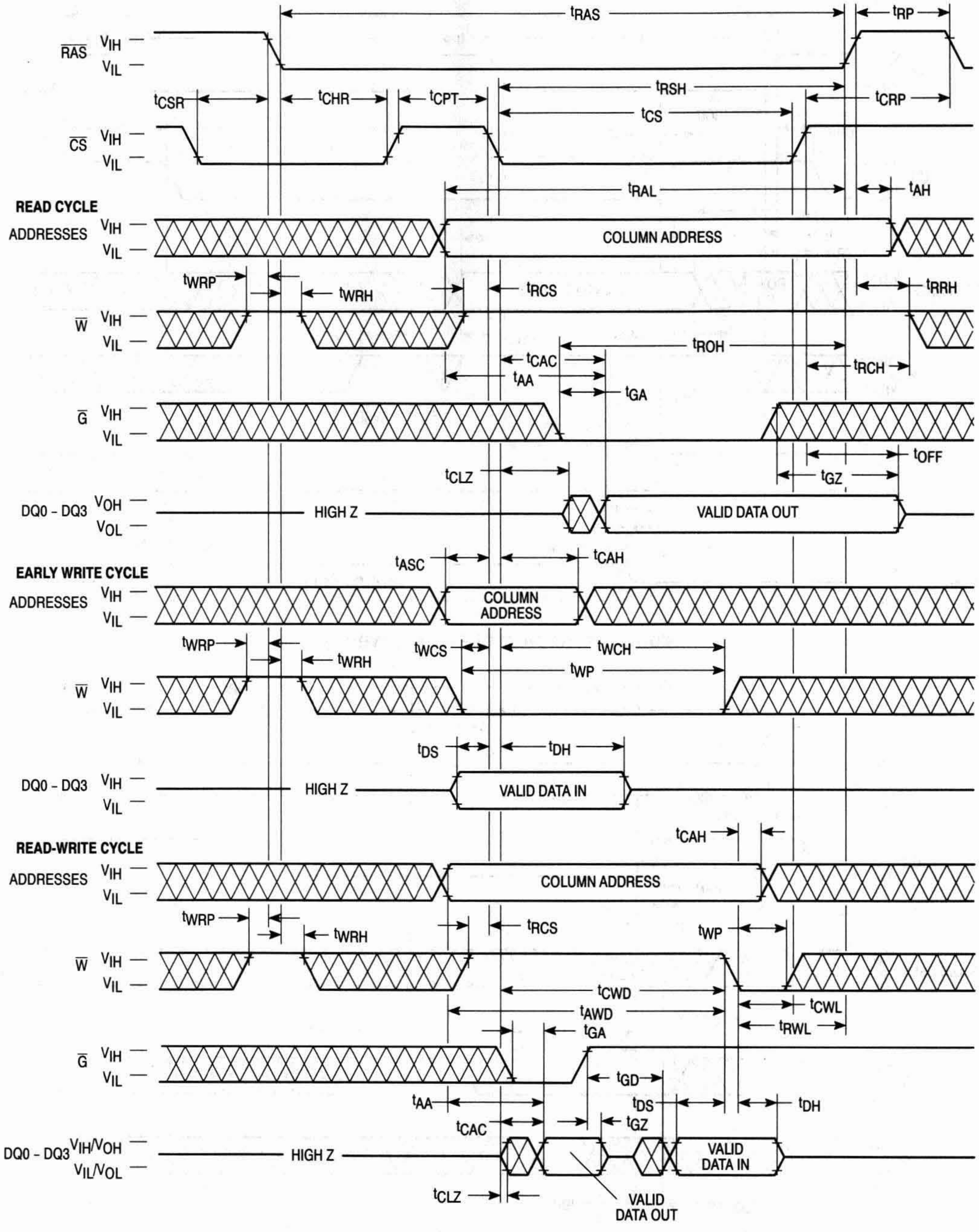
HIDDEN REFRESH CYCLE (READ)


tRC
tRC
tRAS
tRP
tRAS
tRP
RAS
VIH
VIL
tRCD
tCRP
tRAL
tCHR
tCRP
tRSH
CS
VIH
VIL
tRAD
tRAH
tAH
tASR
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
tRCS
tRRH
tWRH
W
VIH
VIL
tAA
tWRP
tGA
tRQH
G
VIH
VIL
tCAC
tCLZ
tOFF
tRAC
tGZ
DQ0 - DQ3
VOH
VOL
VALID DATA OUT

HIDDEN REFRESH CYCLE (EARLY WRITE)


tRC
tRC
tRAS
tRP
tRAS
tRP
RAS
VIH
VIL
tRCD
tRSH
tCHR
tCRP
tCRP
CS
VIH
VIL
tRAD
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
tWCS
tWRP
tWCH
tWRH
tWP
W
VIH
VIL
G
VIH
VIL
tDS
tDH
DQ0 - DQ3
VIH
VIL
VALID DATA IN

$\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE


$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RAS}
t_{RP}
t_{CSR}
t_{CHR}
t_{CPT}
t_{RSH}
t_{CRP}
t_{CS}
$\overline{\text{CS}}$
t_{RAL}
t_{AH}
READ CYCLE
ADDRESSES
COLUMN ADDRESS
t_{WRP}
t_{WRH}
t_{RCS}
t_{RRH}
$\overline{\text{W}}$
t_{CAC}
t_{ROH}
t_{AA}
t_{RCH}
t_{GA}
$\overline{\text{G}}$
t_{OFF}
t_{CLZ}
t_{GZ}
DQ0 - DQ3
V_{OH}
V_{OL}
HIGH Z
VALID DATA OUT
t_{ASC}
t_{CAH}
EARLY WRITE CYCLE
COLUMN ADDRESS
t_{WCS}
t_{WCH}
t_{WP}
t_{DS}
t_{DH}
VALID DATA IN
READ-WRITE CYCLE
t_{CWD}
t_{AWD}
t_{CWL}
t_{RWL}
t_{GD}
t_{GZ}
V_{IH}/V_{OH}
V_{IL}/V_{OL}
VALID DATA IN
VALID DATA OUT

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by the row address strobe ($\overline{RAS}$) clock, into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{RAS}$ active transition latches the row address field. Column addresses are not latched, hence the "static column" designation of this device. Chip select ($\overline{CS}$) active transition (active = V_{IL}, t_{RCD} minimum) follows $\overline{RAS}$ on all read, write, or read-write cycles and is independent of column address. The static column feature allows greater flexibility in setting up the external column addresses into the RAM.

There are three other variations in addressing the 1M x 4 RAM: **$\overline{RAS}$-only refresh cycle, $\overline{CS}$ before $\overline{RAS}$ refresh cycle,** and **Static Column mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, static column mode read cycle, read-write cycle, and static column mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ active transition latching the desired row. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CS}$ active transition, to enable read mode. A valid column address can be provided at any time (t_{RAD} minimum), independent of the $\overline{CS}$ active transition.

Both the $\overline{RAS}$ and $\overline{CS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{CS}$ and output enable ($\overline{G}$) control read access time; $\overline{CS}$ and $\overline{G}$ must be active (and column address must be valid) by t_{RCD} maximum, and $t_{RAC} - t_{GA}$ minimum, respectively, to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{G}$ active transition does not occur in time, read access time is determined by either the $\overline{CS}$ or $\overline{G}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{RAS}$ and $\overline{CS}$ clocks must remain active for minimum times of t_{RAS} and t_{CS}, respectively, to complete the read cycle. The column address must remain valid for t_{AH} after $\overline{RAS}$ inactive transition to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CS}$ and $\overline{G}$ clocks are active. When either the $\overline{CS}$ or $\overline{G}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, static column mode early write, and static column mode read-write. Early and late write modes are discussed here, while static column mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CS}$ leading edge. Minimum active time t_{RAS} and t_{CS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CS}$ active transition. Column address set up and hold times (t_{ASC}, t_{CAH}), and data in (D) set up and hold times (t_{DS}, t_{DH}) are referenced to $\overline{CS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CS}$ active transition, keeping data-out buffers and $\overline{G}$ disabled.

A late write cycle (referred to as $\overline{G}$-controlled write) occurs when $\overline{W}$ active transition is made after $\overline{CS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_{T}) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_{T}) are maintained. Column address and D timing parameters are referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CS}$ active transition but Q may be indeterminate — see note 18 of AC Operating Conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

STATIC COLUMN MODE CYCLES

Static column mode refers to multiple successive data operations performed at any or all 1024 column locations on the selected row of the 1M x 4 dynamic RAM during one $\overline{RAS}$ cycle. Read access time of multiple operations (t_{AA} or t_{CAC}) is considerably faster than the regular $\overline{RAS}$ clock access time t_{RAC}. Multiple operations can be performed simply by keeping $\overline{RAS}$ active. $\overline{CS}$ may be toggled between active and inactive states at any time within the $\overline{RAS}$ cycle.

Once the timing requirements for the initial read, write, or read-write cycle are met and $\overline{RAS}$ remains low, the device is ready for the next operation. Operations can be intermixed in any order, at any column address, subject to normal operating conditions previously described. Every write operation must be clocked with either $\overline{CS}$ or $\overline{W}$, as indicated in **static column mode early write cycle** timing diagrams **A** and **B**.

Column address and D timing parameters are referenced to the signal clocking the write operation. $\overline{\text{CS}}$ must be toggled inactive (t_{CP}) to perform a read operation after an early write operation (to turn output on), as indicated in **static column mode read/write mixed cycle** timing diagram. The maximum number of consecutive operations is limited to t_{RASC}. The cycle ends when $\overline{\text{RAS}}$ transitions to inactive.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54402A require refresh every 16 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54402A. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54402A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle.

The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{\text{RAS}}$ active transition to prevent switching the device into **test mode**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CS}}$ active the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode) as in $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh.

$\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of 8 **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0" which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

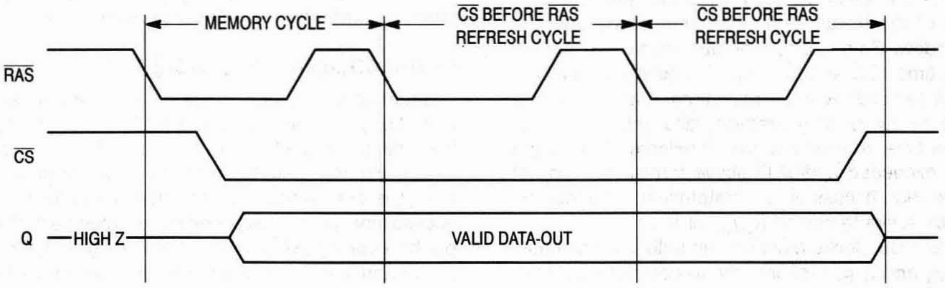


Figure 1. Hidden Refresh Cycle

TEST MODE

The internal organization of this device (512 x 8) allows it to be tested as if it were a 512K x 4 DRAM. Nineteen of the twenty addresses are used when operating the device in test mode. Column address A0 is ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0 – B7) in parallel. External data out is determined by the internal test mode logic of the device. See the following truth table and test mode block diagram.

$\overline{\text{W}}$, $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ timing puts the device in **Test Mode**, as shown in the test mode timing diagram. A **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh cycle** or a **$\overline{\text{RAS}}$-only refresh cycle** puts the device back in normal mode. Refresh is performed in test mode by using a **$\overline{\text{W}}$, $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh cycle** which uses the internal refresh address counter.

TEST MODE TRUTH TABLE

D	B0, B1	B2, B3	B4, B5	B6, B7	Q
0	0	0	0	0	1
1	1	1	1	1	1
—	Any Other				0

TEST MODE
AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

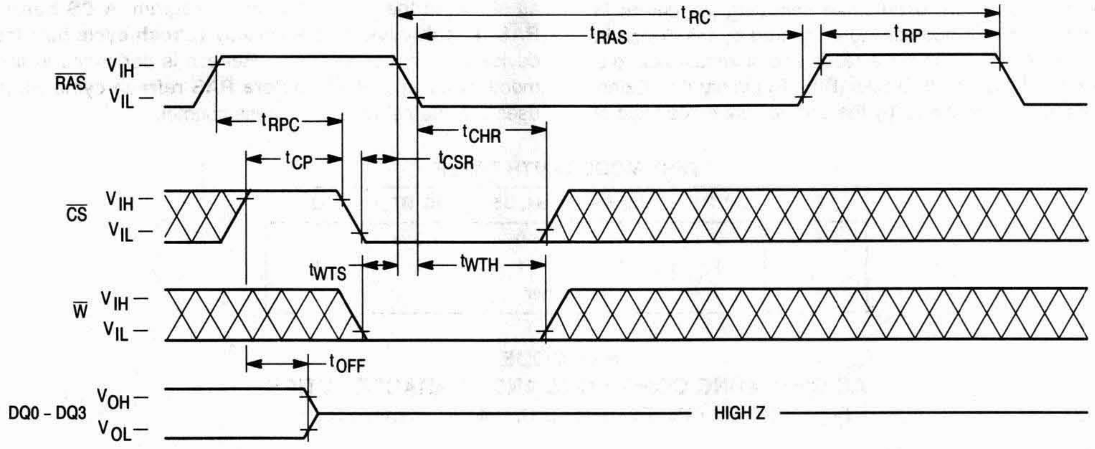
Parameter	Symbol		MCM54402A-60		MCM54402A-70		MCM54402A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	115	—	135	—	155	—	ns	5
Static Column Mode Cycle Time	t_{AVAV}	t_{SC}	40	—	45	—	50	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	65	—	75	—	85	ns	6, 7
Access Time from $\overline{\text{CS}}$	t_{CELQV}	t_{CAC}	—	25	—	25	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	45	ns	6, 9
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	65	10 k	75	10 k	85	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Static Column Mode)	t_{RELREH}	t_{RASC}	65	200 k	75	200 k	85	200 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	25	—	25	—	25	—	ns	
$\overline{\text{CS}}$ Hold Time	t_{RELCEH}	t_{CSH}	65	—	75	—	85	—	ns	
$\overline{\text{CS}}$ Pulse Width	t_{CELCEH}	t_{CS}	25	10 k	25	10 k	25	10 k	ns	
$\overline{\text{CS}}$ Pulse Width (Static Column Mode)	t_{CELCEH}	t_{CSC}	25	200 k	25	200 k	25	200 k	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	45	—	ns	

NOTES:

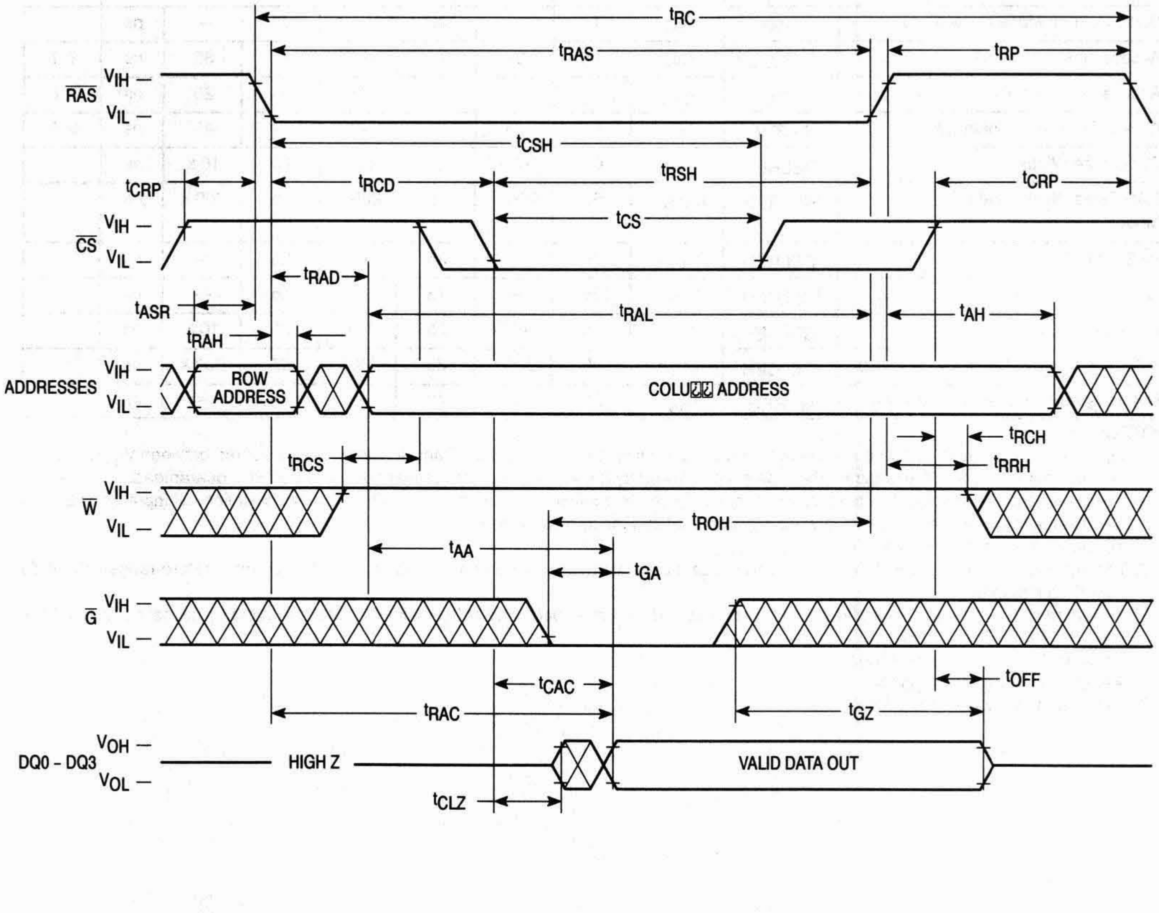
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C $\leq T_A \leq$ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).

W, CS BEFORE RAS REFRESH CYCLE (TEST MODE ENTRY)

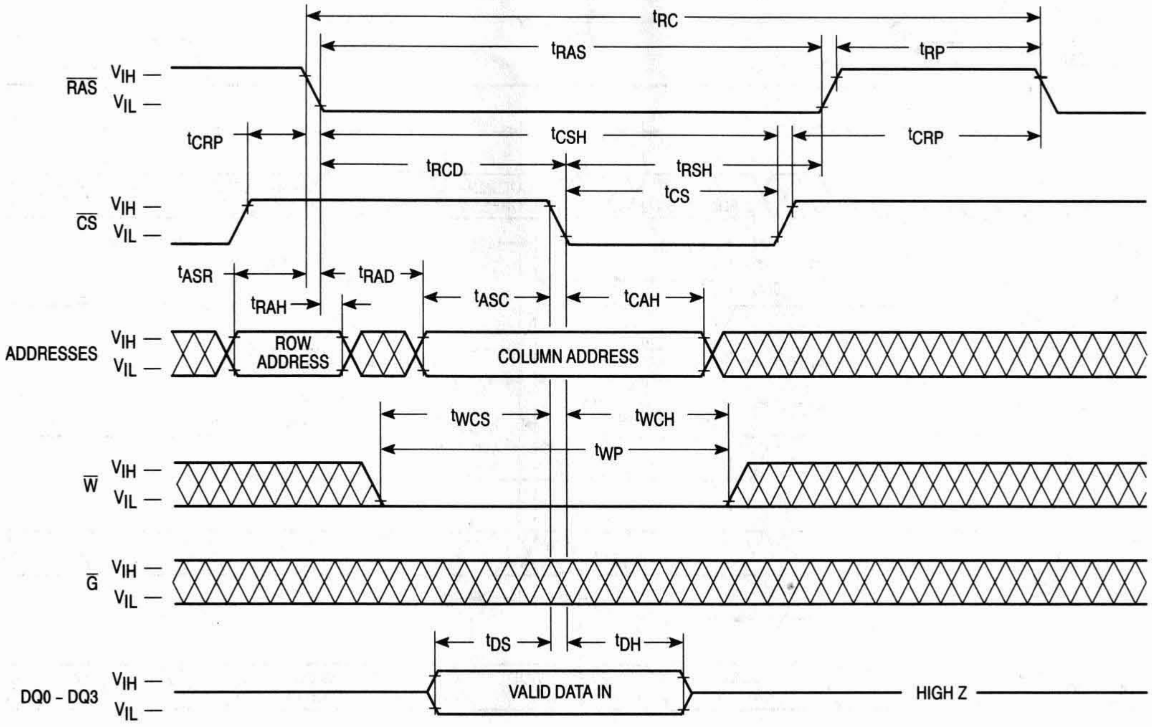
(G and A0 – A9 are Don't Care)


tRC
tRAS
tRP
RAS
VIH –
VIL –
tRPC
tCHR
tCP
tCSR
CS
VIH –
VIL –
tWTS
tWTH
W
VIH –
VIL –
tOFF
DQ0 – DQ3
VOH –
VOL –
HIGH Z

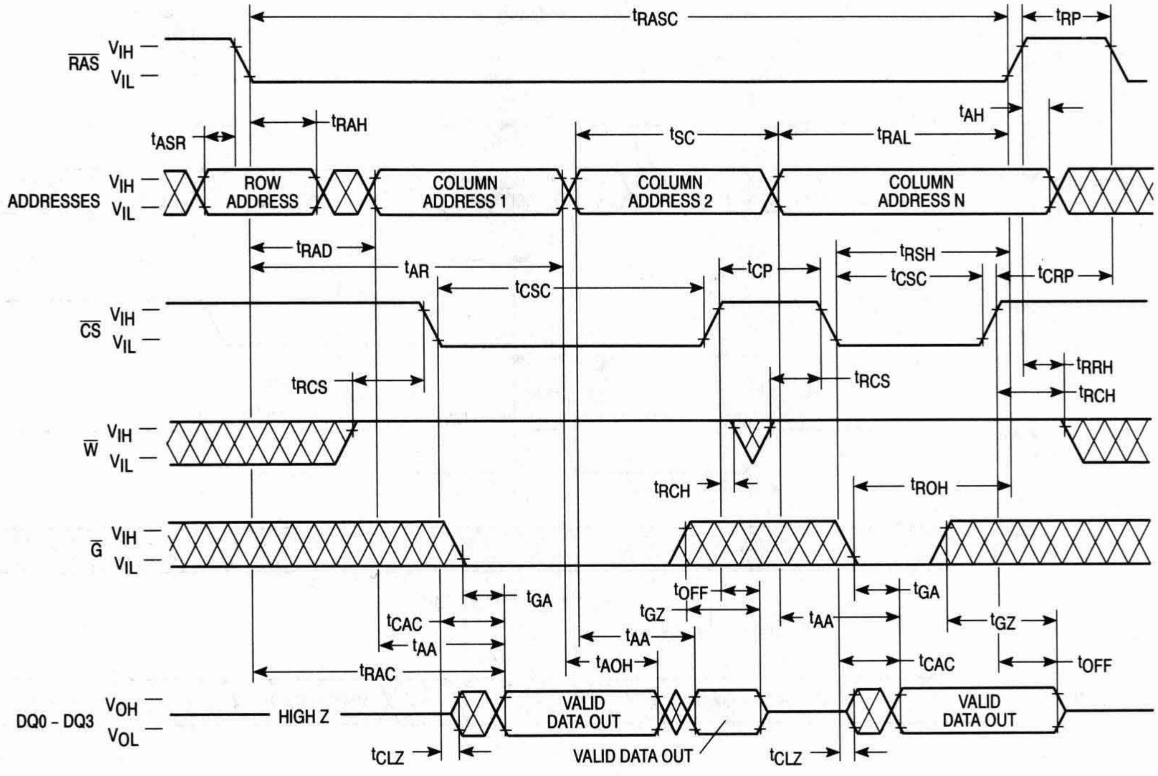
TEST MODE — READ CYCLE


tRC
tRAS
tRP
RAS
VIH –
VIL –
tCSH
tRSH
tCRP
tRCD
tCRP
CS
VIH –
VIL –
tCS
tRAD
tASR
tRAL
tAH
tRAH
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
tRCH
tRCS
tRRH
W
VIH –
VIL –
tROH
tAA
tGA
G
VIH –
VIL –
tCAC
tOFF
tRAC
tGZ
DQ0 – DQ3
VOH –
VOL –
HIGH Z
VALID DATA OUT
tCLZ

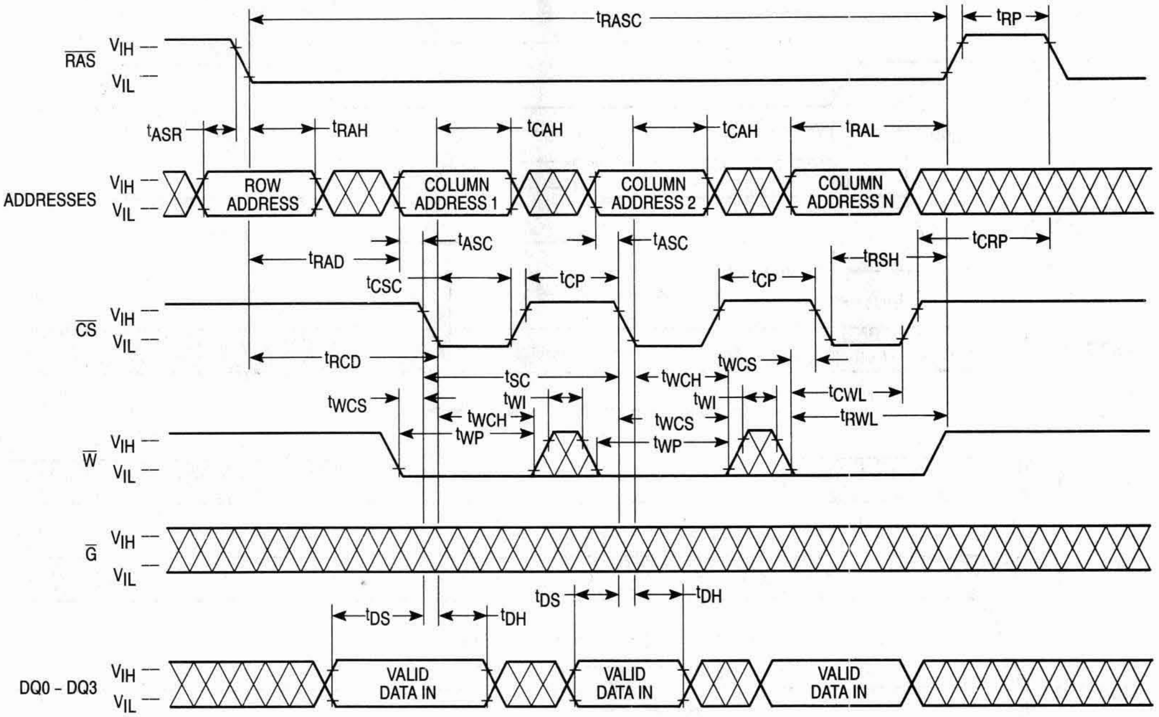
TEST MODE — EARLY WRITE CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tCRP
tCSH
tCRP
tRCD
tRSH
tCS
CS
VIH
VIL
tASR
tRAD
tRAH
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tWCS
tWCH
tWP
W
VIH
VIL
G
VIH
VIL
tDS
tDH
DQ0 - DQ3
VIH
VIL
VALID DATA IN
HIGH Z

TEST MODE — STATIC COLUMN MODE READ CYCLE

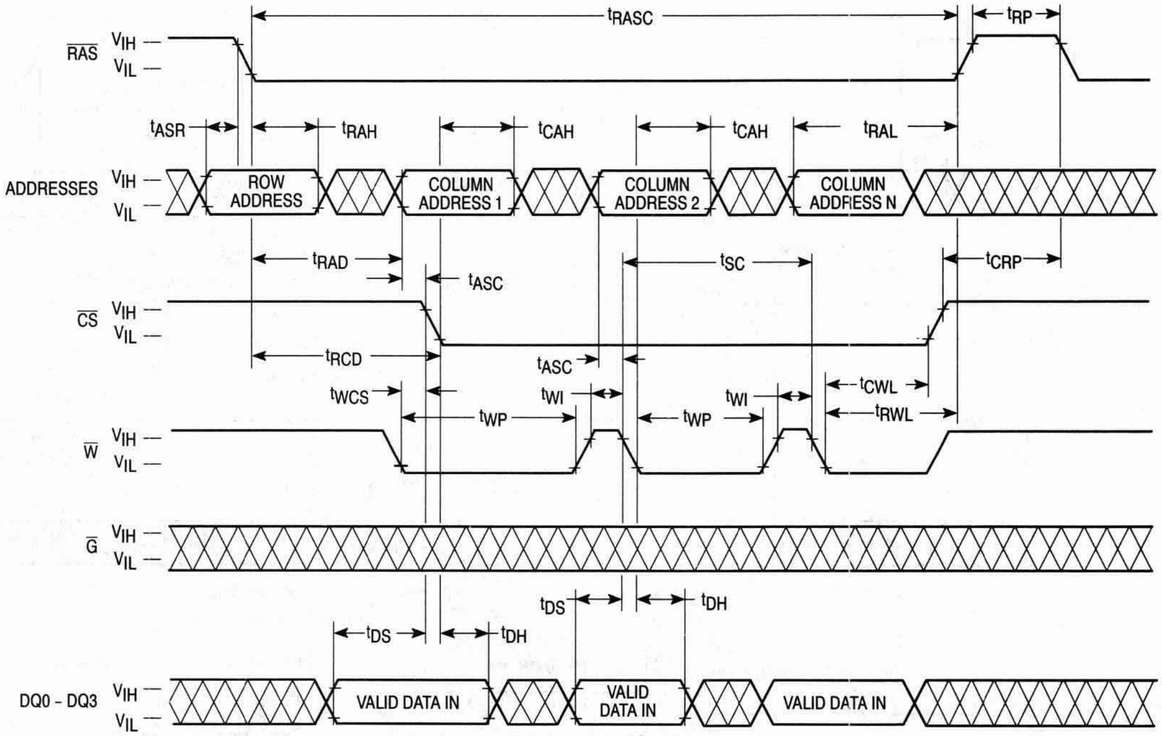

tRASC
tRP
RAS
VIH
VIL
tAH
tASR
tRAH
tSC
tRAL
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS N
tRAD
tAR
tCP
tRSH
tCSC
tCSC
tCRP
CS
VIH
VIL
tRCS
tRCS
tRRH
tRCH
W
VIH
VIL
tRCH
tROH
G
VIH
VIL
tGA
tOFF
tGA
tCAC
tGZ
tAA
tGZ
tAA
tAA
tAOH
tRAC
tCAC
tOFF
DQ0 - DQ3
VOH
VOL
HIGH Z
VALID DATA OUT
VALID DATA OUT
tCLZ
VALID DATA OUT
tCLZ

TEST MODE – STATIC COLUMN MODE EARLY WRITE CYCLE (A)



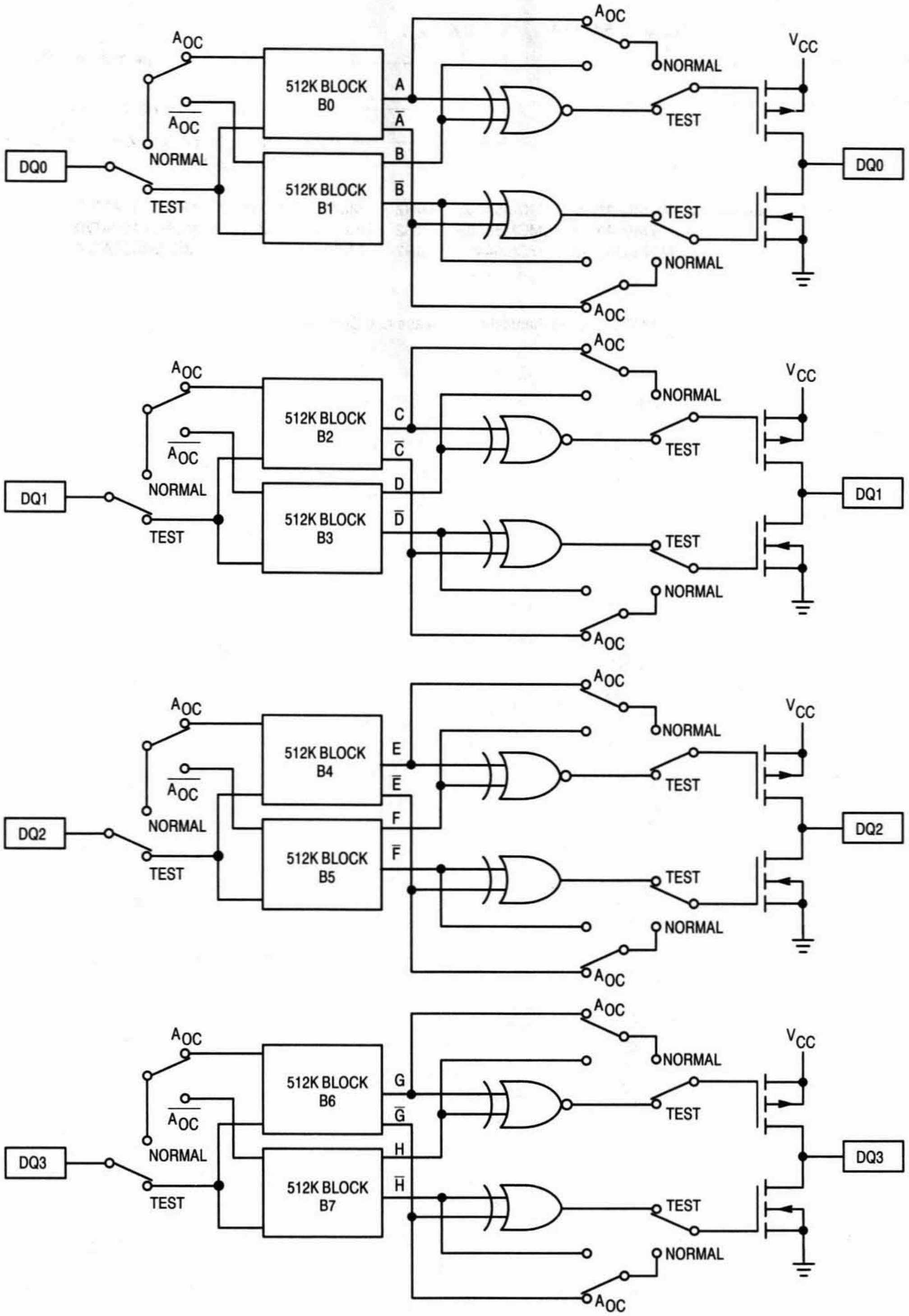
RAS
ADDRESSES
CS
W
G
DQ0 – DQ3
V_IH
V_IL
t_RASC
t_RP
t_ASR
t_RAH
t_CAH
t_CAH
t_RAL
ROW ADDRESS
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS N
t_RAD
t_ASC
t_ASC
t_RSH
t_CRP
t_CSC
t_CP
t_CP
t_RCD
t_SC
t_WCH
t_WCS
t_CWL
t_WCS
t_WI
t_WCH
t_WI
t_WCS
t_RWL
t_WP
t_WP
t_DS
t_DH
t_DS
t_DH
VALID DATA IN
VALID DATA IN
VALID DATA IN

TEST MODE – STATIC COLUMN MODE EARLY WRITE CYCLE (B)



RAS
ADDRESSES
CS
W
G
DQ0 – DQ3
V_IH
V_IL
t_RASC
t_RP
t_ASR
t_RAH
t_CAH
t_CAH
t_RAL
ROW ADDRESS
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS N
t_RAD
t_ASC
t_SC
t_CRP
t_RCD
t_ASC
t_WCS
t_WI
t_WI
t_CWL
t_RWL
t_WP
t_WP
t_DS
t_DH
t_DS
t_DH
VALID DATA IN
VALID DATA IN
VALID DATA IN

TEST MODE BLOCK DIAGRAM



DQ0
DQ1
DQ2
DQ3
512K BLOCK B0
512K BLOCK B1
512K BLOCK B2
512K BLOCK B3
512K BLOCK B4
512K BLOCK B5
512K BLOCK B6
512K BLOCK B7
A_{OC}
$\overline{A_{OC}}$
NORMAL
TEST
A
$\overline{A}$
B
$\overline{B}$
C
$\overline{C}$
D
$\overline{D}$
E
$\overline{E}$
F
$\overline{F}$
G
$\overline{G}$
H
$\overline{H}$
V_{CC}

ORDERING INFORMATION
(Order by Full Part Number)

MCM 54402A X XX XX

Motorola Memory Prefix — MCM

Part Number — 54402A

X — Package (N = 300 mil SOJ, Z = 100 mil Plastic ZIP
T = 300 mil TSOP)

XX — Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns)

XX — Shipping Method (R2 = Tape and Reel, Blank = Rails or Tray)

Full Part Numbers —

MCM54402AN60	MCM54402AN60R2	MCM54402AZ60	MCM54402AT60
MCM54402AN70	MCM54402AN70R2	MCM54402AZ70	MCM54402AT70
MCM54402AN80	MCM54402AN80R2	MCM54402AZ80	MCM54402AT80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM54800A
MCM5L4800A
MCM5V4800A

Advance Information

512K x 8 CMOS Dynamic RAM

Page Mode

The MCM54800A is a 0.7µ CMOS high-speed, dynamic random access memory. It is organized as 524,288 eight-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

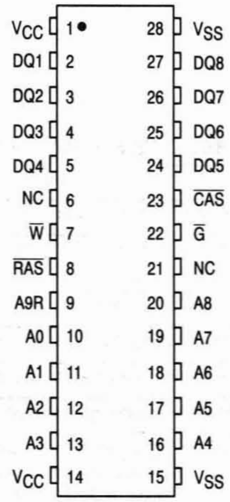
The MCM54800A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 400 mil J-lead small outline package and a 400 mil thin small outline package (TSOP).

- Three-State Data Output
- Fast Page Mode
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- Self Refresh (MCM5V4800A only)
- 1024 Cycle Refresh:
  - MCM54800A = 16 ms
  - MCM5L4800A and MCM5V4800A = 128 ms
- Fast Access Time (t_{RAC}):
  - MCM54800A-70, MCM5L4800A-70, and MCM5V4800A-70 = 70 ns (Max)
  - MCM54800A-80, MCM5L4800A-80, and MCM5V4800A-80 = 80 ns (Max)
  - MCM54800A-10, MCM5L4800A-10, and MCM5V4800A-10 = 100 ns (Max)
- Low Active Power Dissipation:
  - MCM54800A-70, MCM5L4800A-70, and MCM5V4800A-70 = 578 mW (Max)
  - MCM54800A-80, MCM5L4800A-80, and MCM5V4800A-80 = 495 mW (Max)
  - MCM54800A-10, MCM5L4800A-10, and MCM5V4800A-10 = 440 mW (Max)
- Low Standby Power Dissipation:
  - MCM54800A, MCM5L4800A, and MCM5V4800A = 11 mW (Max, TTL Levels)
  - MCM54800A = 5.5 mW (Max, CMOS Levels)
  - MCM54L800A and MCM5V4800A = 1.1 mW (Max, CMOS Levels)
- Battery Backup Power Dissipation:
  - MCM5L4800A = 1.7 mW (Max, Battery Backup Mode, t_{RC} = 125 µs)
- Self Refresh Power Dissipation:
  - MCM5V4800A = 1.1 mW (Max, Self Refresh Mode)

J PACKAGE
400 MIL SOJ
CASE 810-03

T PACKAGE
400 MIL TSOP
CASE 899-01

PIN ASSIGNMENT

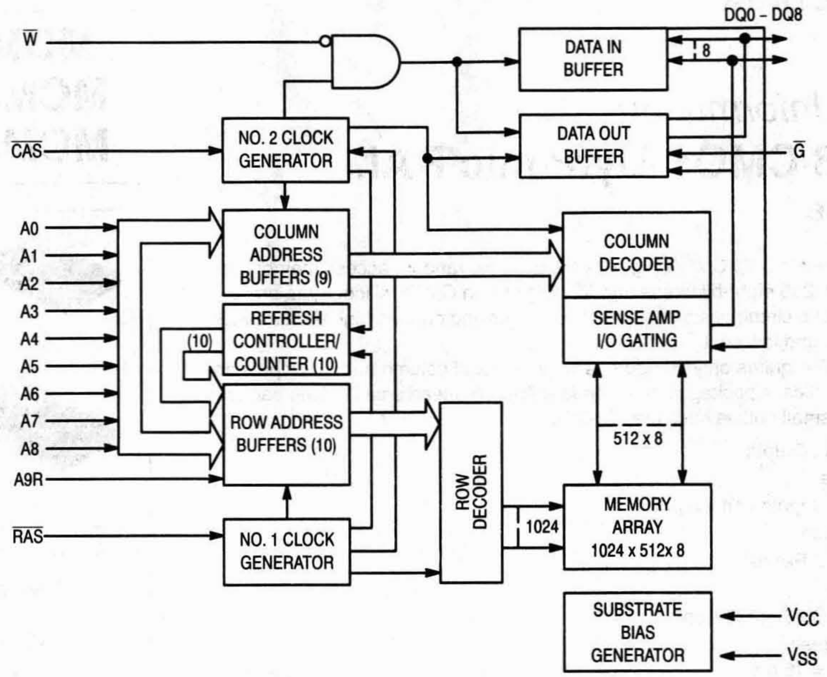


PIN NAMES

A0 – A8, A9R	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{W}}$	Write Input
$\overline{\text{G}}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connect

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM


DQ0 – DQ8
W
DATA IN BUFFER
8
NO. 2 CLOCK GENERATOR
DATA OUT BUFFER
CAS
G
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9R
COLUMN ADDRESS BUFFERS (9)
COLUMN DECODER
REFRESH CONTROLLER/ COUNTER (10)
(10)
SENSE AMP I/O GATING
ROW ADDRESS BUFFERS (10)
512 x 8
ROW DECODER
1024
MEMORY ARRAY 1024 x 512x 8
RAS
NO. 1 CLOCK GENERATOR
SUBSTRATE BIAS GENERATOR
VCC
VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs Except DQ0 – DQ7	V_{IL}	– 1.0*	—	0.8	V
Logic Low Voltage, DQ0 – DQ7	V_{IL}	– 0.5**	—	0.8	V

*– 2.5 V at pulse width ≤ 20 ns

**– 2.0 V at pulse width ≤ 20 ns

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	1, 2
MCM54800A-70, MCM5L4800A-70, and MCM5V4800A-70, t_{RC} = 130 ns		—	105		
MCM54800A-80, MCM5L4800A-80, and MCM5V4800A-80, t_{RC} = 150 ns		—	90		
MCM54800A-10, MCM5L4800A-10, and MCM5V4800A-10, t_{RC} = 180 ns		—	80		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	1, 2
MCM54800A-70, MCM5L4800A-70, and MCM5V4800A-70, t_{RC} = 130 ns		—	105		
MCM54800A-80, MCM5L4800A-80, and MCM5V4800A-80, t_{RC} = 150 ns		—	90		
MCM54800A-10, MCM5L4800A-10, and MCM5V4800A-10, t_{RC} = 180 ns		—	80		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	1, 2
MCM54800A-70, MCM5L4800A-70, and MCM5V4800A-70, t_{PC} = 45 ns		—	75		
MCM54800A-80, MCM5L4800A-80, and MCM5V4800A-80, t_{PC} = 50 ns		—	65		
MCM54800A-10, MCM5L4800A-10, and MCM5V4800A-10, t_{PC} = 60 ns		—	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM54800A	I_{CC5}	—	1.0	mA	
MCM5L4800A and MCM5V4800A		—	200	µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	1
MCM54800A-70, MCM5L4800A-70, and MCM5V4800A-70, t_{RC} = 130 ns		—	105		
MCM54800A-80, MCM5L4800A-80, and MCM5V4800A-80, t_{RC} = 150 ns		—	90		
MCM54800A-10, MCM5L4800A-10, and MCM5V4800A-10, t_{RC} = 180 ns		—	80		
V_{CC} Power Supply Current, Battery Backup Mode—MCM5L4800A Only (t_{RC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0 – A8, A9R, $\overline{W}$, D = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	—	300	µA	1, 3
V_{CC} Power Supply Current, Self Refresh Mode — MCM5V4800A Only ($\overline{RAS}$ = $\overline{CAS}$ = V_{IL}; A0 – A8, A9R, $\overline{W}$, $\overline{G}$ = V_{CC} – 0.2 V or 0.2 V; DQ0–DQ7 = V_{CC} – 0.2 V, 0.2 V, or Open)	I_{CC8}	—	200	µA	
Input Leakage Current (0 V ≤ V_{in} ≤ 7.0 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ 7.0 V, Output Disable)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading. Maximum currents are at the specified cycle time (min) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery back-up. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, periodically sampled, not 100% tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A8, A9R	C_{in}	5	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{G}$		7	
Input/Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0 – DQ7	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\,\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, and 4)

	Symbol		MCM54800A-70 MCM5L4800A-70 MCM5V4800A-70		MCM54800A-80 MCM5L4800A-80 MCM5V4800A-80		MCM54800A-10 MCM5L4800A-10 MCM5V4800A-10			
Parameter	**Std**	**Alt**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	180	—	ns	5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RWC}	185	—	205	—	245	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	50	—	60	—	ns	
Page Mode Read-Modify-Write Cycle Time	t_{CELCEL}	t_{PRWC}	100	—	105	—	125	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	—	100	ns	6, 8, 9
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	50	ns	6, 9
Access Time from $\overline{\text{CAS}}$ Precharge	t_{CEHQV}	t_{CPA}	—	40	—	45	—	55	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	7
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	70	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	8
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	9
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Page Mode Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Hold Time From $\overline{\text{CAS}}$ Precharge (Page Mode Only)	t_{CEHREH}	t_{RHCP}	40	—	45	—	55	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELAX}	t_{AR}	55	—	60	—	75	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	50	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles or 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0 \leq T_A \leq 70$°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. t_{OFF} (max) and t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

	Symbol		MCM54800A-70 MCM5L4800A-70 MCM5V4800A-70		MCM54800A-80 MCM5L4800A-80 MCM5V4800A-80		MCM54800A-10 MCM5L4800A-10 MCM5V4800A-10			
Parameter	**Std**	**Alt**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	10
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{CELWH}	t_{WCH}	15	—	15	—	20	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{RELWH}	t_{WCR}	55	—	60	—	75	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	11
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	20	—	ns	11
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	55	—	60	—	75	—	ns	
Refresh Period MCM54800A MCM5L4800A and MCM5V4800A	t_{RVRV}	t_{RFSH}	—	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	12
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	60	—	ns	12
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	100	—	110	—	135	—	ns	12
Column Address to Write Delay	t_{AVWL}	t_{AWD}	65	—	70	—	85	—	ns	12
$\overline{\text{CAS}}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	70	—	75	—	90	—	ns	12
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle	t_{RELCEH}	t_{CHR}	15	—	15	—	20	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test)	t_{CEHCEL}	t_{CPT}	40	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{G}}$	t_{GLREH}	t_{ROH}	10	—	10	—	20	—	ns	
$\overline{\text{G}}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	20	—	25	ns	6
$\overline{\text{G}}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	25	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{\text{G}}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	25	ns	7
$\overline{\text{G}}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	25	—	ns	
Output Disable Setup Time	t_{GLCEL}	t_{GDS}	0	—	0	—	0	—	ns	

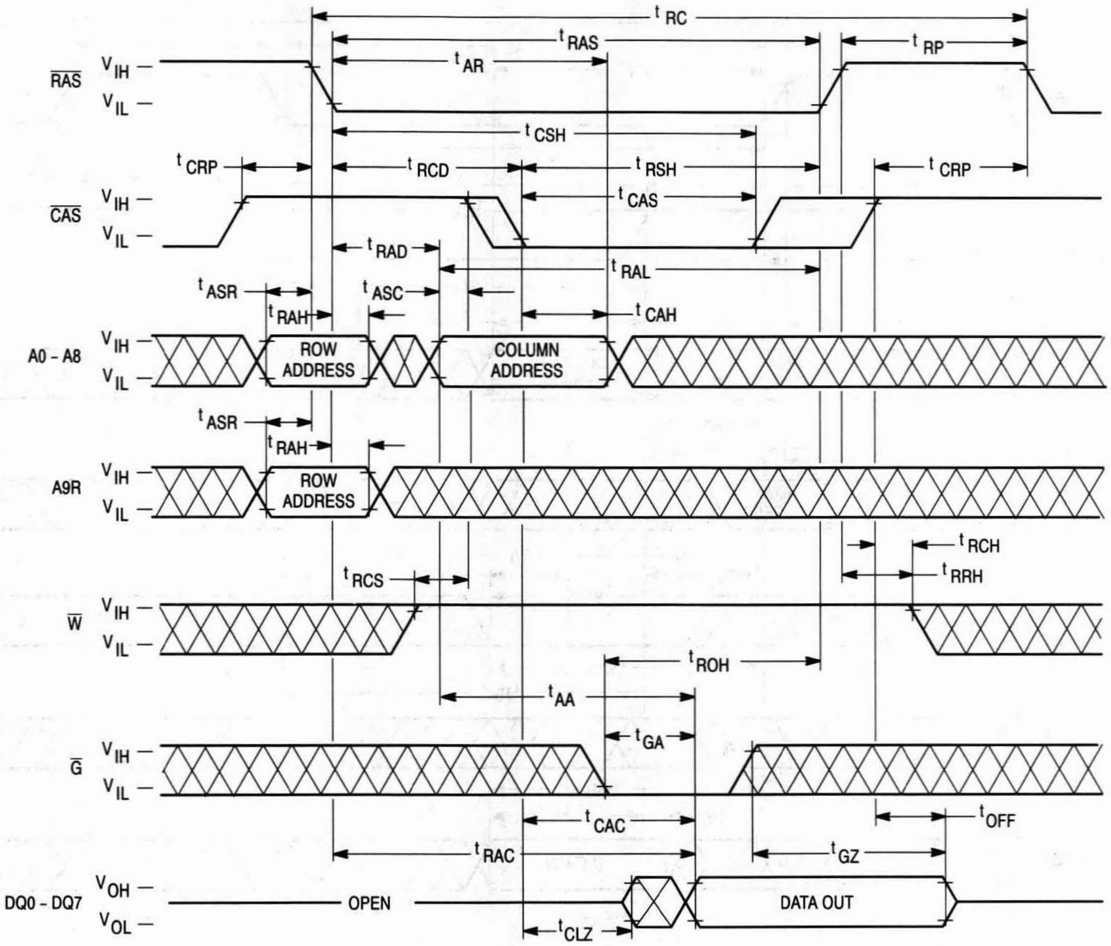
NOTES:

10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in late write or read-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

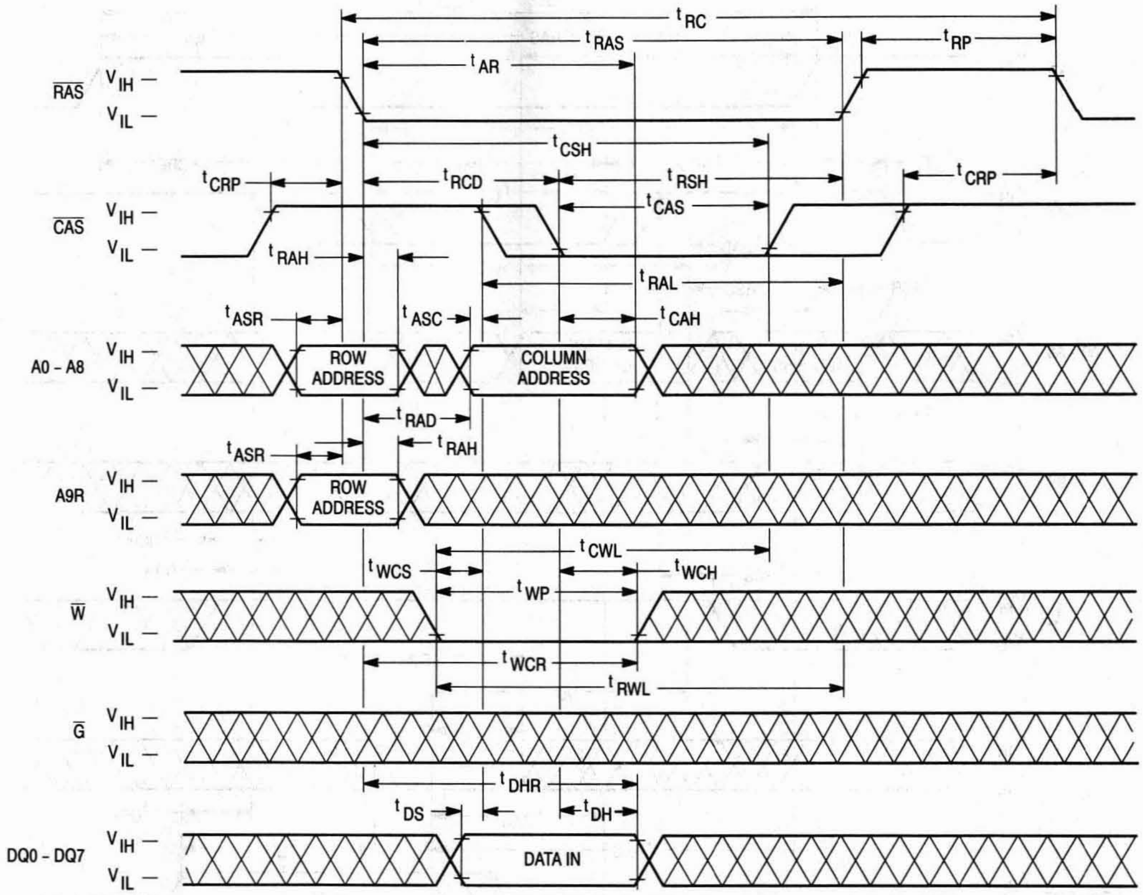
SELF REFRESH CYCLE

Parameter	Symbol		MCM54800A-70 MCM5L4800A-70 MCM5V4800A-70		MCM54800A-80 MCM5L4800A-80 MCM5V4800A-80		MCM54800A-10 MCM5L4800A-10 MCM5V4800A-10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ Before $\overline{RAS}$ Self Refresh, MCM5V4800A Only)	$t_{RELREHS}$	t_{RASS}	100	—	100	—	100	—	µs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Self Refresh, MCM5V4800A Only)	$t_{REHRELS}$	t_{RPS}	130	—	150	—	180	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Self Refresh, MCM5V4800A Only)	t_{REHCEH}	t_{CHS}	− 50	—	− 60	—	− 70	—	ns	

READ CYCLE

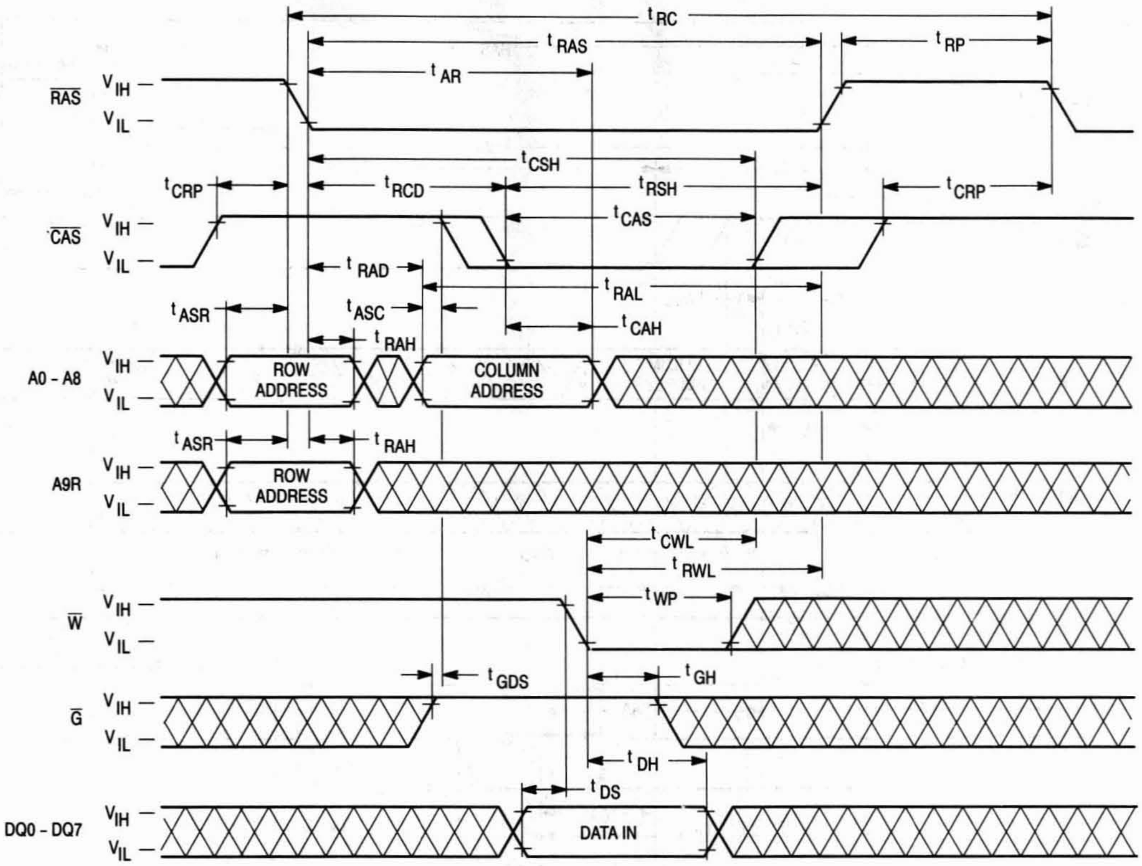

t RC
t RAS
t RP
t AR
RAS
V IH
V IL
t CSH
t CRP
t RCD
t RSH
t CRP
t CAS
CAS
V IH
V IL
t RAD
t RAL
t ASR
t ASC
t RAH
t CAH
A0 - A8
V IH
V IL
ROW ADDRESS
COLUMN ADDRESS
t ASR
t RAH
A9R
V IH
V IL
ROW ADDRESS
t RCH
t RCS
t RRH
W
V IH
V IL
t ROH
t AA
t GA
G
V IH
V IL
t CAC
t OFF
t RAC
t GZ
DQ0 - DQ7
V OH
V OL
OPEN
DATA OUT
t CLZ

EARLY WRITE CYCLE



t_{RC}
t_{RAS}
t_{RP}
t_{AR}
RAS
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
CAS
t_{RAH}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
A0 - A8
ROW ADDRESS
COLUMN ADDRESS
t_{RAD}
t_{RAH}
t_{ASR}
A9R
ROW ADDRESS
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
W
t_{WCR}
t_{RWL}
G
t_{DHR}
t_{DS}
t_{DH}
DQ0 - DQ7
DATA IN

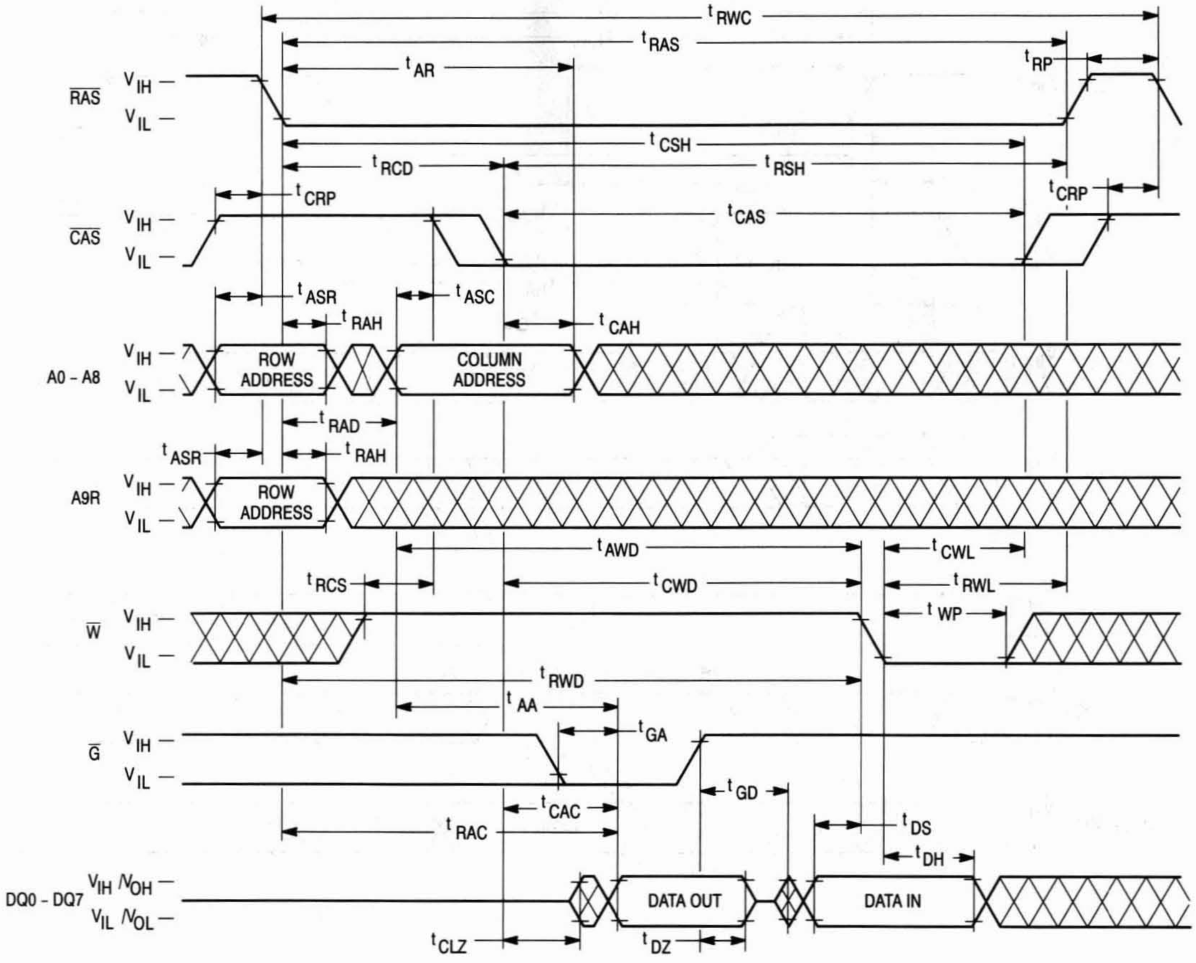
$\overline{G}$ CONTROLLED WRITE CYCLE



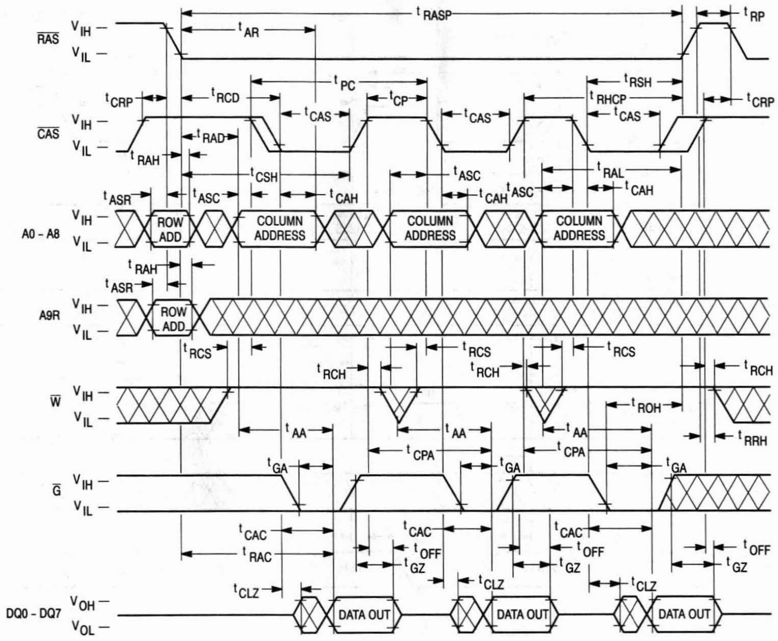
tRC
tRAS
tRP
tAR
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
tRAD
tRAL
tASR
tASC
tCAH
tRAH
A0 - A8
ROW ADDRESS
COLUMN ADDRESS
tASR
tRAH
A9R
ROW ADDRESS
tCWL
tRWL
tWP
W
tGDS
tGH
G
tDH
tDS
DQ0 - DQ7
DATA IN

3

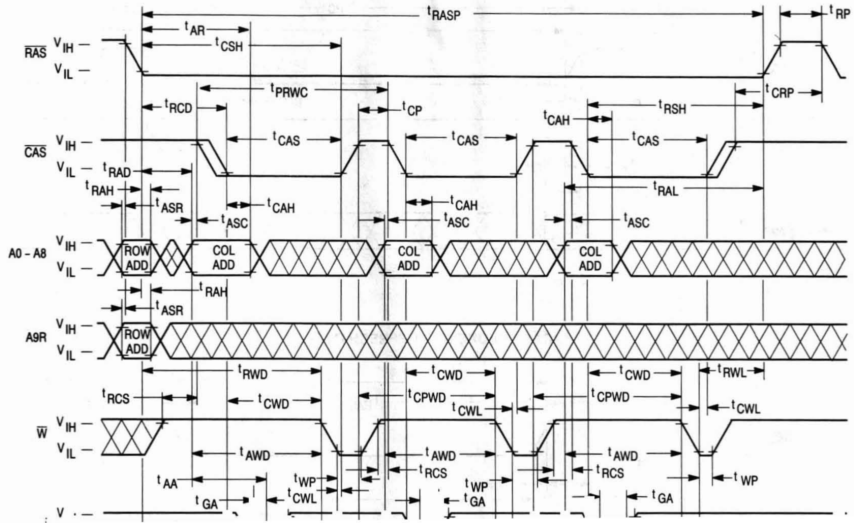
READ-MODIFY-WRITE CYCLE


t RWC
t RAS
t AR
t RP
RAS
V IH
V IL
t CSH
t RCD
t RSH
t CRP
t CRP
CAS
V IH
V IL
t CAS
t ASR
t ASC
t RAH
t CAH
A0 – A8
V IH
V IL
ROW ADDRESS
COLUMN ADDRESS
t RAD
t ASR
t RAH
A9R
V IH
V IL
ROW ADDRESS
t AWD
t CWL
t RCS
t CWD
t RWL
W
V IH
V IL
t WP
t RWD
t AA
G
V IH
V IL
t GA
t GD
t CAC
t DS
t RAC
t DH
DQ0 – DQ7
V IH /V OH
V IL /V OL
DATA OUT
DATA IN
t CLZ
t DZ

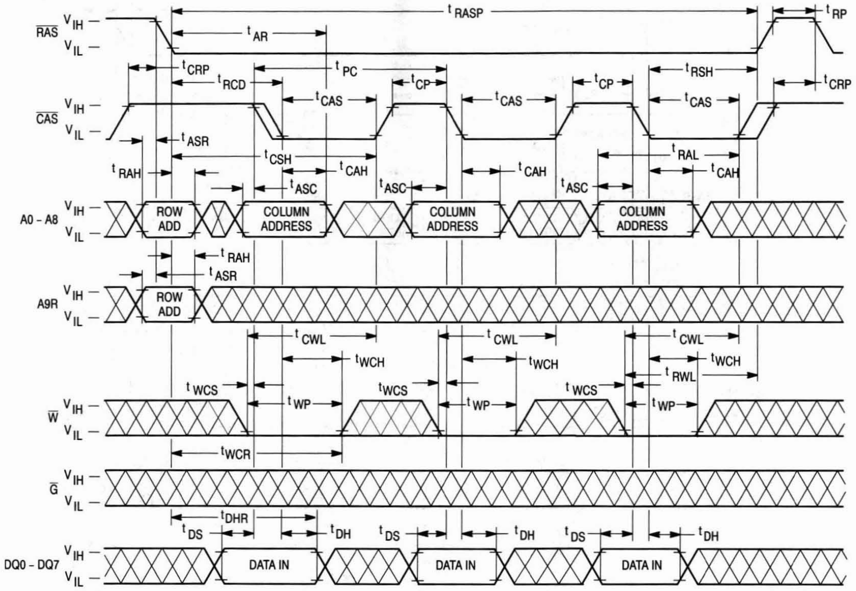
FAST PAGE MODE READ CYCLE


$\overline{RAS}$
V_{IH} –
V_{IL} –
t_{RASP}
t_{RP}
t_{AR}
t_{PC}
t_{RSH}
t_{CRP}
t_{RCD}
t_{CAS}
t_{CP}
t_{RHCP}
$\overline{CAS}$
t_{RAD}
t_{RAH}
t_{CSH}
t_{ASC}
t_{RAL}
t_{ASR}
t_{CAH}
A0 - A8
ROW ADD
COLUMN ADDRESS
A9R
t_{RCS}
t_{RCH}
$\overline{W}$
t_{ROH}
t_{AA}
t_{RRH}
t_{CPA}
t_{GA}
$\overline{G}$
t_{CAC}
t_{RAC}
t_{OFF}
t_{GZ}
t_{CLZ}
DQ0 - DQ7
V_{OH} –
V_{OL} –
DATA OUT

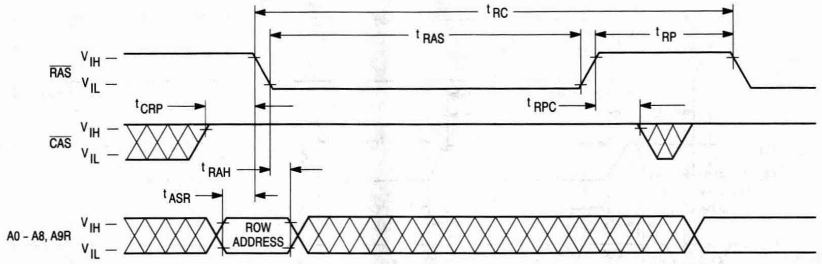
FAST PAGE MODE READ-MODIFY-WRITE CYCLE


$\overline{RAS}$
V_{IH} –
V_{IL} –
t_{RASP}
t_{RP}
t_{AR}
t_{CSH}
t_{PRWC}
t_{RCD}
t_{CP}
t_{CRP}
t_{CAH}
t_{RSH}
t_{CAS}
$\overline{CAS}$
t_{RAD}
t_{RAH}
t_{ASR}
t_{ASC}
t_{RAL}
A0 - A8
ROW ADD
COL ADD
A9R
t_{RWD}
t_{CWD}
t_{RWL}
t_{RCS}
t_{CPWD}
t_{CWL}
$\overline{W}$
t_{AWD}
t_{AA}
t_{WP}
t_{GA}

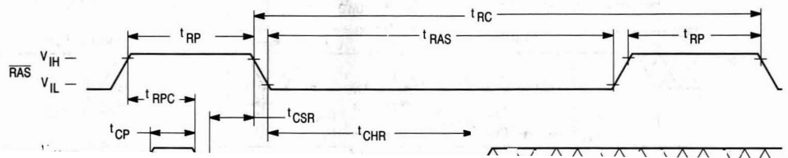
FAST PAGE MODE WRITE CYCLE


tRASP
tRP
tAR
tCRP
tPC
tRCD
tCP
tRSH
tCRP
tCAS
tCAS
tCP
tCAS
RAS
VIH
VIL
CAS
VIH
VIL
tASR
tRAH
tCSH
tCAH
tRAL
tCAH
tCAH
tASC
tASC
tASC
A0 - A8
ROW ADD
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAH
tASR
A9R
ROW ADD
tCWL
tCWL
tCWL
tWCH
tWCH
tWCH
tRWL
tWCS
tWCS
tWCS
tWP
tWP
tWP
W
tWCR
G
tDHR
tDS
tDH
tDS
tDH
tDS
tDH
DQ0 - DQ7
DATA IN
DATA IN
DATA IN

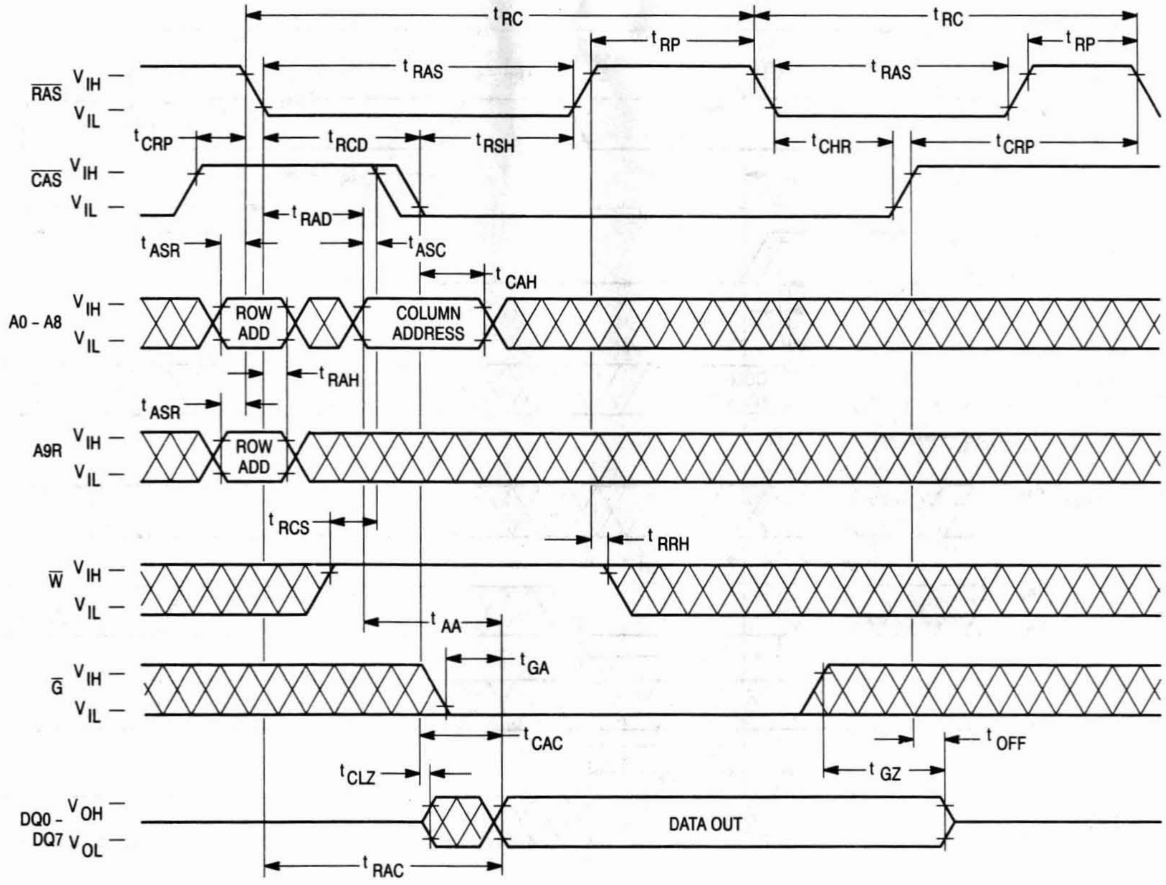
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tCRP
tRPC
CAS
VIH
VIL
tRAH
tASR
A0 - A8, A9R
VIH
VIL
ROW ADDRESS

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

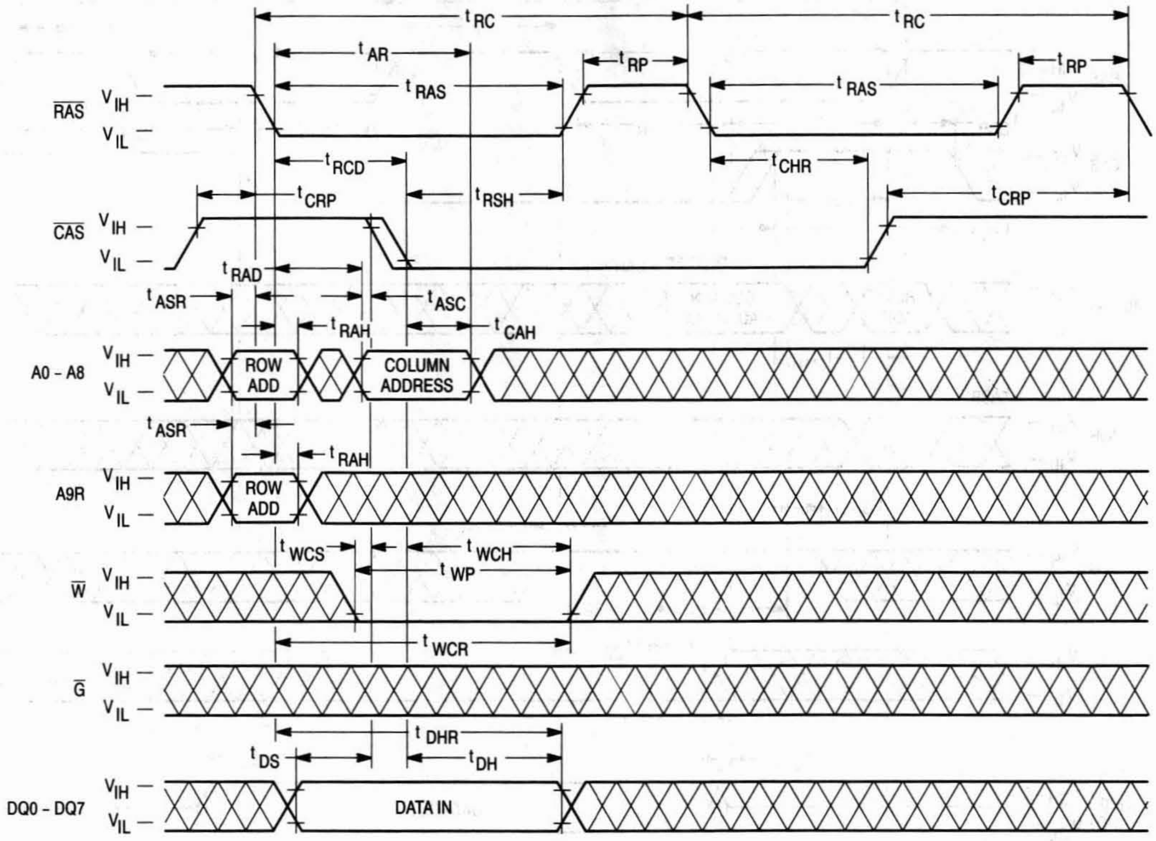

tRC
tRP
tRAS
tRP
RAS
VIH
VIL
tRPC
tCSR
tCP
tCHR

HIDDEN REFRESH CYCLE (READ)

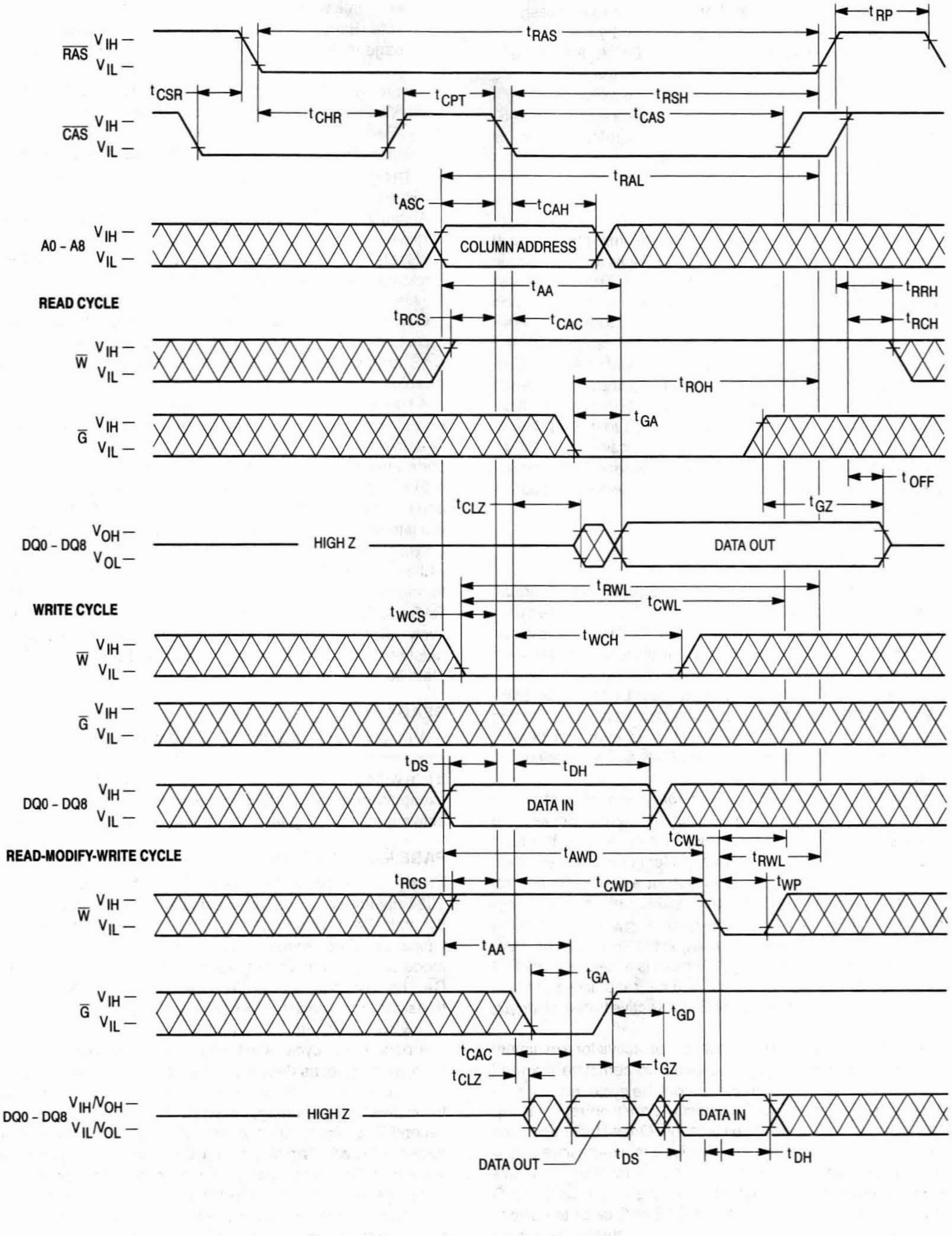


t_{RC}
t_{RC}
t_{RP}
t_{RP}
t_{RAS}
t_{RAS}
RAS
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CRP}
CAS
V_{IH}
V_{IL}
t_{RAD}
t_{ASR}
t_{ASC}
t_{CAH}
A0 - A8
V_{IH}
V_{IL}
ROW ADD
COLUMN ADDRESS
t_{RAH}
t_{ASR}
A9R
V_{IH}
V_{IL}
ROW ADD
t_{RCS}
t_{RRH}
W
V_{IH}
V_{IL}
t_{AA}
t_{GA}
G
V_{IH}
V_{IL}
t_{CAC}
t_{OFF}
t_{CLZ}
t_{GZ}
DQ0 - DQ7
V_{OH}
V_{OL}
DATA OUT
t_{RAC}

HIDDEN REFRESH CYCLE (WRITE)


tRC
tRC
tAR
tRP
tRP
tRAS
tRAS
RAS
VIH
VIL
tRCD
tCHR
tCRP
tRSH
tCRP
CAS
VIH
VIL
tRAD
tASR
tASC
tRAH
tCAH
A0 – A8
VIH
VIL
ROW ADD
COLUMN ADDRESS
tASR
tRAH
A9R
VIH
VIL
ROW ADD
tWCS
tWCH
tWP
W
VIH
VIL
tWCR
G
VIH
VIL
tDHR
tDS
tDH
DQ0 – DQ7
VIH
VIL
DATA IN

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE


RAS V IH
V IL
t RAS
t RP
t CSR
t CPT
t RSH
t CHR
t CAS
CAS V IH
V IL
t RAL
t ASC
t CAH
A0 - A8 V IH
V IL
COLUMN ADDRESS
t AA
t RRH
READ CYCLE
t RCS
t CAC
t RCH
W V IH
V IL
t ROH
t GA
G V IH
V IL
t OFF
t CLZ
t GZ
DQ0 - DQ8 V OH
V OL
HIGH Z
DATA OUT
t RWL
t CWL
WRITE CYCLE
t WCS
t WCH
W V IH
V IL
G V IH
V IL
t DS
t DH
DQ0 - DQ8 V IH
V IL
DATA IN
t CWL
READ-MODIFY-WRITE CYCLE
t AWD
t RWL
t RCS
t CWD
t WP
W V IH
V IL
t AA
t GA
G V IH
V IL
t GD
t CAC
t GZ
t CLZ
DQ0 - DQ8 V IH/V OH
V IL/V OL
HIGH Z
DATA IN
DATA OUT
t DS
t DH

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight $\overline{\text{RAS}}$-Only refresh cycles or $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ refresh cycles to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight $\overline{\text{RAS}}$-Only refresh cycles or $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ refresh cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks and will decode one of the 524,288 bit locations in the device. The row address strobe ($\overline{\text{RAS}}$) latches 10 row addresses, and the column access strobe CAS latches nine column addresses. $\overline{\text{RAS}}$ active transition followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) follows $\overline{\text{RAS}}$ on all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

There are three other variations in addressing the 512K x 8 RAM: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{\text{CAS}}$ and output enable ($\overline{\text{G}}$) control read access time: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum, and $\overline{\text{G}}$ must be active $t_{RAC} - t_{GA}$ (both minimum) to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{\text{G}}$ active transition does not occur in time, read access time is determined by either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ and $\overline{\text{G}}$ clocks are active. When either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers and $\overline{\text{G}}$ disabled.

A late write cycle (referred to as $\overline{\text{G}}$-controlled write) occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but outputs are switched off by $\overline{\text{G}}$ inactive transition, which is required to write to the device. Q may be indeterminate — see note 12 of AC Operating Conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle. $\overline{\text{G}}$ must remain inactive for t_{GH} after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the 512K x 8 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in the prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by

t_{RASP}. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54800A require refresh every 16 milliseconds, while refresh for the MCM5L4800A and MCM5V4800A is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54800A, and 124.8 microseconds for the MCM5L4800A and MCM5V4800A. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54800A, and 128 milliseconds for the MCM5L4800A and MCM5V4800A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decodes. Three other methods of refresh, **RAS-only refresh, CAS before RAS refresh, hidden refresh,** and **self refresh** (MCM5V4800A only) are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure that all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order actives an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1).

Self Refresh (MCM5V4800A Only)

The self refresh is a CAS before RAS refresh where RAS is held low for a period greater than t_{RASS} (100 microseconds). After this time, an internal timer activates a refresh operation of consecutive row addresses in the dynamic RAM. The self refresh mode is exited when either RAS or CAS transitions to high (V_{IH}). Because of the long periods involved for this method of refresh, it is recommended that the self refresh mode only be used for long periods of standby, such as a battery backup.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **eight CAS before RAS** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

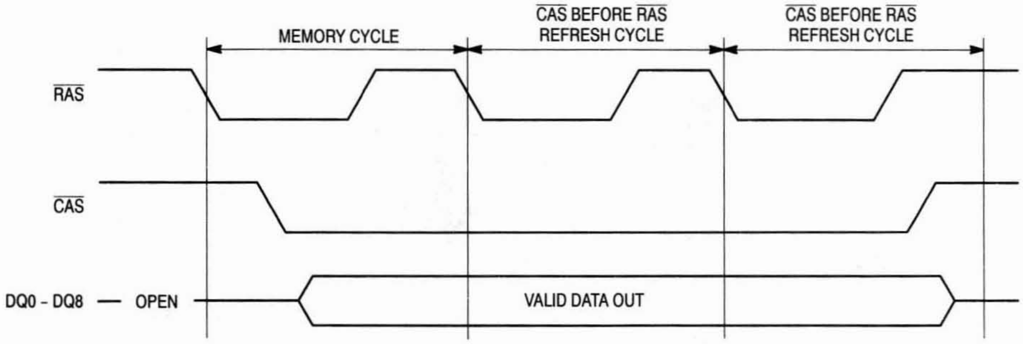


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 54800A XX X XX XX

Motorola Memory Prefix — MCM
Part Number — 54800A
Package (J = 400 mil SOJ, T = 400 mil TSOP) — XX
Temperature Range (C = 0 to 70°C) — X
Speed (70 = 70 ns, 80 = 80 ns, 10 = 100 ns) — XX
Shipping Method (R2 = Tape and Reel, Blank = Rails) — XX

Full Part Numbers —
MCM54800AJ70
MCM54800AJ80
MCM54800AJ10
MCM5L4800AJ70
MCM5L4800AJ80
MCM5L4800AJ10
MCM5V4800AJ70
MCM5V4800AJ80
MCM5V4800AJ10
MCM54800AJ70R2
MCM54800AJ80R2
MCM54800AJ10R2
MCM5L4800AJ70R2
MCM5L4800AJ80R2
MCM5L4800AJ10R2
MCM5V4800AJ70R2
MCM5V4800AJ80R2
MCM5V4800AJ10R2
MCM54800AT70
MCM54800AT80
MCM54800AT10
MCM5L4800AT70
MCM5L4800AT80
MCM5L4800AT10
MCM5V4800AT70
MCM5V4800AT80
MCM5V4800AT10
MCM54800AT70R2
MCM54800AT80R2
MCM54800AT10R2
MCM5L4800AT70R2
MCM5L4800AT80R2
MCM5L4800AT10R2
MCM5V4800AT70R2
MCM5V4800AT80R2
MCM5V4800AT10R2

NOTE: For mechanical data, please see Chapter 10.

CMOS 16M Dynamic RAMs

MCM516100 4-3
MCM516400 4-3
MCM517400 4-3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Advance Information

16M CMOS Dynamic RAM Family
Fast Page Mode, x4 and x1, 2K and 4K Refresh

The family of 16M dynamic RAMs is fabricated using 0.6μ CMOS high-speed silicon-gate process technology. It includes devices organized as 4,194,304 four-bit words and as 16,777,216 one-bit words. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The x4 devices with 4096 cycle refresh (MCM516400) require 12 address lines (12 rows, 10 columns), while the x4 devices with 2048 cycle refresh (MCM517400) require only 11 address lines. The x1 device (MCM516100 page) requires only 12 address lines, as row and column address inputs are multiplexed.

These devices are packaged in a standard 400 mil J-lead small outline package (SOJ) and a 400 mil thin-small-outline package (TSOP).

- Three-State Data Output, x4 and x1 Configurations
- Fast Page Mode
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh: MCM517400 = 32 ms
- 4096 Cycle Refresh: MCM516400 and MCM516100 = 64 ms
- Fast Access Time (t_{RAC}):
  - MCM51xxxx-60 = 60 ns (Max)
  - MCM51xxxx-70 = 70 ns (Max)
- Low Active Power Dissipation:
  - MCM516xxx-60 = 495 mW (Max)
  - MCM516xxx-70 = 440 mW (Max)
  - MCM517xxx-60 = 660 mW (Max)
  - MCM517xxx-70 = 550 mW (Max)
- Low Standby Power Dissipation:
  - All Devices = 11 mW (Max, TTL Levels)
  - All Devices = 5.5 mW (Max, CMOS Levels)

4M x 4

MCM516400
Fast Page Mode
4096 Cycle Refresh

MCM517400
Fast Page Mode
2048 Cycle Refresh

16M x 1

MCM516100
Fast Page Mode
4096 Cycle Refresh

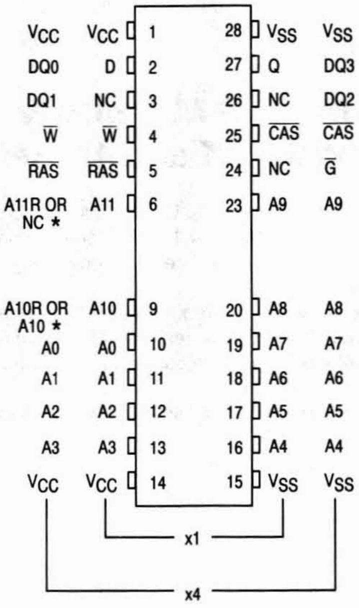
J PACKAGE
400 MIL SOJ
CASE 810C-01

T PACKAGE
400 MIL TSOP II
CASE 899A-01

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN ASSIGNMENTS

400 MIL SOJ
400 MIL TSOP



V_{CC} V_{CC} 1 28 V_{SS} V_{SS}
DQ0 D 2 27 Q DQ3
DQ1 NC 3 26 NC DQ2
$\overline{W}$ $\overline{W}$ 4 25 $\overline{CAS}$ $\overline{CAS}$
$\overline{RAS}$ $\overline{RAS}$ 5 24 NC $\overline{G}$
A11R OR NC * A11 6 23 A9 A9
A10R OR A10 * A10 9 20 A8 A8
A0 A0 10 19 A7 A7
A1 A1 11 18 A6 A6
A2 A2 12 17 A5 A5
A3 A3 13 16 A4 A4
V_{CC} V_{CC} 14 15 V_{SS} V_{SS}
x1
x4

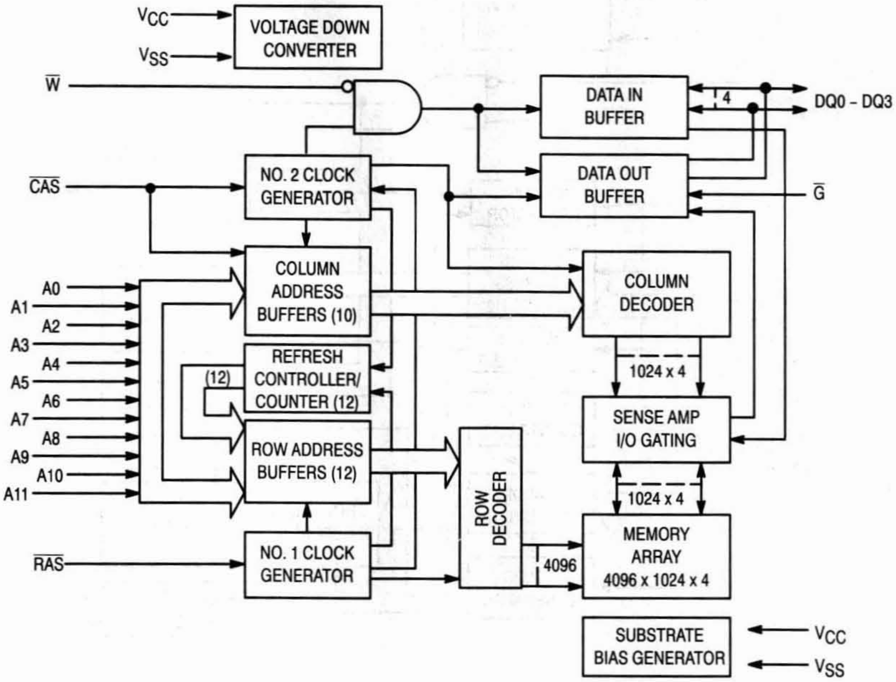
* 4096 Cycle Refresh or
2048 Cycle Refresh
(R suffix = Row Address)

PIN NAMES

A0 – A11	Address Input	$\overline{RAS}$	Row Address Strobe
DQ0 – DQ3	Data Input/Output	$\overline{CAS}$	Column Address Strobe
D	Data Input	V_{CC}	Power Supply (+ 5 V)
Q	Data Output	V_{SS}	Ground
$\overline{G}$	Output Enable	NC	No Connection
$\overline{W}$	Read/Write Enable		

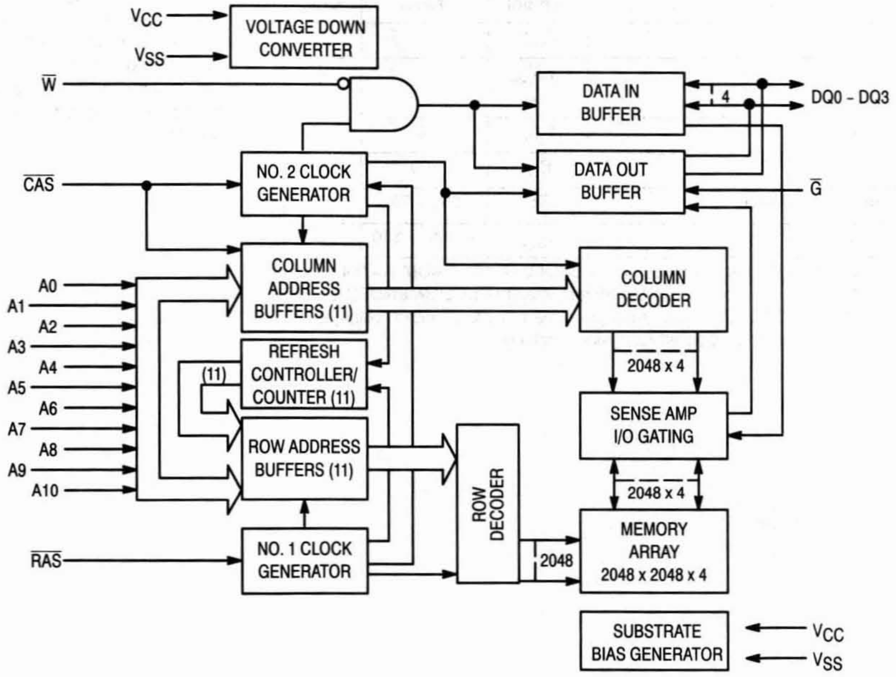
BLOCK DIAGRAMS

4M x 4, 4096 CYCLE REFRESH BLOCK DIAGRAM
MCM516400



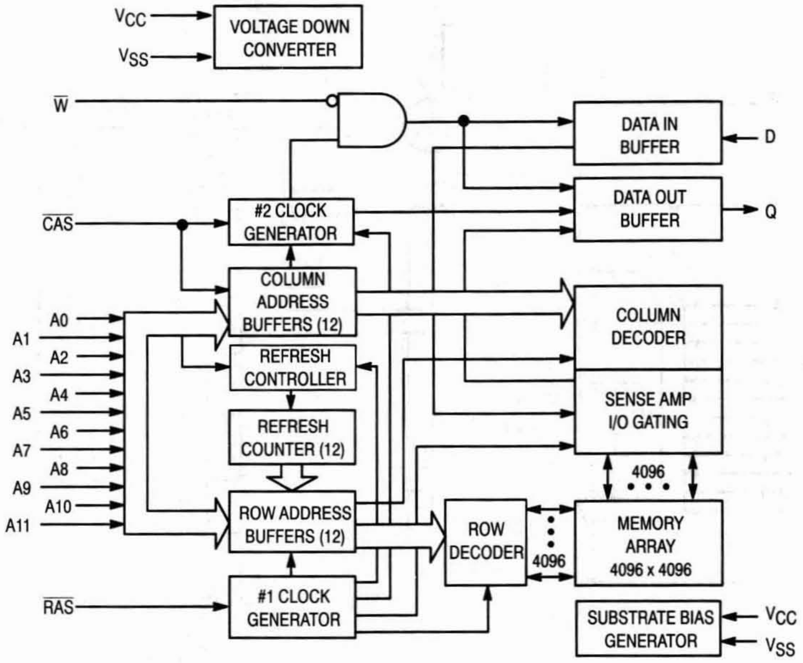
VCC
VSS
VOLTAGE DOWN CONVERTER
W̄
DATA IN BUFFER
4
DQ0 – DQ3
NO. 2 CLOCK GENERATOR
CAS̄
DATA OUT BUFFER
Ḡ
COLUMN ADDRESS BUFFERS (10)
COLUMN DECODER
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
REFRESH CONTROLLER/ COUNTER (12)
(12)
1024 x 4
SENSE AMP I/O GATING
ROW ADDRESS BUFFERS (12)
ROW DECODER
1024 x 4
MEMORY ARRAY 4096 x 1024 x 4
RĀS
NO. 1 CLOCK GENERATOR
4096
SUBSTRATE BIAS GENERATOR
VCC
VSS

4M x 4, 2048 CYCLE REFRESH BLOCK DIAGRAM
MCM517400



VCC
VSS
VOLTAGE DOWN CONVERTER
W̄
DATA IN BUFFER
4
DQ0 – DQ3
NO. 2 CLOCK GENERATOR
CAS̄
DATA OUT BUFFER
Ḡ
COLUMN ADDRESS BUFFERS (11)
COLUMN DECODER
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
REFRESH CONTROLLER/ COUNTER (11)
(11)
2048 x 4
SENSE AMP I/O GATING
ROW ADDRESS BUFFERS (11)
ROW DECODER
2048 x 4
MEMORY ARRAY 2048 x 2048 x 4
RĀS
NO. 1 CLOCK GENERATOR
2048
SUBSTRATE BIAS GENERATOR
VCC
VSS

16M x 1 BLOCK DIAGRAM
MCM516100


V_{CC}
V_{SS}
VOLTAGE DOWN CONVERTER
$\overline{W}$
DATA IN BUFFER
D
DATA OUT BUFFER
Q
$\overline{CAS}$
#2 CLOCK GENERATOR
COLUMN ADDRESS BUFFERS (12)
COLUMN DECODER
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
REFRESH CONTROLLER
REFRESH COUNTER (12)
SENSE AMP I/O GATING
4096
ROW ADDRESS BUFFERS (12)
ROW DECODER
4096
MEMORY ARRAY 4096 x 4096
$\overline{RAS}$
#1 CLOCK GENERATOR
SUBSTRATE BIAS GENERATOR
V_{CC}
V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current	I_{out}	50	mA
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	V_{CC} + 0.5 V	V
Logic Low Voltage, All Inputs	V_{IL}	– 0.5*	—	0.8	V

* –2.0 V at pulse width ≤ 20 ns.

DC CHARACTERISTICS AND SUPPLY CURRENTS (All voltages referenced to V_{SS})

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM516xxx-60, t_{RC} = 110 ns MCM516xxx-70, t_{RC} = 130 ns MCM517400-60, t_{RC} = 110 ns MCM517400-70, t_{RC} = 130 ns	I_{CC1}	 — — — —	 90 80 120 100	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles ($\overline{CAS}$ = V_{IH}) MCM516xxx-60, t_{RC} = 110 ns MCM516xxx-70, t_{RC} = 130 ns MCM517400-60, t_{RC} = 110 ns MCM517400-70, t_{RC} = 130 ns	I_{CC3}	 — — — —	 90 80 120 100	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL}) MCM516100-60, MCM516400-60, MCM517400-60, t_{PC} = 40 ns MCM516100-70, MCM516400-70, MCM517400-70, t_{PC} = 45 ns	$I_{CC4(P)}$	 — —	 70 60	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM516xxx-60, t_{RC} = 110 ns MCM516xxx-70, t_{RC} = 130 ns MCM517400-60, t_{RC} = 110 ns MCM517400-70, t_{RC} = 130 ns	I_{CC6}	 — — — —	 90 80 120 100	mA	1
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC})	$I_{lkg(I)}$	–10	10	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ V_{CC}, Output Disable)	$I_{lkg(O)}$	–10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Address may be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less during t_{PC}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A11, D	C_{in}	5	pF
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0 – DQ3, Q	$C_{I/O}$	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

16M FAMILY AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

ALL DEVICES: READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM51xxxx-60		MCM51xxxx-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	ns	5
Read-Write Cycle Time MCM5161xx MCM5164xx, MCM517400	t_{RELREL}	t_{RWC}	130 155	— —	155 180	— —	ns	5
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	15	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	15	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	15	—	20	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	ns	
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	15	10 k	20	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	45	20	50	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	10	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ALL DEVICES: READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM51xxxx-60		MCM51xxxx-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	15	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	15	—	20	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data In Hold Time	t_{CELDX}	t_{DH}	10	—	15	—	ns	14
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
$\overline{\text{CAS}}$ to Write Delay MCM5161xx MCM5164xx, MCM517400	t_{CELWL}	t_{CWD}	15 40	— —	20 45	— —	ns	15
$\overline{\text{RAS}}$ to Write Delay MCM5161xx MCM5164xx, MCM517400	t_{RELWL}	t_{RWD}	60 85	— —	70 95	— —	ns	15
Column Address to Write Delay MCM5161xx MCM5164xx, MCM517400	t_{AVWL}	t_{AWD}	30 55	— —	35 60	— —	ns	15
Refresh Period MCM5161xx MCM5164xx MCM517400	t_{RVRV}	t_{RFSH}	— — —	64 64 32	— — —	64 64 32	ms	
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	10	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Time	t_{CEHCEL}	t_{CPT}	20	—	30	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	ns	

NOTES:

14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in late write or read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

DEVICE-SPECIFIC AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

4M x 4 CONFIGURATION-SPECIFIC READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM5164xx-60 MCM5174xx-60		MCM5164xx-70 MCM5174xx-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{G}}$	t_{GLREH}	t_{ROH}	10	—	10	—	ns	
$\overline{\text{G}}$ Access Time	t_{GLQV}	t_{GA}	—	15	—	20	ns	5
$\overline{\text{G}}$ to Data Delay	t_{GLHDX}	t_{GD}	15	—	15	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{\text{G}}$	t_{GHQZ}	t_{GZ}	0	15	0	15	ns	6
$\overline{\text{G}}$ Command Hold Time	t_{WLGL}	t_{GH}	15	—	15	—	ns	
Output Disable Setup Time	t_{GHCEL}	t_{ODS}	0	—	0	—	ns	

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
6. t_{OFF} (max) and/or t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

FAST PAGE MODE READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

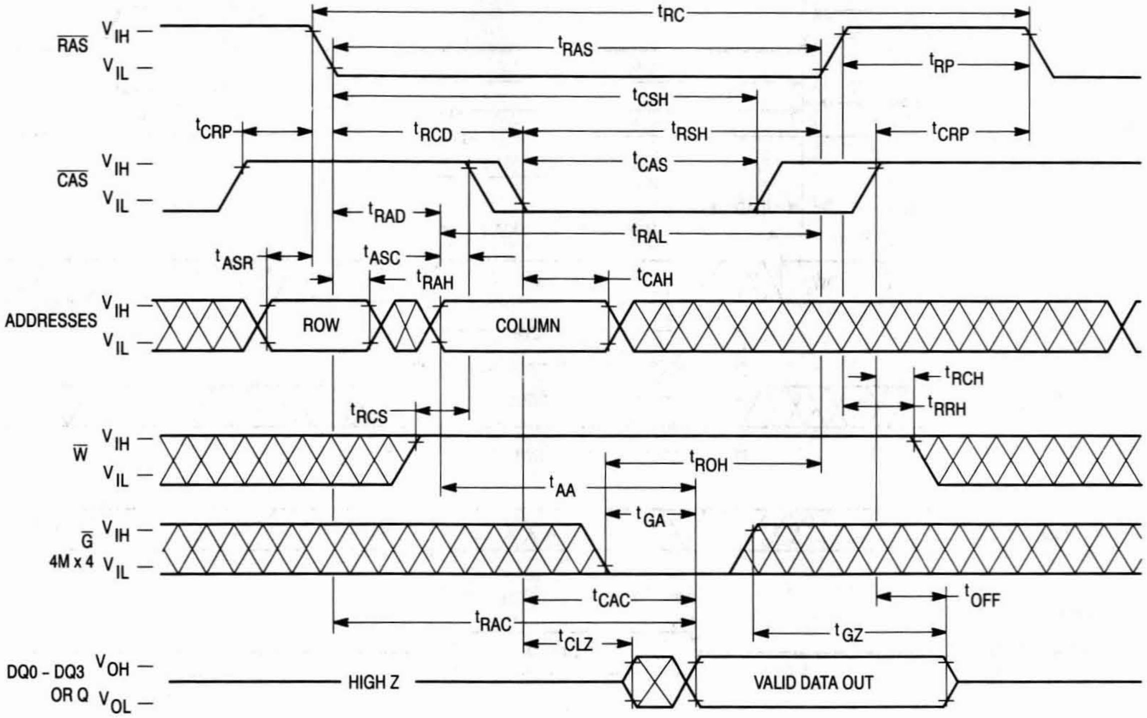
Parameter	Symbol		MCM516100-60 MCM516400-60 MCM517400-60		MCM516100-70 MCM516400-70 MCM517400-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time (Fast Page Mode)	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}					ns	
MCM516100			60	—	70	—		
MCM516400, MCM517400			85	—	90	—		
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}					ns	
MCM516100			60	400 k	70	400 k		
MCM516400, MCM517400			60	200 k	70	200 k		
$\overline{\text{CAS}}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}					ns	5
MCM516100			35	—	40	—		
MCM516400, MCM517400			60	—	65	—		

NOTES:

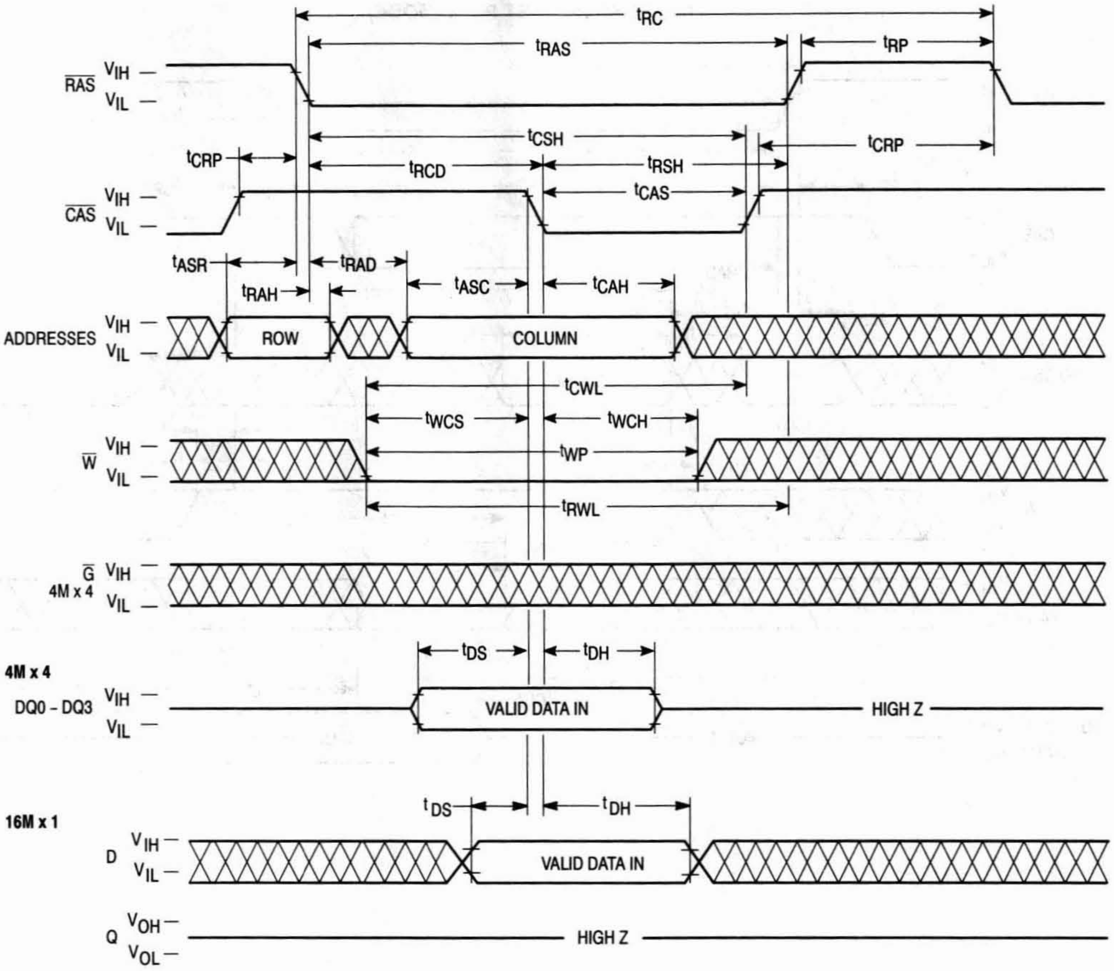
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through-out the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING DIAGRAMS

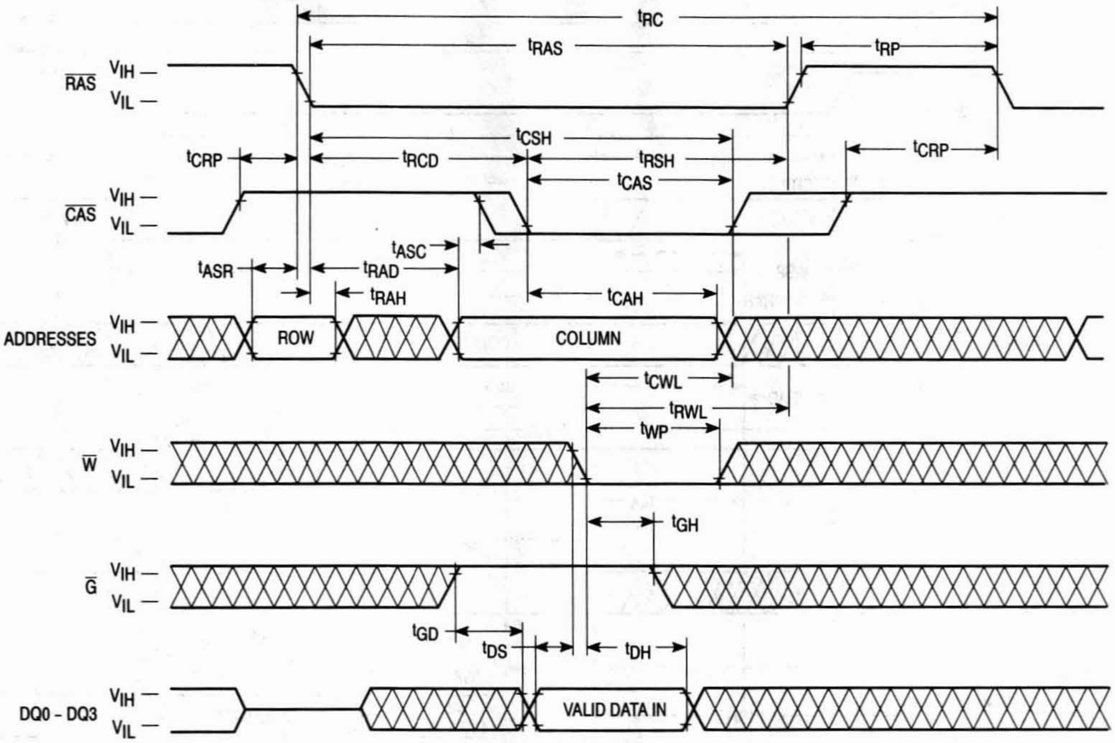
READ CYCLE (FAST PAGE MODE)


RAS
CAS
ADDRESSES
W
G
4M x 4
DQ0 - DQ3
OR Q
VIH
VIL
VOH
VOL
tRC
tRAS
tRP
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
tRAD
tRAL
tASR
tASC
tRAH
tCAH
ROW
COLUMN
tRCH
tRRH
tRCS
tROH
tAA
tGA
tCAC
tOFF
tRAC
tGZ
tCLZ
HIGH Z
VALID DATA OUT

EARLY WRITE CYCLE

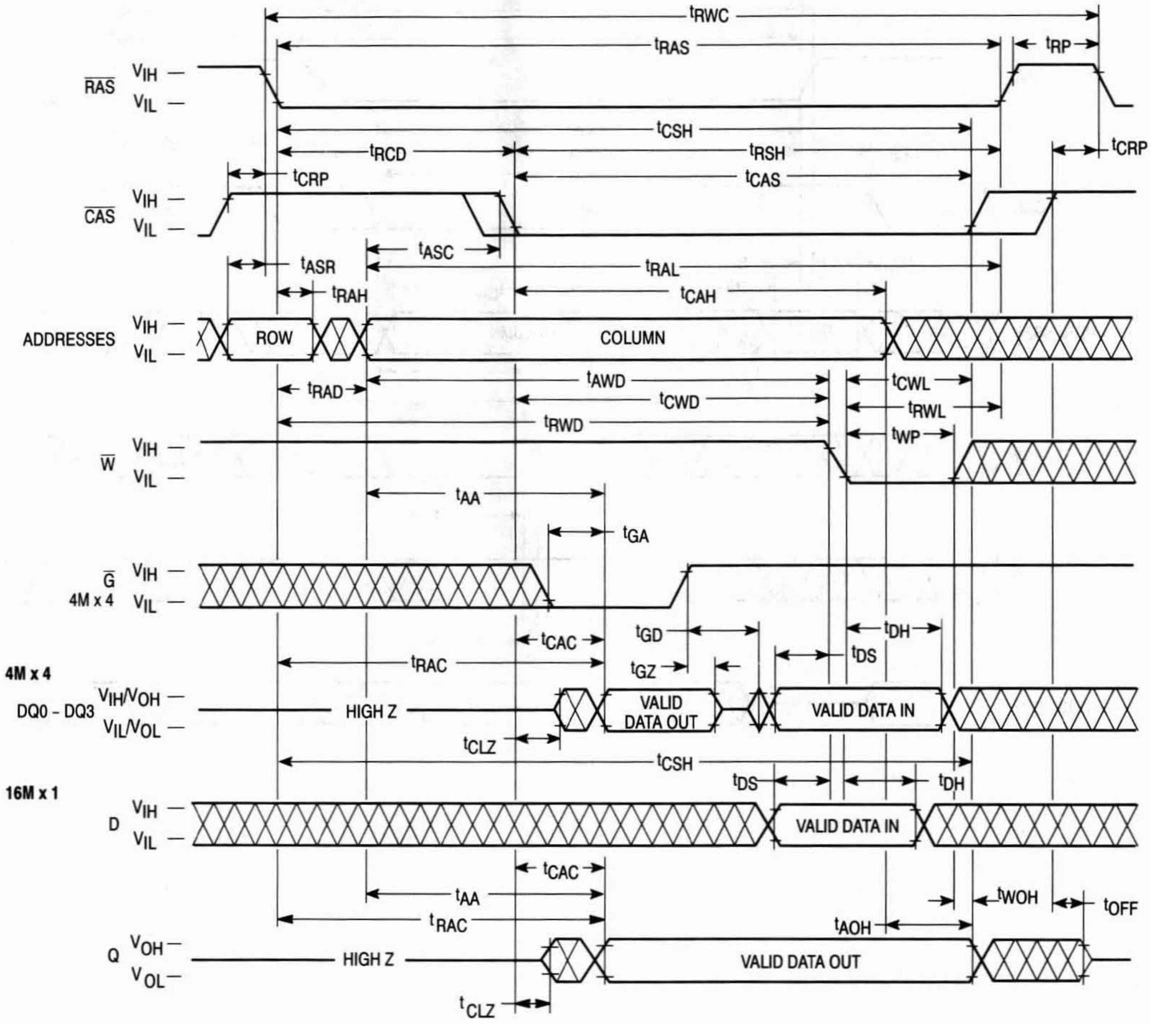

t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH} —
V_{IL} —
t_{CSH}
t_{CRP}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CAS}
$\overline{CAS}$
V_{IH} —
V_{IL} —
t_{ASR}
t_{RAD}
t_{RAH}
t_{ASC}
t_{CAH}
ADDRESSES
V_{IH} —
V_{IL} —
ROW
COLUMN
t_{CWL}
t_{WCS}
t_{WCH}
$\overline{W}$
V_{IH} —
V_{IL} —
t_{WP}
t_{RWL}
$\overline{G}$
4M x 4
V_{IH} —
V_{IL} —
t_{DS}
t_{DH}
4M x 4
DQ0 - DQ3
V_{IH} —
V_{IL} —
VALID DATA IN
HIGH Z
t_{DS}
t_{DH}
16M x 1
D
V_{IH} —
V_{IL} —
VALID DATA IN
Q
V_{OH} —
V_{OL} —
HIGH Z

$\overline{G}$ CONTROLLED LATE WRITE CYCLE (4M x 4)

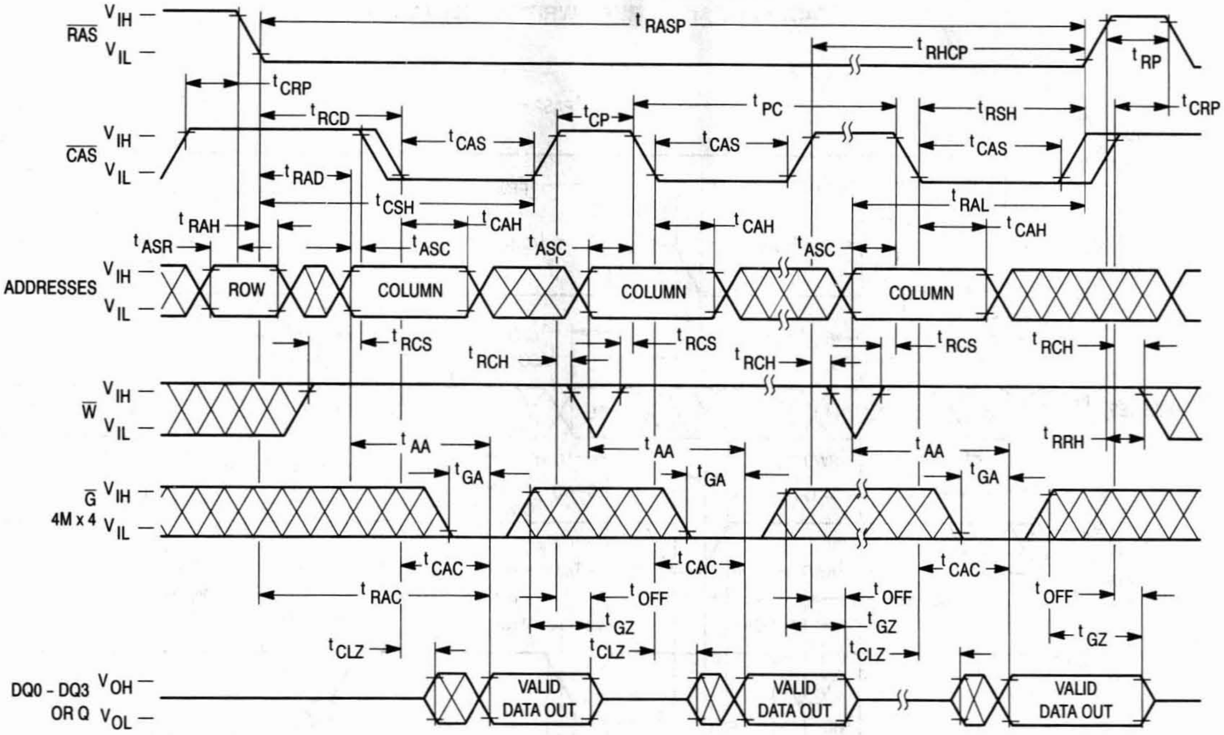


t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CAS}
t_{CRP}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{ASC}
t_{ASR}
t_{RAD}
t_{RAH}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW
COLUMN
t_{CWL}
t_{RWL}
t_{WP}
$\overline{W}$
V_{IH}
V_{IL}
t_{GH}
$\overline{G}$
V_{IH}
V_{IL}
t_{GD}
t_{DS}
t_{DH}
DQ0 - DQ3
V_{IH}
V_{IL}
VALID DATA IN

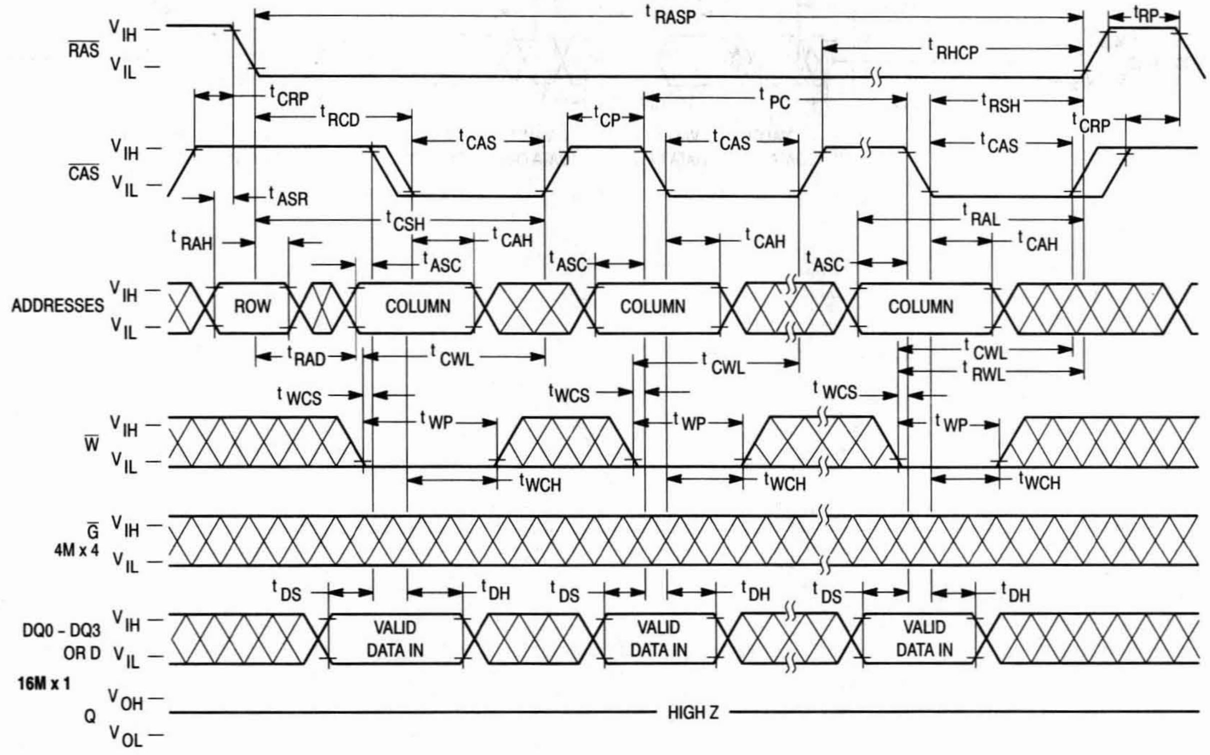
READ-WRITE CYCLE


tRWC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
tCAS
CAS
tASC
tASR
tRAL
tRAH
tCAH
ADDRESSES
ROW
COLUMN
tRAD
tAWD
tCWL
tCWD
tRWL
tRWD
tWP
W
tAA
tGA
G
4M x 4
tGD
tDH
tCAC
tDS
tRAC
tGZ
DQ0 – DQ3
VIH/VOH
VIL/VOL
HIGH Z
VALID DATA OUT
VALID DATA IN
tCLZ
16M x 1
D
tWOH
tOFF
tAOH
Q
VOH
VOL

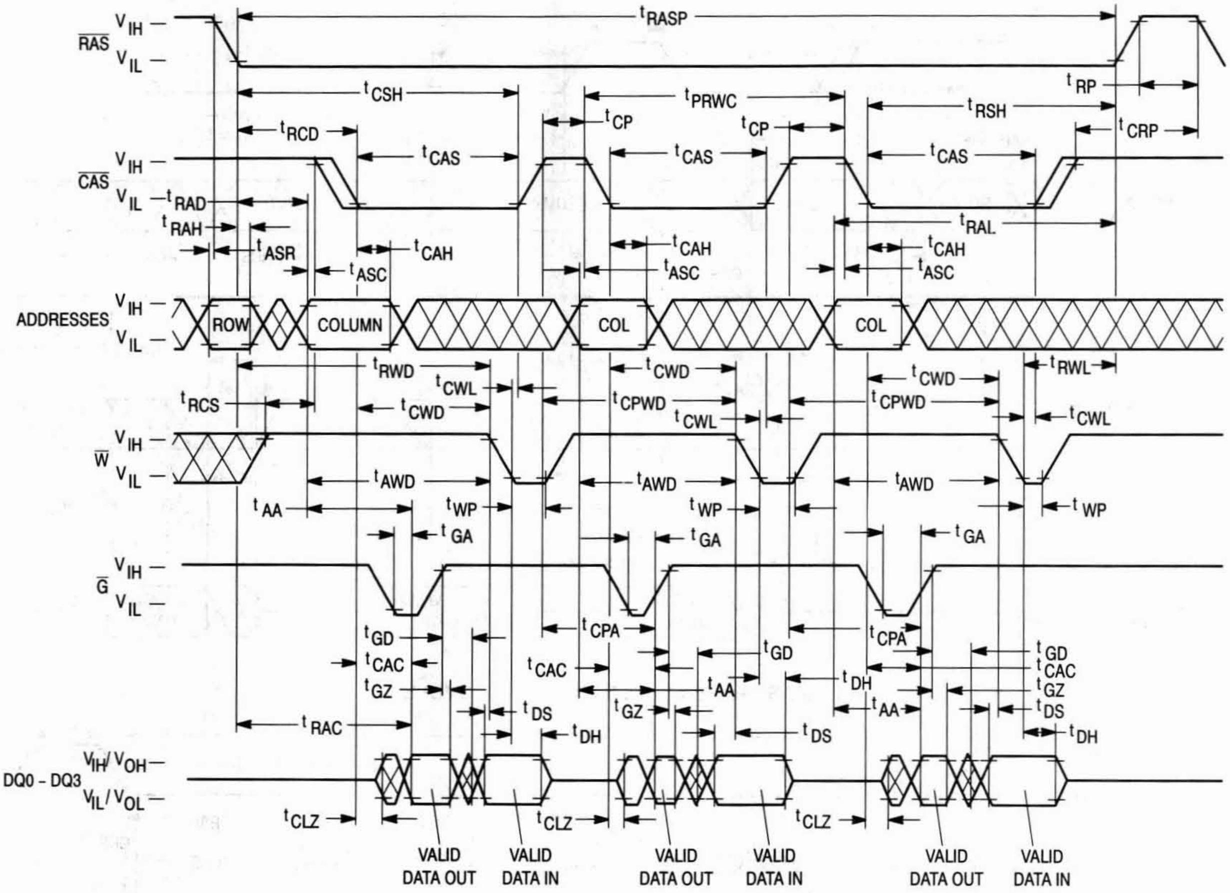
FAST PAGE MODE READ CYCLE


RAS
V IH
V IL
t RASP
t RHCP
t RP
t CRP
t RCD
t CP
t PC
t RSH
t CRP
CAS
t CAS
t RAD
t CSH
t RAL
t RAH
t CAH
t ASR
t ASC
ADDRESSES
ROW
COLUMN
COLUMN
COLUMN
t RCS
t RCH
W
t RRH
t AA
t GA
G
4M x 4
t CAC
t RAC
t OFF
t GZ
t CLZ
DQ0 - DQ3
OR Q
V OH
V OL
VALID DATA OUT
VALID DATA OUT
VALID DATA OUT

FAST PAGE MODE EARLY WRITE CYCLE

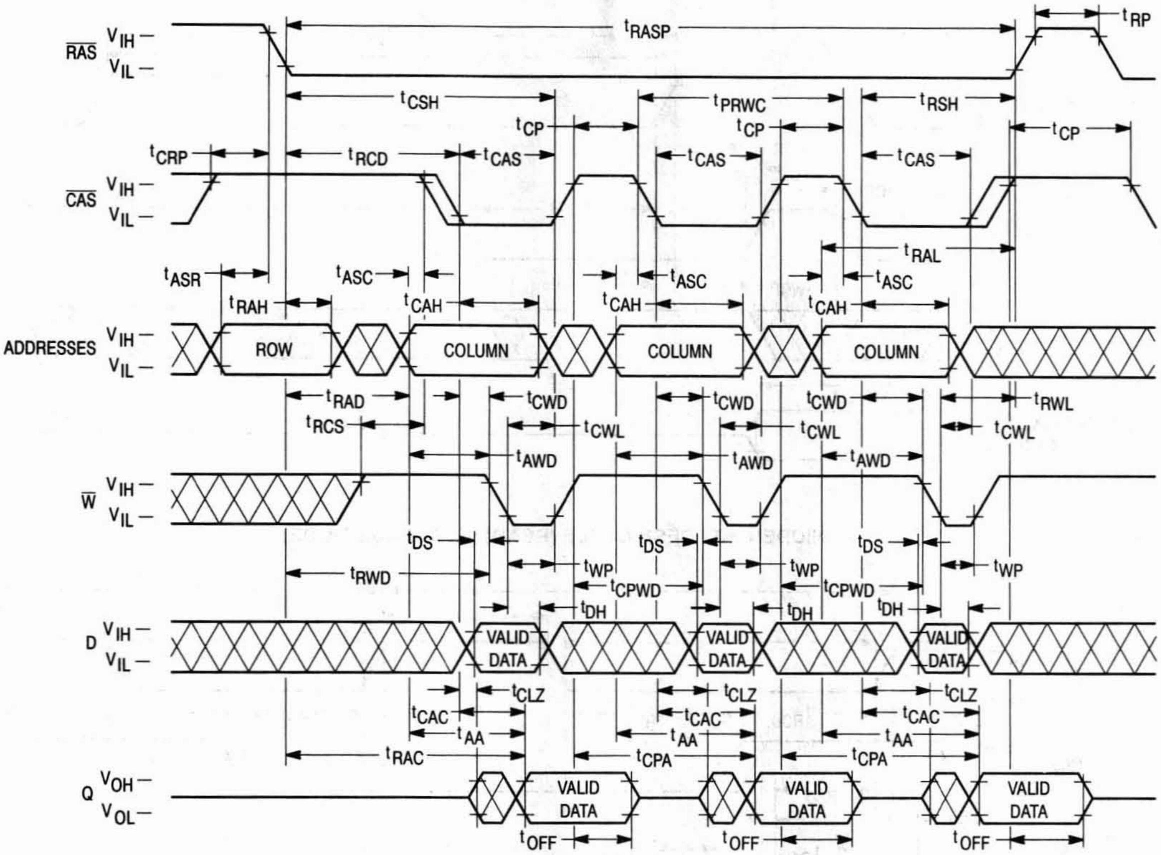

RAS
V IH
V IL
t RASP
t RHCP
t RP
t CRP
t RCD
t CP
t PC
t RSH
CAS
t CAS
t ASR
t CSH
t RAL
t RAH
t CAH
t ASC
ADDRESSES
ROW
COLUMN
COLUMN
COLUMN
t RAD
t CWL
t RWL
t WCS
t WP
t WCH
W
G
4M x 4
t DS
t DH
DQ0 - DQ3
OR D
VALID DATA IN
VALID DATA IN
VALID DATA IN
16M x 1
Q
V OH
V OL
HIGH Z

FAST PAGE MODE READ-WRITE CYCLE (4M x 4)



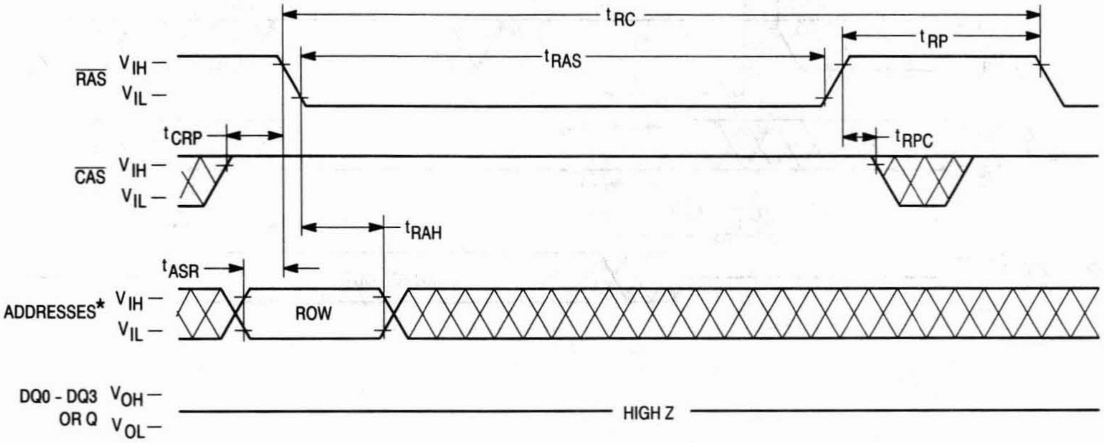
RAS
VIH
VIL
CAS
ADDRESSES
W
G
DQ0 – DQ3
VIH/VOH
VIL/VOL
ROW
COLUMN
COL
COL
tRASP
tRP
tCRP
tCSH
tPRWC
tRSH
tRCD
tCP
tCAS
tRAD
tRAH
tASR
tASC
tCAH
tRAL
tRWD
tCWL
tCWD
tCPWD
tRWL
tRCS
tAWD
tAA
tWP
tGA
tGD
tCAC
tGZ
tCPA
tDH
tDS
tRAC
tCLZ
VALID DATA OUT
VALID DATA IN

FAST PAGE MODE READ-WRITE CYCLE (16M x 1)


$\overline{RAS}$ V_{IH} – V_{IL} –
$\overline{CAS}$ V_{IH} – V_{IL} –
ADDRESSES V_{IH} – V_{IL} –
$\overline{W}$ V_{IH} – V_{IL} –
D V_{IH} – V_{IL} –
Q V_{OH} – V_{OL} –
t_{RASP}
t_{RP}
t_{CSH}
t_{PRWC}
t_{RSH}
t_{CP}
t_{CRP}
t_{RCD}
t_{CAS}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ROW
COLUMN
t_{RAD}
t_{RCS}
t_{CWD}
t_{CWL}
t_{RWL}
t_{AWD}
t_{DS}
t_{WP}
t_{RWD}
t_{CPWD}
t_{DH}
VALID DATA
t_{CLZ}
t_{CAC}
t_{AA}
t_{RAC}
t_{CPA}
t_{OFF}

$\overline{RAS}$-ONLY REFRESH CYCLE

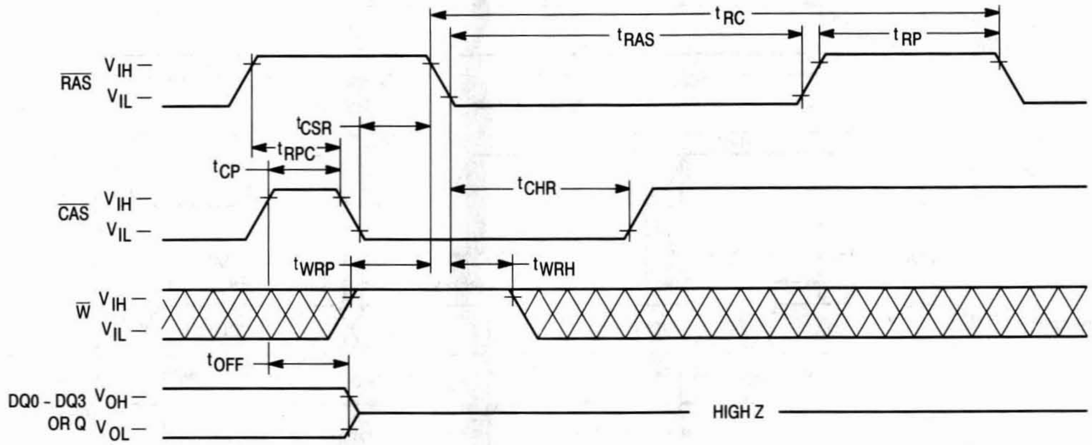
($\overline{W}$ and $\overline{G}$ (4M x 4) are Don't Care)


$\overline{RAS}$ V_{IH} – V_{IL} –
$\overline{CAS}$ V_{IH} – V_{IL} –
ADDRESSES* V_{IH} – V_{IL} –
DQ0 - DQ3 OR Q V_{OH} – V_{OL} –
t_{RC}
t_{RP}
t_{RAS}
t_{CRP}
t_{RPC}
t_{RAH}
t_{ASR}
ROW
HIGH Z

*MCM516xxx – A0 – A11; MCM517400 – A0 – A10.

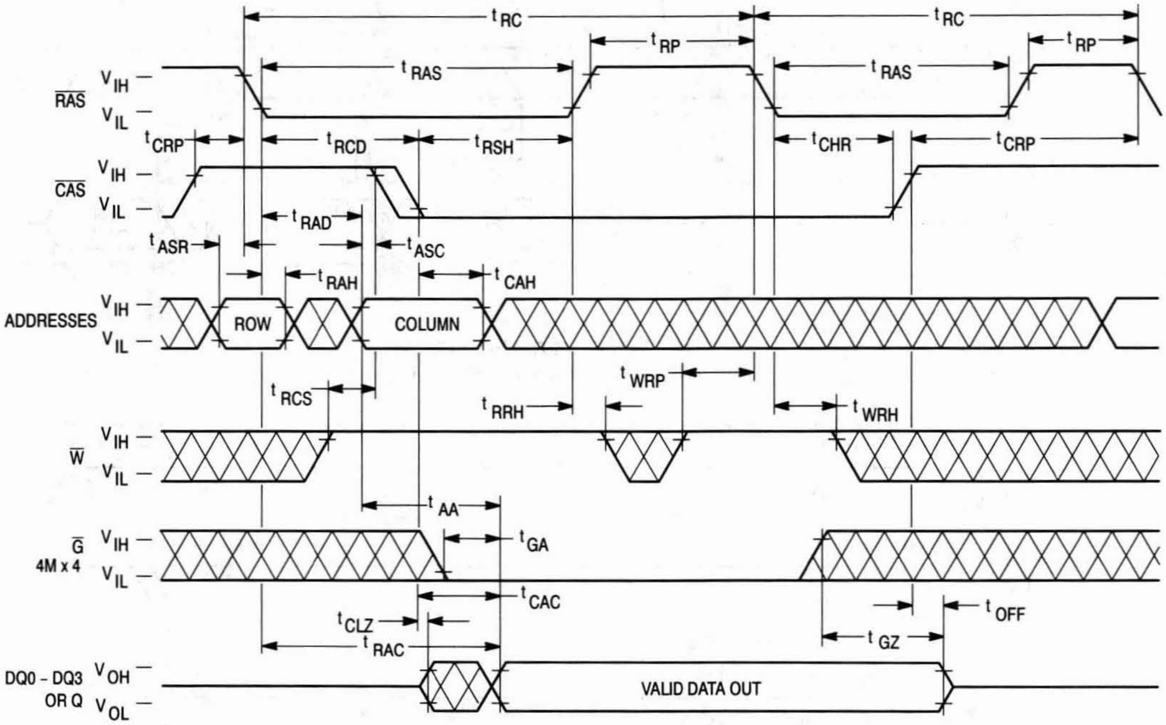
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{G}}$ (4M x 4), D (16M x 1), and A0 – A10 or A11 are Don't Care)



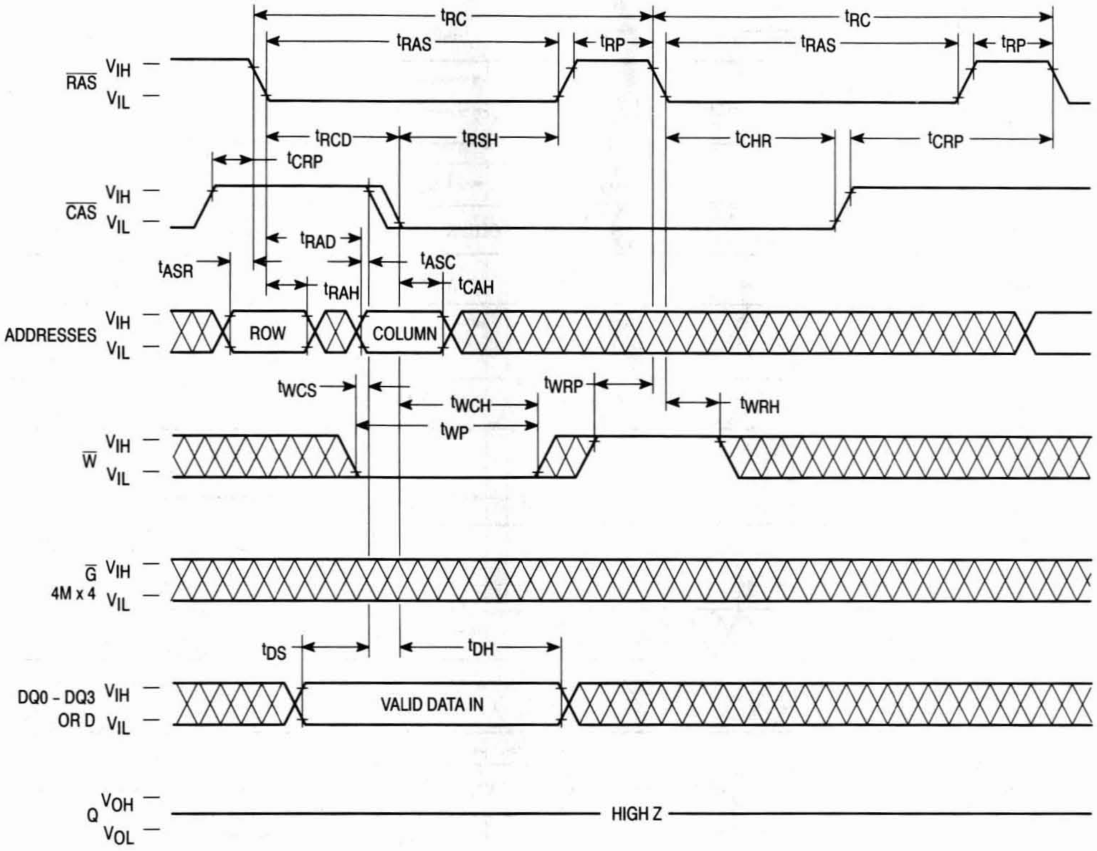
t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CSR}
t_{RPC}
t_{CP}
t_{CHR}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{WRP}
t_{WRH}
$\overline{\text{W}}$
V_{IH}
V_{IL}
t_{OFF}
DQ0 - DQ3
OR Q
V_{OH}
V_{OL}
HIGH Z

HIDDEN REFRESH CYCLE (READ) (FAST PAGE MODE)



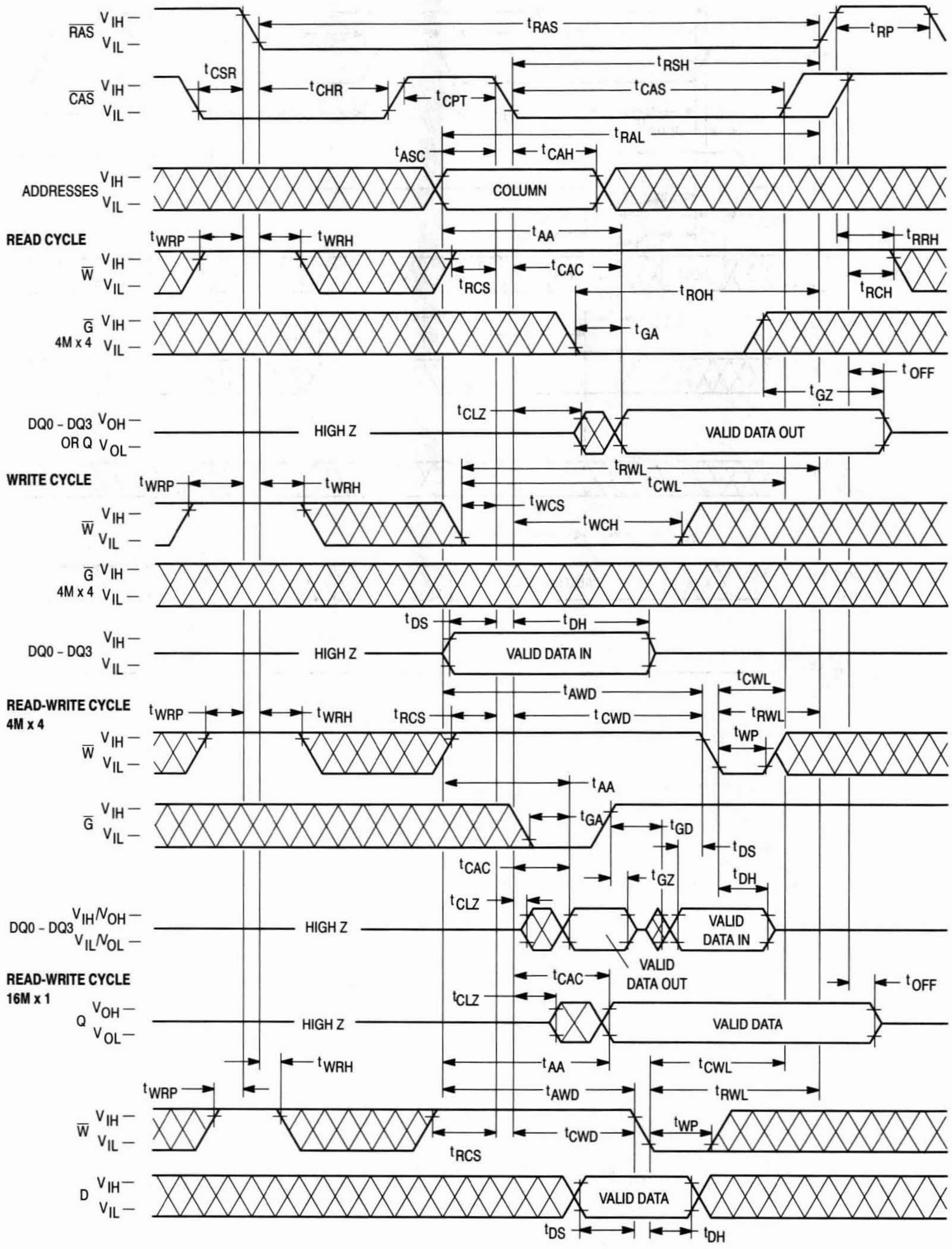
t_{RC}
t_{RC}
t_{RP}
t_{RP}
t_{RAS}
t_{RAS}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CRP}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW
COLUMN
t_{WRP}
t_{RCS}
t_{RRH}
t_{WRH}
$\overline{\text{W}}$
V_{IH}
V_{IL}
t_{AA}
$\overline{\text{G}}$
4M x 4
V_{IH}
V_{IL}
t_{GA}
t_{CAC}
t_{CLZ}
t_{OFF}
t_{RAC}
t_{GZ}
DQ0 - DQ3
OR Q
V_{OH}
V_{OL}
VALID DATA OUT

HIDDEN REFRESH CYCLE (EARLY WRITE)



t_{RC}
t_{RAS}
t_{RP}
t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$ V_{IH} V_{IL}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CRP}
t_{CRP}
$\overline{CAS}$ V_{IH} V_{IL}
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES V_{IH} V_{IL}
ROW
COLUMN
t_{WCS}
t_{WRP}
t_{WCH}
t_{WRH}
t_{WP}
$\overline{W}$ V_{IH} V_{IL}
$\overline{G}$ 4M x 4 V_{IH} V_{IL}
t_{DS}
t_{DH}
DQ0 - DQ3 OR D V_{IH} V_{IL}
VALID DATA IN
Q V_{OH} V_{OL}
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



$\overline{\text{RAS}}$ V_{IH} V_{IL}
$\overline{\text{CAS}}$ V_{IH} V_{IL}
ADDRESSES V_{IH} V_{IL}
COLUMN
READ CYCLE
$\overline{\text{W}}$ V_{IH} V_{IL}
$\overline{\text{G}}$ 4M x 4 V_{IH} V_{IL}
DQ0 - DQ3 OR Q V_{OH} V_{OL}
HIGH Z
VALID DATA OUT
WRITE CYCLE
$\overline{\text{W}}$ V_{IH} V_{IL}
$\overline{\text{G}}$ 4M x 4 V_{IH} V_{IL}
DQ0 - DQ3 V_{IH} V_{IL}
HIGH Z
VALID DATA IN
READ-WRITE CYCLE 4M x 4
$\overline{\text{W}}$ V_{IH} V_{IL}
$\overline{\text{G}}$ V_{IH} V_{IL}
DQ0 - DQ3 V_{IH}/V_{OH} V_{IL}/V_{OL}
HIGH Z
VALID DATA OUT
VALID DATA IN
READ-WRITE CYCLE 16M x 1
Q V_{OH} V_{OL}
HIGH Z
VALID DATA
$\overline{\text{W}}$ V_{IH} V_{IL}
D V_{IH} V_{IL}
VALID DATA
t_{RAS}
t_{RP}
t_{RSH}
t_{CSR}
t_{CHR}
t_{CPT}
t_{CAS}
t_{RAL}
t_{ASC}
t_{CAH}
t_{WRP}
t_{WRH}
t_{AA}
t_{RRH}
t_{RCS}
t_{CAC}
t_{ROH}
t_{RCH}
t_{GA}
t_{OFF}
t_{GZ}
t_{CLZ}
t_{RWL}
t_{CWL}
t_{WCS}
t_{WCH}
t_{DS}
t_{DH}
t_{AWD}
t_{CWD}
t_{WP}
t_{GD}

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 32 milliseconds or 64 milliseconds, for MCM5174xx and MCM516xxx, respectively), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

MCM516100: The twelve address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe $\overline{\text{RAS}}$ and column address strobe $\overline{\text{CAS}}$, into two separate 12-bit address fields. A total of twenty four address bits, twelve rows and twelve columns, will decode one of the 16,777,216 one bit word locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

MCM516400: The twelve address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate address fields. A total of twenty two address bits, twelve rows and ten columns, will decode one of the 4,194,304 four bit word locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

MCM517400: The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 11-bit address fields. A total of twenty two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 four bit word locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the 16M DRAM Family per device: $\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle, and page mode. All are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, fast page mode read cycle, read-write cycle, and fast page mode read-write cycle. The normal read cycle is outlined here,while the other cycles are discussed in separate sections.

The normal read cycle begins as described in ADDRESSING THE RAM, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ or active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window.

For **MCM516100**, $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ clock active transition (t_{CAC}).

For **MCM516400 and MCM517400**, both $\overline{\text{CAS}}$ and output enable ($\overline{\text{G}}$) control read access time: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum and $\overline{\text{G}}$ must be active t_{RAC}-t_{GA} (both minimum) after $\overline{\text{RAS}}$ active transition to guarantee valid data out (Q) at t_{RAC}. If the t_{RCD} maximum is exceeded and/or $\overline{\text{G}}$ active transition does not occur in time, read access time is determined by either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock active transition (t_{CAC} or t_{GA}).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, fast page mode early write, and fast page mode read-write. Early and late write modes are discussed here, while fast page mode write operation is covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP}, apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Column address setup and hold times (t_{ASC}, t_{CAH}) and data in (D) setup and hold times (t_{DS}, t_{DH}) are referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers disabled. ($\overline{\text{G}}$ also is disabled for 4M x 4 devices.) For 16M x 1 devices, this feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles to prevent bus contention.

A late-write cycle (referred to as $\overline{\text{G}}$-controlled write, for 4M x 4) occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D timing parameters are referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition. 4M x 4 outputs are switched off by $\overline{\text{G}}$ inactive transition, which is required to write to the device. Q may be indeterminate (see note 15 of AC Operating Conditions table). $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle. $\overline{\text{G}}$ (4M x 4) devices must remain inactive for t_{GH} after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all column locations (MCM516100: 4096 columns; MCM516400: 1024 columns; and MCM517400: 2048 columns) on a selected row of the 16M DRAM family. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM516100 and MCM516400 require refresh every 64 milliseconds, while refresh time for the MCM517400 is 32 milliseconds.

This is accomplished by cycling through the 4096 and 2048 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the 16M DRAM device family. Burst refresh, a refresh of all rows consecutively, must be performed every 64 milliseconds on the MCM516100 and MCM516400, and 32 milliseconds on the MCM517400.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096 or 2048) associated with the particular row decodes. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter should be employed to ensure that all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{\text{RAS}}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode entry) as in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 4096 or 2048 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 4096 or 2048 times, depending on device type.
3. Read the "1"s that were written in step 2 in normal read mode.

4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 4096 or 2048 times, depending on device type.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

TEST MODE

The internal organization of the MCM516100 allows the device to be tested as if it were a 1M x 16 DRAM. In **Test Mode** operation, column addresses A11, A10, A1, and A0 are ignored. A test mode cycle reads and/or writes data to a bit in each of the sixteen 1M blocks in parallel. If all 16 bits are equal (all 0s or all 1s) during a read operation, Q (Data Output) pin will indicate a '1'. Otherwise, Q pin will indicate a '0'. See "Test Mode" block diagram.

The internal organization of the MCM516400 and MCM517400 allows the device to be tested as if it were a 1M x 16 DRAM. In **Test Mode** operation, column addresses A1 and A0 are ignored. A test mode cycle reads and/or writes data to a bit in each of the sixteen 1M blocks in parallel. During a write cycle, data is written using only DQ0, while during a read cycle, if all 16 bits are equal (all 0s or all 1s), DQ3 will indicate a '1'. Otherwise, DQ3 will indicate a '0'. DQ0, DQ1, and DQ2 always indicate a '1' during test mode read cycle. See "Test Mode" block diagram.

$\overline{\text{W}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ timing puts the device in **Test Mode**, as shown in the test mode timing diagram. A **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** refresh cycle or a **$\overline{\text{RAS}}$ only** refresh cycle places the device back in normal mode. Refresh is performed in test mode by using a **$\overline{\text{W}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** refresh cycle which uses the internal refresh address counter.

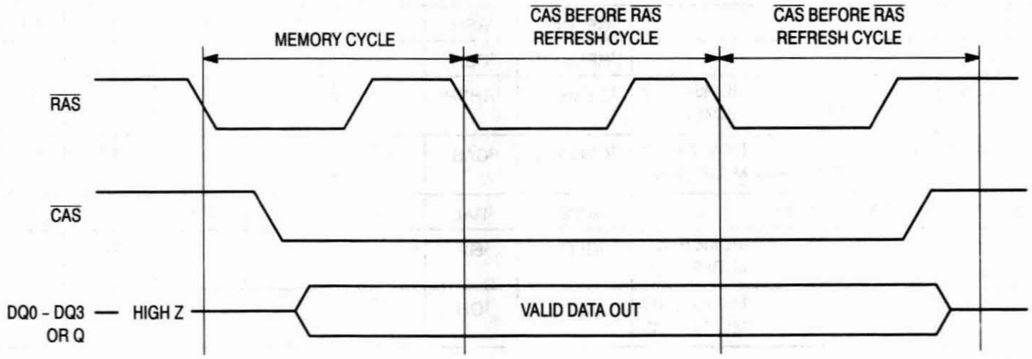

MEMORY CYCLE
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
DQ0 - DQ3 — HIGH Z
OR Q
VALID DATA OUT

Figure 1. Hidden Refresh Cycle

TEST MODE AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM51xxxx-60		MCM51xxxx-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	115	—	135	—	ns	5
Fast Page Mode Cycle Time MCM516100 MCM516400, MCM517400	t_{CELCEL}	t_{PC}	45	—	50	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	65	—	75	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$ MCM516100 MCM516400, MCM517400	t_{CEHQV}	t_{CPA}	—	40	—	45	ns	6
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	65	10 k	75	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode) MCM516100 MCM516400, MCM517400	t_{RELREH}	t_{RASP}	65 65	400 k 200 k	75 75	400 k 200 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	25	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	65	—	75	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time MCM516100 MCM516400, MCM517400	t_{CEHREH}	t_{RHCP}	40	—	45	—	ns	
$\overline{\text{CAS}}$ Pulse Width MCM516100 MCM516400, MCM517400	t_{CELCEH}	t_{CAS}	20	10 k	25	10 k	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
$\overline{\text{G}}$ Access Time MCM516400 MCM517400	t_{GLQV}	t_{GA}	—	20	—	25	ns	6
$\overline{\text{G}}$ Command Hold Time MCM516400 MCM517400	t_{WLGL}	t_{GH}	20	—	20	—	ns	

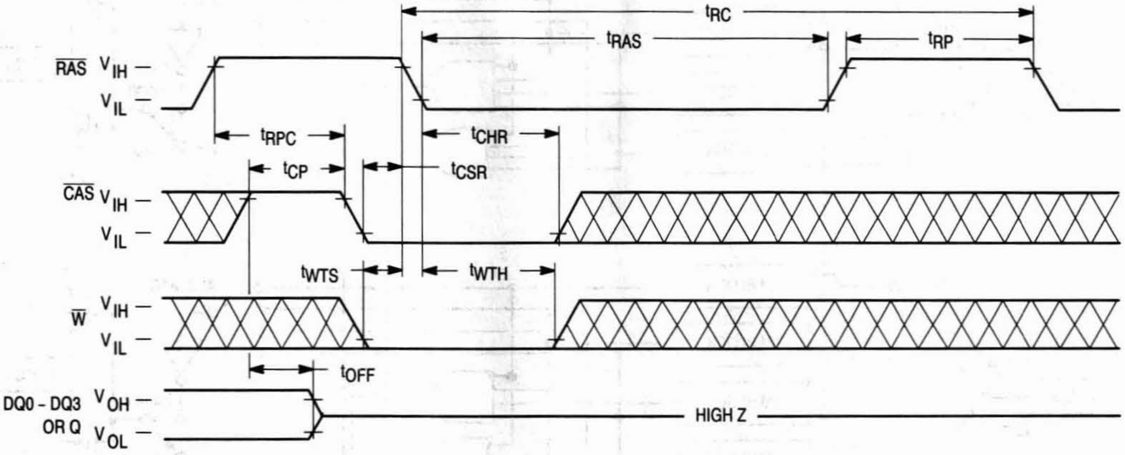
NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).

TEST MODE TIMING DIAGRAMS

$\overline{\text{WRITE}}$ OR $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE (TEST MODE ENTRY)

($\overline{\text{G}}$ (4M x 4), D (16M x 1) and A0 – A10 or 11 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$ V_{IH} –
V_{IL} –
t_{RPC}
t_{CHR}
t_{CP}
t_{CSR}
$\overline{\text{CAS}}$ V_{IH} –
V_{IL} –
t_{WTS}
t_{WTH}
$\overline{\text{W}}$ V_{IH} –
V_{IL} –
t_{OFF}
DQ0 - DQ3 V_{OH} –
OR Q V_{OL} –
HIGH Z

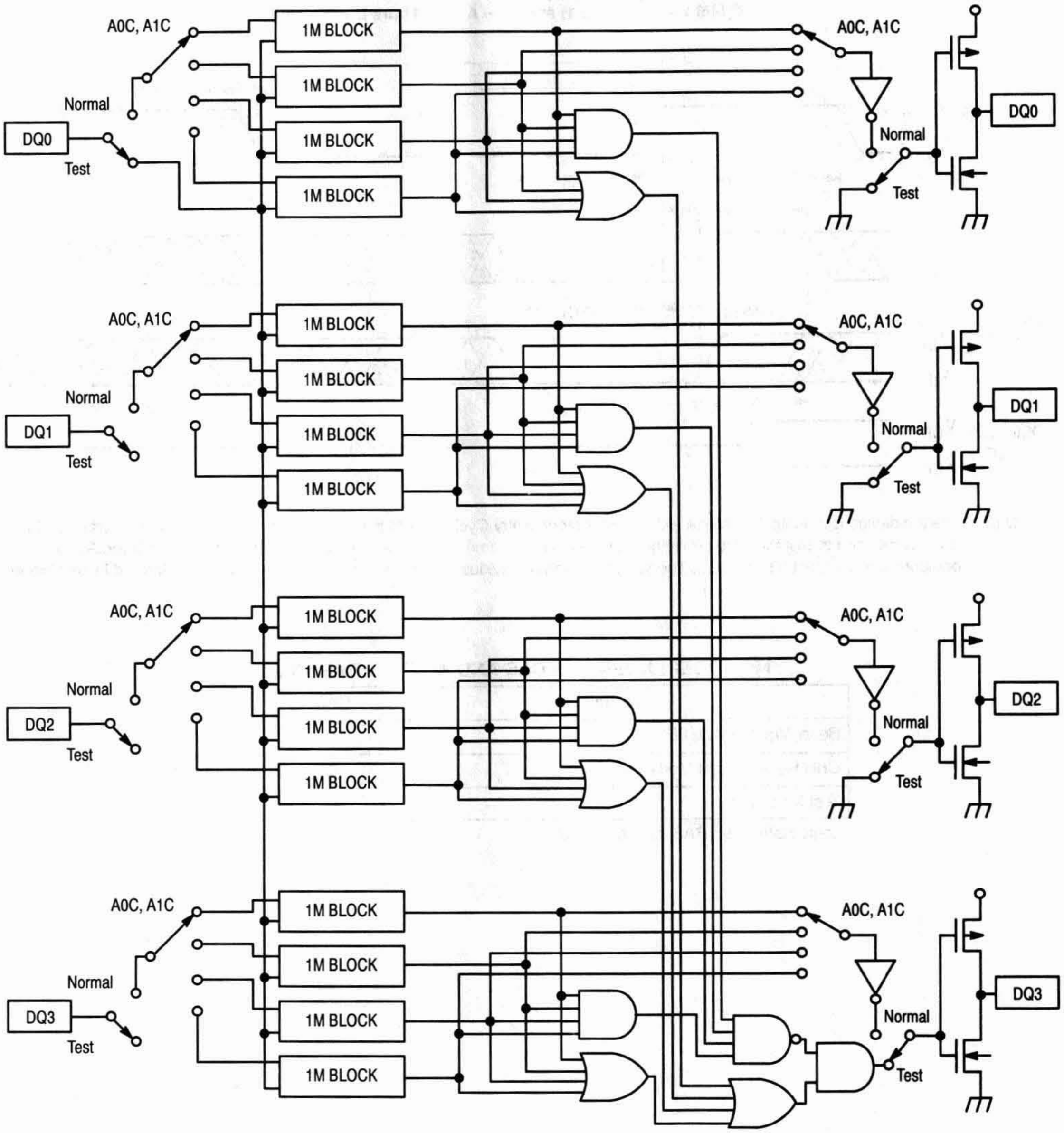
NOTE: Once the device is put into Test Mode with the Test Mode Entry Cycle, any of the standard cycles (Read, Write, Fast Page Mode, etc.) may be used to test the part, providing that the timing parameters are modified as described in the Test Mode AC Operating Conditions and Characteristics table. The timing diagrams previously presented are valid for all cycles performed in Test Mode.

MODE DEPENDENT ON $\overline{\text{CAS}}$ AND $\overline{\text{W}}$ WHEN $\overline{\text{RAS}}$ FALLS

Mode	$\overline{\text{CAS}}$	$\overline{\text{W}}$*
Read, Write, RMW, FPM	1	0
CBR Refresh, Test Mode Exit	0	1
Test Mode Entry	0	0

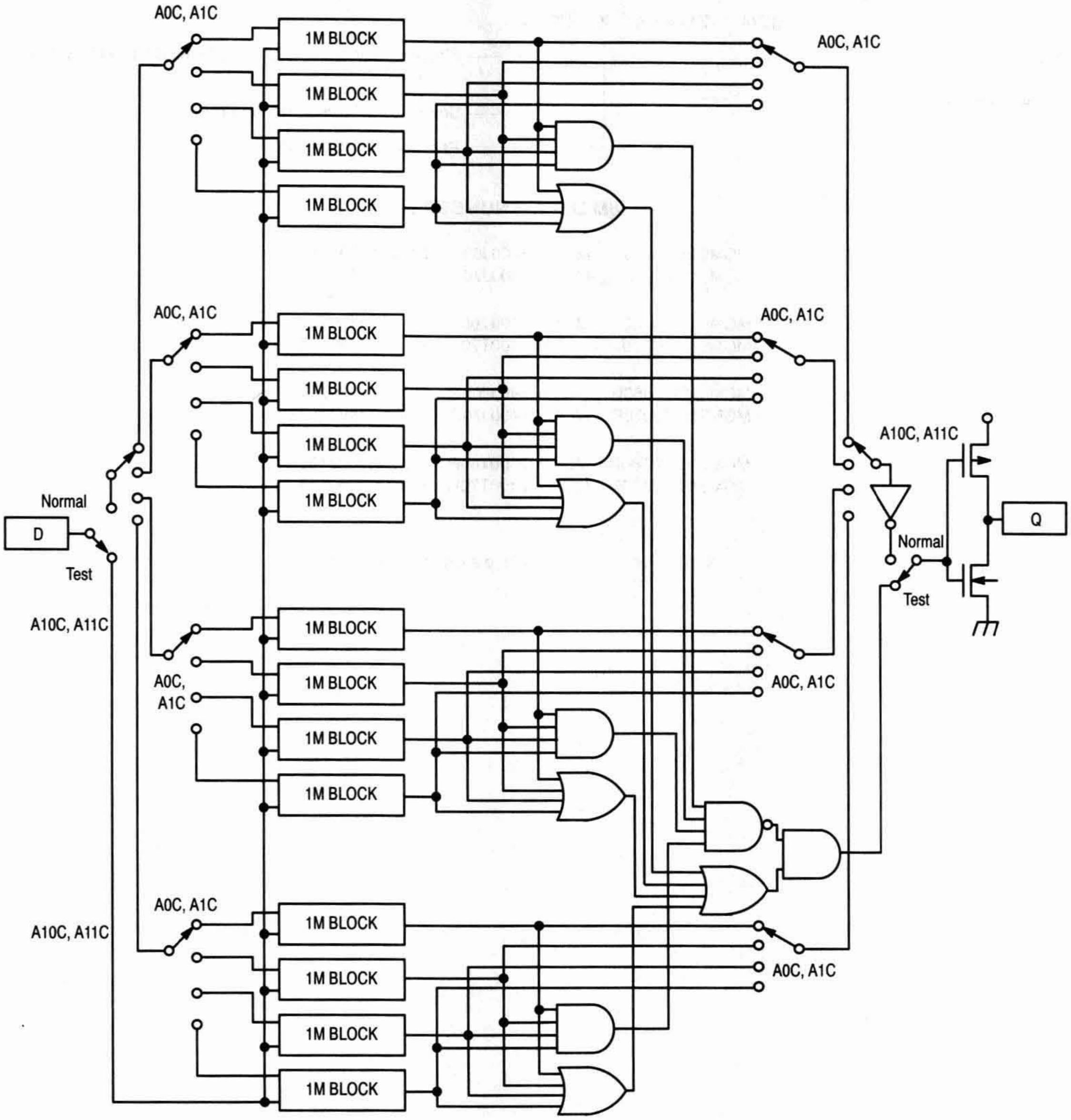
*Logic state when $\overline{\text{RAS}}$ transitions low.

TEST MODE BLOCK DIAGRAM (4M x 4)
(MCM516400, MCM517400)



A0C, A1C
Normal
DQ0
Test
1M BLOCK
1M BLOCK
1M BLOCK
1M BLOCK
A0C, A1C
Normal
Test
DQ0
A0C, A1C
Normal
DQ1
Test
1M BLOCK
1M BLOCK
1M BLOCK
1M BLOCK
A0C, A1C
Normal
Test
DQ1
A0C, A1C
Normal
DQ2
Test
1M BLOCK
1M BLOCK
1M BLOCK
1M BLOCK
A0C, A1C
Normal
Test
DQ2
A0C, A1C
Normal
DQ3
Test
1M BLOCK
1M BLOCK
1M BLOCK
1M BLOCK
A0C, A1C
Normal
Test
DQ3

TEST MODE BLOCK DIAGRAM (16M x 1)
(MCM516100)


A0C, A1C
1M BLOCK
1M BLOCK
1M BLOCK
1M BLOCK
A0C, A1C
A0C, A1C
1M BLOCK
1M BLOCK
1M BLOCK
1M BLOCK
A0C, A1C
A10C, A11C
Normal
D
Test
Q
Normal
Test
A10C, A11C
A0C, A1C
1M BLOCK
1M BLOCK
1M BLOCK
1M BLOCK
A0C, A1C
A10C, A11C
A0C, A1C
1M BLOCK
1M BLOCK
1M BLOCK
1M BLOCK
A0C, A1C

ORDERING INFORMATION
(Order by Full Part Number)

MCM 51XXXX X XX X

Motorola Memory Prefix — MCM
Part Number — 51XXXX
Package (J = 400 mil SOJ, T = 400 mil TSOP II) — X
Speed (60 = 60 ns, 70 = 70 ns) — XX
Shipping Method (R = Tape and Reel, Blank = Rails for SOJ, Trays for TSOP II) — X

16M DEVICE NUMBERS

MCM516100J60	MCM516400J60	MCM517400J60
MCM516100J70	MCM516400J70	MCM517400J70
MCM516100T60	MCM516400T60	MCM517400T60
MCM516100T70	MCM516400T70	MCM517400T70
MCM516100J60R	MCM516400J60R	MCM517400J60R
MCM516100J70R	MCM516400J70R	MCM517400J70R
MCM516100T60R	MCM516400T60R	MCM517400T60R
MCM516100T70R	MCM516400T70R	MCM517400T70R

NOTE: For mechanical data, please see Chapter 10.

Dynamic RAM Modules

Modules Organized x 8 Bits

256K x 8 MCM84256 5-3
1M x 8 MCM81000 5-15
MCM81430 5-27
4M x 8 MCM84000 5-39
MCM84030 5-39
16M x 8 MCM81600 5-51

Modules Organized x 9 Bits

256K x 9 MCM94256 5-53
1M x 9 MCM91000 5-65
MCM91430 5-77
4M x 9 MCM94000 5-88
MCM94030 5-88
16M x 9 MCM91600 5-100

Modules Organized x 32 Bits

256K x 32 MCM32256 5-102
512K x 32 MCM32512 5-114
1M x 32 MCM32130 5-126
2M x 32 MCM32230 5-138
4M x 32 MCM32400 5-150
8M x 32 MCM32800 5-152

Modules Organized x 36 Bits

256K x 36 MCM36256 5-155
512K x 36 MCM36512 5-167
1M x 36 MCM36100 5-179
2M x 36 MCM36200 5-191
4M x 36 MCM36400 5-203
8M x 36 MCM36800 5-206

Modules Organized x 40 Bits

256K x 40 MCM40256 5-209
512K x 40 MCM40512 5-225
1M x 40 MCM40100 5-241
2M x 40 MCM40200 5-257
4M x 40 MCM40400 5-273
8M x 40 MCM40800 5-276

Modules Organized x 72 Bits

1M x 72 MCM72100 5-279
2M x 72 MCM72200 5-282
4M x 72 MCM72400 5-285
8M x 72 MCM72800 5-288

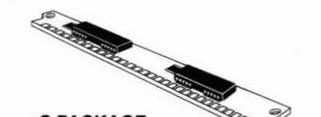
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM84256
MCM8L4256

256K x 8 Bit Dynamic Random Access Memory Module

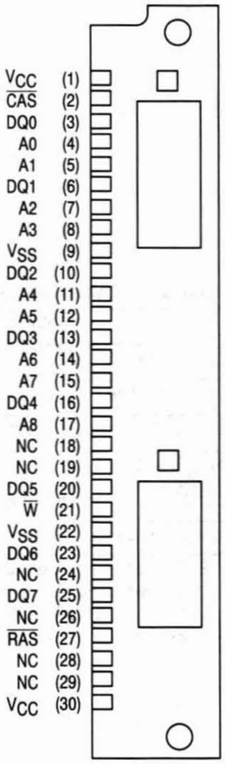
The MCM84256 is a 2M dynamic random access memory (DRAM) module organized as 262,144 x 8 bits. The module is a 30-lead single-in-line memory module (SIMM) consisting of two MCM514256A DRAMs housed in 20/26 J-lead small outline package (SOJ) and mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted adjacent to each DRAM. The MCM514256A is a 1.0µ CMOS high-speed dynamic random access memory organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  - MCM84256 = 8 ms (Max)
  - MCM8L4256 = 64 ms (Max)
- Consists of Two 256K x 4 DRAMs and Two 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM84256-70 = 70 ns (Max)
  - MCM84256-80 = 80 ns (Max)
- Low Active Power Dissipation:
  - MCM84256-70 = 0.9 W (Max)
  - MCM84256-80 = 0.8 W (Max)
- Low Standby Power Dissipation:
  - TTL Levels = 22 mW (Max)
  - CMOS Levels (MCM84256) = 11 mW (Max)
  - (MCM8L4256) = 2.2 mW (Max)
- $\overline{\text{CAS}}$ Control for Eight Common I/O Lines
- Available in Edge Connector



S PACKAGE
SIMM MODULE
CASE 839A-01

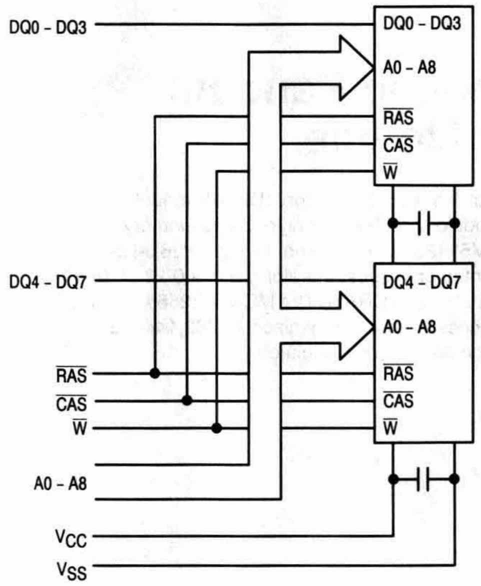
30-PIN
SINGLE-IN-LINE PACKAGE
(TOP VIEW)



V_{CC} (1)
$\overline{\text{CAS}}$ (2)
DQ0 (3)
A0 (4)
A1 (5)
DQ1 (6)
A2 (7)
A3 (8)
V_{SS} (9)
DQ2 (10)
A4 (11)
A5 (12)
DQ3 (13)
A6 (14)
A7 (15)
DQ4 (16)
A8 (17)
NC (18)
NC (19)
DQ5 (20)
$\overline{\text{W}}$ (21)
V_{SS} (22)
DQ6 (23)
NC (24)
DQ7 (25)
NC (26)
$\overline{\text{RAS}}$ (27)
NC (28)
NC (29)
V_{CC} (30)

PIN NAMES	
A0 – A8	Address Inputs
DQ0 – DQ7	Data Input/Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	1.2	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM84256-70, t_{RC} = 130 ns MCM84256-80, t_{RC} = 150 ns	I_{CC1}	— —	160 140	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	4	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles MCM84256-70, t_{RC} = 130 ns MCM84256-80, t_{RC} = 150 ns	I_{CC3}	 — —	 160 140	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM84256-70, t_{PC} = 40 ns MCM84256-80, t_{PC} = 45 ns	I_{CC4}	 — —	 120 100	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM84256 MCM8L4256	I_{CC5}	— —	2 400	mA µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM84256-70, t_{RC} = 130 ns MCM84256-80, t_{RC} = 150 ns	I_{CC6}	 — —	 160 140	mA	1
V_{CC} Power Supply Current, Battery Backup Mode — MCM8L4256 Only (t_{RC} = 125 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$ = V_{CC} – 0.2 V; DQ = V_{CC} – 0.2 V or Open; A0 – A8 = V_{CC} – 0.2 or 0.2 V) t_{RAS} = min to 1 µs	I_{CC7}	—	0.6	mA	1, 3
Input Leakage Current (0 $V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 20	20	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery backup. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A8, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$	C_{in}	24	pF
Input/Output Capacitance	DQ0 – DQ7	$C_{I/O}$	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM84256-70 MCM8L4256-70		MCM84256-80 MCM8L4256-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELAX}	t_{AR}	55	—	60	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

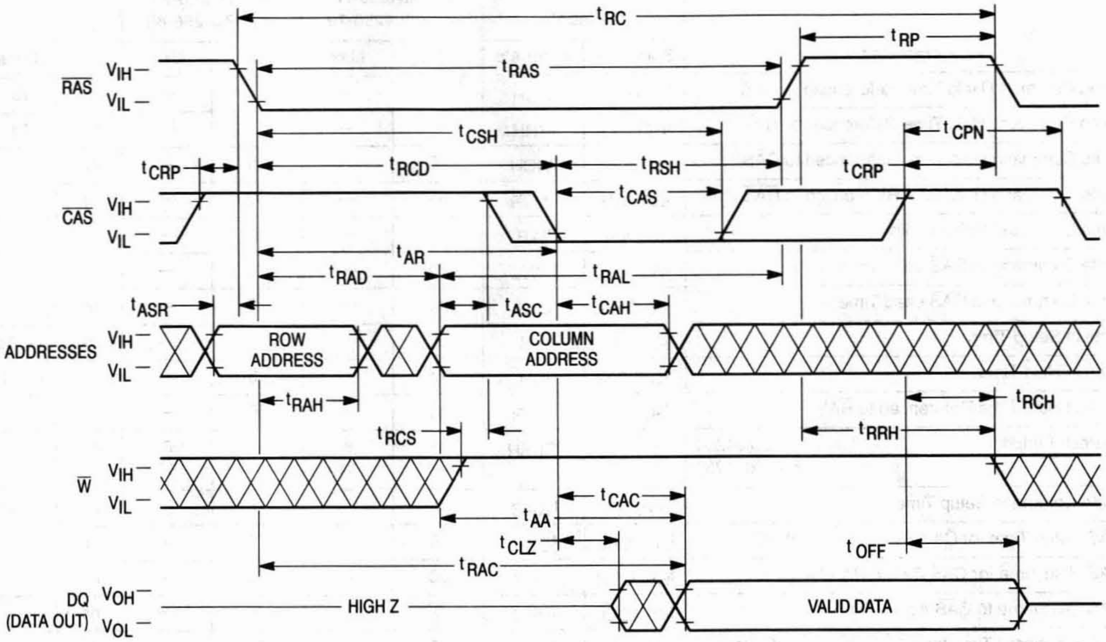
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM84256-70 MCM8L4256-70		MCM84256-80 MCM8L4256-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	—	15	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	—	60	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14, 15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14, 15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	—	60	—	ns	
Refresh Period MCM84256 MCM8L4256	t_{RVRV}	t_{RFSH}	— —	8 64	— —	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15, 16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	ns	

NOTES:

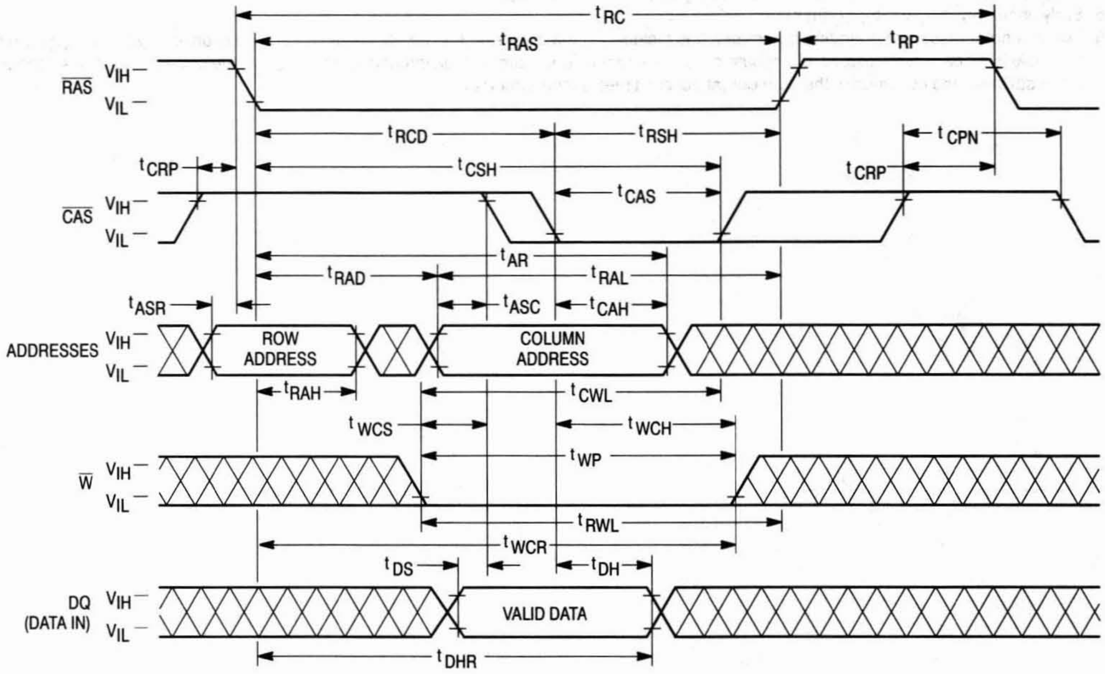
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



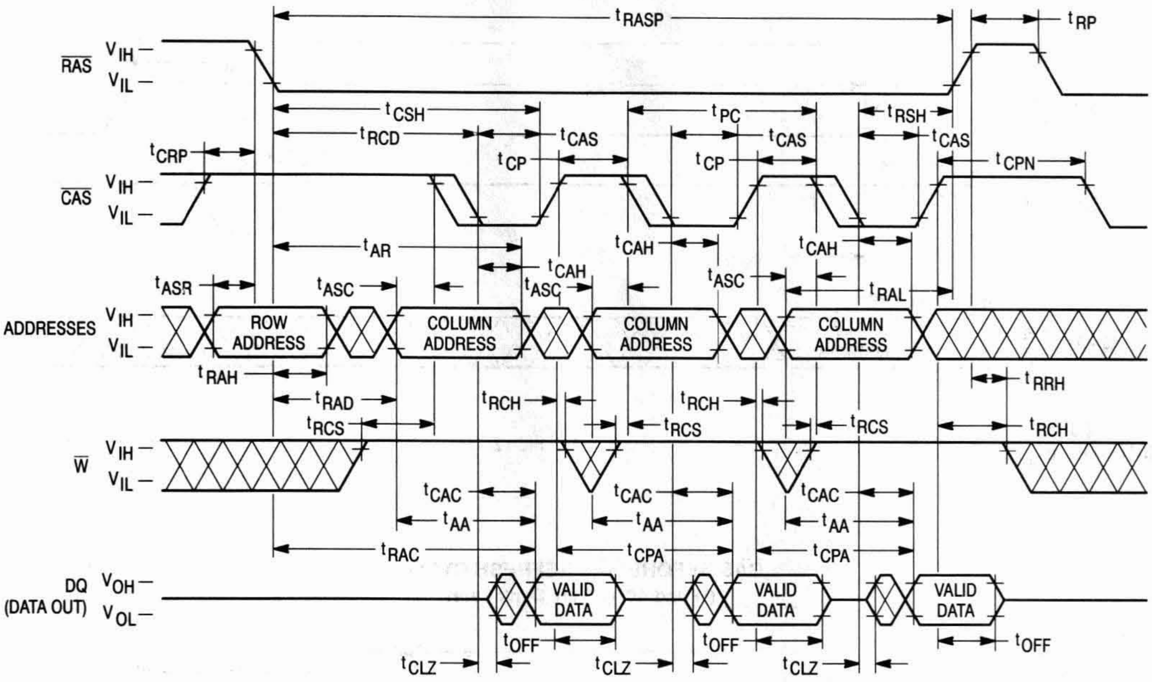
tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCPN
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W
VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
DQ (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA

EARLY WRITE CYCLE

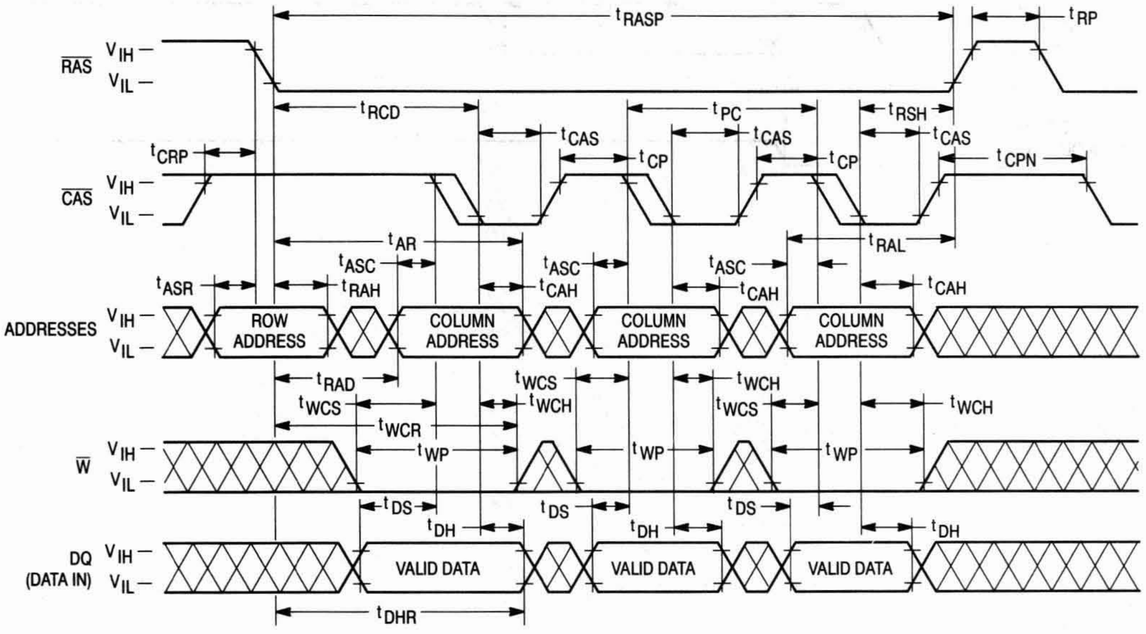


tRC
tRAS
tRP
RAS
VIH
VIL
tRCD
tRSH
tCPN
tCRP
tCSH
tCRP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWP
W
VIH
VIL
tRWL
tWCR
tDS
tDH
DQ (DATA IN)
VIH
VIL
VALID DATA
tDHR

FAST PAGE MODE READ CYCLE

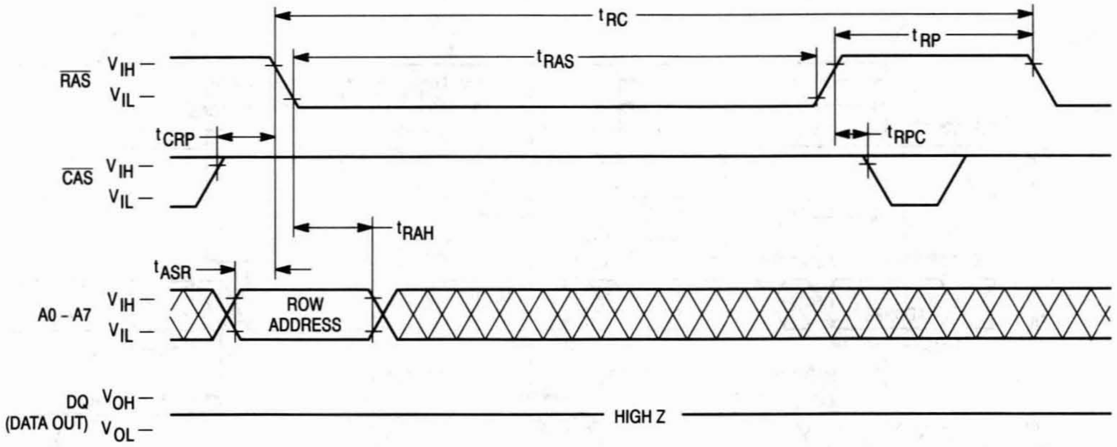

tRASP
tRP
RAS VIH VIL
tCSH
tPC
tRSH
tRCD
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCPN
CAS VIH VIL
tAR
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
tRAL
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAH
tRAD
tRCH
tRCH
tRRH
tRCS
tRCS
tRCS
tRCH
W VIH VIL
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
DQ (DATA OUT) VOH VOL
VALID DATA
VALID DATA
VALID DATA
tOFF
tOFF
tOFF
tCLZ
tCLZ
tCLZ

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)


tRASP
tRP
RAS VIH VIL
tRCD
tPC
tRSH
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCPN
CAS VIH VIL
tAR
tRAL
tASC
tASC
tASC
tASR
tRAH
tCAH
tCAH
tCAH
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tWCS
tWCH
tWCS
tWCH
tWCS
tWCH
tWCR
tWP
tWP
tWP
W VIH VIL
tDS
tDS
tDS
tDH
tDH
tDH
DQ (DATA IN) VIH VIL
VALID DATA
VALID DATA
VALID DATA
tDHR

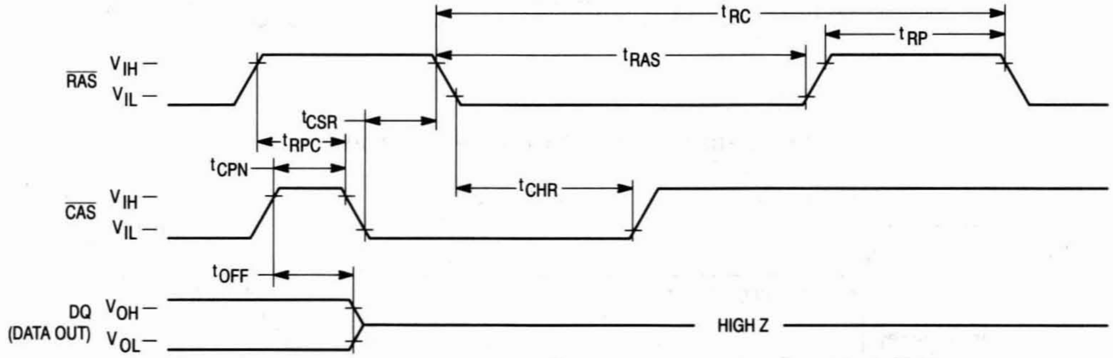
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

($\overline{\text{W}}$ and A8 are Don't Care)

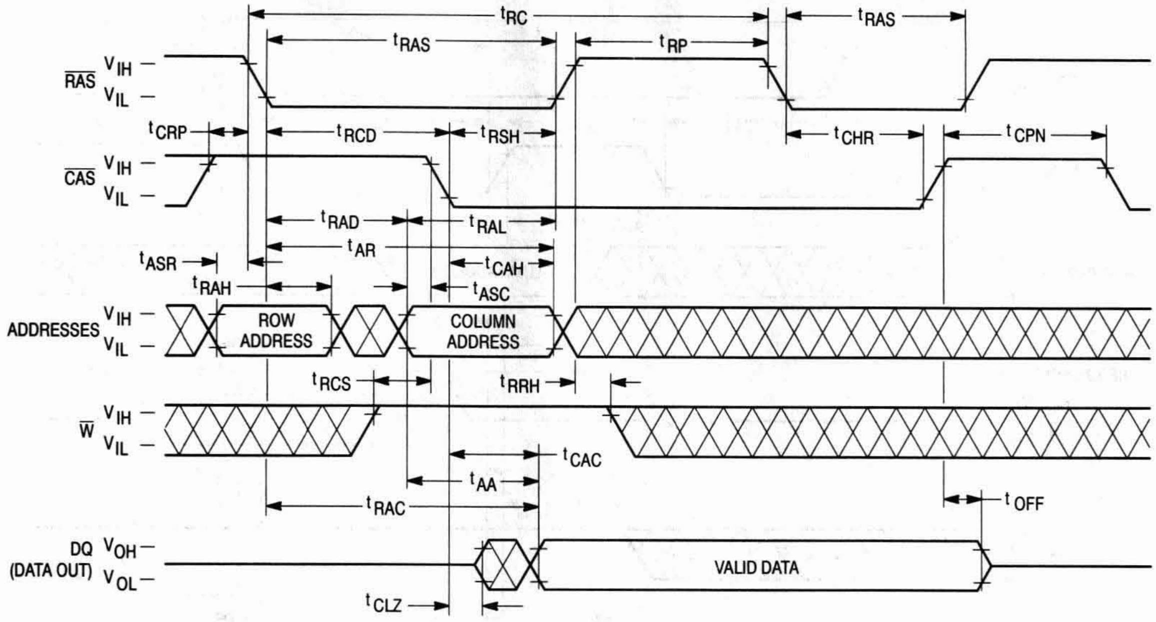

t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
A0 - A7
V_{IH}
V_{IL}
ROW ADDRESS
DQ (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{W}}$ and A0 – A8 are Don't Care)

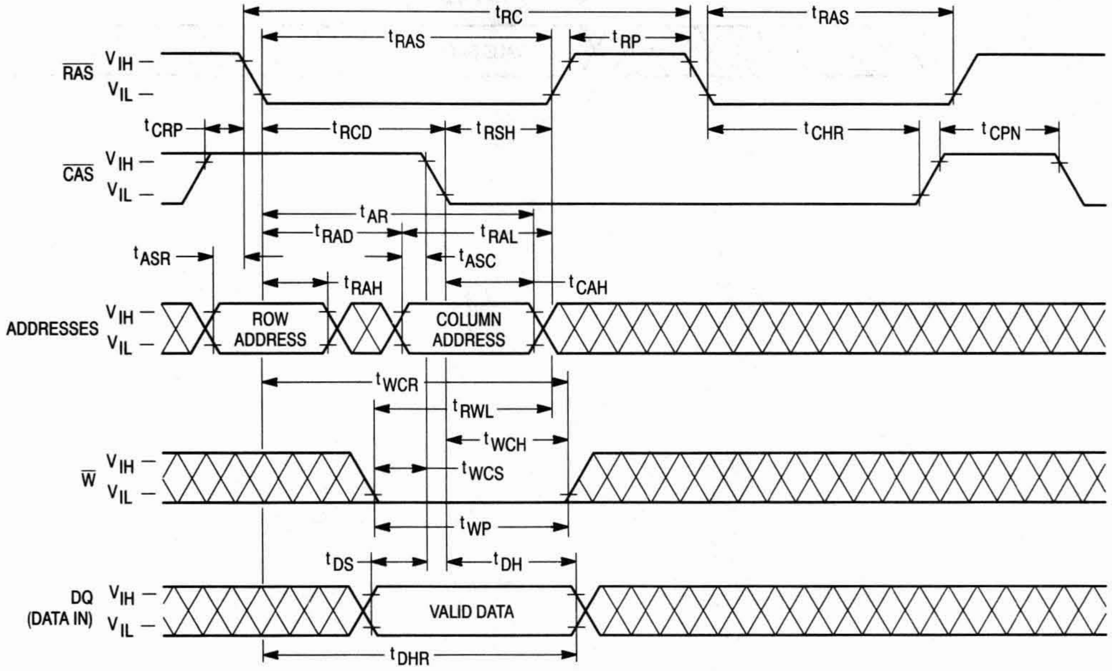

t_{RC}
t_{RP}
t_{RAS}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CSR}
t_{RPC}
t_{CPN}
t_{CHR}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{OFF}
DQ (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

HIDDEN REFRESH CYCLE (READ)



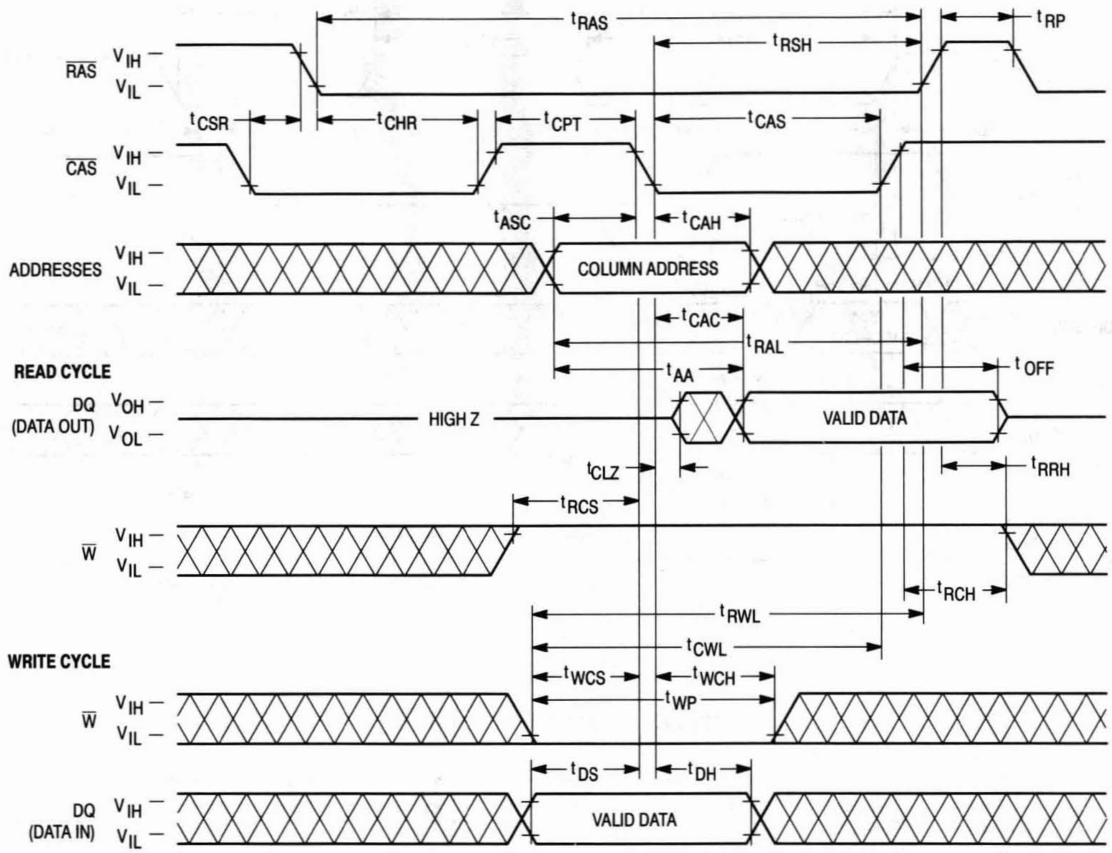
tRC
tRAS
tRAS
tRP
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCPN
CAS
VIH
VIL
tRAD
tRAL
tAR
tASR
tCAH
tRAH
tASC
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRCS
tRRH
W
VIH
VIL
tCAC
tAA
tRAC
tOFF
DQ (DATA OUT)
VOH
VOL
VALID DATA
tCLZ

HIDDEN REFRESH CYCLE (WRITE)



tRC
tRAS
tRAS
tRP
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCPN
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tWCR
tRWL
tWCH
tWCS
W
VIH
VIL
tWP
tDS
tDH
DQ (DATA IN)
VIH
VIL
VALID DATA
tDHR

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



t_{RAS}
t_{RP}
t_{RSH}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSR}
t_{CHR}
t_{CPT}
t_{CAS}
$\overline{CAS}$
t_{ASC}
t_{CAH}
ADDRESSES
COLUMN ADDRESS
t_{CAC}
t_{RAL}
READ CYCLE
t_{AA}
t_{OFF}
DQ (DATA OUT)
V_{OH}
V_{OL}
HIGH Z
VALID DATA
t_{CLZ}
t_{RRH}
t_{RCS}
$\overline{W}$
t_{RCH}
t_{RWL}
t_{CWL}
WRITE CYCLE
t_{WCS}
t_{WCH}
t_{WP}
t_{DS}
t_{DH}
DQ (DATA IN)
VALID DATA

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe ($\overline{\text{RAS}}$) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 byte locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This gate feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are two other variations in addressing the module: **$\overline{\text{RAS}}$-only refresh cycle** and **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either a normal random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. $\overline{\text{CAS}}$ controls read access time; $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} after inactive transition.

WRITE CYCLE

The DRAM may be written with either an early write or page mode early write cycle. The early write mode is discussed here, while the page mode write operation is covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early write mode is distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data In (DQ) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 512 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time (t_{RAC}). Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically refreshed (recharged) to maintain the correct bit state. Bits in the MCM84256 require refresh every 8 milliseconds while refresh time for the MCM8L4256 is 64 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM84256 and 124.8 microseconds for the MCM8L4256A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM84256A and 64 milliseconds on the MCM8L4256A.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **Hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read cycle**. Repeat this operation 512 times.
3. Select a column address, and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, write cycle**. Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

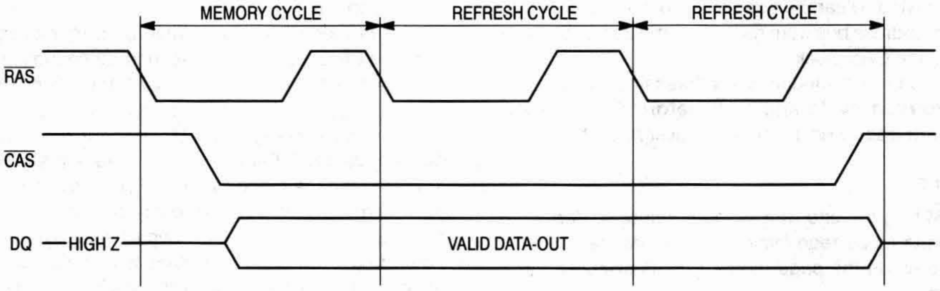


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION

(Order by Full Part Number)

MCM 84256 or 8L4256 X XX

Motorola Memory Prefix — MCM
Part Number — 84256 or 8L4256
Package (S = SIMM) — X
Speed (70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers — MCM84256S70 MCM8L4256S70
MCM84256S80 MCM8L4256S80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

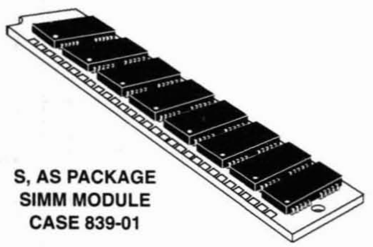
MCM81000
MCM8L1000

1M x 8 Bit Dynamic Random Access Module

The MCM81000 and MCM8L1000 are 8M dynamic random access memory (DRAM) modules organized as 1,048,576 x 8 bits. The modules are 30-lead single-in-line memory modules (SIMM) or 30-lead single-in-line packages (SIP) consisting of eight MCM511000A DRAMs housed in a 20/26 J-lead small outline package (SOJ) and mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM511000A is a 1.0µ CMOS high speed, dynamic random access memory organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM81000 = 8 ms (Max)
  MCM8L1000 = 64 ms (Max)
- Consists of Eight 1M DRAMs and Eight 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM81000-70 = 70 ns (Max)
  MCM81000-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM81000-70 = 3.6 W (Max)
  MCM81000-80 = 3.1 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 88 mW (Max)
  CMOS Levels (MCM81000) = 45 mW (Max)
  (MCM8L1000) = 9 mW (Max)
- $\overline{\text{CAS}}$ Control for Eight Common I/O Lines
- Available in Edge Connector (MCM81000S) or Two-Layer PCB Edge Connector (MCM81000AS)
- Available in Pin Connector (MCM81000L) or Double-Sided Low Height Pin Connector (MCM81000LH)
- For Application Requiring $\overline{\text{W}}$ to be Don't Care During $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycles
- 1M x 8 Modules are Available in Two-Chip Versions (MCM81430S)

PIN NAMES	
A0 – A9	Address Inputs
DQ0 – DQ7	Data Input/Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

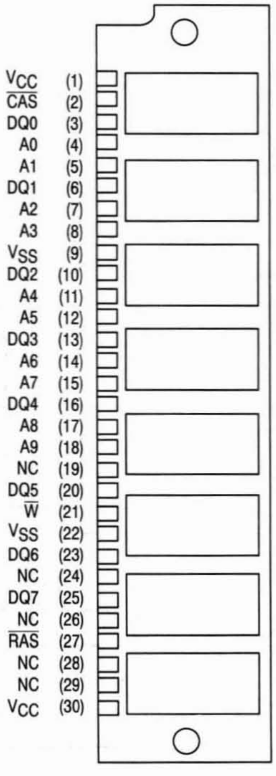


S, AS PACKAGE
SIMM MODULE
CASE 839-01

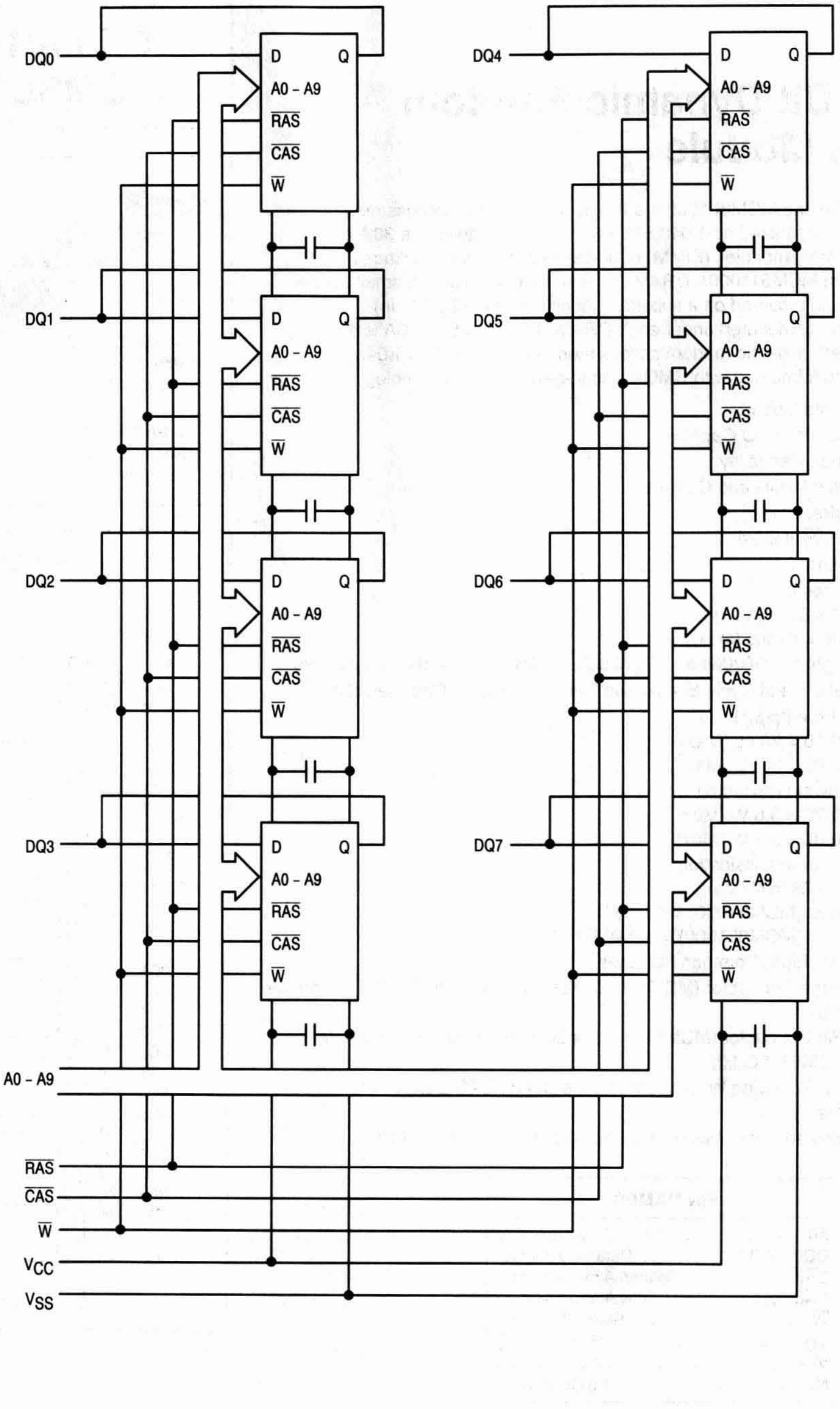
L PACKAGE
SIP MODULE
CASE 852-02

LH PACKAGE
LOW HEIGHT SIP
CASE 852A-02

TOP VIEW



FUNCTIONAL BLOCK DIAGRAM



DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
D
Q
A0 – A9
$\overline{RAS}$
$\overline{CAS}$
$\overline{W}$
A0 – A9
$\overline{RAS}$
$\overline{CAS}$
$\overline{W}$
V_{CC}
V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	4.8	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit
V_{CC} Power Supply Current MCM81000-70, t_{RC} = 130 ns MCM81000-80, t_{RC} = 150 ns	I_{CC1}	— —	640 560	mA
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	16	mA
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles MCM81000-70, t_{RC} = 130 ns MCM81000-80, t_{RC} = 150 ns	I_{CC3}	— —	640 560	mA
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM81000-70, t_{PC} = 40 ns MCM81000-80, t_{PC} = 45 ns	I_{CC4}	— —	480 400	mA
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM81000 MCM8L1000	I_{CC5}	— —	8 1.6	mA
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM81000-70, t_{RC} = 130 ns MCM81000-80, t_{RC} = 150 ns	I_{CC6}	— —	640 560	mA
V_{CC} Power Supply Current, Battery Backup Mode — MCM8L1000 Only (t_{RAC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0 – A9, $\overline{W}$, DQ = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	—	2.4	mA
Input Leakage Current ($V_{SS} \leq V_{in} \leq V_{CC}$)	$I_{lkg(I)}$	– 80	80	µA
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \leq V_{in} \leq V_{CC}$)	$I_{lkg(O)}$	– 20	20	µA
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V

NOTE: Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$	C_{in}	50	pF
Input/Output Capacitance	DQ0 – DQ7	$C_{I/O}$	15	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\,\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM81000-70 MCM8L1000-70		MCM81000-80 MCM8L1000-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
Access Time from RAS	t_{RELQV}	t_{RAC}	—	70	—	80	ns	6, 7
Access Time from CAS	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	6, 9
Access Time from Precharge CAS	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
CAS to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
RAS Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	ns	
RAS Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	ns	
RAS Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
CAS Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
CAS Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	ns	
RAS to CAS Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	ns	11
RAS to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	ns	12
CAS to RAS Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
CAS Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address Hold Time Referenced to RAS	t_{RELAX}	t_{AR}	55	—	60	—	ns	
Column Address to RAS Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

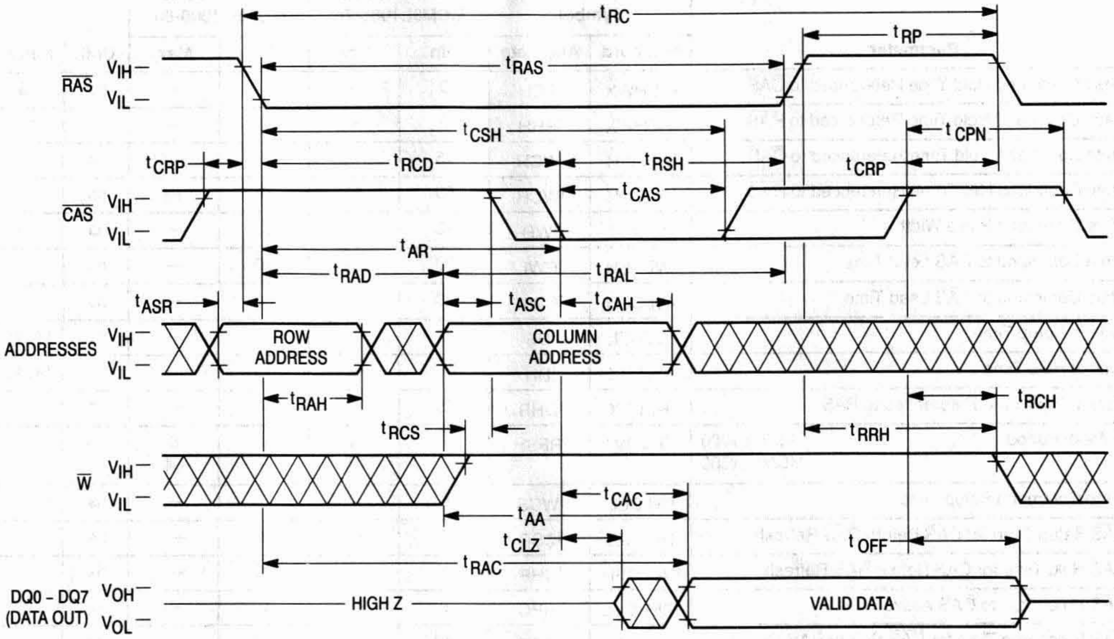
READ AND WRITE CYCLES (Continued)

	Symbol		MCM81000-70 MCM8L1000-70		MCM81000-80 MCM8L1000-80			
Parameter	**Standard**	**Alternate**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	15	—	15	—	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELWH}	t_{WCR}	55	—	60	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14, 15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14, 15
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	55	—	60	—	ns	
Refresh Period MCM81000 MCM8L1000	t_{RVRV}	t_{RFSH}	— —	8 64	— —	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15, 16
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	ns	

NOTES:

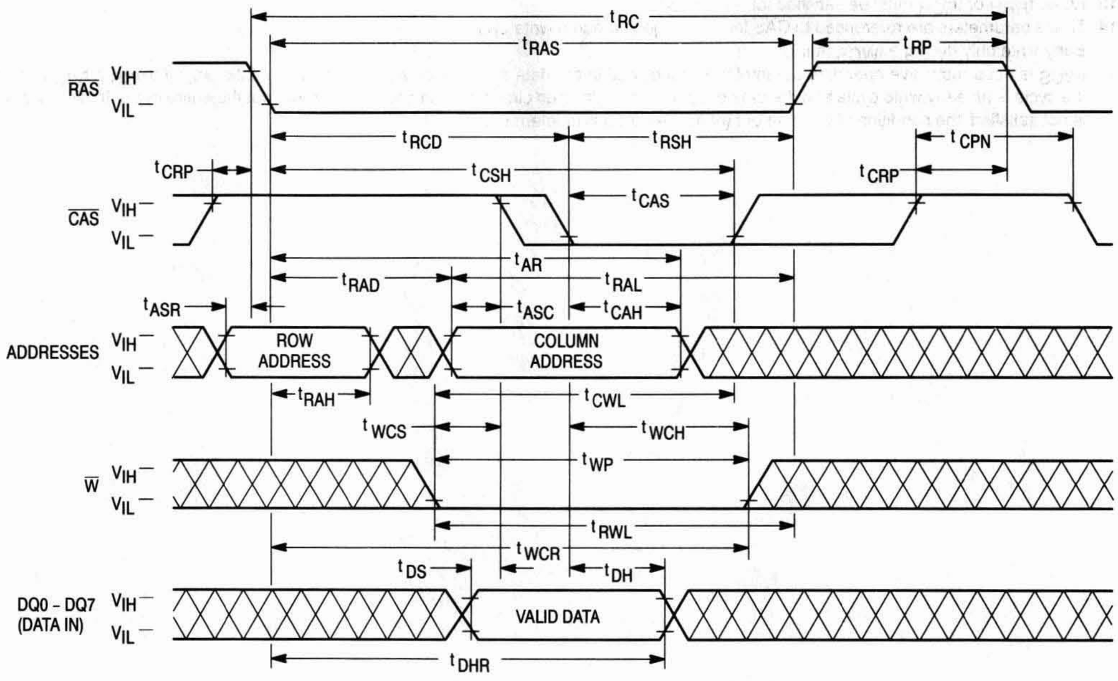
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



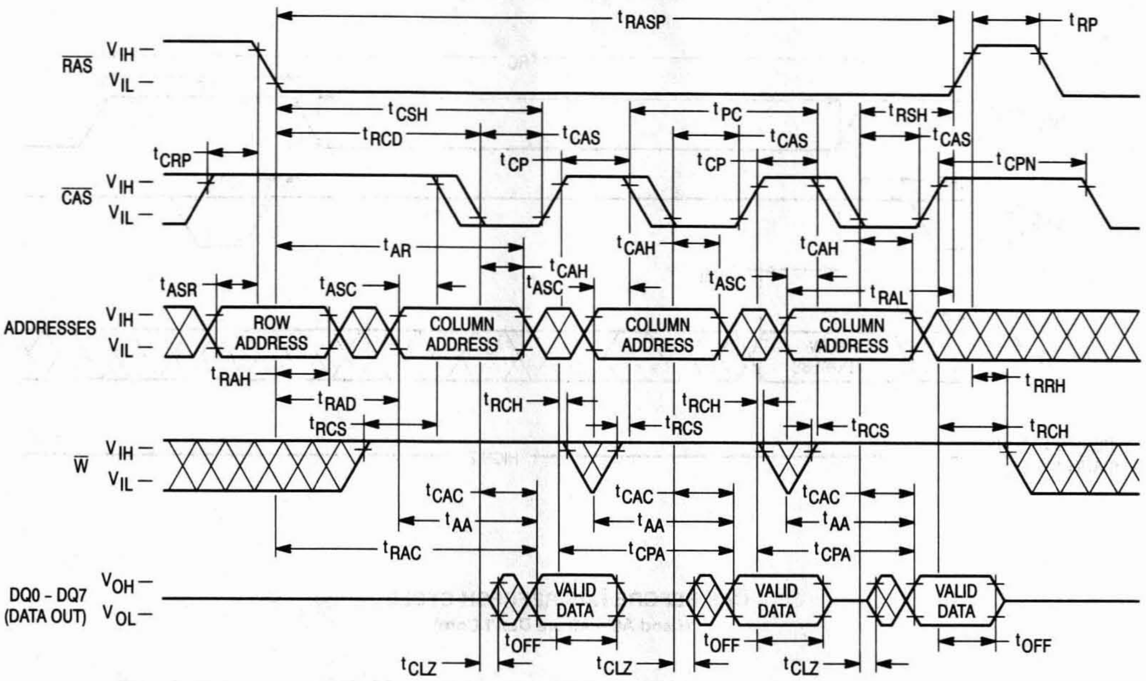
t_{RC}
t_{RP}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{CPN}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{AR}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RAH}
t_{RCH}
t_{RCS}
t_{RRH}
$\overline{W}$
V_{IH}
V_{IL}
t_{CAC}
t_{AA}
t_{CLZ}
t_{OFF}
t_{RAC}
DQ0 - DQ7 (DATA OUT)
V_{OH}
V_{OL}
HIGH Z
VALID DATA

EARLY WRITE CYCLE



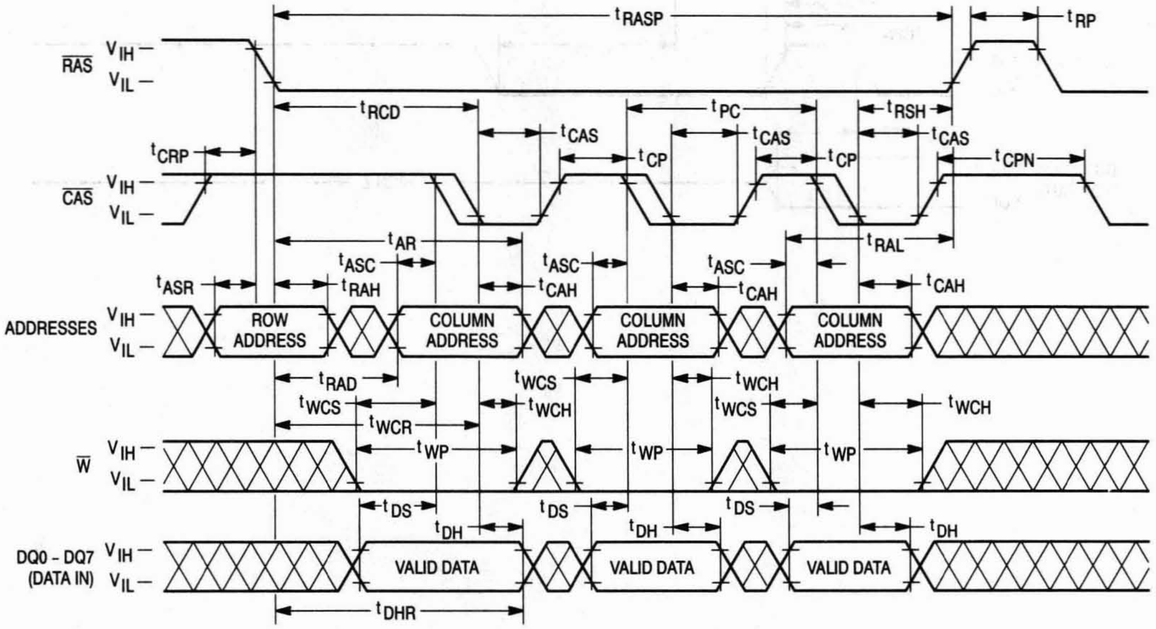
t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RCD}
t_{RSH}
t_{CPN}
t_{CRP}
t_{CSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{AR}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RAH}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{W}$
V_{IH}
V_{IL}
t_{RWL}
t_{WCR}
t_{DS}
t_{DH}
DQ0 - DQ7 (DATA IN)
V_{IH}
V_{IL}
VALID DATA
t_{DHR}

FAST PAGE MODE READ CYCLE



tRASP
tRP
RAS
VIH
VIL
tCSH
tPC
tRSH
tRCD
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCPN
CAS
VIH
VIL
tAR
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
tRAL
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAH
tRRH
tRAD
tRCH
tRCH
tRCS
tRCS
tRCS
tRCH
W
VIH
VIL
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
DQ0 - DQ7 (DATA OUT)
VOH
VOL
VALID DATA
VALID DATA
VALID DATA
tOFF
tOFF
tOFF
tCLZ
tCLZ
tCLZ

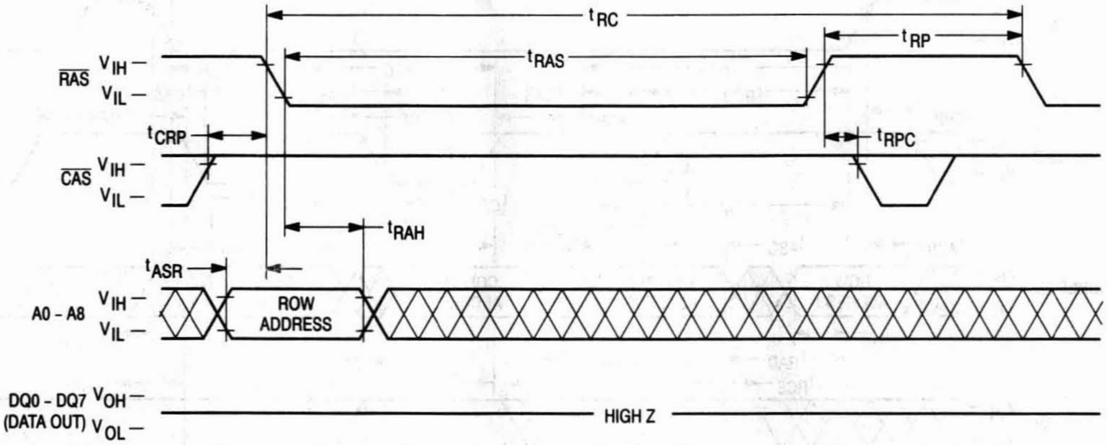
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



tRASP
tRP
RAS
VIH
VIL
tRCD
tPC
tRSH
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCPN
CAS
VIH
VIL
tAR
tRAL
tASC
tASC
tASC
tASR
tRAH
tCAH
tCAH
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tWCS
tWCS
tWCS
tWCH
tWCH
tWCH
tWCR
tWP
tWP
tWP
W
VIH
VIL
tDS
tDS
tDS
tDH
tDH
tDH
DQ0 - DQ7 (DATA IN)
VIH
VIL
VALID DATA
VALID DATA
VALID DATA
tDHR

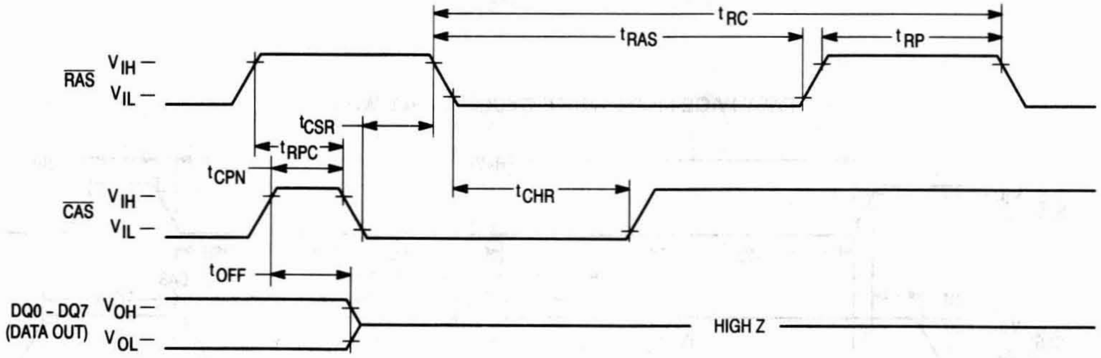
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

($\overline{\text{W}}$ and A9 are Don't Care)

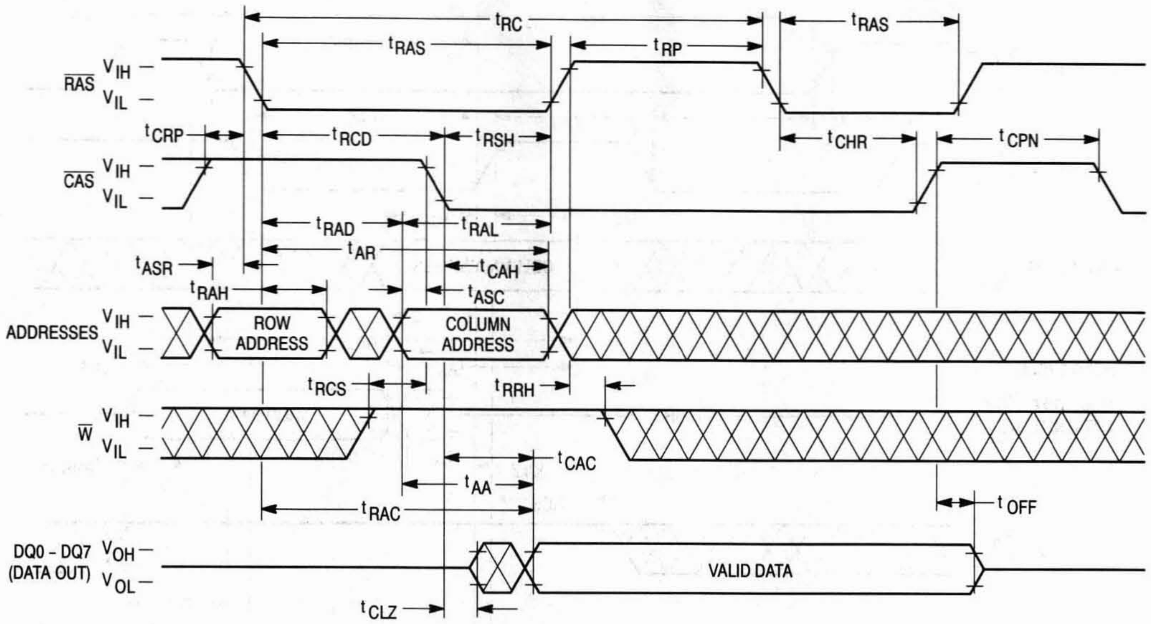

t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
A0 – A8
V_{IH}
V_{IL}
ROW ADDRESS
DQ0 – DQ7
(DATA OUT)
V_{OH}
V_{OL}
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

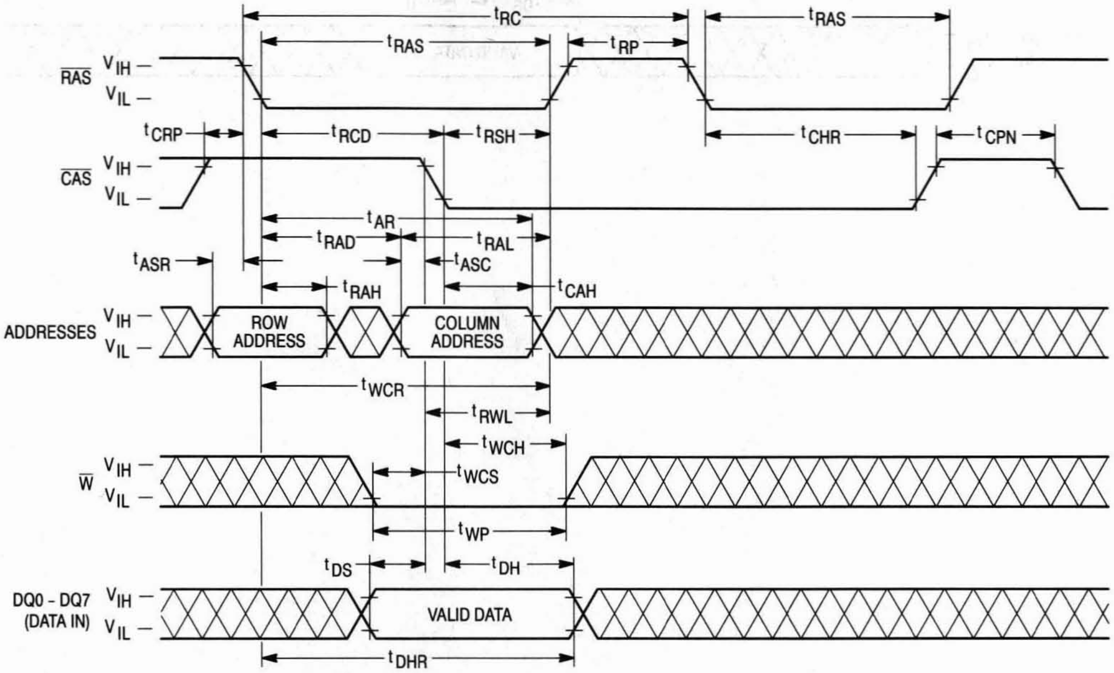
($\overline{\text{W}}$ and A0 – A9 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CSR}
t_{RPC}
t_{CPN}
t_{CHR}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{OFF}
DQ0 – DQ7
(DATA OUT)
V_{OH}
V_{OL}
HIGH Z

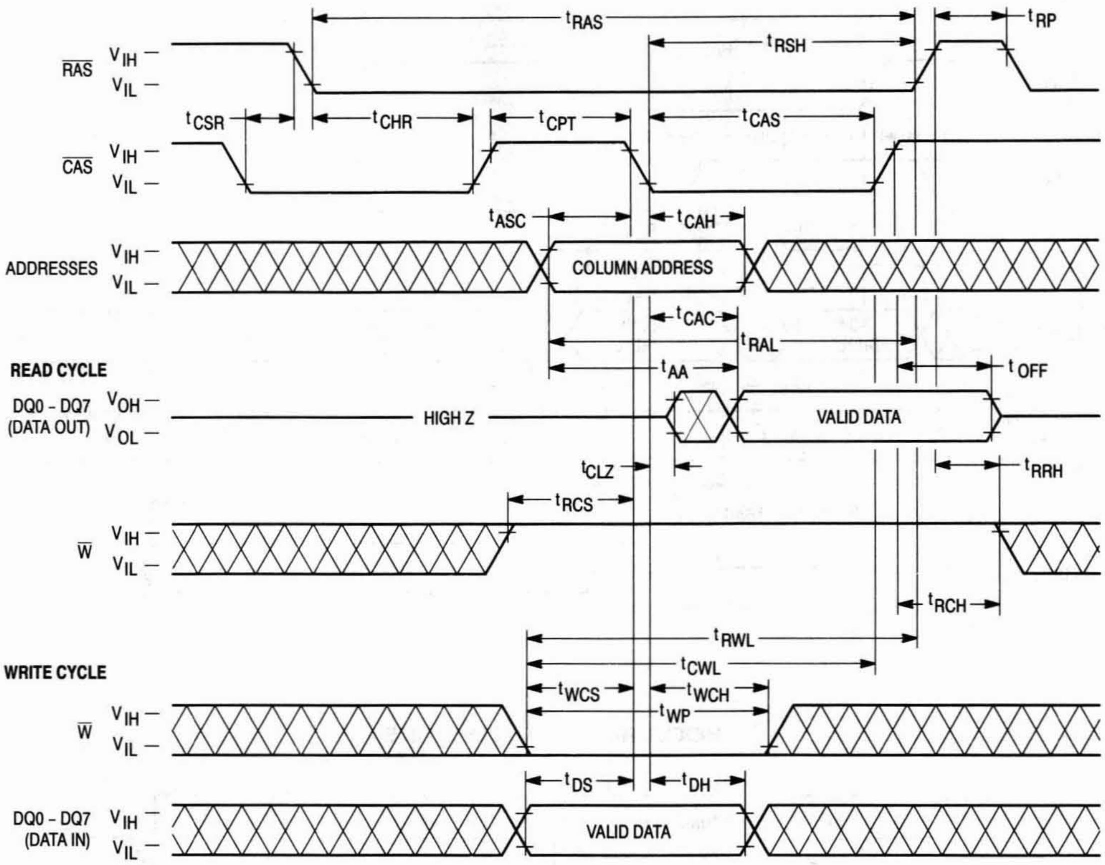
HIDDEN REFRESH CYCLE (READ)


t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$ V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CPN}
$\overline{CAS}$ V_{IH}
V_{IL}
t_{RAD}
t_{RAL}
t_{AR}
t_{ASR}
t_{CAH}
t_{RAH}
t_{ASC}
ADDRESSES V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RCS}
t_{RRH}
$\overline{W}$ V_{IH}
V_{IL}
t_{CAC}
t_{AA}
t_{RAC}
t_{OFF}
DQ0 - DQ7 (DATA OUT) V_{OH}
V_{OL}
VALID DATA
t_{CLZ}

HIDDEN REFRESH CYCLE (WRITE)


t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$ V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CPN}
$\overline{CAS}$ V_{IH}
V_{IL}
t_{AR}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{WCR}
t_{RWL}
t_{WCH}
$\overline{W}$ V_{IH}
V_{IL}
t_{WCS}
t_{WP}
t_{DS}
t_{DH}
DQ0 - DQ7 (DATA IN) V_{IH}
V_{IL}
VALID DATA
t_{DHR}

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



t_{RAS}
t_{RP}
t_{RSH}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CSR}
t_{CHR}
t_{CPT}
t_{CAS}
$\overline{\text{CAS}}$
t_{ASC}
t_{CAH}
ADDRESSES
COLUMN ADDRESS
t_{CAC}
t_{RAL}
READ CYCLE
t_{AA}
t_{OFF}
DQ0 - DQ7 (DATA OUT)
V_{OH}
V_{OL}
HIGH Z
VALID DATA
t_{CLZ}
t_{RRH}
t_{RCS}
$\overline{\text{W}}$
t_{RCH}
t_{RWL}
WRITE CYCLE
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
t_{DS}
t_{DH}
DQ0 - DQ7 (DATA IN)
VALID DATA

5

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the module are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 byte locations in the module. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are two other variations in addressing the 1M RAM: **$\overline{RAS}$-only refresh cycle,** and **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either the "normal" random read cycle or the page mode read cycle. The normal read cycle is outlined here, while the page mode is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired byte location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. However, $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for times t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device cir-cuitry for the next active cycle. Data out (DQ) is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z.

WRITE CYCLE

The user can write to the module with either of two cycles: early write or page mode early write. Early write mode is discussed here, while the page mode write operation is covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (DQ) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the 1M dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum of t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bytes in the MCM81000 require refresh every 8 milliseconds, while refresh time for the MCM8L1000 is 64 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM81000, and 124.8 microseconds for the MCM8L1000. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM81000 and 64 milliseconds on the MCM8L1000.

A normal read, write, or read-write operation to the RAM will refresh all the bytes associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order actives an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode cycle) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 CAS before RAS** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, and read "0" out of the cell by performing **CAS before RAS refresh counter test, read cycle**. Repeat this operation 512 times.
3. Select a column address and write "1" into the cell by performing the **CAS before RAS refresh counter test, write cycle**. Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

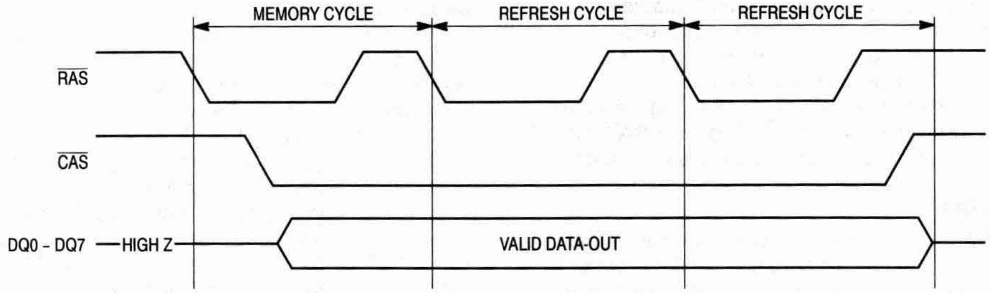


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM **81000 / 8L1000** **X** **XX**

Motorola Memory Prefix — MCM
Part Number — 81000 / 8L1000
Package (L = SIP, LH = Low Height SIP, S = 4-Layer SIMM, AS = 2-Layer SIMM) — X
Speed (70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers —			
MCM81000AS70	MCM81000S70	MCM81000L70	MCM81000LH70
MCM81000AS80	MCM81000S80	MCM81000L80	MCM81000LH80
MCM8L1000AS70	MCM8L1000S70	MCM8L1000L70	MCM8L4030LH70
MCM8L1000AS80	MCM8L1000S80	MCM8L1000L80	MCM8L4030LH80

NOTE: For mechanical data, please see Chapter 10.

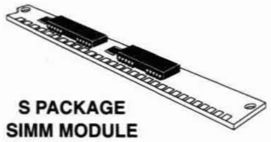
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM81430
MCM8L1430

1M x 8 Bit Dynamic Random Access Module

The MCM81430 and MCM8L1430 are 8M dynamic random access memory (DRAM) modules organized as 1,048,576 x 8 bits. The modules are 30-lead single-in-line memory modules (SIMM) consisting of two MCM54400AN DRAMs housed in a 20/26 J-lead small outline package (SOJ) and mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted adjacent to each DRAM. The MCM54400AN is a CMOS high-speed dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.

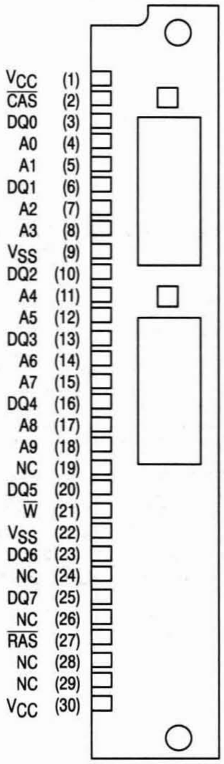
- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  - MCM81430 = 16 ms (Max)
  - MCM8L1430 = 128 ms (Max)
- Consists of Two 4M DRAMs and Two 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM81430-60 = 60 ns (Max)
  - MCM81430-70 = 70 ns (Max)
  - MCM81430-80 = 80 ns (Max)
- Low Active Power Dissipation:
  - MCM81430-60 = 1.32 W (Max)
  - MCM81430-70 = 1.10 W (Max)
  - MCM81430-80 = 0.94 W (Max)
- Low Standby Power Dissipation:
  - TTL Levels = 22 mW (Max)
  - CMOS Levels (MCM81430) = 11 mW (Max)
  - (MCM8L1430) = 2.2 mW (Max)
- $\overline{\text{CAS}}$ Control for Eight Common I/O Lines
- Available in Edge Connector (MCM81430S) or Pin Connector (MCM81430L)



S PACKAGE
SIMM MODULE
CASE 839A-01

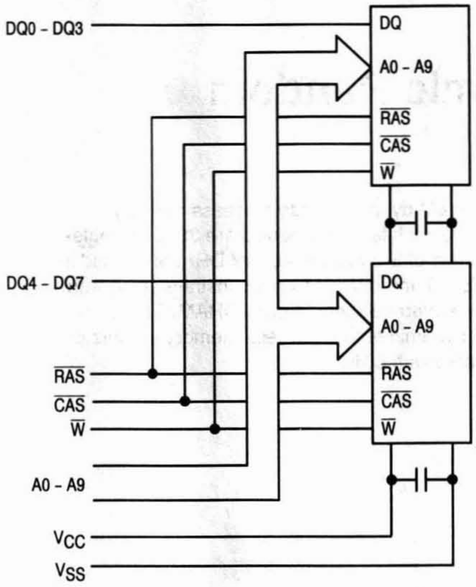
L PACKAGE
SIP MODULE
CASE 852A-02

TOP VIEW



PIN NAMES	
A0 – A9	Address Inputs
DQ0 – DQ7	Data Input/Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	1.4	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM81430-60, t_{RC} = 110 ns MCM81430-70, t_{RC} = 130 ns MCM81430-80, t_{RC} = 150 ns	I_{CC1}	— — —	240 200 170	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	4	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles MCM81430-60, t_{RC} = 110 ns MCM81430-70, t_{RC} = 130 ns MCM81430-80, t_{RC} = 150 ns	I_{CC3}	 — — —	 240 200 170	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM81430-60, t_{PC} = 45 ns MCM81430-70, t_{PC} = 45 ns MCM81430-80, t_{PC} = 50 ns	I_{CC4}	 — — —	 140 140 120	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM81430 MCM8L1430	I_{CC5}	— —	2 0.4	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM81430-60, t_{RC} = 110 ns MCM81430-70, t_{RC} = 130 ns MCM81430-80, t_{RC} = 150 ns	I_{CC6}	 — — —	 240 200 170	mA	1
V_{CC} Power Supply Current, Battery Backup Mode — MCM81430 Only (t_{RAC} = 125 μs; t_{RAS} = 1 μs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0 – A9, $\overline{W}$, DQ = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	—	0.6	mA	1, 3
Input Leakage Current (0 $V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 20	20	μA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	– 10	10	μA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. t_{RAS} (max) = 1 μs is only applied to refresh of battery backup. t_{RAS} (max) = 10 μs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$	C_{in}	24	pF
Input/Output Capacitance	DQ0 – DQ7	$C_{I/O}$	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM81430-60 MCM8L1430-60		MCM81430-70 MCM8L1430-70		MCM81430-80 MCM8L1430-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	50	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	40	—	40	—	45	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	200 k	70	200 k	80	200 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	20	10 k	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

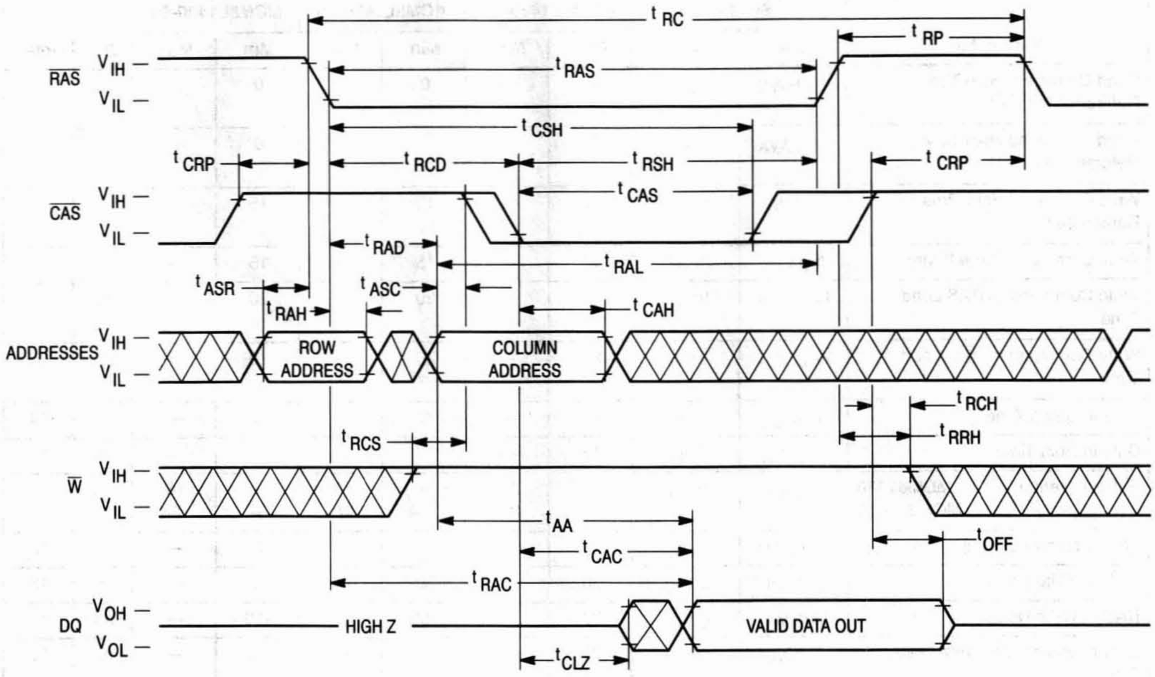
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM81430-60 MCM8L1430-60		MCM81430-70 MCM8L1430-70		MCM81430-80 MCM8L1430-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	14
Refresh Period MCM81430 MCM8L1430	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	50	—	ns	15
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	90	—	100	—	110	—	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	60	—	65	—	70	—	ns	15
$\overline{\text{CAS}}$ Precharge to Write Delay Time (Page Mode)	t_{CEHWL}	t_{CPWD}	70	—	70	—	75	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Time	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	

NOTES:

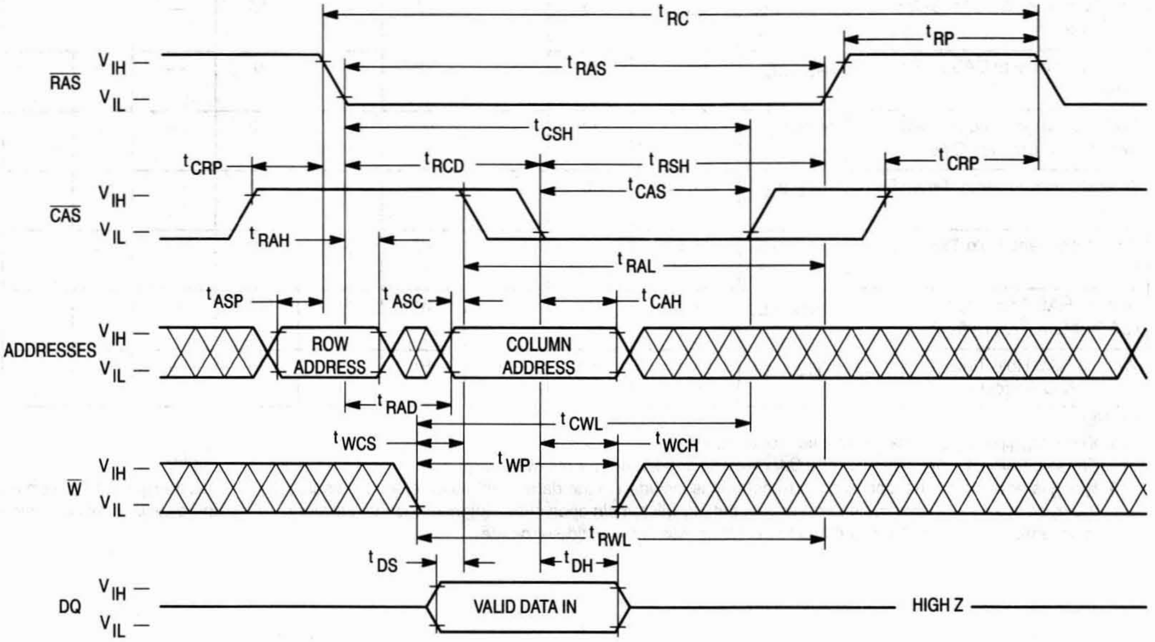
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



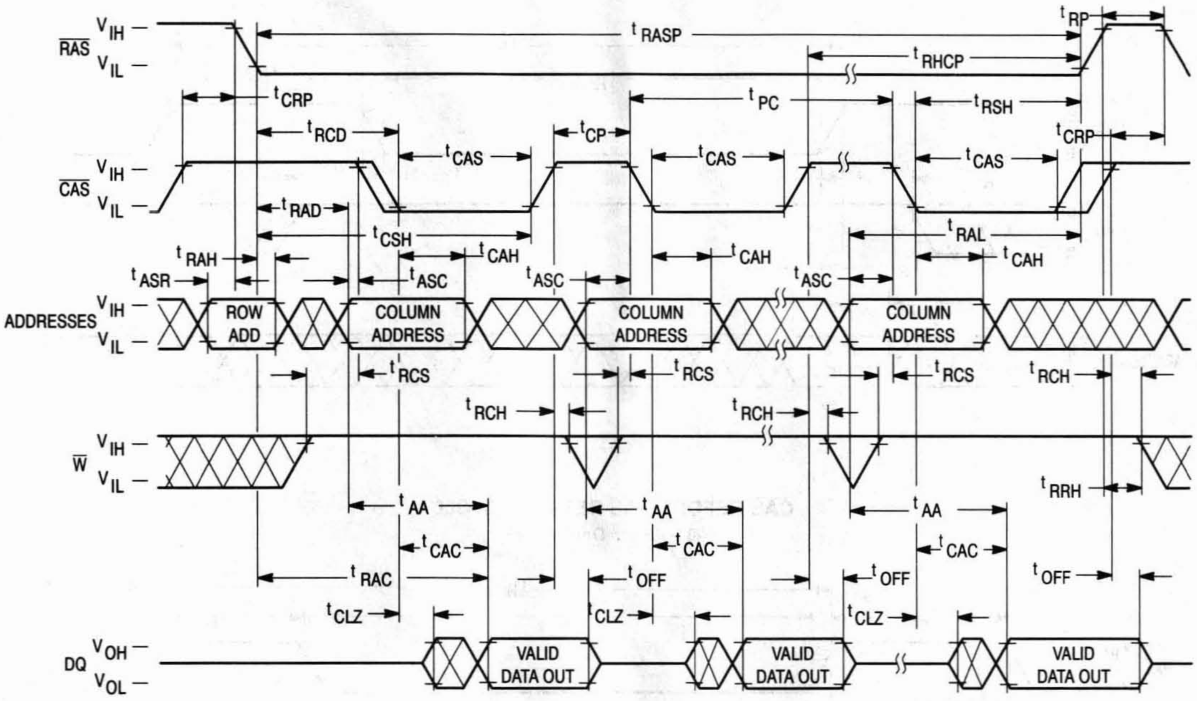
t RC
t RP
t RAS
RAS
V IH
V IL
t CSH
t CRP
t RCD
t RSH
t CRP
t CAS
CAS
V IH
V IL
t RAD
t RAL
t ASR
t ASC
t RAH
t CAH
ADDRESSES
V IH
V IL
ROW ADDRESS
COLUMN ADDRESS
t RCH
t RRH
t RCS
W
V IH
V IL
t AA
t OFF
t CAC
t RAC
DQ
V OH
V OL
HIGH Z
VALID DATA OUT
t CLZ

EARLY WRITE CYCLE

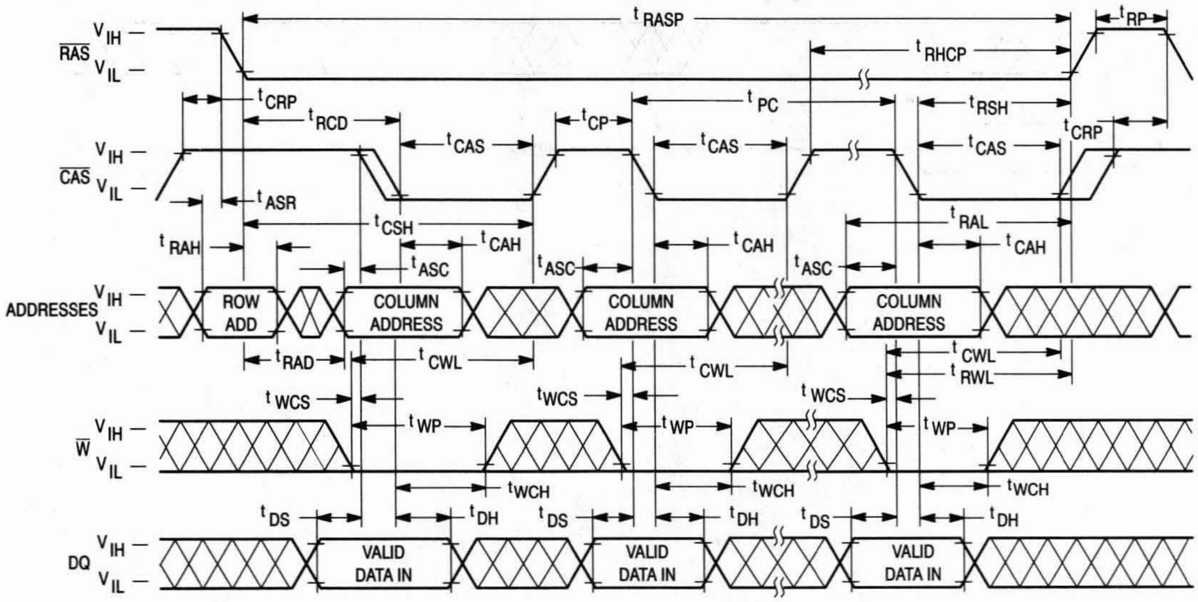


t RC
t RP
t RAS
RAS
V IH
V IL
t CSH
t CRP
t RCD
t RSH
t CRP
t CAS
CAS
V IH
V IL
t RAH
t RAL
t ASP
t ASC
t CAH
ADDRESSES
V IH
V IL
ROW ADDRESS
COLUMN ADDRESS
t RAD
t CWL
t WCS
t WCH
t WP
W
V IH
V IL
t RWL
t DS
t DH
DQ
V IH
V IL
VALID DATA IN
HIGH Z

FAST PAGE MODE READ CYCLE

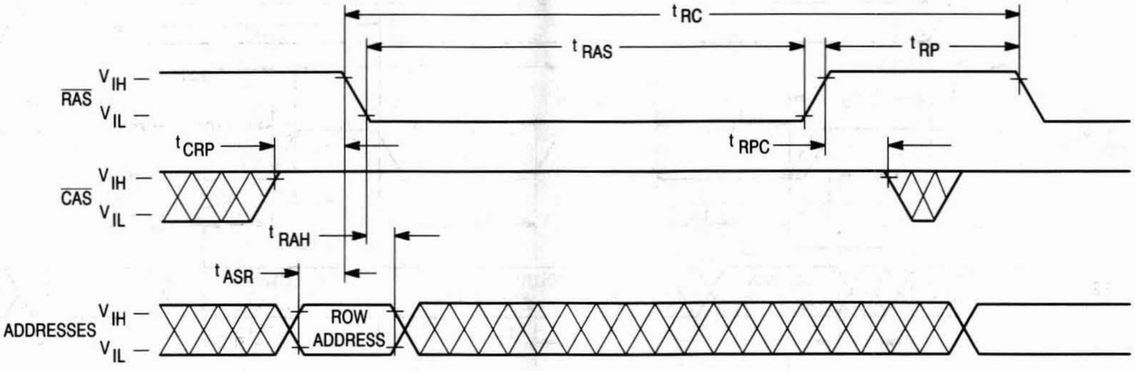

RAS
VIH
VIL
tRASP
tRP
tRHCP
tCRP
tPC
tRSH
tRCD
tCP
tCAS
tCRP
CAS
VIH
VIL
tRAD
tCSH
tRAL
tRAH
tCAH
tASR
tASC
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRCS
tRCH
W
VIH
VIL
tRRH
tAA
tCAC
tRAC
tOFF
tCLZ
DQ
VOH
VOL
VALID DATA OUT
VALID DATA OUT
VALID DATA OUT

FAST PAGE MODE EARLY WRITE CYCLE


RAS
VIH
VIL
tRASP
tRP
tRHCP
tCRP
tRCD
tCP
tPC
tRSH
tCAS
tCRP
CAS
VIH
VIL
tASR
tCSH
tRAL
tRAH
tCAH
tASC
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tCWL
tRWL
tWCS
tWP
W
VIH
VIL
tWCH
tDS
tDH
DQ
VIH
VIL
VALID DATA IN
VALID DATA IN
VALID DATA IN

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

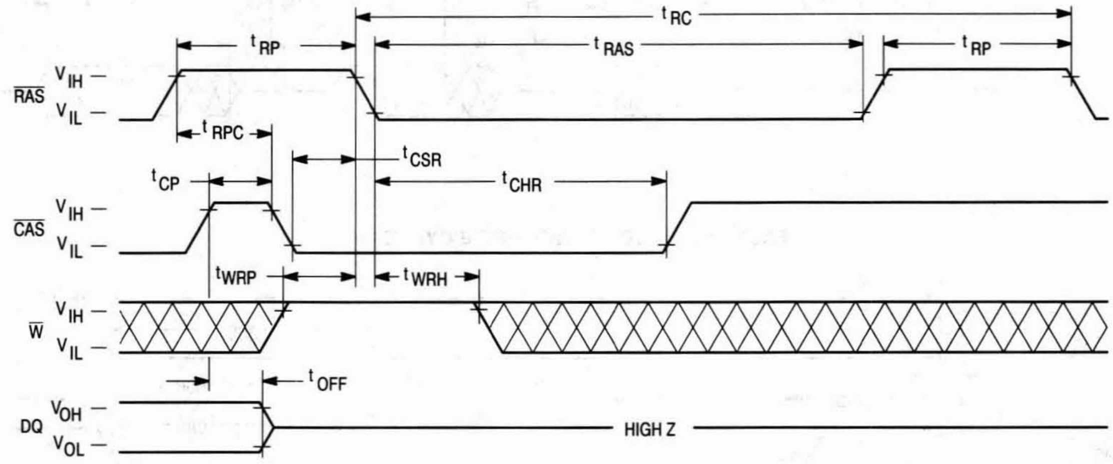
($\overline{\text{W}}$ is Don't Care)



t RC
t RAS
t RP
V IH
RAS
V IL
t CRP
t RPC
CAS
t RAH
t ASR
ADDRESSES
ROW ADDRESS

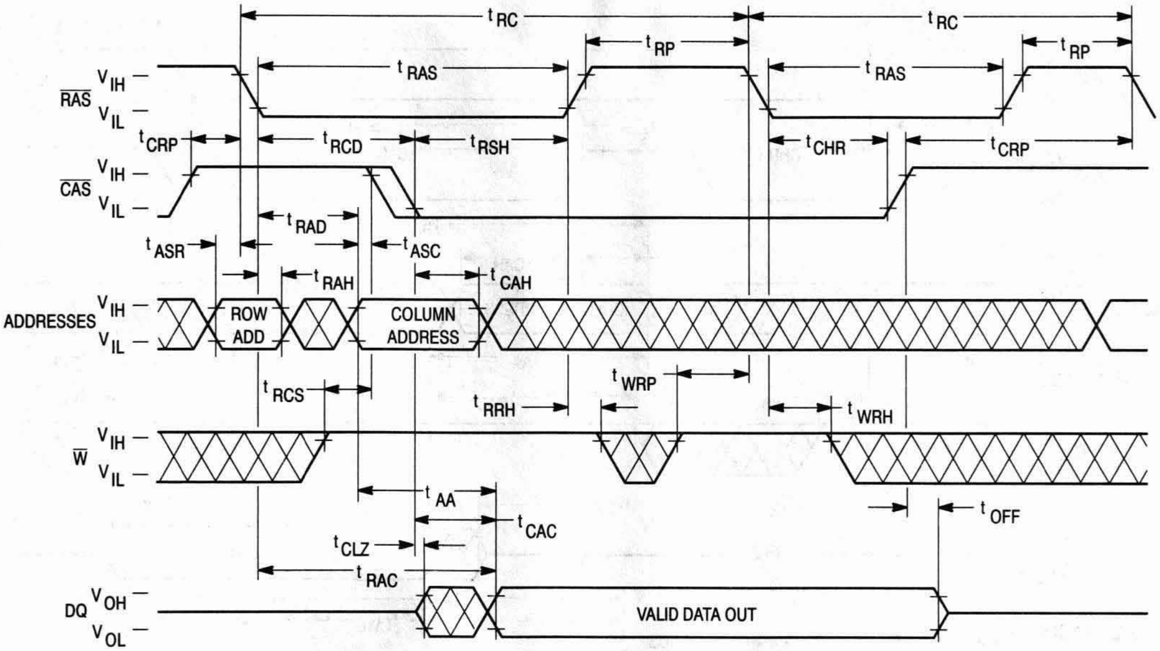
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

(A0 – A9 are Don't Care)



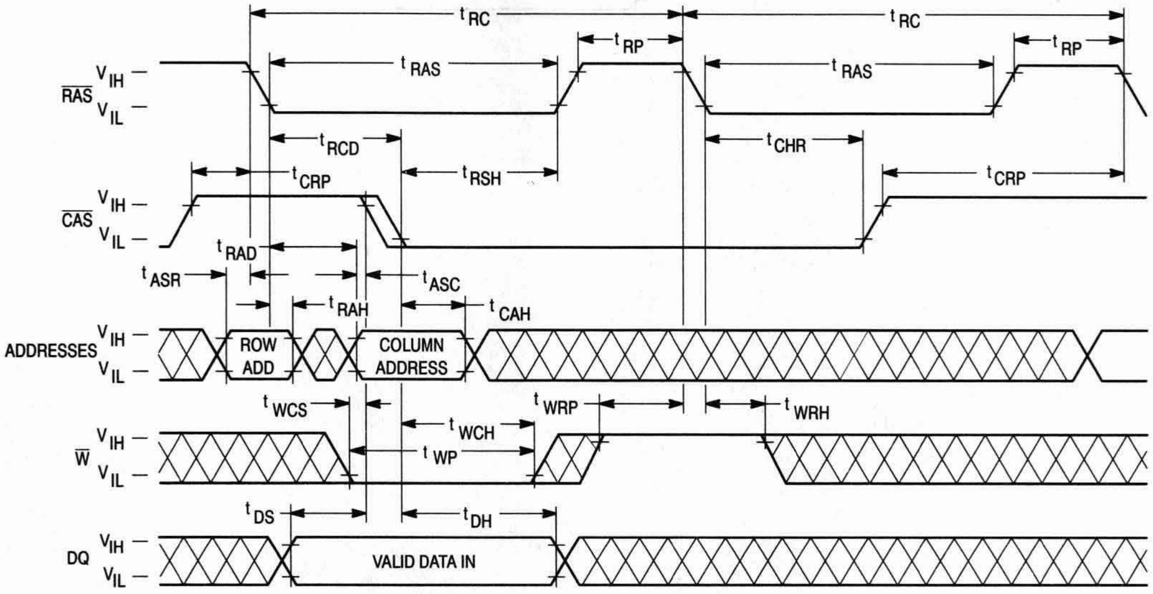
t RC
t RP
t RAS
t RP
V IH
RAS
V IL
t RPC
t CSR
t CP
t CHR
CAS
t WRP
t WRH
W
t OFF
V OH
DQ
V OL
HIGH Z

HIDDEN REFRESH CYCLE (READ)



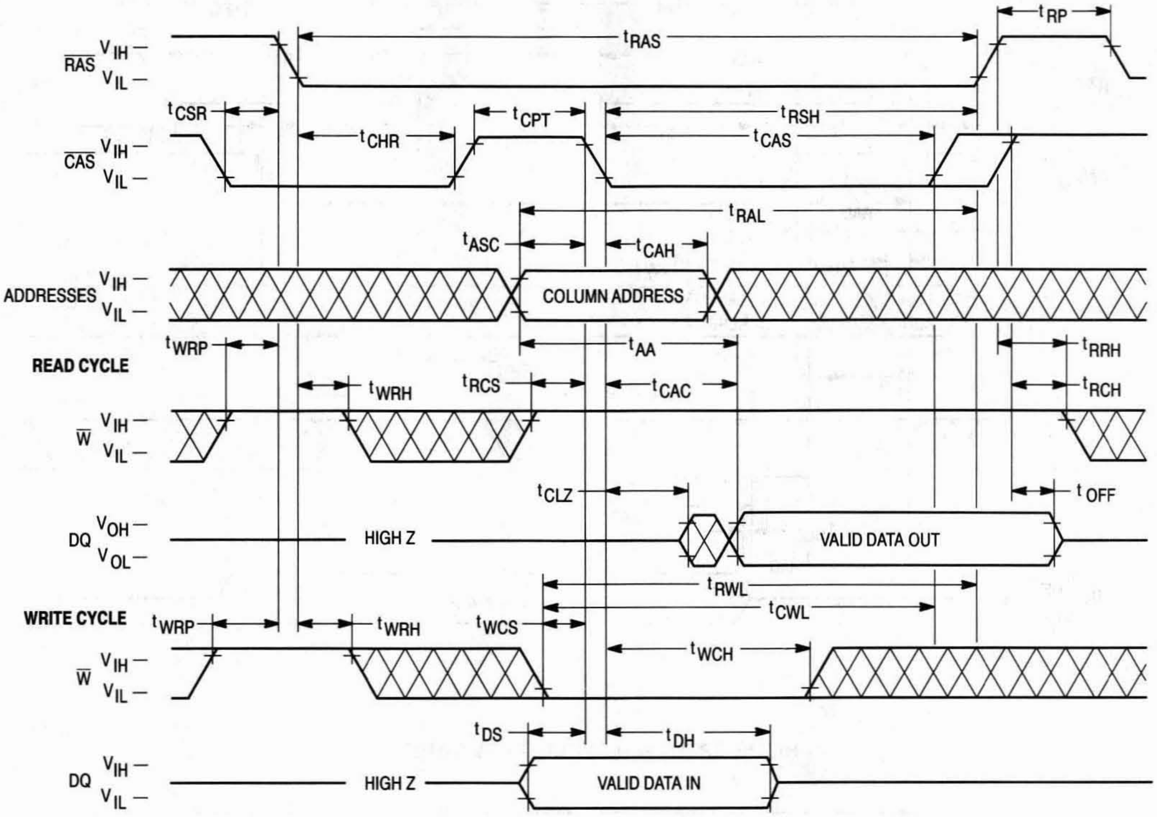
tRC
tRC
tRP
tRP
tRAS
tRAS
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCRP
CAS
VIH
VIL
tRAD
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
tRCS
tWRP
tRRH
tWRH
W
VIH
VIL
tAA
tCAC
tOFF
tCLZ
tRAC
DQ
VOH
VOL
VALID DATA OUT

HIDDEN REFRESH CYCLE (EARLY WRITE)



tRC
tRC
tRP
tRP
tRAS
tRAS
RAS
VIH
VIL
tRCD
tCHR
tRSH
tCRP
tCRP
CAS
VIH
VIL
tRAD
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
tWCS
tWRP
tWRH
tWCH
tWP
W
VIH
VIL
tDS
tDH
DQ
VIH
VIL
VALID DATA IN

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE


$\overline{\text{RAS}}$
V_{IH} —
V_{IL} —
t_{RAS}
t_{RP}
$\overline{\text{CAS}}$
t_{CSR}
t_{CHR}
t_{CPT}
t_{RSH}
t_{CAS}
t_{RAL}
t_{ASC}
t_{CAH}
ADDRESSES
COLUMN ADDRESS
t_{WRP}
t_{AA}
t_{RRH}
READ CYCLE
t_{WRH}
t_{RCS}
t_{CAC}
t_{RCH}
$\overline{W}$
t_{CLZ}
t_{OFF}
DQ
V_{OH} —
V_{OL} —
HIGH Z
VALID DATA OUT
t_{RWL}
t_{CWL}
WRITE CYCLE
t_{WRP}
t_{WRH}
t_{WCS}
t_{WCH}
t_{DS}
t_{DH}
HIGH Z
VALID DATA IN

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 byte locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the module: **$\overline{\text{RAS}}$ only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either a "normal" random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. $\overline{\text{CAS}}$ controls read access time: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ clock active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with either an early write or page mode early write cycle. Early write mode is discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early write mode is distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (DQ) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM81430 require refresh every 16 milliseconds, while refresh time for the MCM8L1430 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM81430, and 124.8 microseconds for the MCM8L1430. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM81430 and 128 milliseconds on the MCM8L1430.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{\text{RAS}}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode cycle) as in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 test cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, and read "0" out of the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read cycle**. Repeat this operation 512 times.
3. Select a column address and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, write cycle**. Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

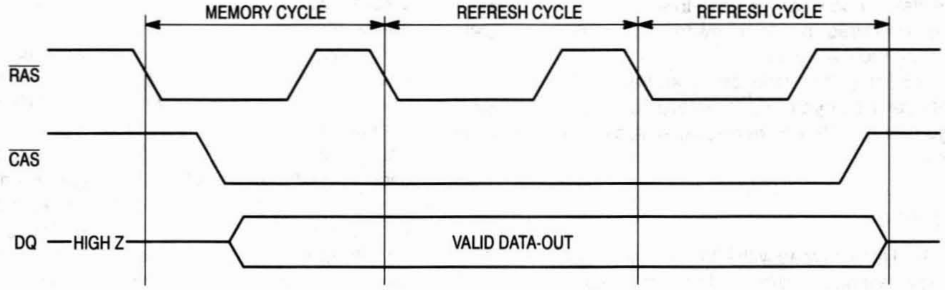


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 81430 or 8L1430 X XX

Motorola Memory Prefix — MCM
Part Number — 81430 or 8L1430
Package (S = SIMM, L = SIP) — X
Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers — MCM81430S60 MCM81430L60
MCM81430S70 MCM81430L70
MCM81430S80 MCM81430L80

MCM8L1430S60 MCM8L1430L60
MCM8L1430S70 MCM8L1430L70
MCM8L1430S80 MCM8L1430L80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

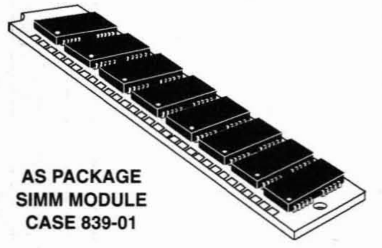
MCM84000
MCM8L4000
MCM84030

4M x 8 Bit Dynamic Random Access Memory Module

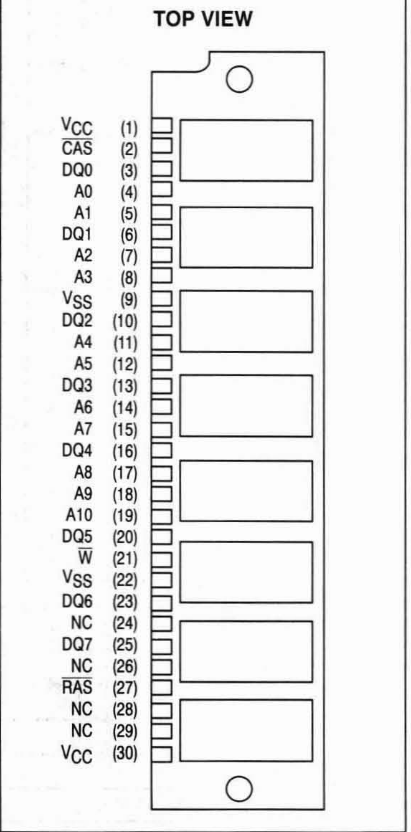
The MCM84000 is a 32M dynamic random access memory (DRAM) module organized as 4,194,304 x 8 bits. The module is a 30-lead single-in-line memory modules (SIMM) consisting of eight MCM54100A DRAMs housed in a 20/26 J lead small outline packages (SOJ) mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM54100A is a CMOS high speed, dynamic random access memory organized as 4,194,304 one bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  MCM84000 = 16 ms (Max)
  MCM8L4000 = 128 ms (Max)
- Consists of Eight 4M x 1 DRAMs and Eight 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM84000-60 = 60 ns (Max)
  MCM84000-70 = 70 ns (Max)
  MCM84000-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM84000-60 and MCM8L4000-60 = 5.28 W (Max)
  MCM84000-70 and MCM8L4000-70 = 4.40 W (Max)
  MCM84000-80 and MCM8L4000-80 = 3.74 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 88 mW (Max)
  CMOS Levels (MCM84000) = 44 mW (Max)
  (MCM8L4000) = 8.8 mW (Max)
- $\overline{\text{CAS}}$ Control for Eight Common I/O Lines
- Available in Edge Connector (MCM84000AS), Pin Connector (MCM84000L), or Low Height Pin Connector (MCM84030LH)

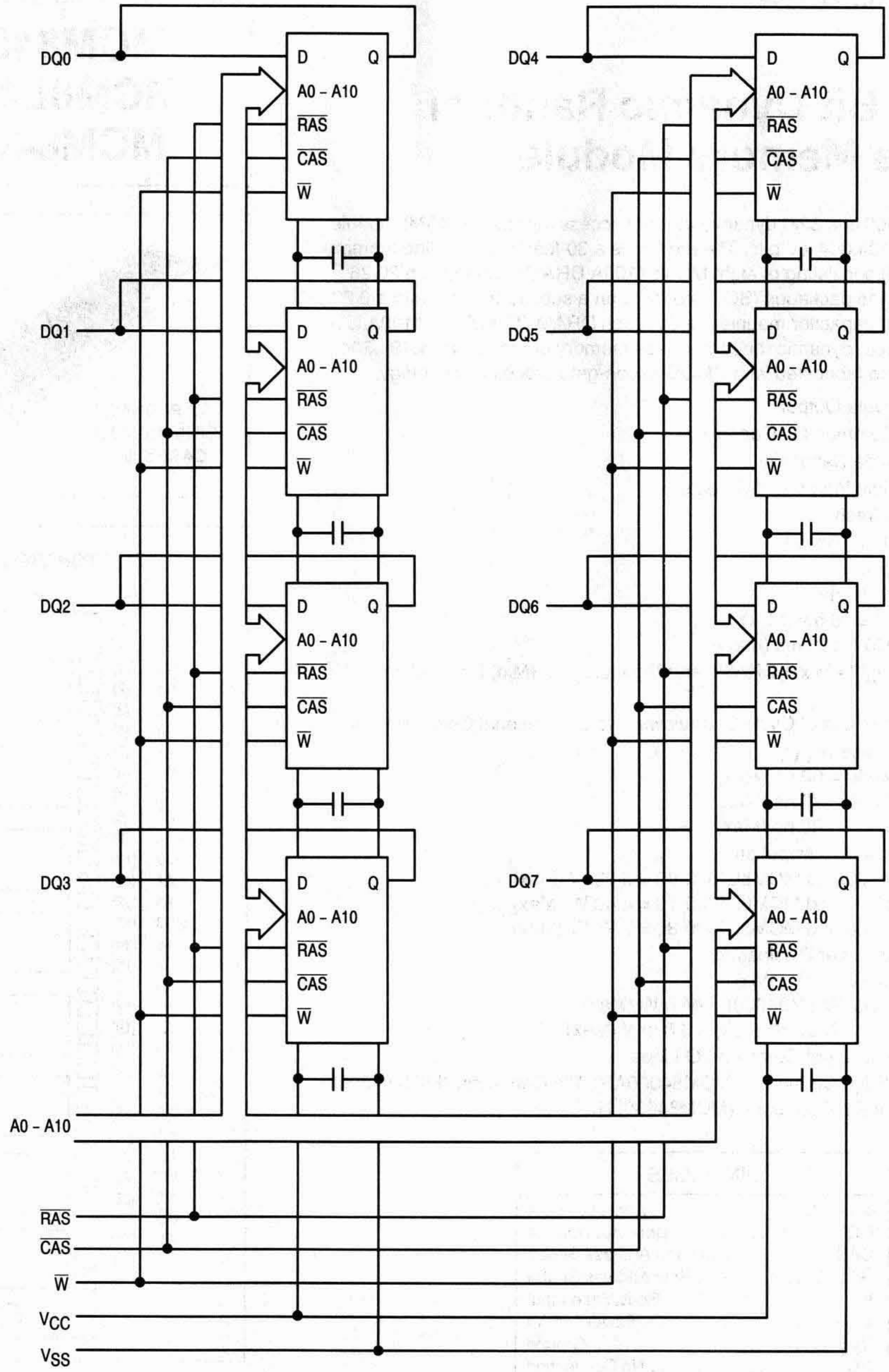
PIN NAMES	
A0 – A10	Address Inputs
DQ0 – DQ7	Data Input/Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection



AS PACKAGE
SIMM MODULE
CASE 839-01



FUNCTIONAL BLOCK DIAGRAM


DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
D
Q
A0 – A10
RAS
CAS
W
A0 – A10
RAS
CAS
W
V_{CC}
V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	5.6	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM84000-60, t_{RC} = 110 ns MCM84000-70, t_{RC} = 130 ns MCM84000-80, t_{RC} = 150 ns	I_{CC1}	— — —	960 800 680	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	16	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles MCM84000-60, t_{RC} = 110 ns MCM84000-70, t_{RC} = 130 ns MCM84000-80, t_{RC} = 150 ns	I_{CC3}	— — —	960 800 680	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM84000-60, t_{PC} = 45 ns MCM84000-70, t_{PC} = 45 ns MCM84000-80, t_{PC} = 50 ns	I_{CC4}	— — —	480 480 400	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM84000 MCM8L4000	I_{CC5}	— —	8 1.6	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM84000-60, t_{RC} = 110 ns MCM84000-70, t_{RC} = 130 ns MCM84000-80, t_{RC} = 150 ns	I_{CC6}	— — —	960 800 680	mA	1
V_{CC} Power Supply Current, Battery Backup Mode — MCM8L4000 Only (t_{RC} = 125 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$ = V_{CC} – 0.2 V; DQ = V_{CC} – 0.2 V, 0.2 V or Open; A0 – A10 = V_{CC} – 0.2 V or 0.2 V) t_{RAS} = Min to 1 µs	I_{CC7}	—	2.4	mA	1, 3
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 80	80	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(O)}$	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery backup. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A10, $\overline{\text{W}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$	C_{in}	50	pF
Input/Output Capacitance	DQ0 – DQ7	$C_{I/O}$	22	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

	Symbol		MCM84000-60 MCM8L4000-60 MCM84030-60		MCM84000-70 MCM8L4000-70 MCM84030-70		MCM84000-80 MCM8L4000-80 MCM84030-80			
Parameter	Std	Alt	Min	Max	Min	Max	Min	Max	Unit	Notes
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	50	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	40	—	40	—	45	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	200 k	70	200 k	80	200 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	20	10 k	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

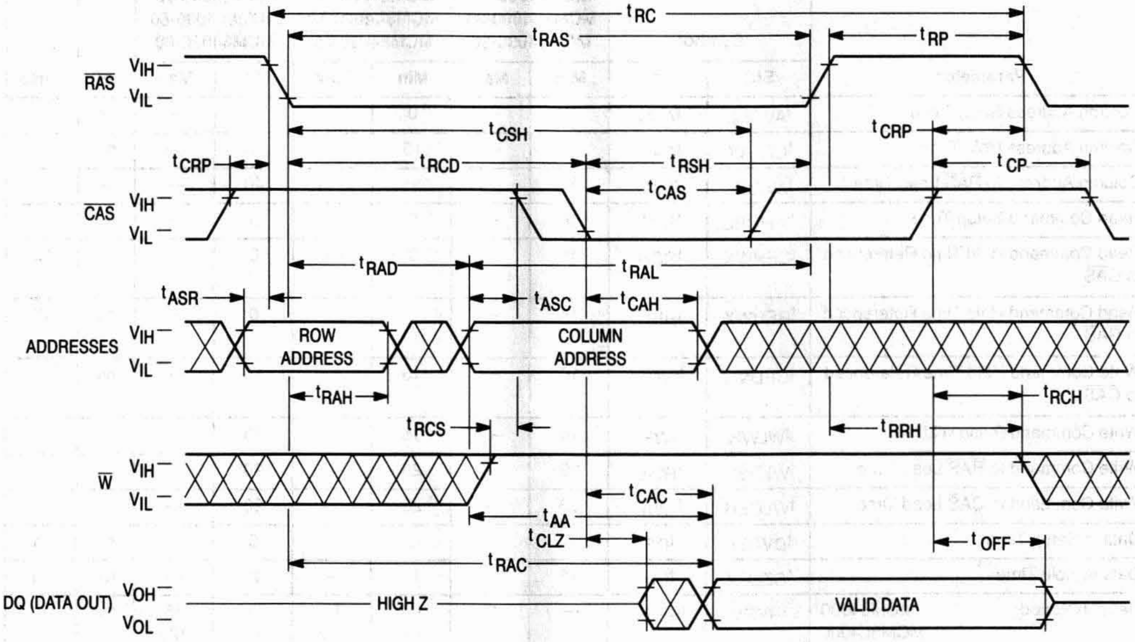
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM84000-60 MCM8L4000-60 MCM84030-60		MCM84000-70 MCM8L4000-70 MCM84030-70		MCM84000-80 MCM8L4000-80 MCM84030-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	14
Refresh Period MCM84000 MCM8L4000	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Time	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	

NOTES:

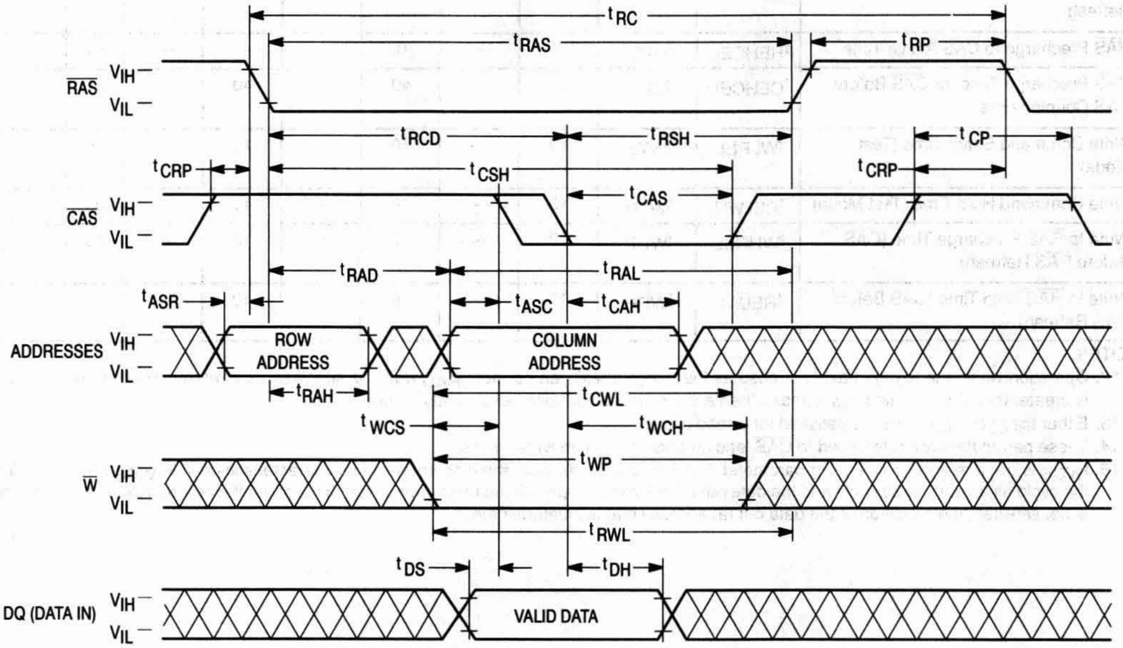
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.

READ CYCLE



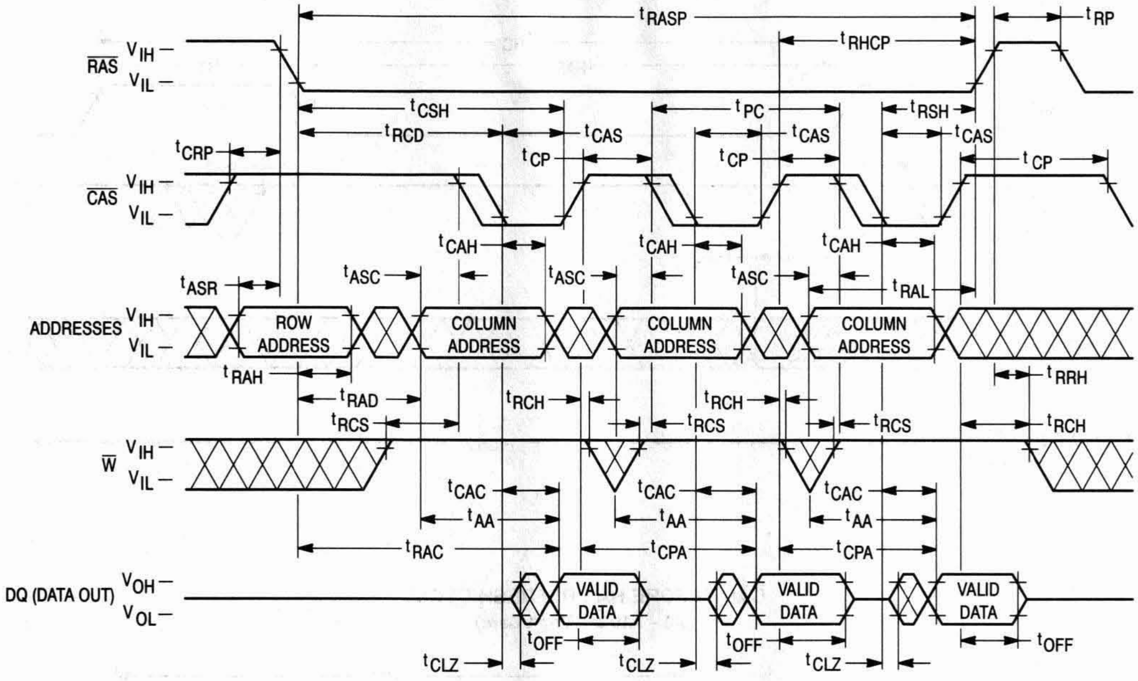
tRC
tRAS
tRP
RAS
VIH —
VIL —
tCSH
tCRP
tCRP
tRCD
tRSH
tCP
tCAS
CAS
VIH —
VIL —
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH —
VIL —
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W
VIH —
VIL —
tCAC
tAA
tCLZ
tOFF
tRAC
DQ (DATA OUT)
VOH —
VOL —
HIGH Z
VALID DATA

EARLY WRITE CYCLE

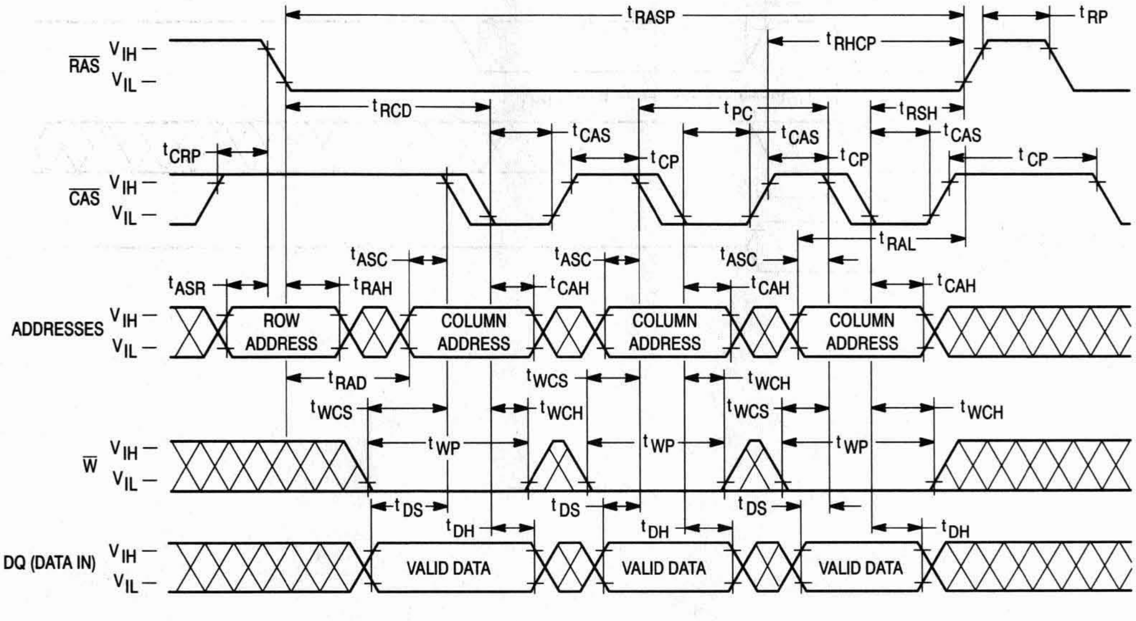


tRC
tRAS
tRP
RAS
VIH —
VIL —
tRCD
tRSH
tCP
tCRP
tCSH
tCRP
tCAS
CAS
VIH —
VIL —
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH —
VIL —
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWP
W
VIH —
VIL —
tRWL
tDS
tDH
DQ (DATA IN)
VIH —
VIL —
VALID DATA

FAST PAGE MODE READ CYCLE

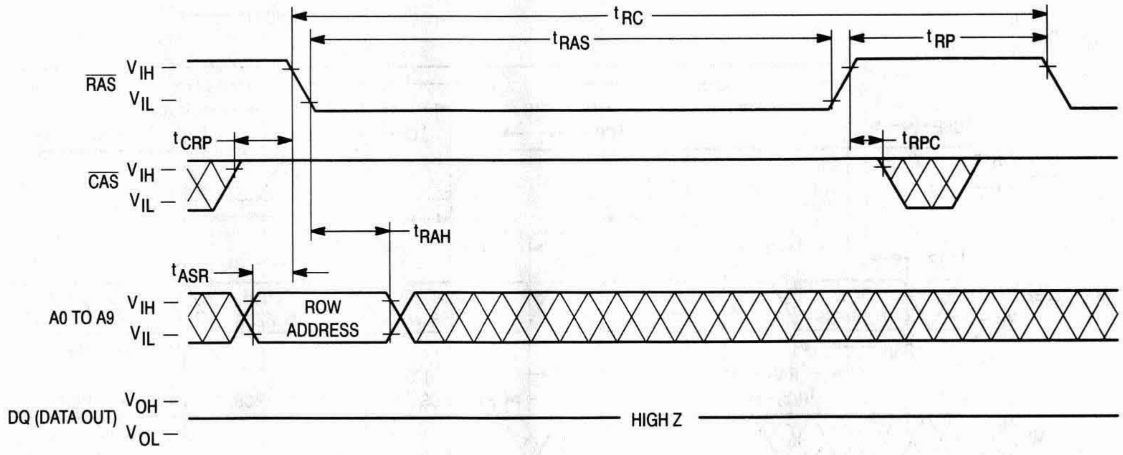

tRASP
tRP
tRHCP
RAS
VIH –
VIL –
tCSH
tPC
tRSH
tRCD
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCP
CAS
VIH –
VIL –
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
tRAL
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAH
tRRH
tRAD
tRCH
tRCH
tRCS
tRCS
tRCS
tRCH
W
VIH –
VIL –
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
DQ (DATA OUT)
VOH –
VOL –
VALID DATA
VALID DATA
VALID DATA
tOFF
tOFF
tOFF
tCLZ
tCLZ
tCLZ

FAST PAGE MODE EARLY WRITE CYCLE


tRASP
tRP
tRHCP
RAS
VIH –
VIL –
tRCD
tPC
tRSH
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCP
CAS
VIH –
VIL –
tRAL
tASC
tASC
tASC
tASR
tRAH
tCAH
tCAH
tCAH
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tWCS
tWCH
tWCS
tWCH
tWCS
tWCH
tWP
tWP
tWP
W
VIH –
VIL –
tDS
tDS
tDS
tDH
tDH
tDH
DQ (DATA IN)
VIH –
VIL –
VALID DATA
VALID DATA
VALID DATA

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

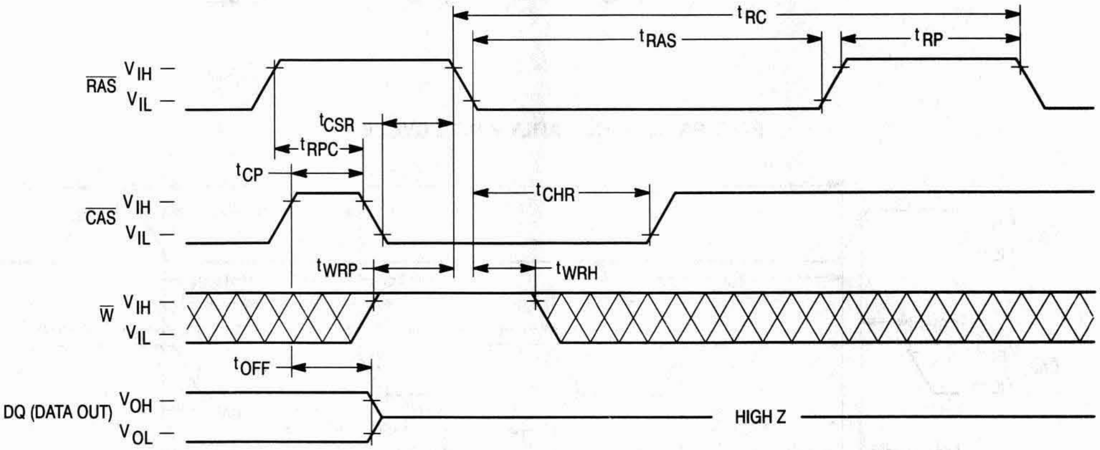
($\overline{\text{W}}$ and A10 are Don't Care)



t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
A0 TO A9
V_{IH}
V_{IL}
ROW ADDRESS
DQ (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

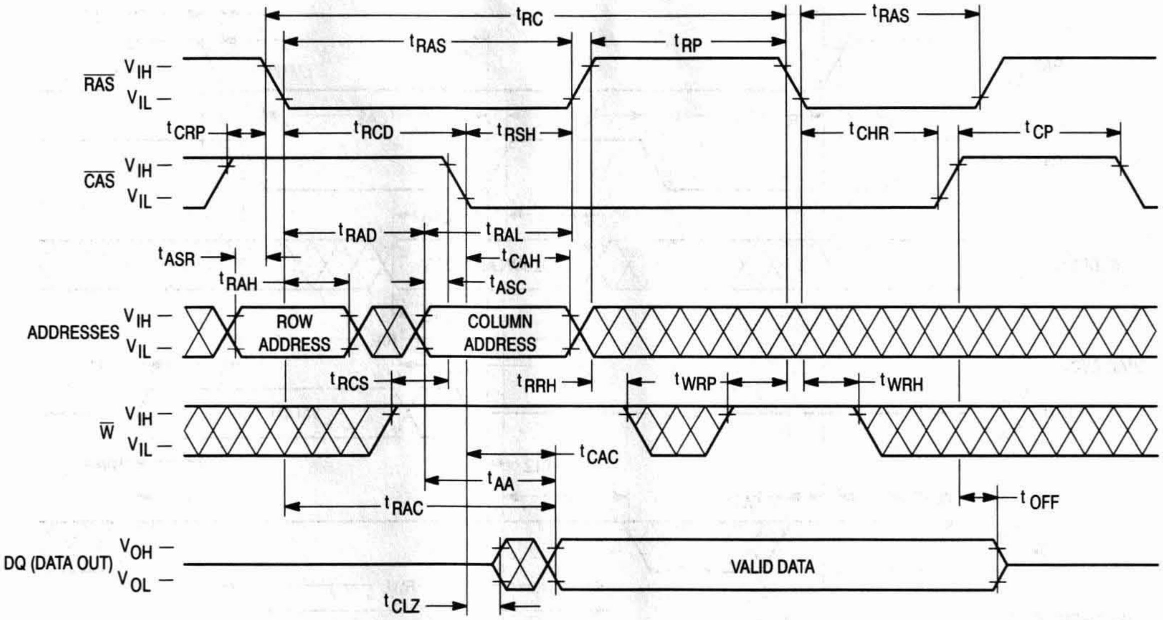
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

(A0 – A10 are Don't Care)



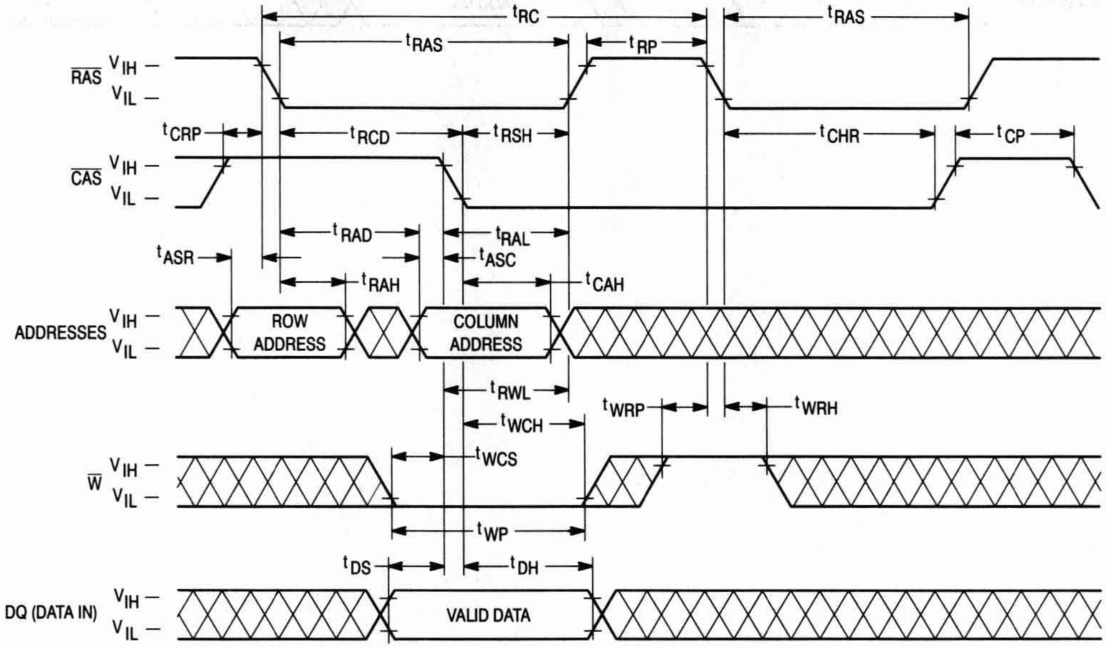
t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CSR}
t_{RPC}
t_{CP}
t_{CHR}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{WRP}
t_{WRH}
$\overline{\text{W}}$
V_{IH}
V_{IL}
t_{OFF}
DQ (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

HIDDEN REFRESH CYCLE (READ)



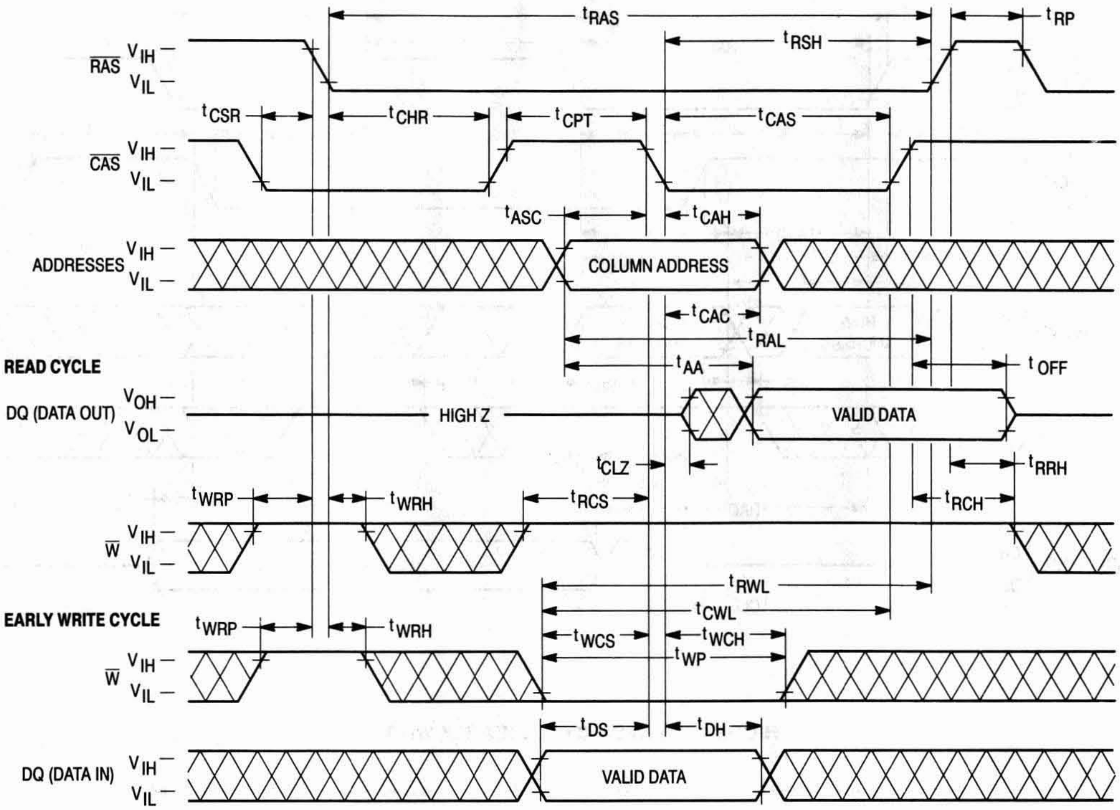
tRC
tRAS
tRAS
tRP
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCP
CAS
VIH
VIL
tRAD
tRAL
tCAH
tASR
tRAH
tASC
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRCS
tRRH
tWRP
tWRH
W
VIH
VIL
tCAC
tAA
tRAC
tOFF
DQ (DATA OUT)
VOH
VOL
VALID DATA
tCLZ

HIDDEN REFRESH CYCLE (EARLY WRITE)



tRC
tRAS
tRAS
tRP
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCP
CAS
VIH
VIL
tRAD
tRAL
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRWL
tWRP
tWRH
tWCH
tWCS
W
VIH
VIL
tWP
tDS
tDH
DQ (DATA IN)
VIH
VIL
VALID DATA

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE


tRAS
tRP
tRSH
RAS VIH VIL
tCSR
tCHR
tCPT
tCAS
CAS VIH VIL
tASC
tCAH
ADDRESSES VIH VIL
COLUMN ADDRESS
tCAC
tRAL
READ CYCLE
tAA
tOFF
DQ (DATA OUT) VOH VOL
HIGH Z
VALID DATA
tCLZ
tRRH
tWRP
tWRH
tRCS
tRCH
W VIH VIL
tRWL
tCWL
EARLY WRITE CYCLE
tWRP
tWRH
tWCS
tWCH
tWP
W VIH VIL
tDS
tDH
DQ (DATA IN) VIH VIL
VALID DATA

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 11-bit address fields. A total of twenty-two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 word locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the module: **$\overline{RAS}$ only refresh cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle,** and **page mode**.

READ CYCLE

The DRAM may be read with either a "normal" random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window; however, $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with either an early write or page mode early write cycle. Early write mode is discussed here, while page mode write operation is covered elsewhere.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early write mode is distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (DQ) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time (t_{RAC}). Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum of t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM84000 require refresh every 16 milliseconds, while refresh time for the MCM8L4000 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM84000, and 124.8 microseconds for the MCM8L4000. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM84000 and 128 milliseconds on the MCM8L4000.

A normal read or write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle.

The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{\text{RAS}}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode cycle) as in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read cycle.** Repeat this operation 1024 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, write cycle.** Repeat this operation 1024 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

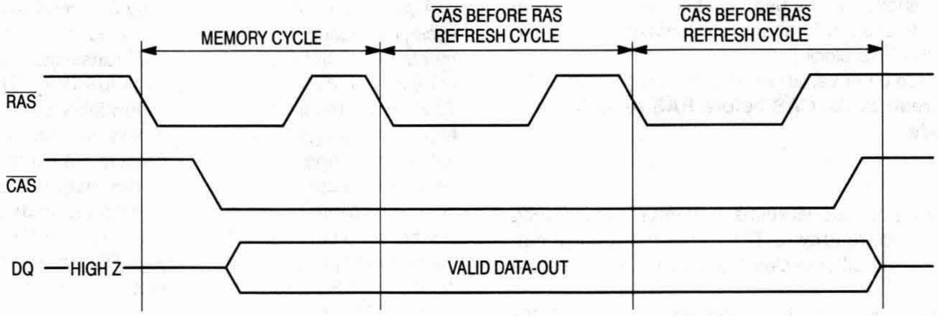

MEMORY CYCLE
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
DQ
HIGH Z
VALID DATA-OUT

Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION

(Order by Full Part Number)

MCM **84000 / 8L4000 / 84030** **X** **XX**

Motorola Memory Prefix — MCM
Part Number — 84000, 8L4000, 84030
Package (AS = SIMM, L = SIP, LH = Low Height SIP (84030 Only)) — X
Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers —

MCM84000AS60	MCM84000L60	MCM84030LH60
MCM84000AS70	MCM84000L70	MCM84030LH70
MCM84000AS80	MCM84000L80	MCM84030LH80
MCM8L4000AS60	MCM8L4000L60	MCM8L4030LH60
MCM8L4000AS70	MCM8L4000L70	MCM8L4030LH70
MCM8L4000AS80	MCM8L4000L80	MCM8L4030LH80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM81600
MCM8L1600

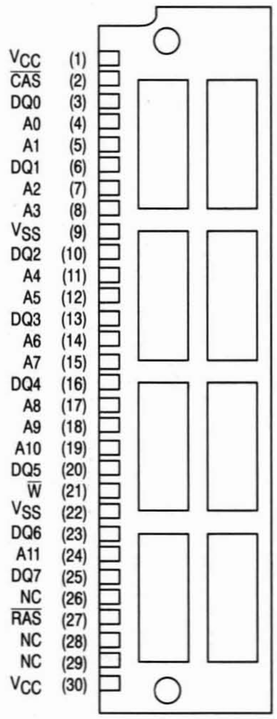
Product Preview

16M x 8 Bit Dynamic Random Access Memory Module

The MCM81600 is a dynamic random access memory (DRAM) module organized as 16,777,216 x 8 bits. The module is a 30-lead single-in-line memory module (SIMM) consisting of eight MCM517400 DRAMs housed in 400 mil J-lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM517400 is a CMOS high-speed dynamic random access memory organized as 16,777,216 one-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh:
  MCM81600 = 32 ms
- Consists of Eight 16M x 1 DRAMs and Eight 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM81600-60 = 60 ns (Max)
  MCM81600-70 = 70 ns (Max)
  MCM81600-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM81600-60 = 5.28 W (Max)
  MCM81600-70 = 4.4 W (Max)
  MCM81600-80 = 3.74 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 88 mW (Max)
  CMOS Levels = 44 mW (Max)

TOP VIEW

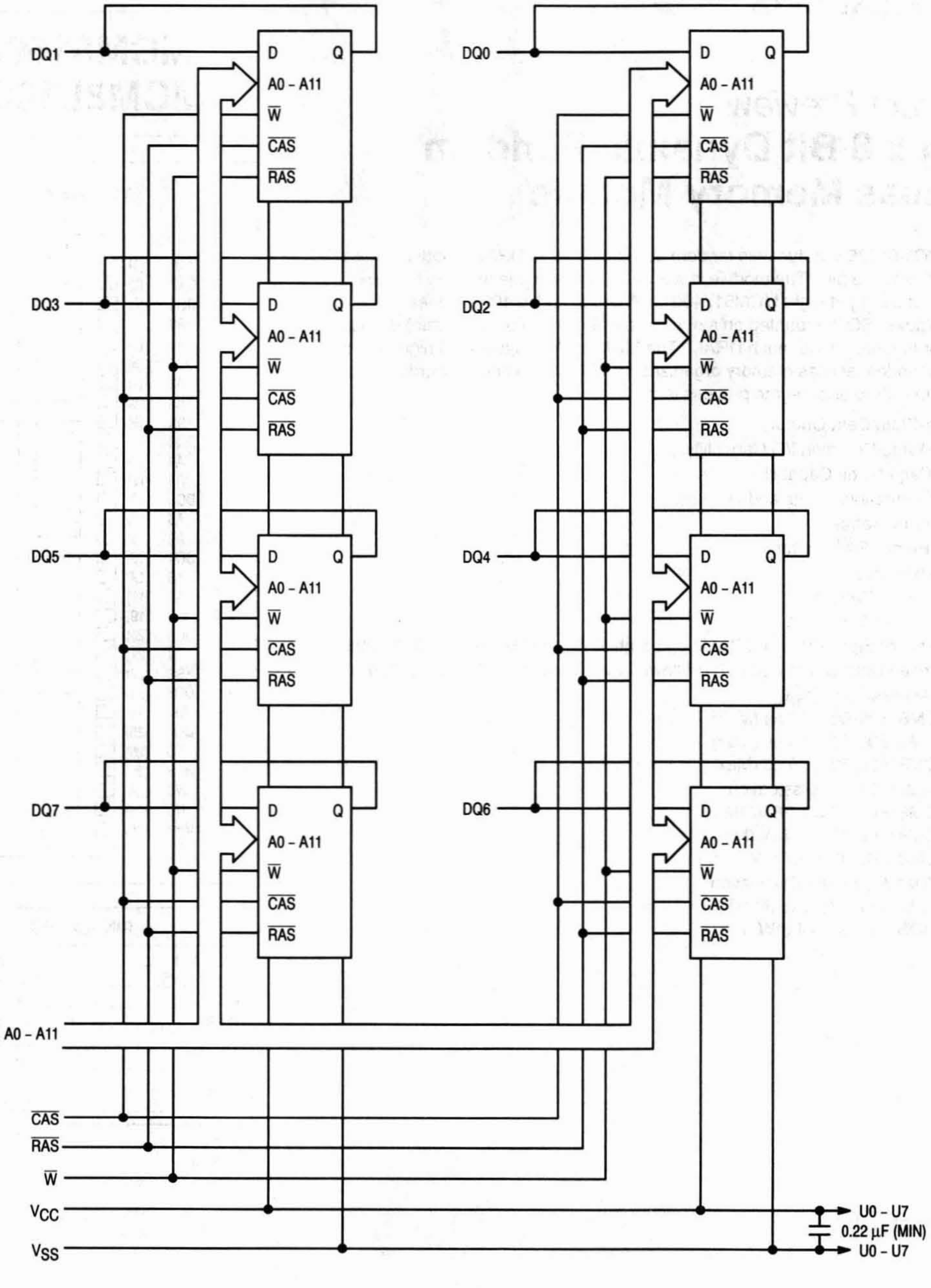

V_{CC} (1)
$\overline{\text{CAS}}$ (2)
DQ0 (3)
A0 (4)
A1 (5)
DQ1 (6)
A2 (7)
A3 (8)
V_{SS} (9)
DQ2 (10)
A4 (11)
A5 (12)
DQ3 (13)
A6 (14)
A7 (15)
DQ4 (16)
A8 (17)
A9 (18)
A10 (19)
DQ5 (20)
$\overline{\text{W}}$ (21)
V_{SS} (22)
DQ6 (23)
A11 (24)
DQ7 (25)
NC (26)
$\overline{\text{RAS}}$ (27)
NC (28)
NC (29)
V_{CC} (30)

PIN NAMES

A0 – A11	Address Inputs
DQ0 – DQ7	Data Input/Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

16M x 8 BLOCK DIAGRAM


DQ1
DQ0
DQ3
DQ2
DQ5
DQ4
DQ7
DQ6
D
Q
A0 – A11
W
CAS
RAS
A0 – A11
CAS
RAS
W
VCC
VSS
U0 – U7
0.22 µF (MIN)
U0 – U7

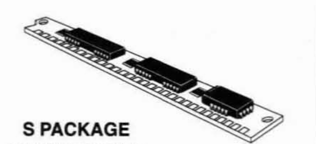
NOTE: For mechanical data, please see Chapter 10.

MCM94256

256K x 9 Bit Dynamic Random Access Memory Module

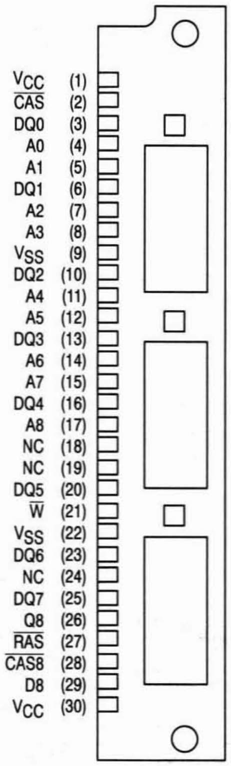
The MCM94256 is a 2.25M dynamic random access memory (DRAM) module organized as 262,144 x 9 bits. The module is a 30-lead single-in-line memory module (SIMM) consisting of two MCM514256A DRAMs housed in 20/26 J-lead small outline packages (SOJ) and one CMOS 256K x 1 DRAM housed in an 18-lead PLCC package, mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted adjacent to each DRAM. The MCM514256A is a 1.0µ CMOS high-speed dynamic random access memory organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM94256 = 8 ms (Max)
- Consists of Two 256K x 4 DRAMs, One 256K x 1 DRAM, and Three 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM94256-70 = 70 ns (Max)
  MCM94256-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM94256-70 = 1.32 W (Max)
  MCM94256-80 = 1.16 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 33 mW (Max)
  CMOS Levels = 16.5 mW (Max)
- $\overline{\text{CAS}}$ Control for Eight Common I/O Lines
- $\overline{\text{CAS}}$ Control for Separate I/O Pair



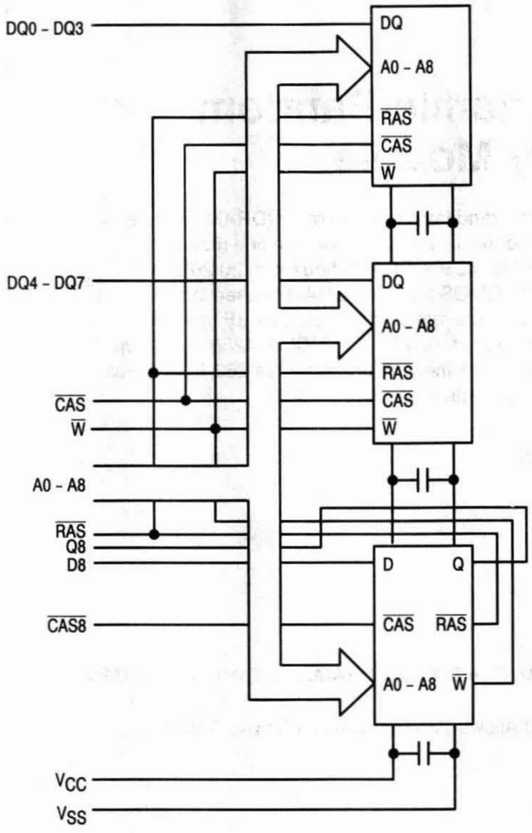
S PACKAGE
SIMM MODULE
CASE 839A-01

TOP VIEW


V_{CC} (1)
$\overline{\text{CAS}}$ (2)
DQ0 (3)
A0 (4)
A1 (5)
DQ1 (6)
A2 (7)
A3 (8)
V_{SS} (9)
DQ2 (10)
A4 (11)
A5 (12)
DQ3 (13)
A6 (14)
A7 (15)
DQ4 (16)
A8 (17)
NC (18)
NC (19)
DQ5 (20)
$\overline{\text{W}}$ (21)
V_{SS} (22)
DQ6 (23)
NC (24)
DQ7 (25)
Q8 (26)
$\overline{\text{RAS}}$ (27)
$\overline{\text{CAS8}}$ (28)
D8 (29)
V_{CC} (30)

PIN NAMES	
A0 – A8	Address Inputs
DQ0 – DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{CAS8}}$	Column Address Strobe
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



DQ0 - DQ3
DQ4 - DQ7
$\overline{CAS}$
$\overline{W}$
A0 - A8
$\overline{RAS}$
Q8
D8
$\overline{CAS8}$
V_{CC}
V_{SS}
DQ
A0 - A8
$\overline{RAS}$
$\overline{CAS}$
$\overline{W}$
D
Q
$\overline{CAS}$
$\overline{RAS}$
$\overline{W}$

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	1.8	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM94256-70, t_{RC} = 130 ns MCM94256-80, t_{RC} = 150 ns	I_{CC1}	— —	225 195	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	6	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles	I_{CC3}			mA	1
MCM94256-70, t_{RC} = 130 ns MCM94256-80, t_{RC} = 150 ns		— —	225 195		
V_{CC} Power Supply Current During Fast Page Mode Cycle	I_{CC4}			mA	1, 2
MCM94256-70, t_{PC} = 40 ns MCM94256-80, t_{PC} = 45 ns		— —	160 135		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	3	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	1
MCM94256-70, t_{RC} = 130 ns MCM94256-80, t_{RC} = 150 ns		— —	225 195		
Input Leakage Current ($V_{SS} \leq V_{in} \leq V_{CC}$)	$I_{lkg(I)}$	– 30	30	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \leq V_{out} \leq V_{CC}$)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A8, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$	C_{in}	30	pF
	D8, $\overline{CAS8}$		17	
Input/Output Capacitance	DQ0 – DQ7	$C_{I/O}$	17	pF
Output Capacitance	Q8	C_{out}	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM94256-70		MCM94256-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELAX}	t_{AR}	55	—	60	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

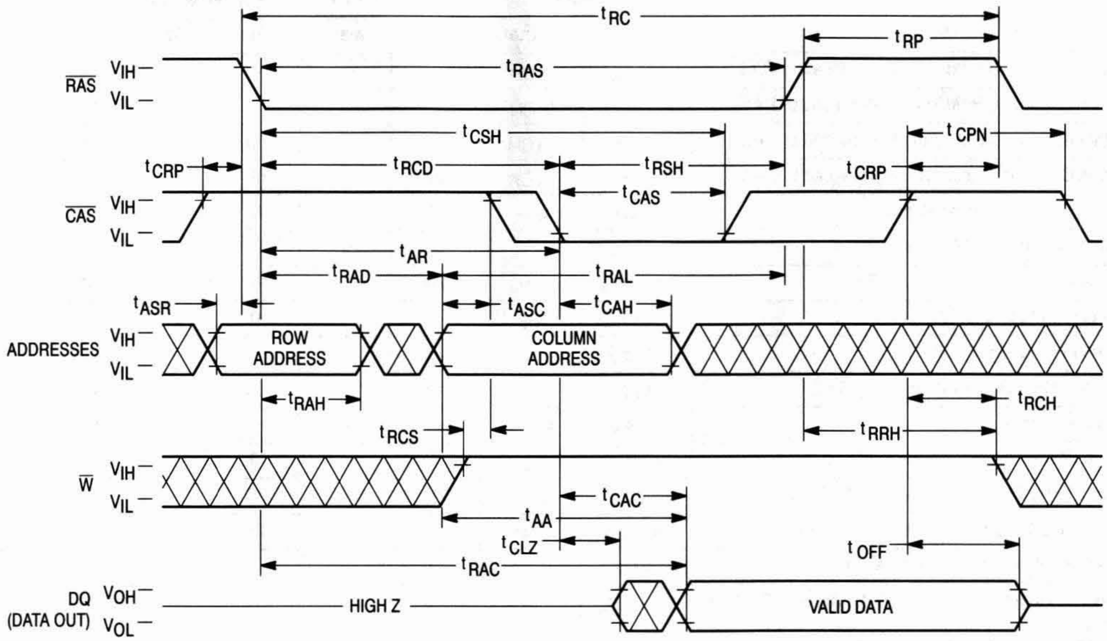
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM94256-70		MCM94256-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	15	—	15	—	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELWH}	t_{WCR}	55	—	60	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	55	—	60	—	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	—	8	—	8	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	ns	
Fast Page Mode Cycle Time	$t_{CELCELP}$	t_{PCP}	45	—	45	—	ns	16
Output Buffer and Turn-Off Delay	t_{CEHQZP}	t_{OFFP}	0	25	0	25	ns	10, 16
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQVP}	t_{CPAP}	—	45	—	45	ns	10, 16

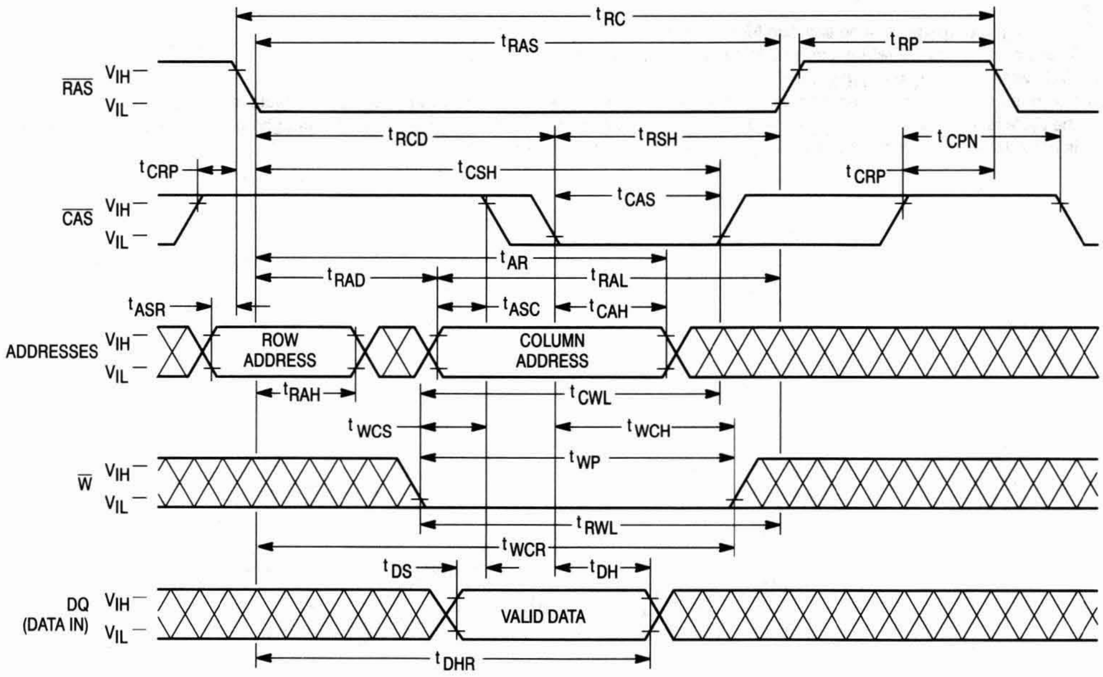
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

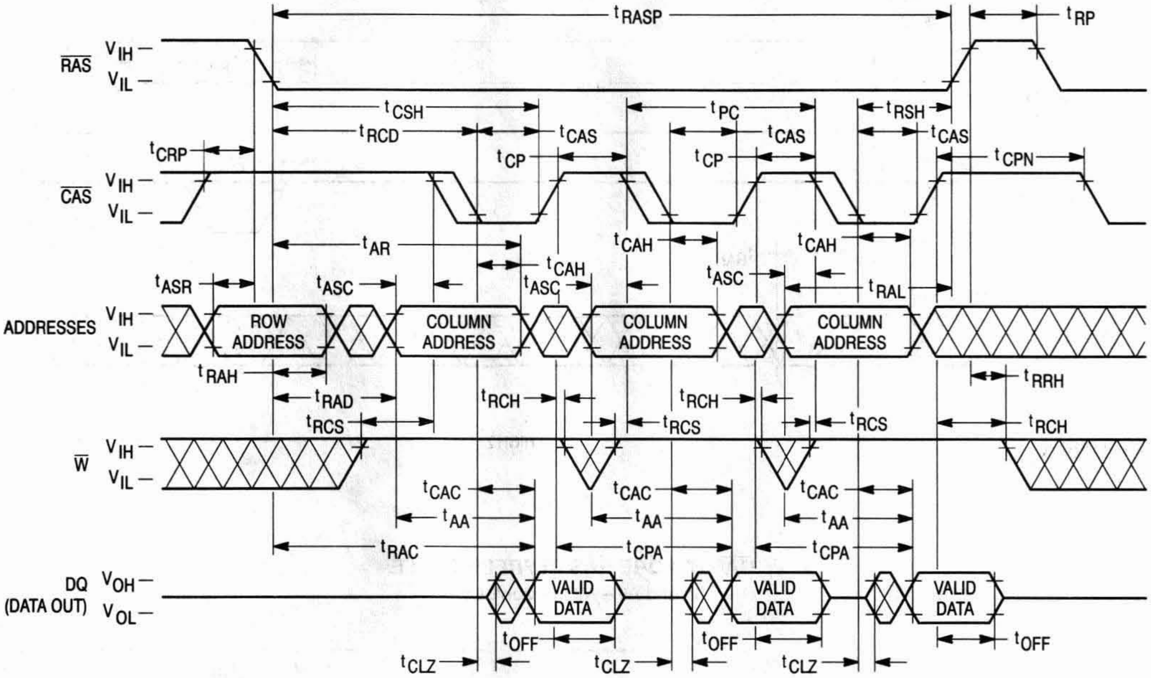
READ CYCLE


t RC
t RP
t RAS
RAS
VIH
VIL
t CSH
t CPN
t CRP
t RCD
t RSH
t CRP
CAS
VIH
VIL
t CAS
t AR
t RAD
t RAL
t ASR
t ASC
t CAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
t RAH
t RCH
t RCS
t RRH
W
VIH
VIL
t CAC
t AA
t CLZ
t OFF
t RAC
DQ (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA

EARLY WRITE CYCLE

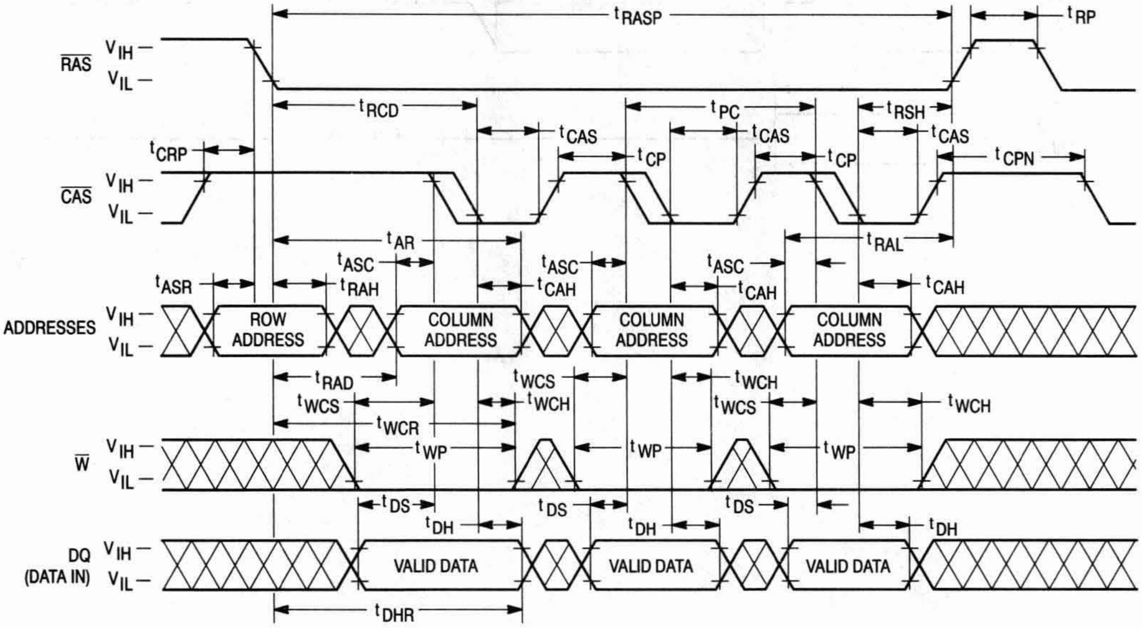

t RC
t RAS
t RP
RAS
VIH
VIL
t RCD
t RSH
t CPN
t CRP
t CSH
t CRP
CAS
VIH
VIL
t CAS
t AR
t RAD
t RAL
t ASR
t ASC
t CAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
t RAH
t CWL
t WCS
t WCH
t WP
W
VIH
VIL
t RWL
t WCR
t DS
t DH
DQ (DATA IN)
VIH
VIL
VALID DATA
t DHR

FAST PAGE MODE READ CYCLE



t_{RASP}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{PC}
t_{RSH}
t_{RCD}
t_{CAS}
t_{CAS}
t_{CAS}
t_{CRP}
t_{CP}
t_{CP}
t_{CPN}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{AR}
t_{CAH}
t_{CAH}
t_{CAH}
t_{ASR}
t_{ASC}
t_{ASC}
t_{ASC}
t_{RAL}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
t_{RAH}
t_{RRH}
t_{RAD}
t_{RCH}
t_{RCH}
t_{RCS}
t_{RCS}
t_{RCS}
t_{RCH}
$\overline{W}$
V_{IH}
V_{IL}
t_{CAC}
t_{CAC}
t_{CAC}
t_{AA}
t_{AA}
t_{AA}
t_{RAC}
t_{CPA}
t_{CPA}
DQ (DATA OUT)
V_{OH}
V_{OL}
VALID DATA
VALID DATA
VALID DATA
t_{OFF}
t_{OFF}
t_{OFF}
t_{CLZ}
t_{CLZ}
t_{CLZ}

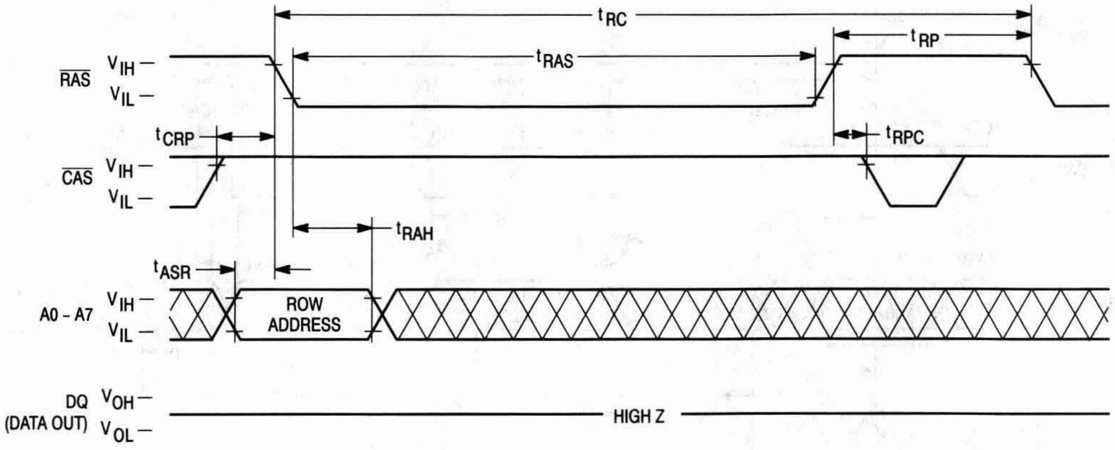
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



t_{RASP}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RCD}
t_{PC}
t_{RSH}
t_{CAS}
t_{CAS}
t_{CAS}
t_{CRP}
t_{CP}
t_{CP}
t_{CPN}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{AR}
t_{RAL}
t_{ASC}
t_{ASC}
t_{ASC}
t_{ASR}
t_{RAH}
t_{CAH}
t_{CAH}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
t_{RAD}
t_{WCS}
t_{WCH}
t_{WCS}
t_{WCH}
t_{WCS}
t_{WCH}
t_{WCR}
$\overline{W}$
V_{IH}
V_{IL}
t_{WP}
t_{WP}
t_{WP}
t_{DS}
t_{DS}
t_{DS}
t_{DH}
t_{DH}
t_{DH}
DQ (DATA IN)
V_{IH}
V_{IL}
VALID DATA
VALID DATA
VALID DATA
t_{DHR}

$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

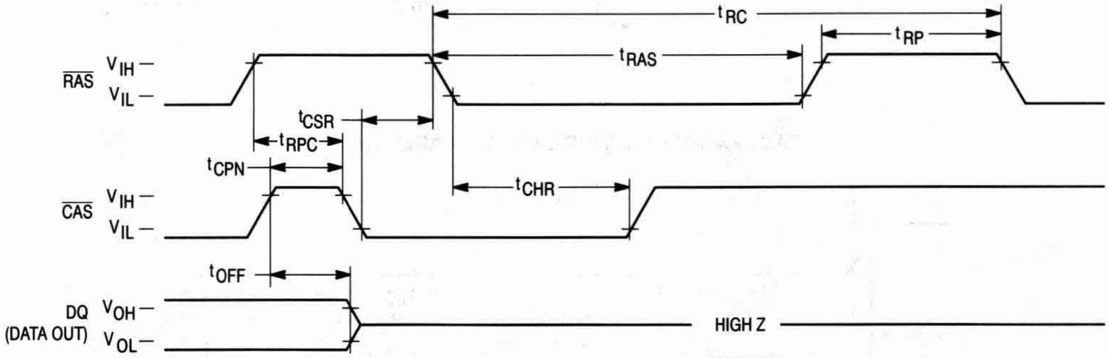
($\overline{\text{W}}$ and A8 are Don't Care)



tRC
tRP
tRAS
RAS
VIH
VIL
tCRP
tRPC
CAS
VIH
VIL
tRAH
tASR
A0 - A7
VIH
VIL
ROW ADDRESS
DQ
(DATA OUT)
VOH
VOL
HIGH Z

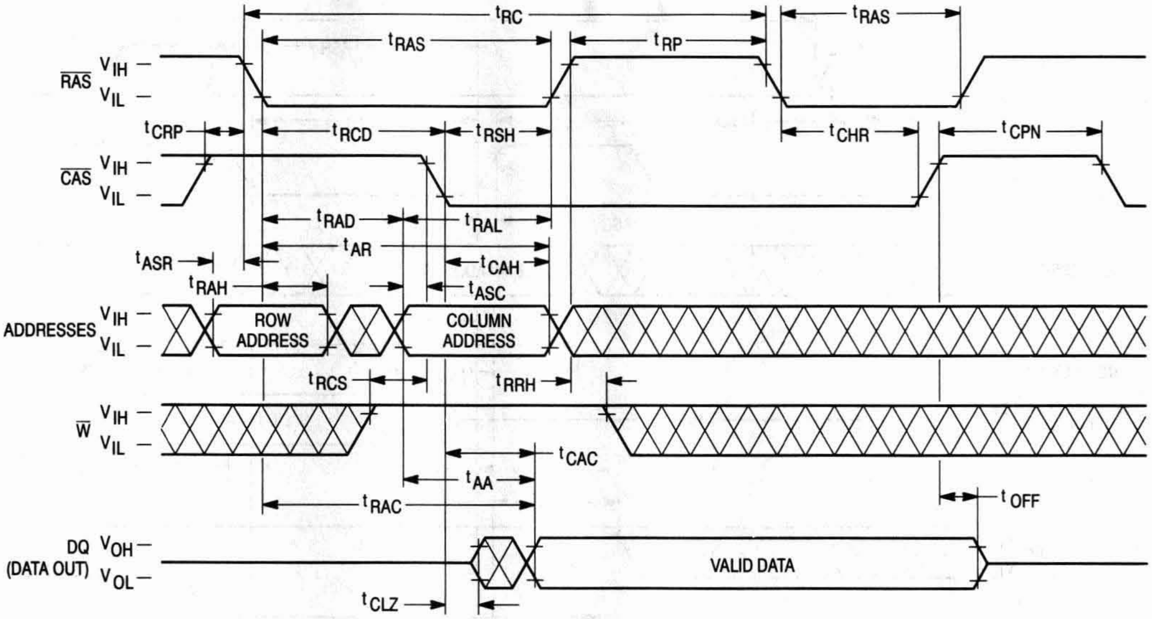
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{W}}$ and A0 – A8 are Don't Care)



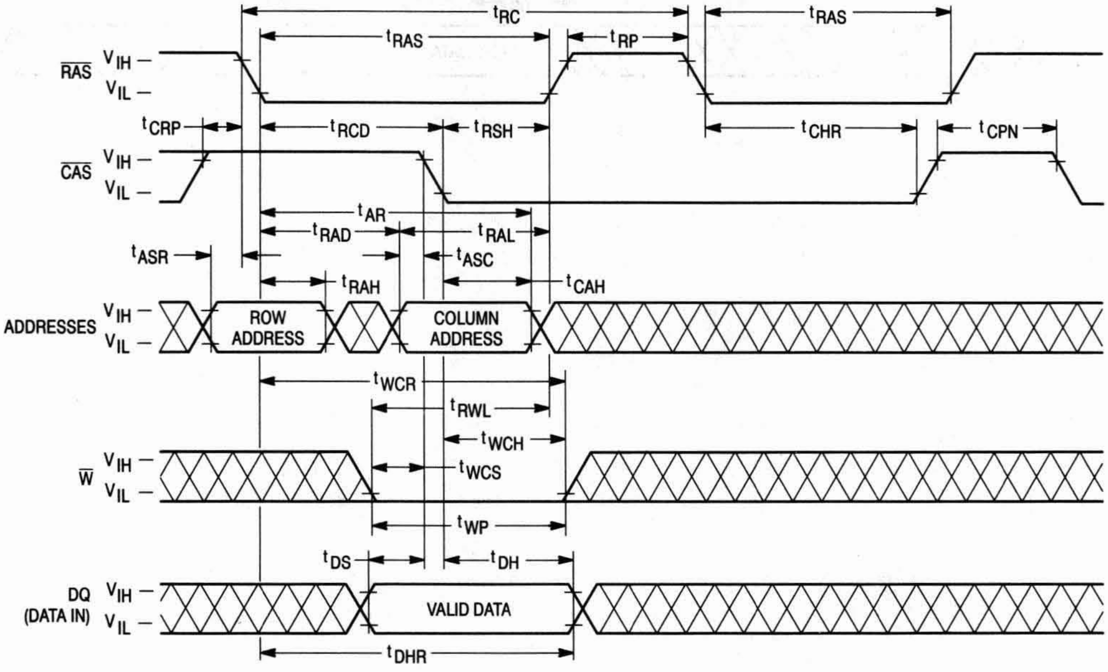
tRC
tRP
tRAS
RAS
VIH
VIL
tCSR
tRPC
tCPN
tCHR
CAS
VIH
VIL
tOFF
DQ
(DATA OUT)
VOH
VOL
HIGH Z

HIDDEN REFRESH CYCLE (READ)



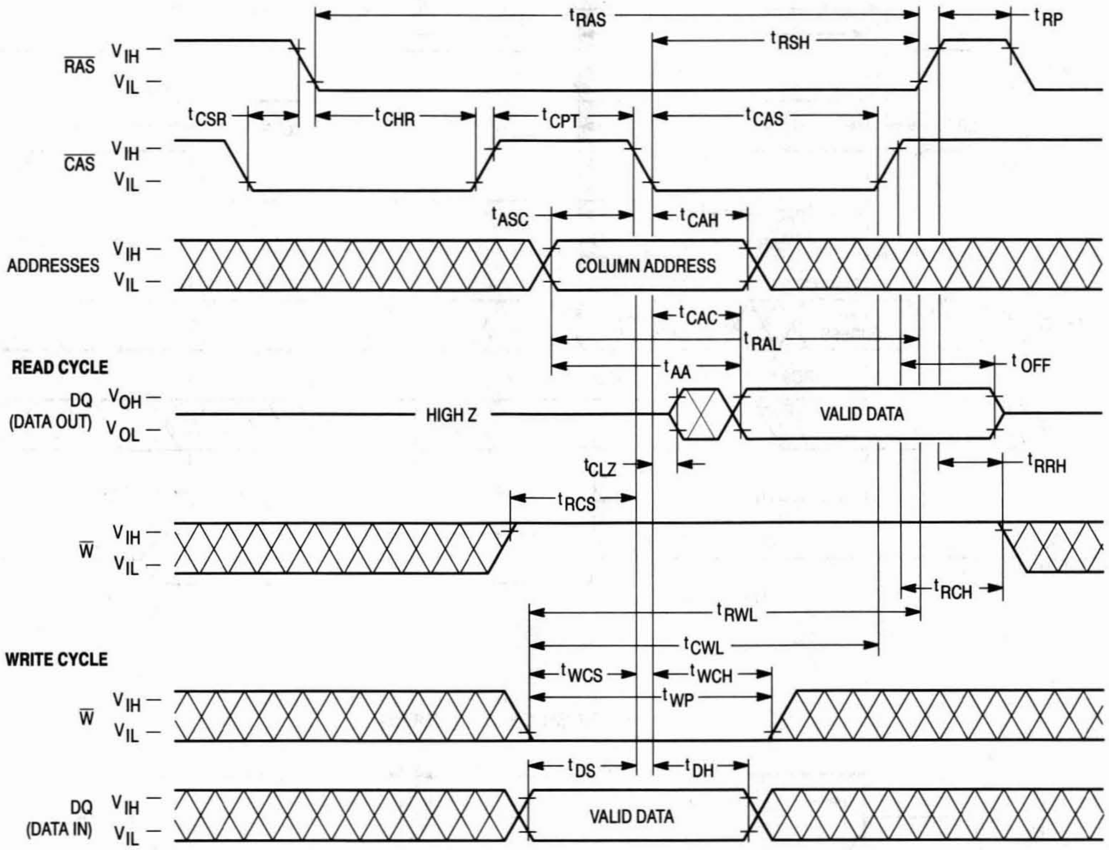
t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$ V_{IH} — V_{IL} —
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CPN}
$\overline{CAS}$ V_{IH} — V_{IL} —
t_{RAD}
t_{RAL}
t_{AR}
t_{ASR}
t_{CAH}
t_{RAH}
t_{ASC}
ADDRESSES V_{IH} — V_{IL} —
ROW ADDRESS
COLUMN ADDRESS
t_{RCS}
t_{RRH}
$\overline{W}$ V_{IH} — V_{IL} —
t_{CAC}
t_{AA}
t_{RAC}
t_{OFF}
DQ (DATA OUT) V_{OH} — V_{OL} —
VALID DATA
t_{CLZ}

HIDDEN REFRESH CYCLE (WRITE)



t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$ V_{IH} — V_{IL} —
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CPN}
$\overline{CAS}$ V_{IH} — V_{IL} —
t_{AR}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES V_{IH} — V_{IL} —
ROW ADDRESS
COLUMN ADDRESS
t_{WCR}
t_{RWL}
t_{WCH}
t_{WCS}
$\overline{W}$ V_{IH} — V_{IL} —
t_{WP}
t_{DS}
t_{DH}
DQ (DATA IN) V_{IH} — V_{IL} —
VALID DATA
t_{DHR}

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



tRAS
tRP
tRSH
RAS
VIH
VIL
tCSR
tCHR
tCPT
tCAS
CAS
VIH
VIL
tASC
tCAH
ADDRESSES
VIH
VIL
COLUMN ADDRESS
tCAC
tRAL
tOFF
tAA
READ CYCLE
DQ
(DATA OUT)
VOH
VOL
HIGH Z
VALID DATA
tCLZ
tRRH
tRCS
W
VIH
VIL
tRCH
tRWL
WRITE CYCLE
tCWL
tWCS
tWCH
tWP
W
VIH
VIL
tDS
tDH
DQ
(DATA IN)
VIH
VIL
VALID DATA

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe ($\overline{RAS}$) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 word locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gate feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are two other variations in addressing the module: **$\overline{RAS}$-only refresh cycle** and **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either a normal random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. $\overline{CAS}$ controls read access time; $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} after inactive transition.

WRITE CYCLE

The DRAM may be written with either an early write or page mode early write cycle. The early write mode is discussed here, while the page mode write operation is covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early write mode is distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data In (DQ) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 512 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time (t_{RAC}). Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically refreshed (recharged) to maintain the correct bit state. Bits in the MCM94256 require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM94256. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM94256A.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure that all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1).

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 CAS before RAS** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **CAS before RAS refresh counter test, read cycle**. Repeat this operation 512 times.
3. Select a column address, and write "1" into the cell by performing the **CAS before RAS refresh counter test, write cycle**. Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

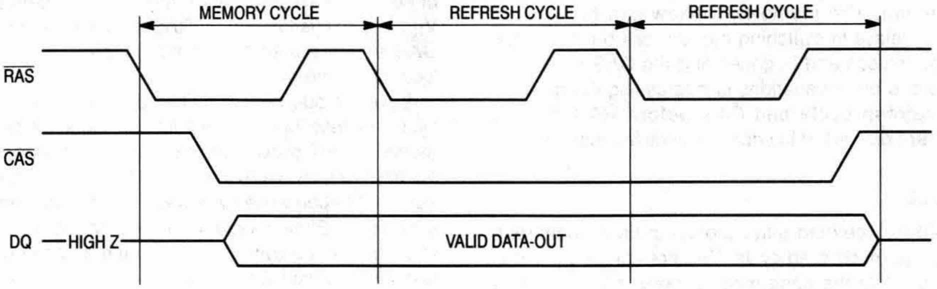
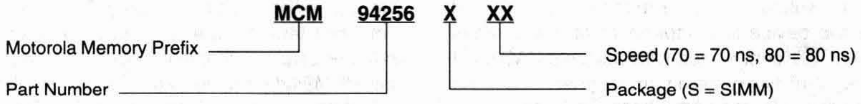


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM94256S70
MCM94256S80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

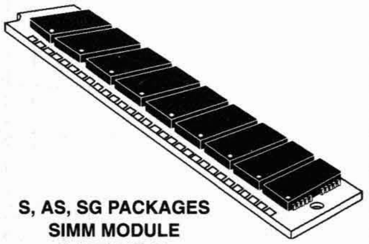
MCM91000
MCM9L1000

1M x 9 Bit Dynamic Random Access Memory Module

The MCM91000 and MCM9L1000 are 9M dynamic random access memory (DRAM) modules organized as 1,048,576 x 9 bits. The modules are 30-lead single-in-line memory modules (SIMM) or 30-pin single-in-line packages (SIP) consisting of nine MCM511000A DRAMs housed in a 20/26 J-lead small outline package (SOJ) and mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM511000A is a 1.0µ CMOS high-speed dynamic random access memory organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh: MCM91000 = 8 ms (Max)
  MCM9L1000 = 64 ms (Max)
- Consists of Nine 1M DRAMs and Nine 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM91000-70 = 70 ns (Max)
  MCM91000-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM91000-70 = 4.0 W (Max)
  MCM91000-80 = 3.5 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 99 mW (Max)
  CMOS Levels (MCM91000) = 50 mW (Max)
  (MCM9L1000) = 10 mW (Max)
- $\overline{\text{CAS}}$ Control for Eight Common I/O Lines
- $\overline{\text{CAS}}$ Control for Separate I/O Pair
- Available in Edge Connector (MCM91000AS) or Four-Layer PCB Edge Connector (MCM91000S)
- Available in Gold Pad Edge Connector (MCM91000SG)
- Available in Pin Connector (MCM91000L) or Double-Sided Low Height Pin Connector (MCM91000LH)
- For Applications Requiring $\overline{\text{W}}$ to be Don't Care during $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycles
- 1M x 9 Modules are also Available in 3-Chip Versions (See Data Sheet for MCM91430)

PIN NAMES	
A0 – A9	Address Inputs
DQ0 – DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{CAS8}}$	Column Address Strobe
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

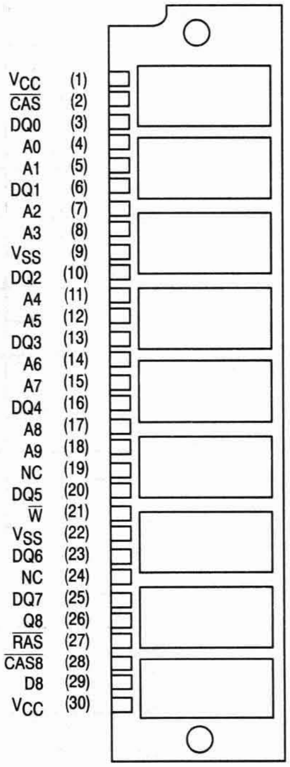


S, AS, SG PACKAGES
SIMM MODULE
CASE 839-01

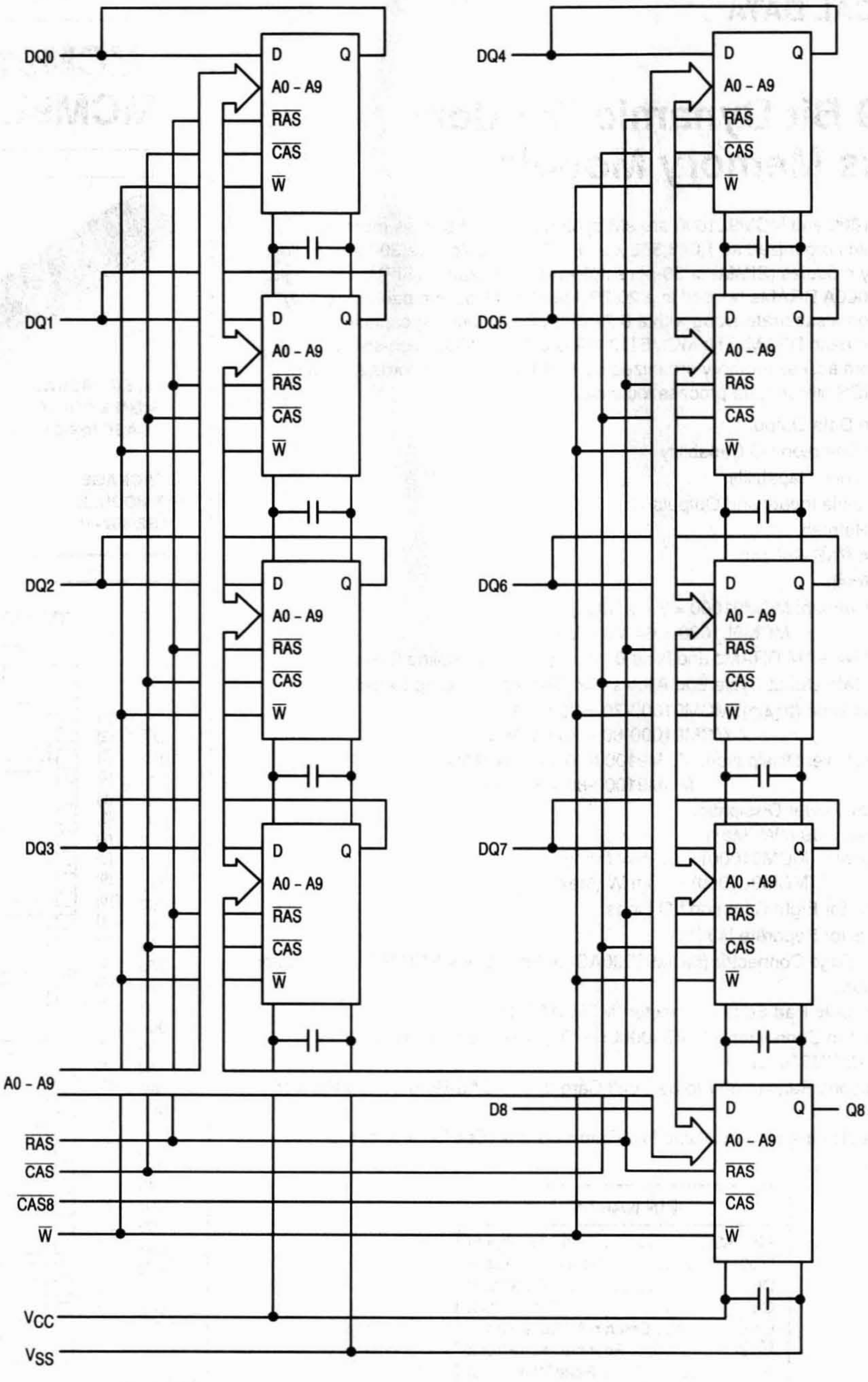
L PACKAGE
SIP MODULE
CASE 852-01

LH PACKAGE
SIP MODULE
CASE 852A-02

TOP VIEW



FUNCTIONAL BLOCK DIAGRAM



DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
D8
Q8
D
Q
A0 – A9
RAS
CAS
W
A0 – A9
RAS
CAS
CAS8
W
VCC
VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	5.4	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM91000-70, t_{RC} = 130 ns MCM91000-80, t_{RC} = 150 ns	I_{CC1}	— —	720 630	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	18	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles MCM91000-70, t_{RC} = 130 ns MCM91000-80, t_{RC} = 150 ns	I_{CC3}	 — —	 720 630	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM91000-70, t_{PC} = 40 ns MCM91000-80, t_{PC} = 45 ns	I_{CC4}	 — —	 540 450	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM91000 MCM9L1000	I_{CC5}	— —	9 1.8	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM91000-70, t_{RC} = 130 ns MCM91000-80, t_{RC} = 150 ns	I_{CC6}	 — —	 720 630	mA	1
V_{CC} Power Supply Current, Battery Backup Mode — MCM9L1000 and MCM9L1000 Only (t_{RAC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0 – A9, $\overline{W}$, DQ = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	—	2.7	mA	
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 90	90	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTE: 1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$	C_{in}	60	pF
	D8, $\overline{CAS8}$		7	pF
Input/Output Capacitance	DQ0 – DQ7	$C_{I/O}$	15	pF
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q8	C_{out}	10	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM91000-70 MCM9L1000-70		MCM91000-80 MCM9L1000-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
Access Time from RAS	t_{RELQV}	t_{RAC}	—	70	—	80	ns	6, 7
Access Time from CAS	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	6, 9
Access Time from Precharge CAS	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
CAS to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
RAS Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	ns	
RAS Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
RAS Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	ns	
RAS Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
CAS Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
CAS Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	ns	
RAS to CAS Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	ns	11
RAS to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	ns	12
CAS to RAS Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
CAS Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address Hold Time Referenced to RAS	t_{RELAX}	t_{AR}	55	—	60	—	ns	
Column Address to RAS Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	

NOTES:

(continued)

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

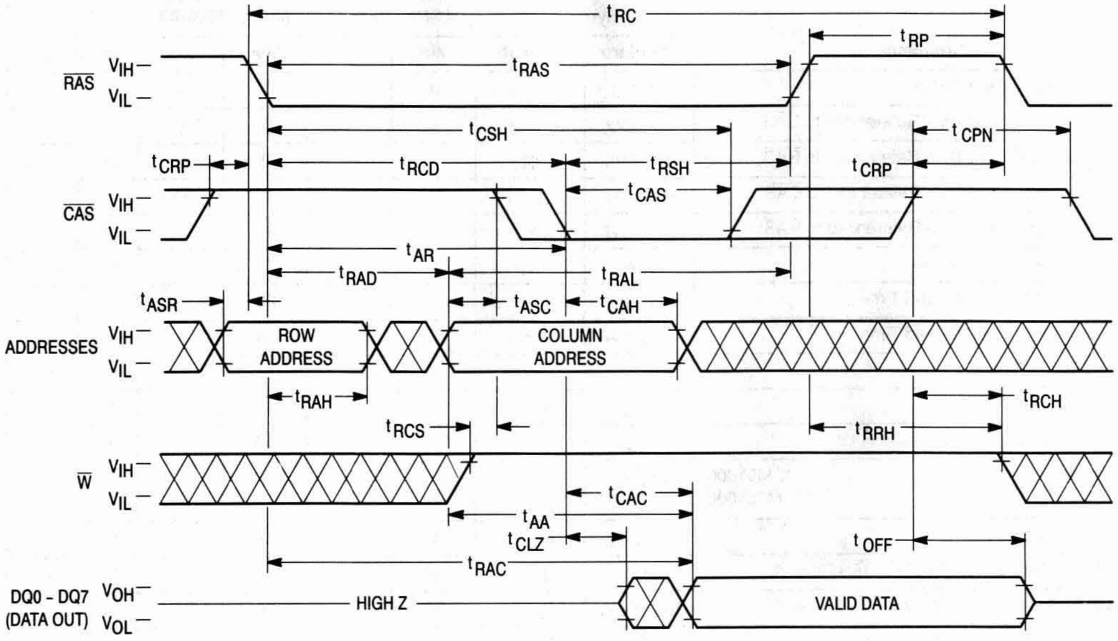
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM91000-70 MCM9L1000-70		MCM91000-80 MCM9L1000-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	15	—	15	—	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELWH}	t_{WCR}	55	—	60	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14, 15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14, 15
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	55	—	60	—	ns	
Refresh Period MCM91000 MCM9L1000	t_{RVRV}	t_{RFSH}	— —	8 64	— —	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15, 16
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	ns	

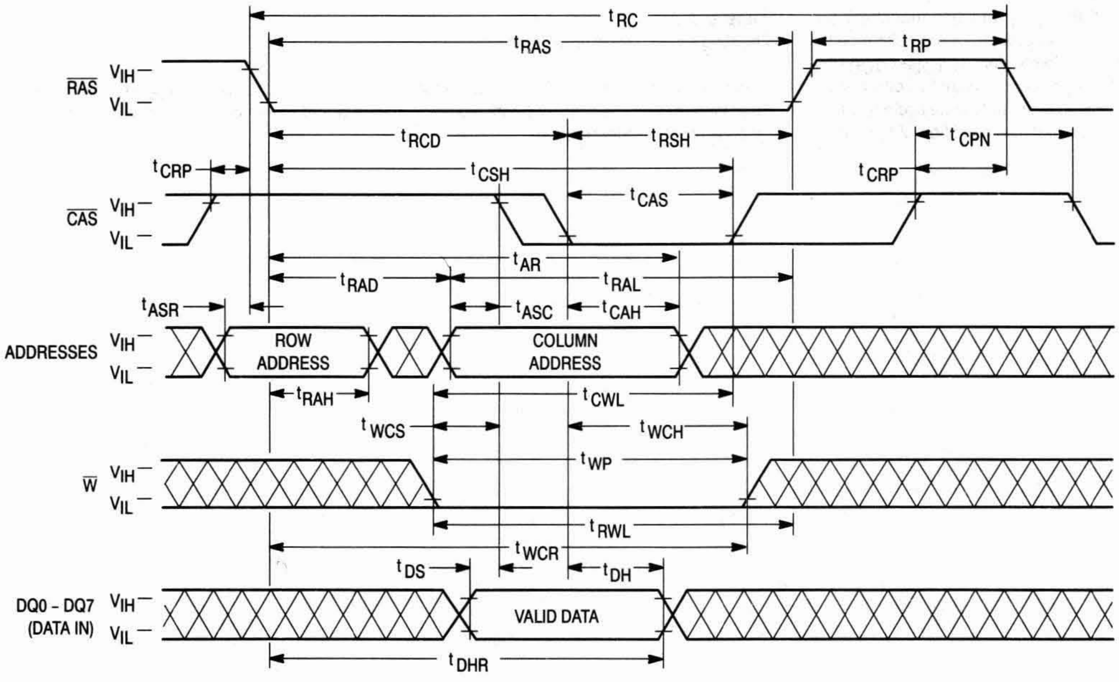
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

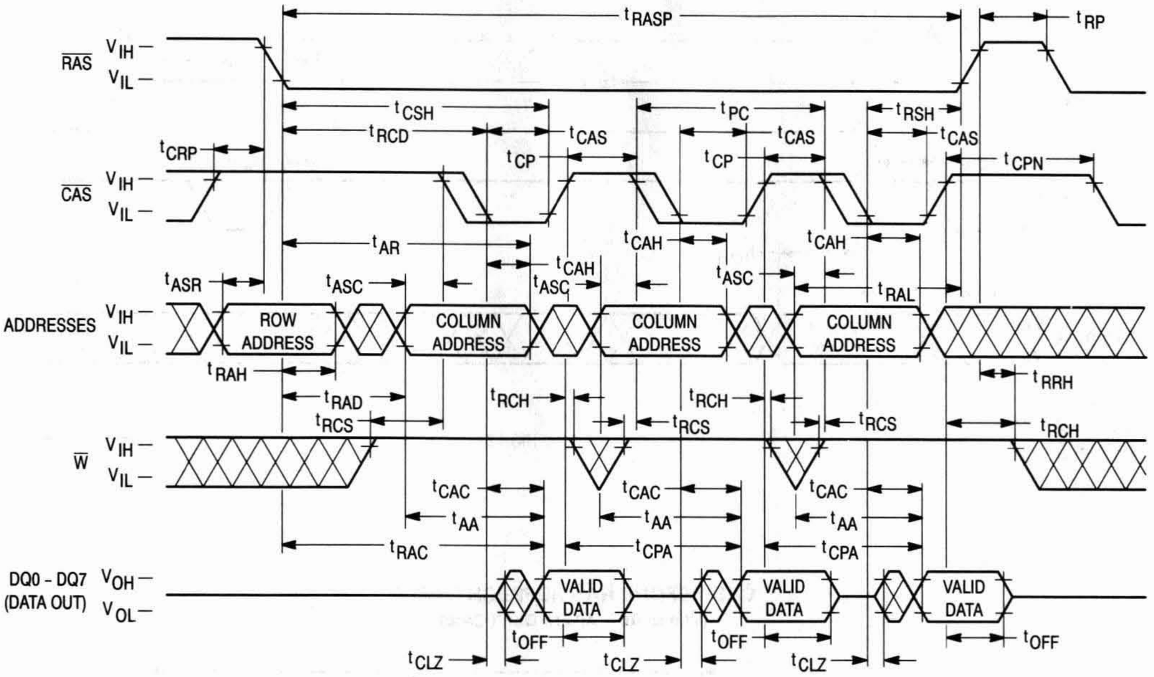
READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCPN
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W
VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
DQ0 - DQ7 (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA

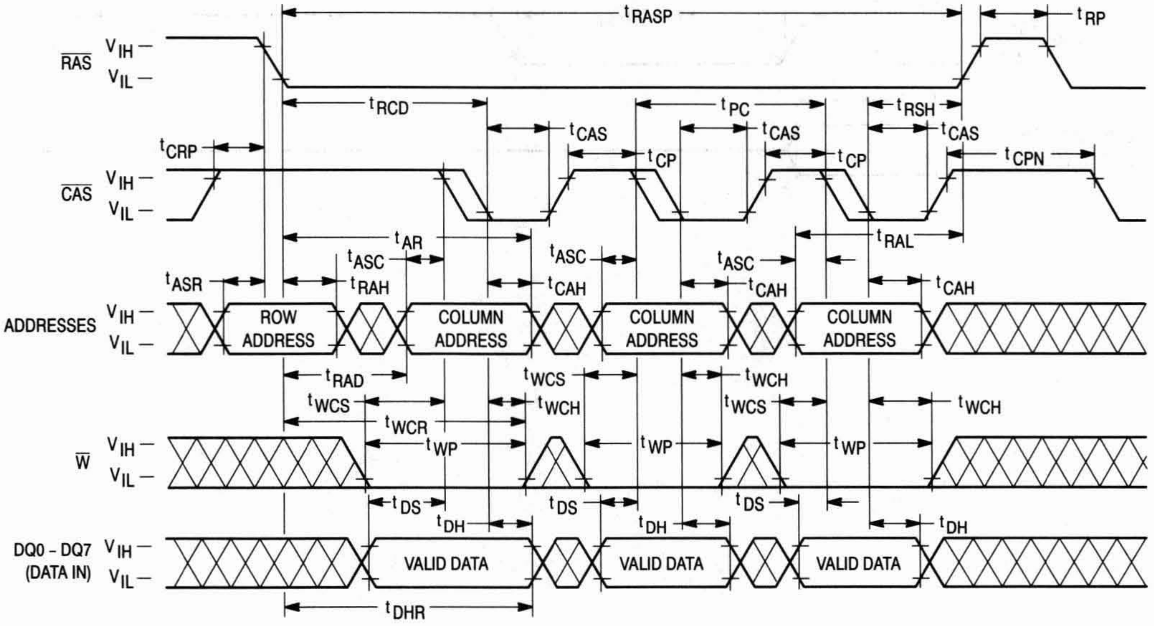
EARLY WRITE CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tRCD
tRSH
tCPN
tCRP
tCSH
tCRP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWP
W
VIH
VIL
tRWL
tWCR
tDS
tDH
DQ0 - DQ7 (DATA IN)
VIH
VIL
VALID DATA
tDHR

FAST PAGE MODE READ CYCLE

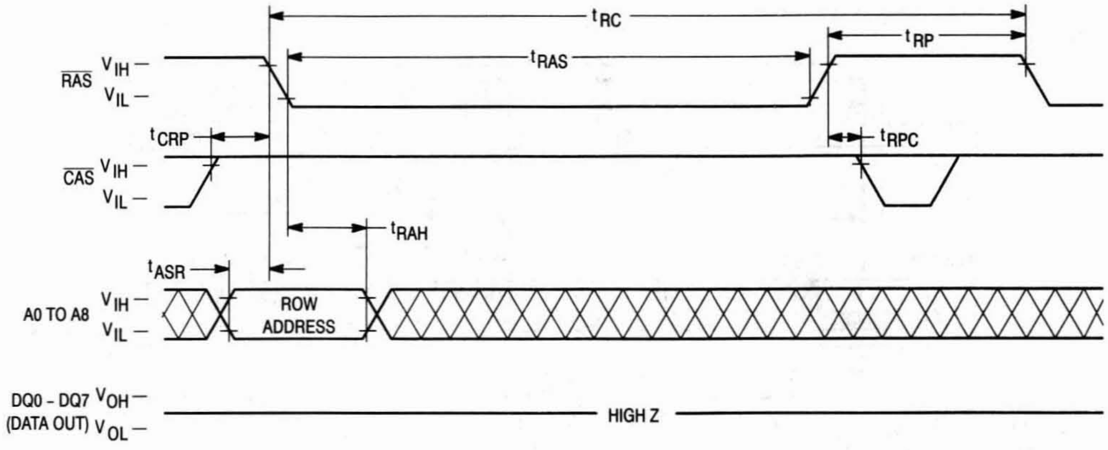

tRASP
tRP
RAS
VIH –
VIL –
tCSH
tPC
tRSH
tRCD
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCPN
CAS
VIH –
VIL –
tAR
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
tRAL
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAH
tRRH
tRAD
tRCH
tRCH
tRCS
tRCS
tRCS
tRCH
W
VIH –
VIL –
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
DQ0 - DQ7
(DATA OUT)
VOH –
VOL –
VALID DATA
VALID DATA
VALID DATA
tOFF
tOFF
tOFF
tCLZ
tCLZ
tCLZ

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)


tRASP
tRP
RAS
VIH –
VIL –
tRCD
tPC
tRSH
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCPN
CAS
VIH –
VIL –
tAR
tRAL
tASC
tASC
tASC
tASR
tRAH
tCAH
tCAH
tCAH
ADDRESSES
VIH –
VIL –
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tWCS
tWCH
tWCS
tWCH
tWCS
tWCH
tWCR
tWP
tWP
tWP
W
VIH –
VIL –
tDS
tDS
tDS
tDH
tDH
tDH
DQ0 - DQ7
(DATA IN)
VIH –
VIL –
VALID DATA
VALID DATA
VALID DATA
tDHR

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

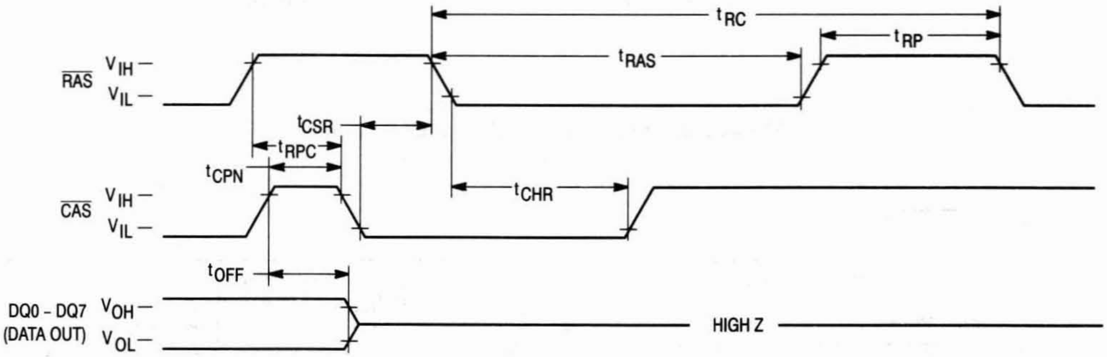
($\overline{\text{W}}$ and A9 are Don't Care)



tRC
tRAS
tRP
RAS
VIH
VIL
tCRP
tRPC
CAS
VIH
VIL
tRAH
tASR
A0 TO A8
VIH
VIL
ROW ADDRESS
DQ0 - DQ7 VOH
(DATA OUT) VOL
HIGH Z

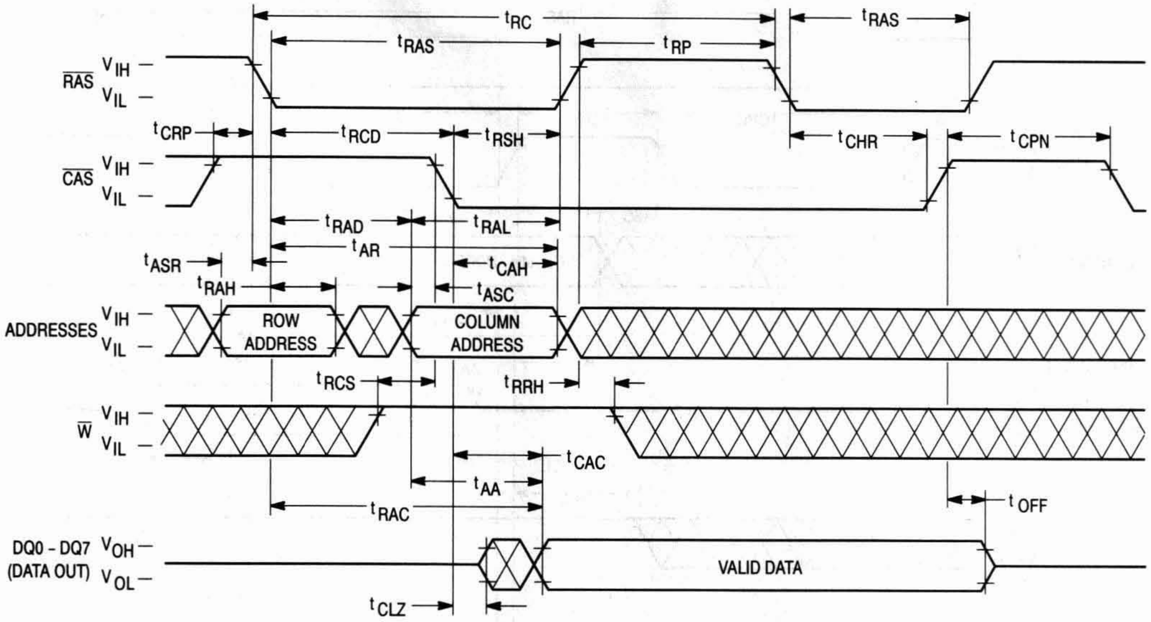
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{W}}$ and A0 – A9 are Don't Care)

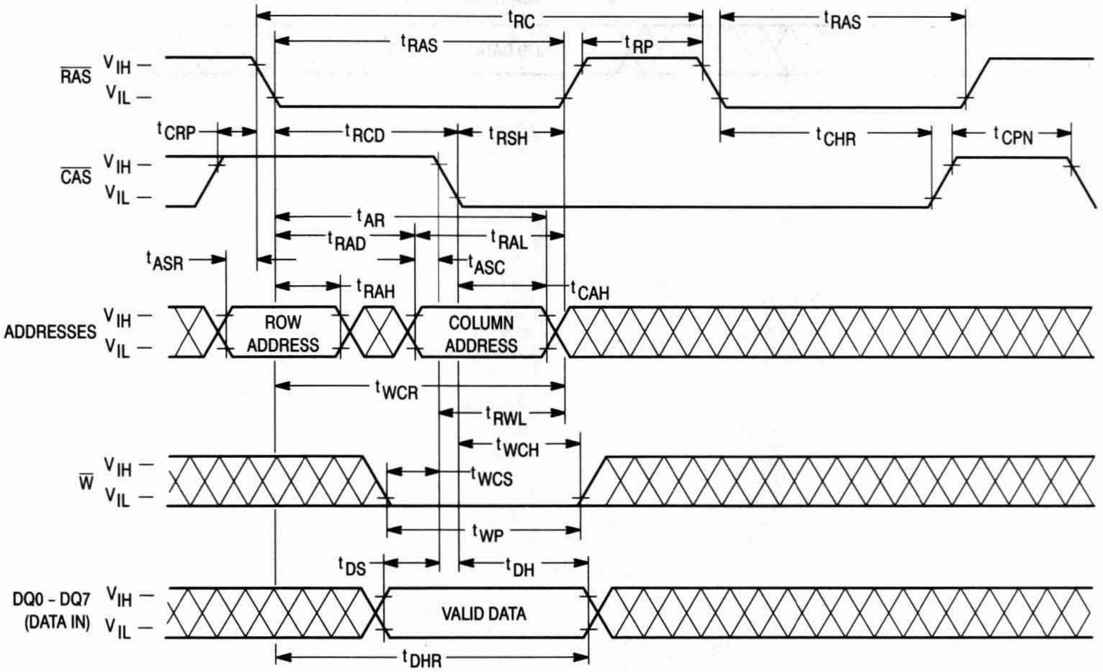


tRC
tRP
tRAS
RAS
VIH
VIL
tCSR
tRPC
tCPN
tCHR
CAS
VIH
VIL
tOFF
DQ0 - DQ7 VOH
(DATA OUT) VOL
HIGH Z

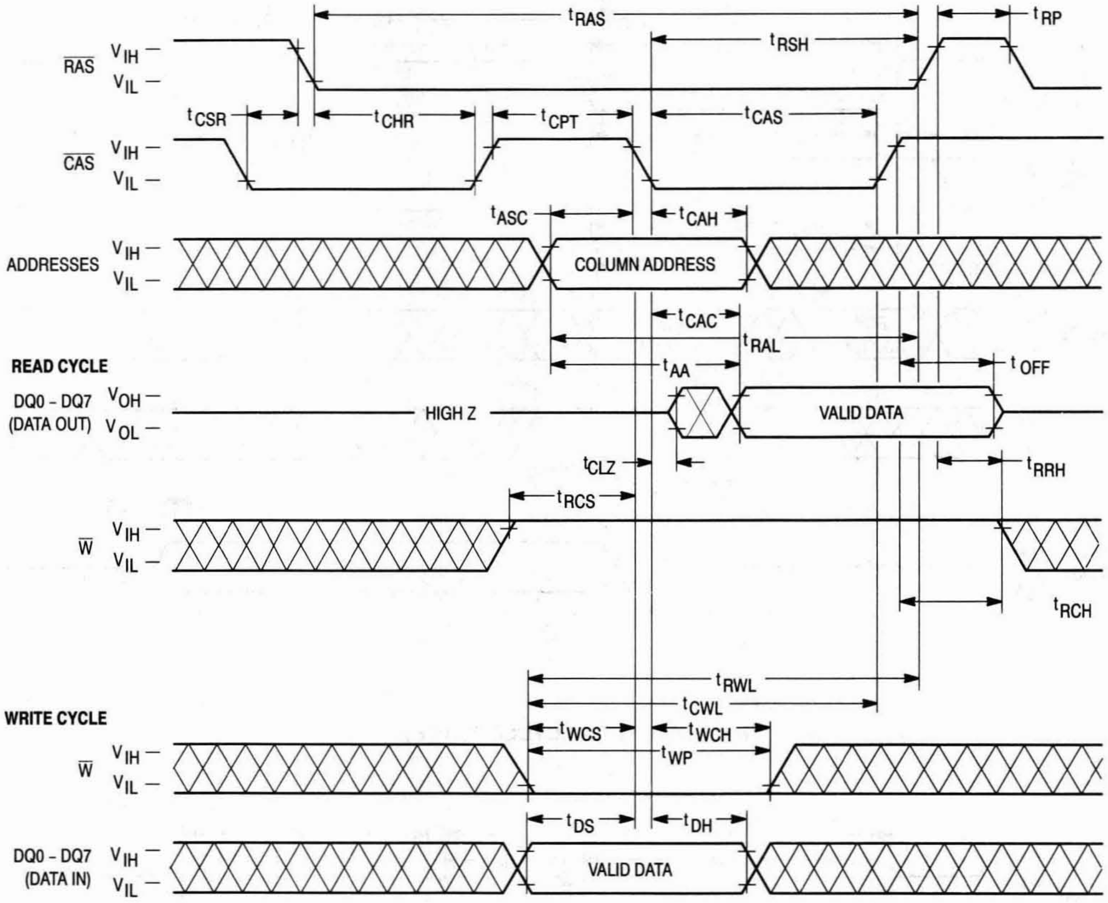
HIDDEN REFRESH CYCLE (READ)


t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$ V_{IH} V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CPN}
$\overline{CAS}$ V_{IH} V_{IL}
t_{RAD}
t_{RAL}
t_{AR}
t_{ASR}
t_{CAH}
t_{RAH}
t_{ASC}
ADDRESSES V_{IH} V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RCS}
t_{RRH}
$\overline{W}$ V_{IH} V_{IL}
t_{CAC}
t_{AA}
t_{RAC}
t_{OFF}
DQ0 - DQ7 (DATA OUT) V_{OH} V_{OL}
VALID DATA
t_{CLZ}

HIDDEN REFRESH CYCLE (WRITE)


t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$ V_{IH} V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CPN}
$\overline{CAS}$ V_{IH} V_{IL}
t_{AR}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES V_{IH} V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{WCR}
t_{RWL}
t_{WCH}
t_{WCS}
$\overline{W}$ V_{IH} V_{IL}
t_{WP}
t_{DS}
t_{DH}
DQ0 - DQ7 (DATA IN) V_{IH} V_{IL}
VALID DATA
t_{DHR}

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



tRAS
tRSH
tRP
RAS
VIH
VIL
tCSR
tCHR
tCPT
tCAS
CAS
VIH
VIL
tASC
tCAH
ADDRESSES
VIH
VIL
COLUMN ADDRESS
tCAC
tRAL
READ CYCLE
tAA
tOFF
DQ0 - DQ7 (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA
tCLZ
tRRH
tRCS
W
VIH
VIL
tRCH
tRWL
tCWL
WRITE CYCLE
tWCS
tWCH
tWP
W
VIH
VIL
tDS
tDH
DQ0 - DQ7 (DATA IN)
VIH
VIL
VALID DATA

5

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the module are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 word locations in the module. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are two other variations in addressing the 1M RAM: **$\overline{RAS}$-only refresh cycle,** and **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either the "normal" random read cycle or the page mode read cycle. The normal read cycle is outlined here, while the page mode is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired word location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. However, $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Data out (DQ) is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z.

WRITE CYCLE

The user can write to the module with either of two cycles: early write or page mode early write. Early write mode is discussed here, while the page mode write operation is covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (DQ) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the 1M dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum of t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature; therefore, each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Words in the MCM91000 require refresh every 8 milliseconds, while refresh time for the MCM9L1000 is 64 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM91000, and 124.8 microseconds for the MCM9L1000. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM91000 and 64 milliseconds on the MCM9L1000.

A normal read or write operation to the RAM will refresh all the words associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test.** This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read cycle**. Repeat this operation 512 times.
3. Select a column address and write "1" into the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, write cycle**. Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

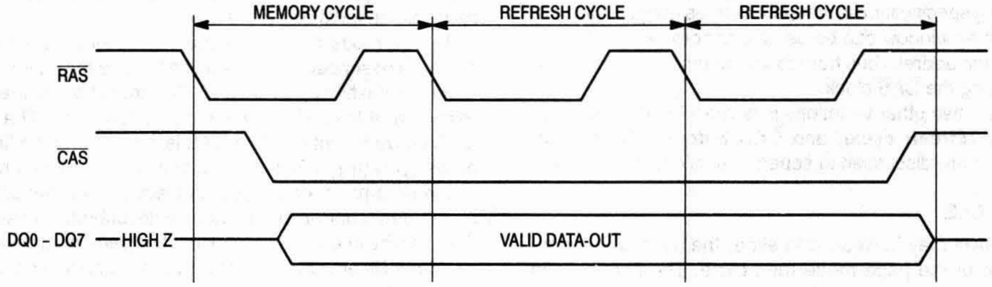


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION

(Order by Full Part Number)

MCM 91000 or 9L1000 X XX

Motorola Memory Prefix — MCM
Part Number — 91000 or 9L1000
Package (L/LH = SIP, S/AS = SIMM, SG = Gold Pad SIMM) — X
Speed (70 = 70 ns, 80 = 80 ns) — XX

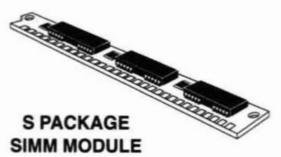
Full Part Numbers —	MCM91000L70	MCM91000LH70	MCM91000S70	MCM91000AS70	MCM91000SG70
	MCM91000L80	MCM91000LH80	MCM91000S80	MCM91000AS80	MCM91000SG80
	MCM9L1000L70	MCM9L1000LH70	MCM9L1000S70	MCM9L1000AS70	MCM9L1000SG70
	MCM9L1000L80	MCM9L1000LH80	MCM9L1000S80	MCM9L1000AS80	MCM9L1000SG80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM91430
MCM9L1430

1M x 9 Bit Dynamic Random Access Memory Module



S PACKAGE
SIMM MODULE
CASE 839A-01

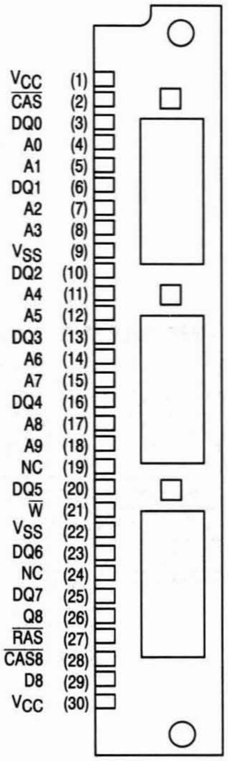
L PACKAGE
SIP MODULE
CASE 852A-02

The MCM91430 and MCM9L1430 are 9M dynamic random access memory (DRAM) modules organized as 1,048,576 x 9 bits. The modules are 30-lead single-in-line memory modules (SIMM) consisting of two MCM54400AN and one 1M DRAM housed in a 20/26 J-lead small outline package (SOJ) and mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted adjacent to each DRAM. The MCM54400AN is a CMOS high-speed dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.

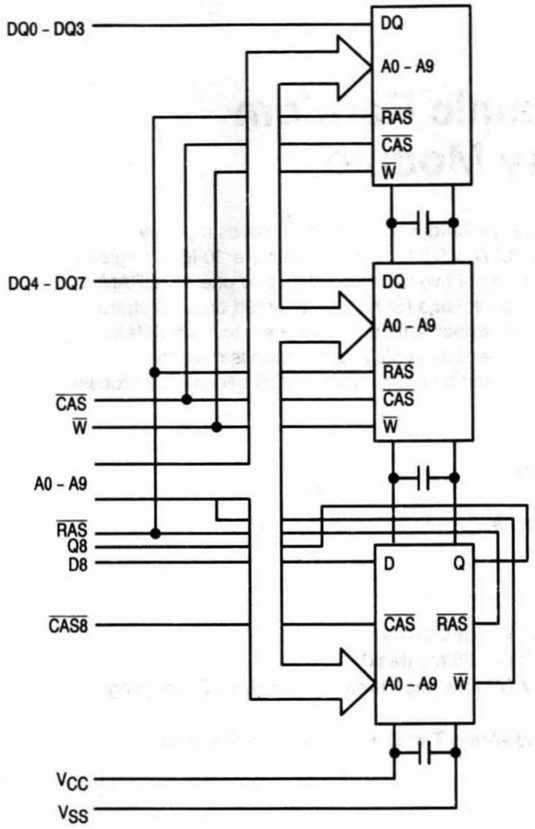
- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM91430 = 16 ms (Max)
  MCM9L1430 = 128 ms (Max)
- Consists of Two 4M and One 1M DRAMs and Three 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM91430-60 = 60 ns (Max)
  MCM91430-70 = 70 ns (Max)
  MCM91430-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM91430-60 = 1.82 W (Max)
  MCM91430-70 = 1.54 W (Max)
  MCM91430-80 = 1.32 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 33 mW (Max)
  CMOS Levels (MCM91430) = 16.5 mW (Max)
  (MCM9L1430) = 3.3 mW (Max)
- $\overline{\text{CAS}}$ Control for Eight Common I/O Lines
- $\overline{\text{CAS}}$ Control for Separate I/O Pair
- Available in Edge Connector (MCM91430S), and Pin Connector (MCM91430L)
- Available in Industrial Temperature Range (– 40°C to + 85°C): MCM91430SC

PIN NAMES	
A0 – A9	Address Inputs
DQ0 – DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{CAS8}}$	Column Address Strobe
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

30-PIN
SINGLE IN-LINE PACKAGE
(TOP VIEW, MCM91430S/9L1430S)



FUNCTIONAL BLOCK DIAGRAM


DQ0 - DQ3
DQ
A0 - A9
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
$\overline{\text{W}}$
DQ4 - DQ7
DQ
A0 - A9
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
$\overline{\text{W}}$
$\overline{\text{CAS}}$
$\overline{\text{W}}$
A0 - A9
$\overline{\text{RAS}}$
Q8
D8
D
Q
$\overline{\text{CAS8}}$
$\overline{\text{CAS}}$
$\overline{\text{RAS}}$
A0 - A9
$\overline{\text{W}}$
V_{CC}
V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	2.48	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	− 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM91430-60, t_{RC} = 110 ns MCM91430-70, t_{RC} = 130 ns MCM91430-80, t_{RC} = 150 ns	I_{CC1}	 — — —	 330 280 240	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	6	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles MCM91430-60, t_{RC} = 110 ns MCM91430-70, t_{RC} = 130 ns MCM91430-80, t_{RC} = 150 ns	I_{CC3}	 — — —	 330 280 240	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM91430-60, t_{PC} = 45 ns MCM91430-70, t_{PC} = 45 ns MCM91430-80, t_{PC} = 50 ns	I_{CC4}	 — — —	 200 200 170	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2 V) MCM91430 MCM9L1430	I_{CC5}	— —	3 0.6	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM91430-60, t_{RC} = 110 ns MCM91430-70, t_{RC} = 130 ns MCM91430-80, t_{RC} = 150 ns	I_{CC6}	 — — —	 330 280 240	mA	1
V_{CC} Power Supply Current, Battery Backup Mode — MCM9L1430 Only (t_{RAC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0 – A9, $\overline{W}$, DQ = V_{CC} − 0.2 V or 0.2 V)	I_{CC7}	—	0.9	mA	1, 3
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	− 30	30	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	− 10	10	µA	
Output High Voltage (I_{OH} = − 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery backup. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$	C_{in}	25	pF
	D8, $\overline{CAS8}$		17	pF
Input/Output Capacitance	DQ0 – DQ7	$C_{I/O}$	17	pF
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q8	C_{out}	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\,\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM91430-60 MCM9L1430-60		MCM91430-70 MCM9L1430-70		MCM91430-80 MCM9L1430-80			
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Unit	Notes
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	50	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	40	—	40	—	45	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	100 k	70	100 k	80	100 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	40	—	45	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	20	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

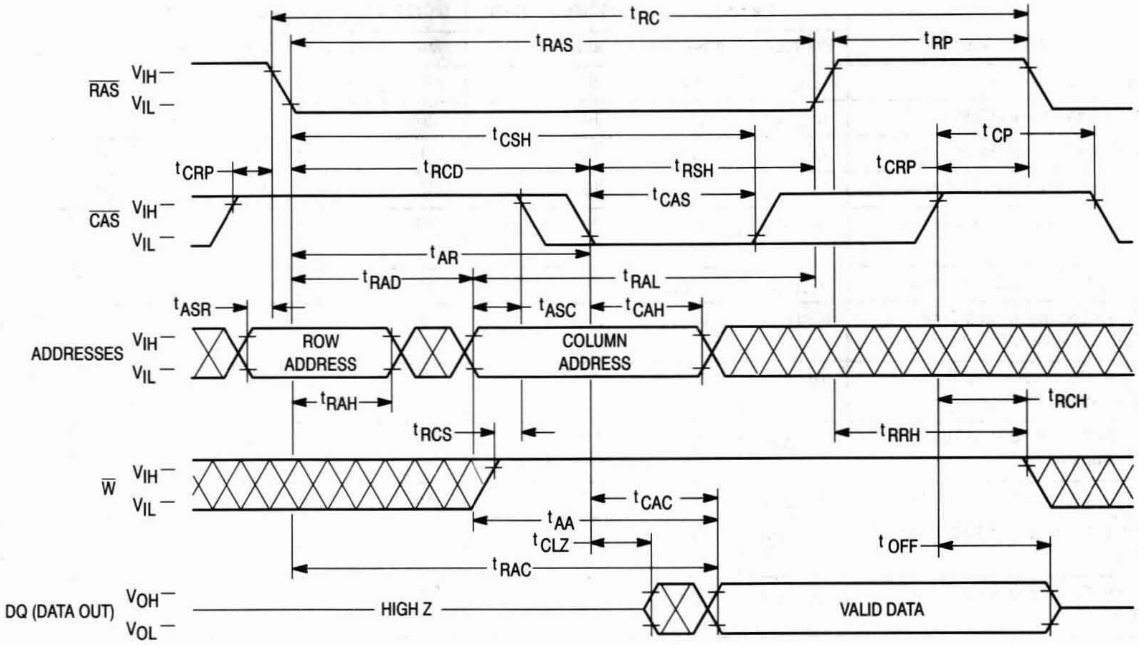
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM91430-60 MCM9L1430-60		MCM91430-70 MCM9L1430-70		MCM91430-80 MCM9L1430-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	14
Refresh Period MCM91430 MCM9L1430	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	30	—	30	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELAX}	t_{AR}	50	—	55	—	60	—	ns	
Data In Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	50	—	55	—	60	—	ns	16

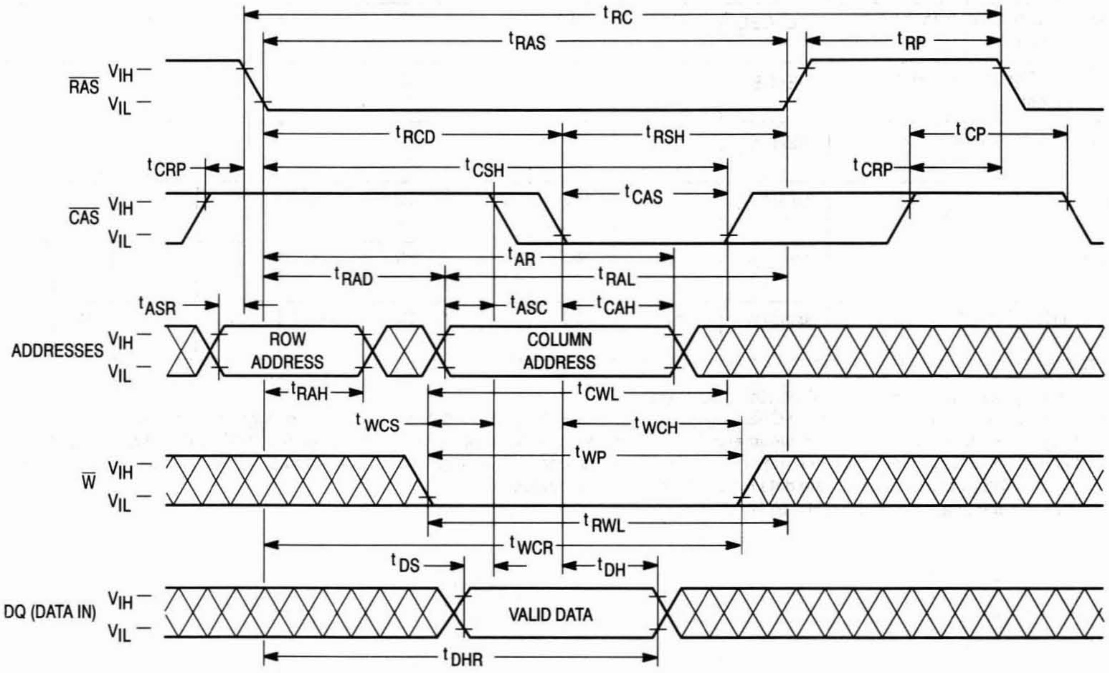
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in late write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.
16. This parameter applies to the parity bit D8/Q8 only.

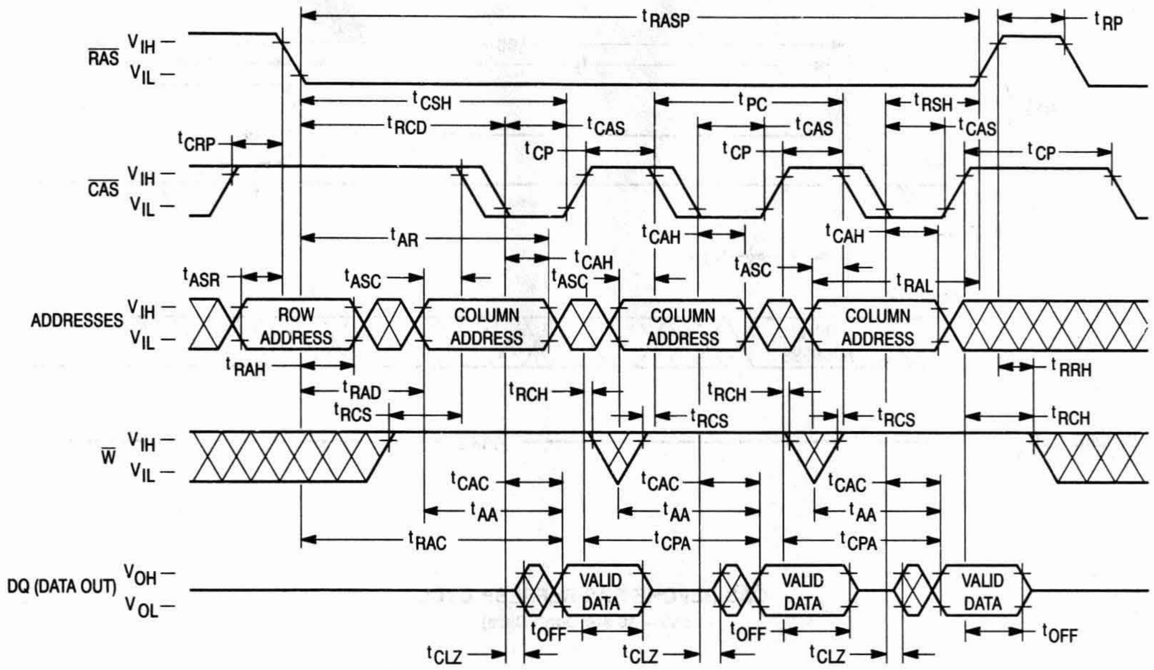
READ CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCP
tCRP
tRCD
tRSH
tCRP
CAS
VIH
VIL
tCAS
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W
VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
DQ (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA

EARLY WRITE CYCLE

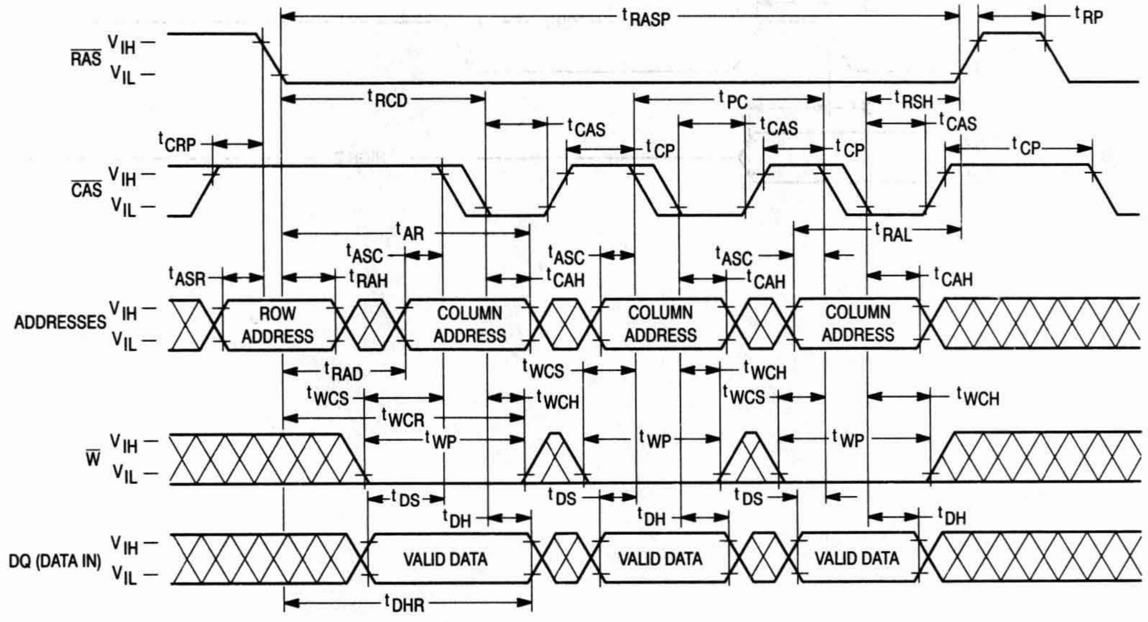

tRC
tRAS
tRP
RAS
VIH
VIL
tRCD
tRSH
tCP
tCRP
tCSH
tCRP
CAS
VIH
VIL
tCAS
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWP
W
VIH
VIL
tRWL
tWCR
tDS
tDH
DQ (DATA IN)
VIH
VIL
VALID DATA
tDHR

FAST PAGE MODE READ CYCLE



RAS
CAS
ADDRESSES
W
DQ (DATA OUT)
V_{IH}
V_{IL}
V_{OH}
V_{OL}
t_{RASP}
t_{RP}
t_{CSH}
t_{PC}
t_{RSH}
t_{RCD}
t_{CAS}
t_{CRP}
t_{CP}
t_{AR}
t_{CAH}
t_{ASR}
t_{ASC}
t_{RAL}
ROW ADDRESS
COLUMN ADDRESS
t_{RAH}
t_{RAD}
t_{RRH}
t_{RCS}
t_{RCH}
t_{CAC}
t_{AA}
t_{RAC}
t_{CPA}
VALID DATA
t_{OFF}
t_{CLZ}

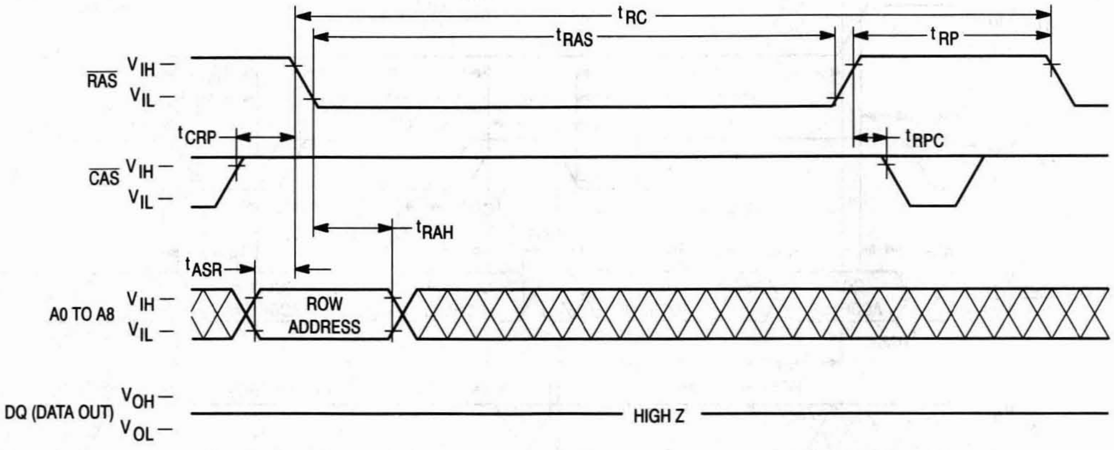
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



RAS
CAS
ADDRESSES
W
DQ (DATA IN)
V_{IH}
V_{IL}
t_{RASP}
t_{RP}
t_{RCD}
t_{PC}
t_{RSH}
t_{CAS}
t_{CRP}
t_{CP}
t_{AR}
t_{RAL}
t_{ASC}
t_{ASR}
t_{RAH}
t_{CAH}
ROW ADDRESS
COLUMN ADDRESS
t_{RAD}
t_{WCS}
t_{WCH}
t_{WCR}
t_{WP}
t_{DS}
t_{DH}
VALID DATA
t_{DHR}

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

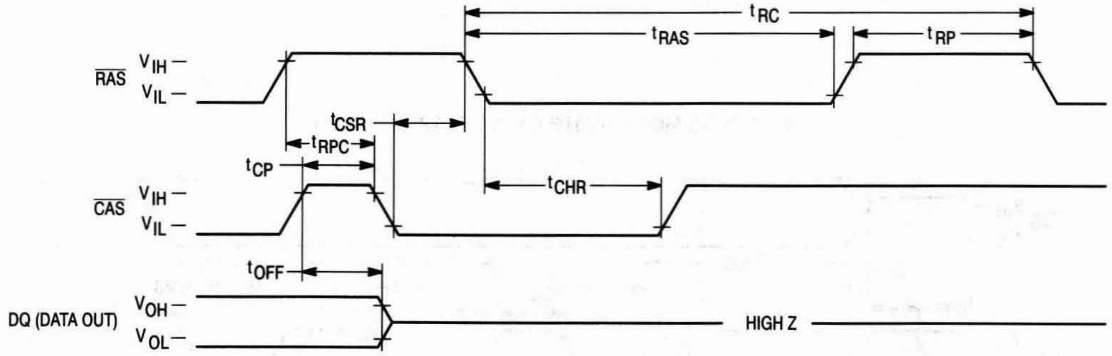
($\overline{\text{W}}$ and A9 are Don't Care)



t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
A0 TO A8
V_{IH}
V_{IL}
ROW
ADDRESS
DQ (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

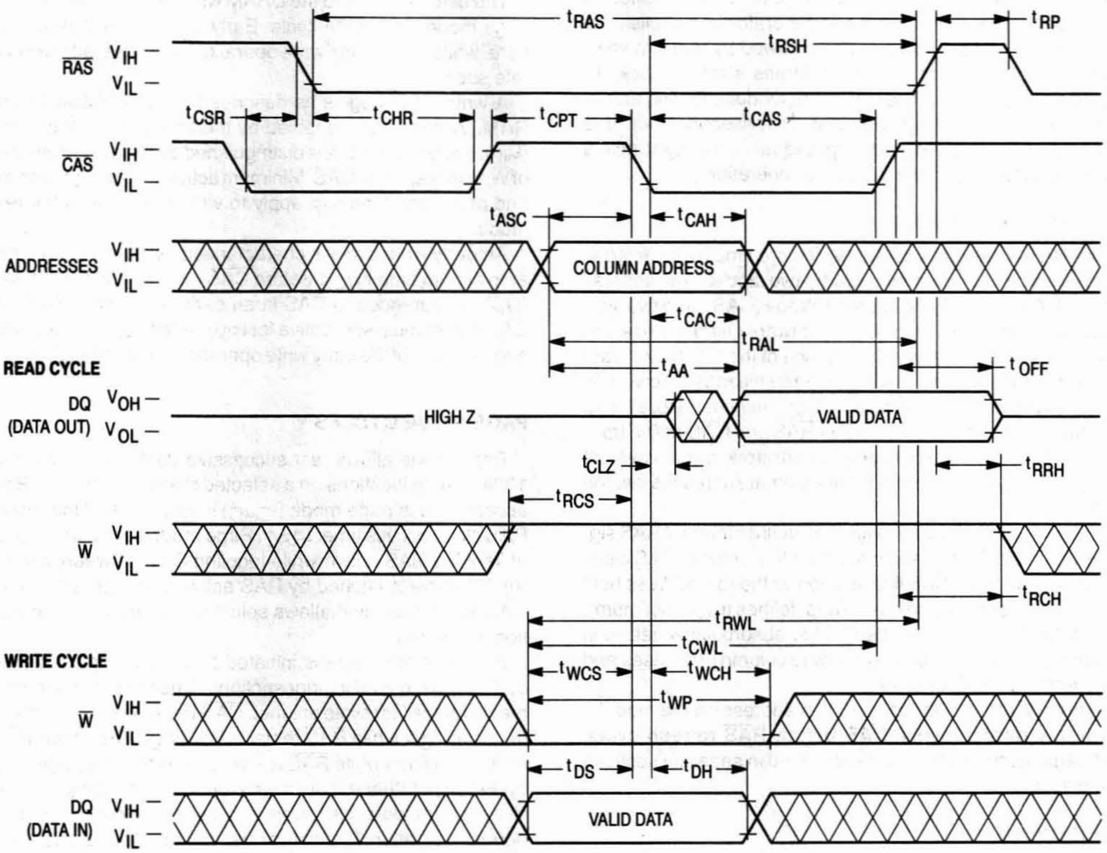
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

(A0 – A9 are Don't Care)



t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CSR}
t_{RPC}
t_{CP}
t_{CHR}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{OFF}
DQ (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



t_{RAS}
t_{RP}
t_{RSH}
$\overline{\text{RAS}}$ V_{IH} – V_{IL} –
t_{CSR}
t_{CHR}
t_{CPT}
t_{CAS}
$\overline{\text{CAS}}$ V_{IH} – V_{IL} –
t_{ASC}
t_{CAH}
ADDRESSES V_{IH} – V_{IL} –
COLUMN ADDRESS
t_{CAC}
t_{RAL}
READ CYCLE
t_{AA}
t_{OFF}
DQ (DATA OUT) V_{OH} – V_{OL} –
HIGH Z
VALID DATA
t_{CLZ}
t_{RRH}
t_{RCS}
$\overline{\text{W}}$ V_{IH} – V_{IL} –
t_{RCH}
t_{RWL}
t_{CWL}
WRITE CYCLE
t_{WCS}
t_{WCH}
t_{WP}
$\overline{\text{W}}$ V_{IH} – V_{IL} –
t_{DS}
t_{DH}
DQ (DATA IN) V_{IH} – V_{IL} –
VALID DATA

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 word locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the module: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either a "normal" random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. $\overline{\text{CAS}}$ controls read access time; $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ clock active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with either an early write or page mode early write cycle. Early write mode is discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early write mode is distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (DQ) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM91430 require refresh every 16 milliseconds, while refresh time for the MCM9L1430 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM91430, and 124.8 microseconds for the MCM9L1430. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM91430 and 128 milliseconds on the MCM9L1430.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode cycle) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 CAS before RAS** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **CAS before RAS refresh counter test, read cycle**. Repeat this operation 512 times.
3. Select a column address and write "1" into the cell by performing **CAS before RAS refresh counter test, write cycle**. Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

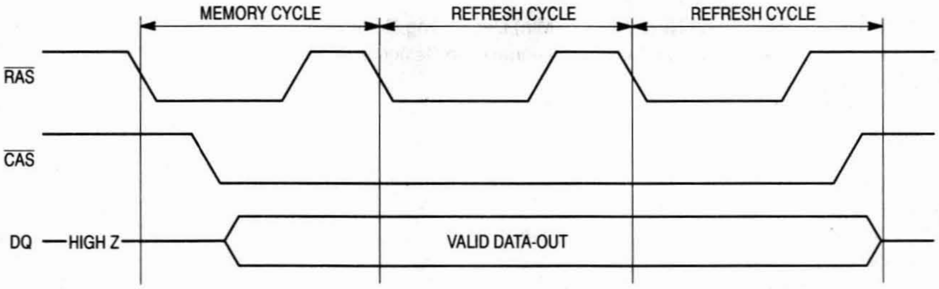


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION

(Order by Full Part Number)

MCM 91430 or 9L1430 X XX

Motorola Memory Prefix — MCM
Part Number — 91430 or 9L1430
X — Package (S = SIMM, L = SIP, SC = Industrial Temperature SIMM)
XX — Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns)

Full Part Numbers —

MCM91430S60	MCM91430L60	MCM91430SC60
MCM91430S70	MCM91430L70	MCM91430SC70
MCM91430S80	MCM91430L80	MCM91430SC80
MCM9L1430S60	MCM9L1430L60	MCM9L1430SC60
MCM9L1430S70	MCM9L1430L70	MCM9L1430SC70
MCM9L1430S80	MCM9L1430L80	MCM9L1430SC80

NOTE: Contact your Motorola representative for further information on INDUSTRIAL TEMPERATURE MODULE PRODUCTS.

NOTE: For mechanical data, please see Chapter 10.

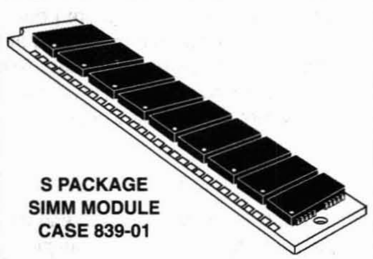
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM94000
MCM9L4000
MCM94030

4M x 9 Bit Dynamic Random Access Memory Module

The MCM94000 is a 36M dynamic random access memory (DRAM) module organized as 4,194,304 x 9 bits. The module is a 30-lead single-in-line memory module (SIMM) consisting of nine MCM54100A DRAMs housed in a 20/26 J-lead small outline packages (SOJ) mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM54100A is a CMOS high-speed dynamic random access memory organized as 4,194,304 one-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM94000 = 16 ms
  MCM9L4000 = 128 ms
- Consists of Nine 4M x 1 DRAMs and Nine 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM94000-60 = 60 ns (Max)
  - MCM94000-70 = 70 ns (Max)
  - MCM94000-80 = 80 ns (Max)
- Low Active Power Dissipation:
  - MCM94000-60 = 5.94 W (Max)
  - MCM94000-70 = 4.95 W (Max)
  - MCM94000-80 = 4.21 W (Max)
- Low Standby Power Dissipation:
  - TTL Levels = 99 mW (Max)
  - CMOS Levels (MCM94000) = 50 mW (Max)
  - (MCM9L4000) = 10 mW (Max)
- $\overline{CAS}$ Control for Eight Common I/O Lines
- $\overline{CAS}$ Control for Separate I/O Pair
- Available in Edge Connector (MCM94000AS), Gold Pad Edge Connector (MCM94000ASG), Pin Connector (MCM94000L), or Low Height Pin Connector (MCM94030LH)
- Available in Industrial Temperature Range (– 40°C to + 85°C): MCM94000ASC

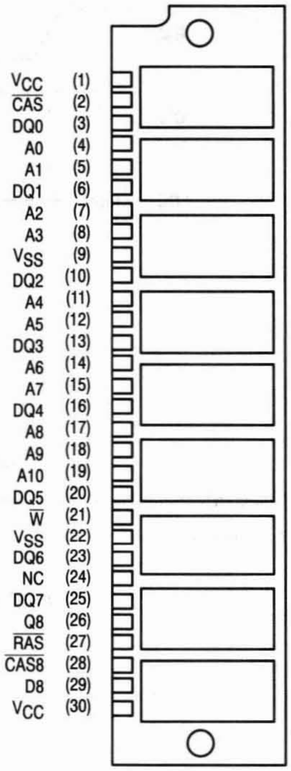


S PACKAGE
SIMM MODULE
CASE 839-01

L PACKAGE
SIP MODULE
CASE 852-01

LH PACKAGE
SIP MODULE
CASE 852A-02

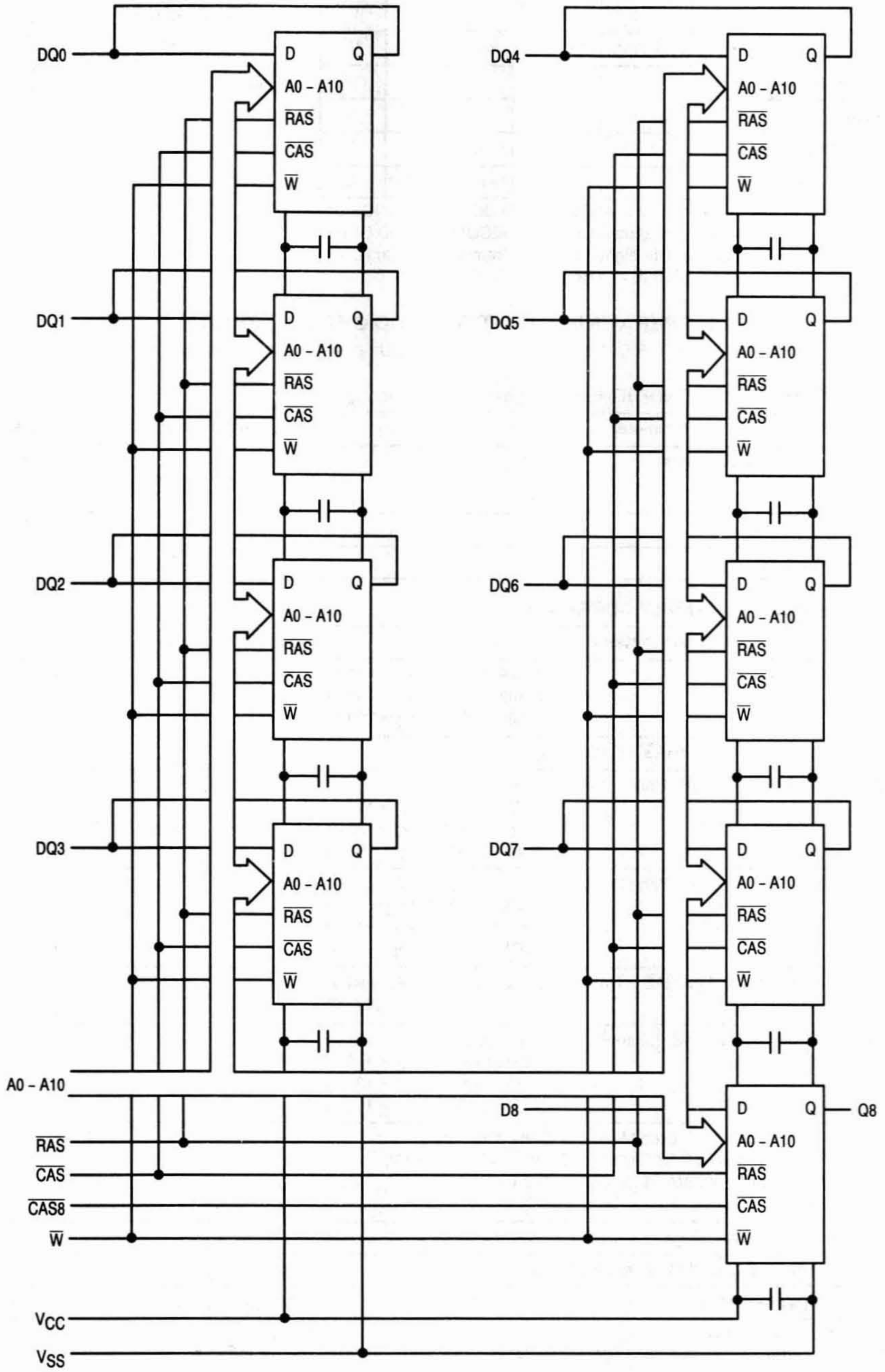
TOP VIEW



PIN NAMES

A0 – A10	Address Inputs
DQ0 – DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM


DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
D
Q
A0 – A10
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
$\overline{\text{W}}$
D8
Q8
A0 – A10
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
$\overline{\text{CAS8}}$
$\overline{\text{W}}$
V_{CC}
V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	6.3	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM94000-60, t_{RC} = 110 ns MCM94000-70, t_{RC} = 130 ns MCM94000-80, t_{RC} = 150 ns	I_{CC1}	— — —	1080 900 765	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	18	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles MCM94000-60, t_{RC} = 110 ns MCM94000-70, t_{RC} = 130 ns MCM94000-80, t_{RC} = 150 ns	I_{CC3}	 — — —	 1080 900 765	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM94000-60, t_{PC} = 45 ns MCM94000-70, t_{PC} = 45 ns MCM94000-80, t_{PC} = 50 ns	I_{CC4}	 — — —	 540 540 450	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM94000 MCM9L4000	I_{CC5}	— —	9 1.8	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM94000-60, t_{RC} = 110 ns MCM94000-70, t_{RC} = 130 ns MCM94000-80, t_{RC} = 150 ns	I_{CC6}	 — — —	 1080 900 765	mA	1
V_{CC} Power Supply Current, Battery Backup Mode — MCM9L4000 Only (t_{RC} = 125 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$ = V_{CC} – 0.2 V; DQ = V_{CC} – 0.2 V, 0.2 V or Open; A0 – A10 = V_{CC} – 0.2 V or 0.2 V) t_{RAS} = Min to 1 µs	I_{CC7}	—	2.7	mA	1, 3
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 90	90	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(O)}$	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery backup. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A10, $\overline{\text{W}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$	C_{in}	55	pF
	D8, $\overline{\text{CAS8}}$		17	pF
Input/Output Capacitance	DQ0 – DQ7	$C_{I/O}$	22	pF
Output Capacitance ($\overline{\text{CAS}}$ = V_{IH} to Disable Output)	Q8	C_{out}	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\,\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

	Symbol		MCM94000-60 MCM9L4000-60 MCM94030-60		MCM94000-70 MCM9L4000-70 MCM94030-70		MCM94000-80 MCM9L4000-80 MCM94030-80			
Parameter	**Std**	**Alt**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	50	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	40	—	40	—	45	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	200 k	70	200 k	80	200 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	20	10 k	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	11

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C $\le T_A \le$ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

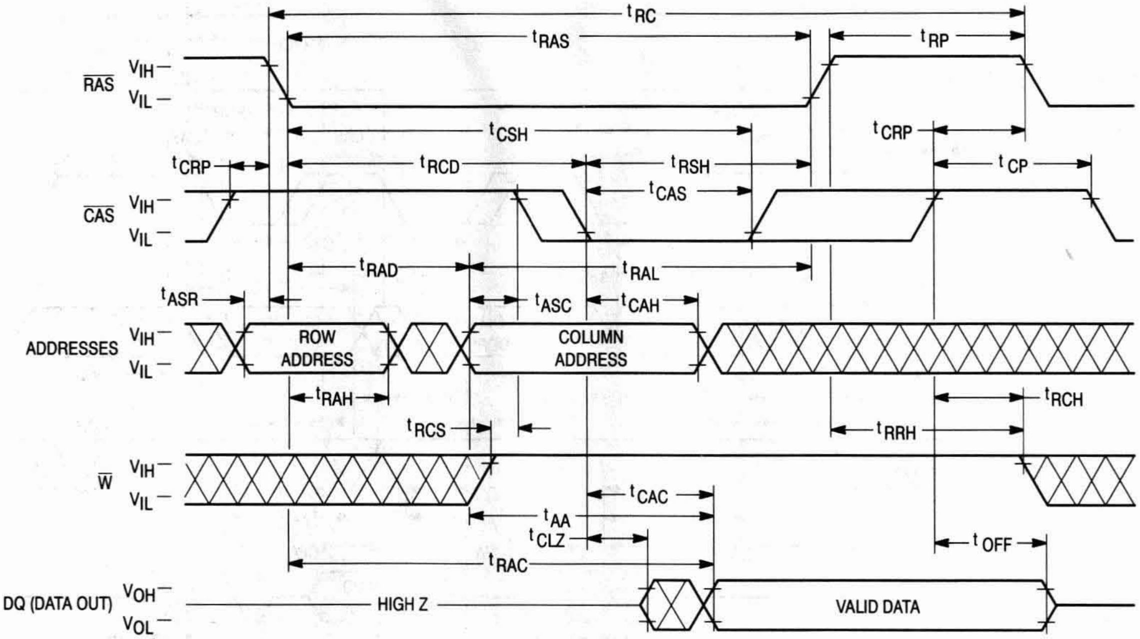
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM94000-60 MCM9L4000-60 MCM94030-60		MCM94000-70 MCM9L4000-70 MCM94030-70		MCM94000-80 MCM9L4000-80 MCM94030-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	14
Refresh Period MCM94000 MCM9L4000	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Time	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	

NOTES:

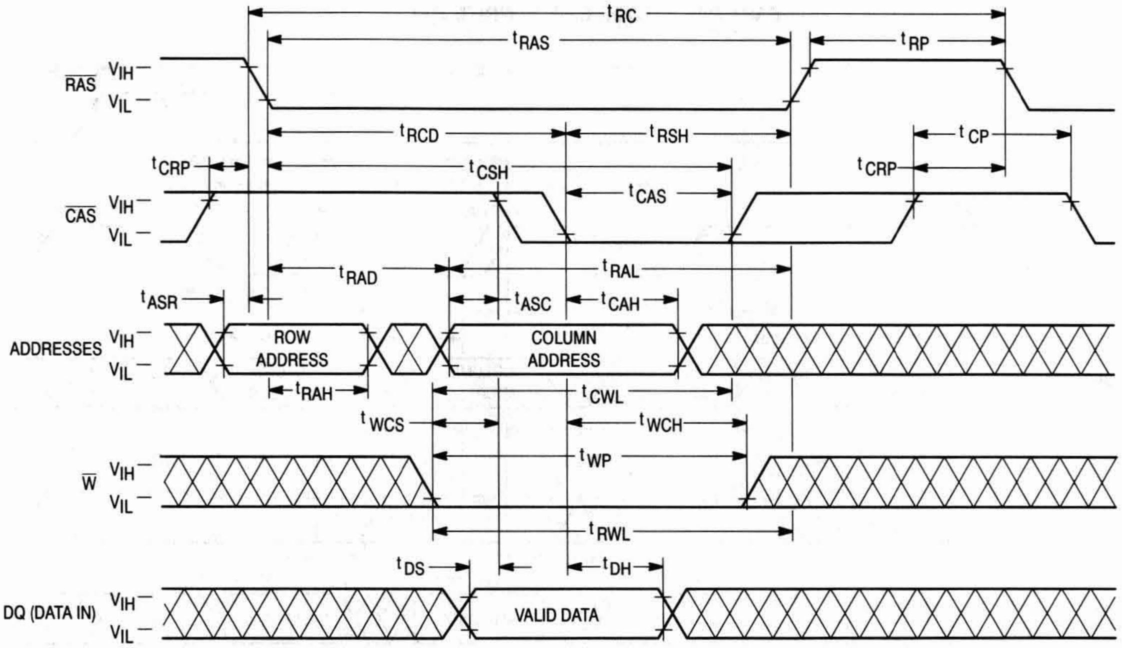
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



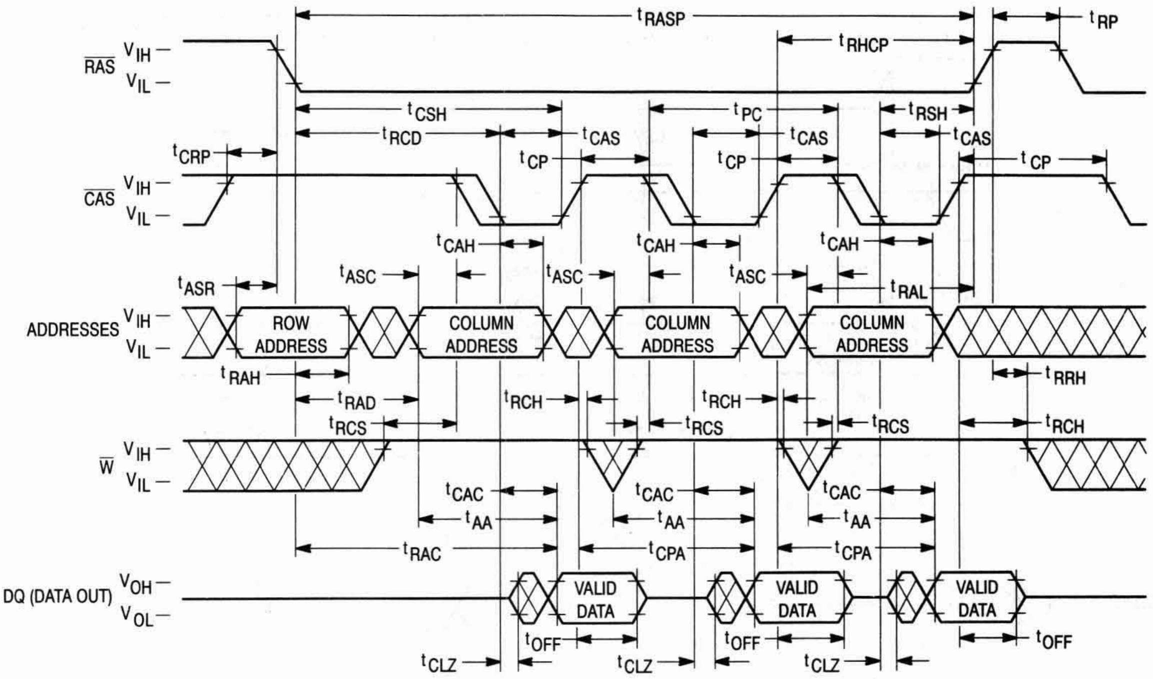
tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tCRP
tRCD
tRSH
tCP
tCAS
CAS
VIH
VIL
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W
VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
DQ (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA

EARLY WRITE CYCLE

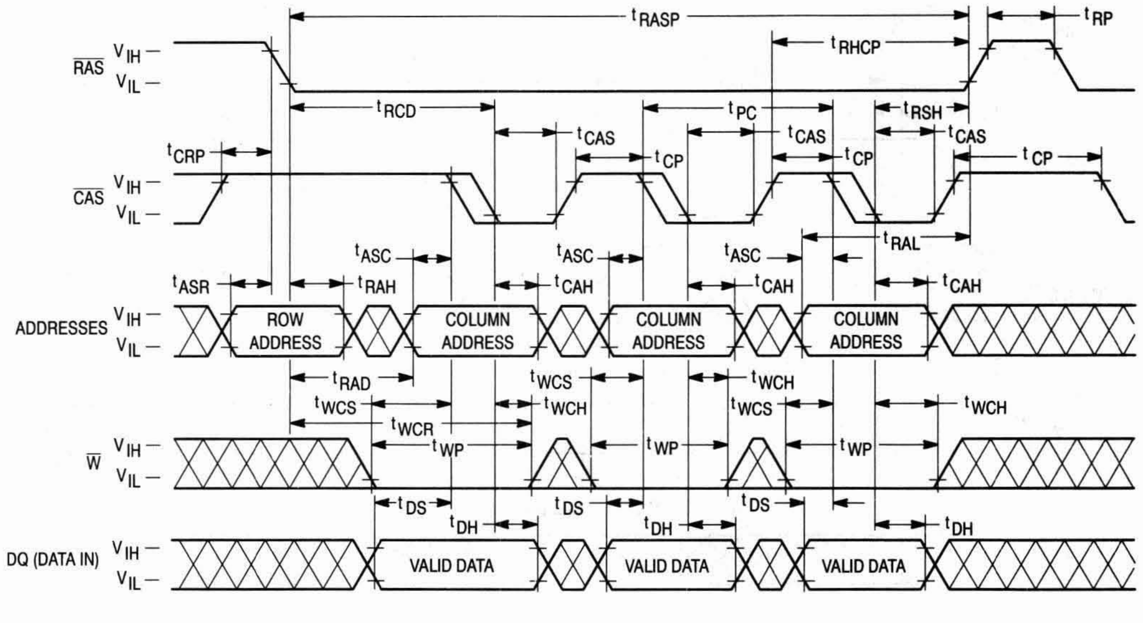


tRC
tRAS
tRP
RAS
VIH
VIL
tRCD
tRSH
tCP
tCRP
tCSH
tCRP
tCAS
CAS
VIH
VIL
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWP
W
VIH
VIL
tRWL
tDS
tDH
DQ (DATA IN)
VIH
VIL
VALID DATA

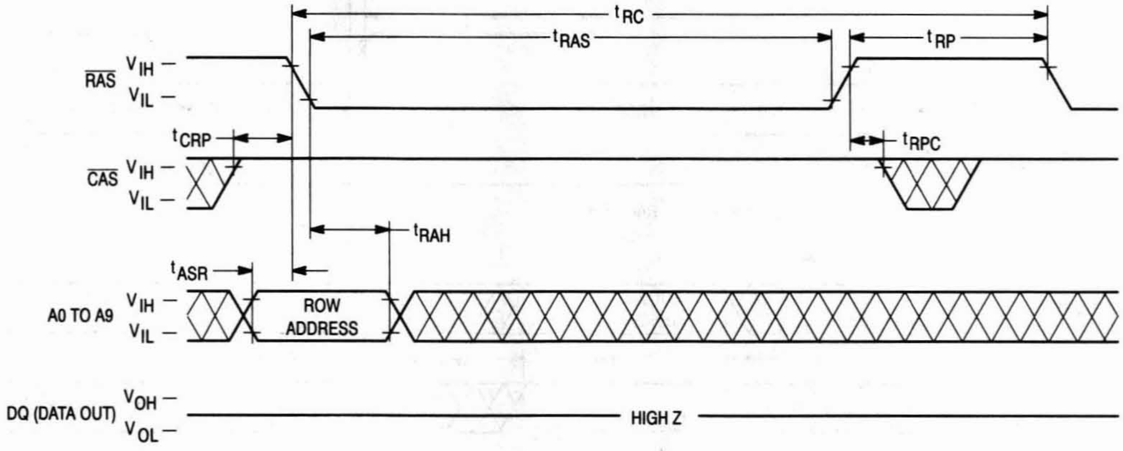
FAST PAGE MODE READ CYCLE


RAS
V IH
V IL
CAS
ADDRESSES
W
DQ (DATA OUT)
V OH
V OL
t RASP
t RHCP
t RP
t CSH
t PC
t RSH
t RCD
t CAS
t CRP
t CP
t CAH
t ASR
t ASC
t RAL
ROW ADDRESS
COLUMN ADDRESS
t RAH
t RRH
t RAD
t RCH
t RCS
t CAC
t AA
t RAC
t CPA
VALID DATA
t OFF
t CLZ

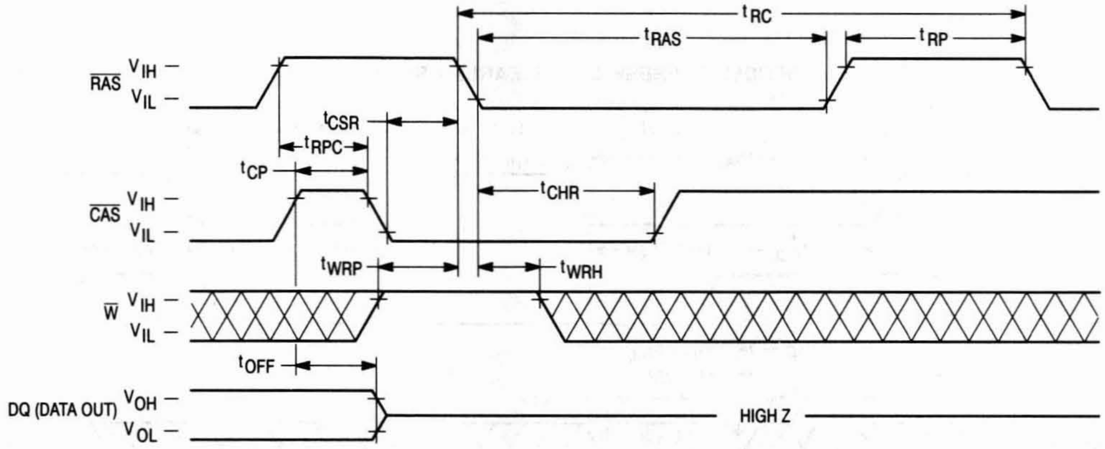
FAST PAGE MODE EARLY WRITE CYCLE


RAS
V IH
V IL
CAS
ADDRESSES
W
DQ (DATA IN)
t RASP
t RHCP
t RP
t RCD
t PC
t RSH
t CAS
t CRP
t CP
t RAL
t ASC
t ASR
t RAH
t CAH
ROW ADDRESS
COLUMN ADDRESS
t RAD
t WCS
t WCH
t WCR
t WP
t DS
t DH
VALID DATA

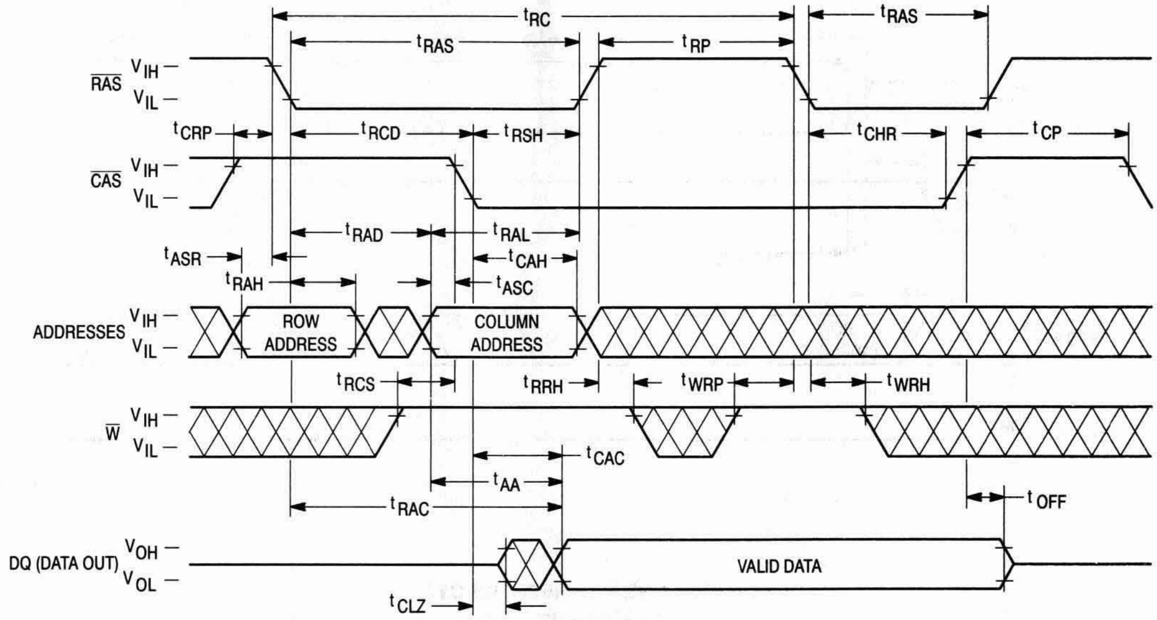
$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A10 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
A0 TO A9
V_{IH}
V_{IL}
ROW ADDRESS
DQ (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

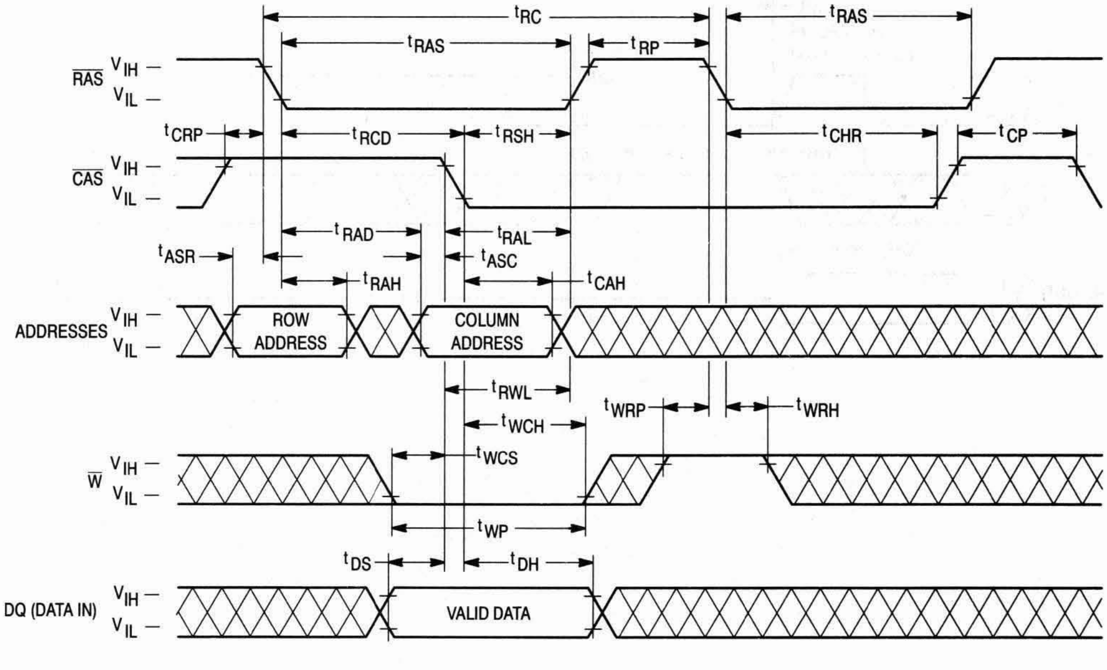
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
(A0 – A10 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSR}
t_{RPC}
t_{CP}
t_{CHR}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{WRP}
t_{WRH}
$\overline{W}$
V_{IH}
V_{IL}
t_{OFF}
DQ (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

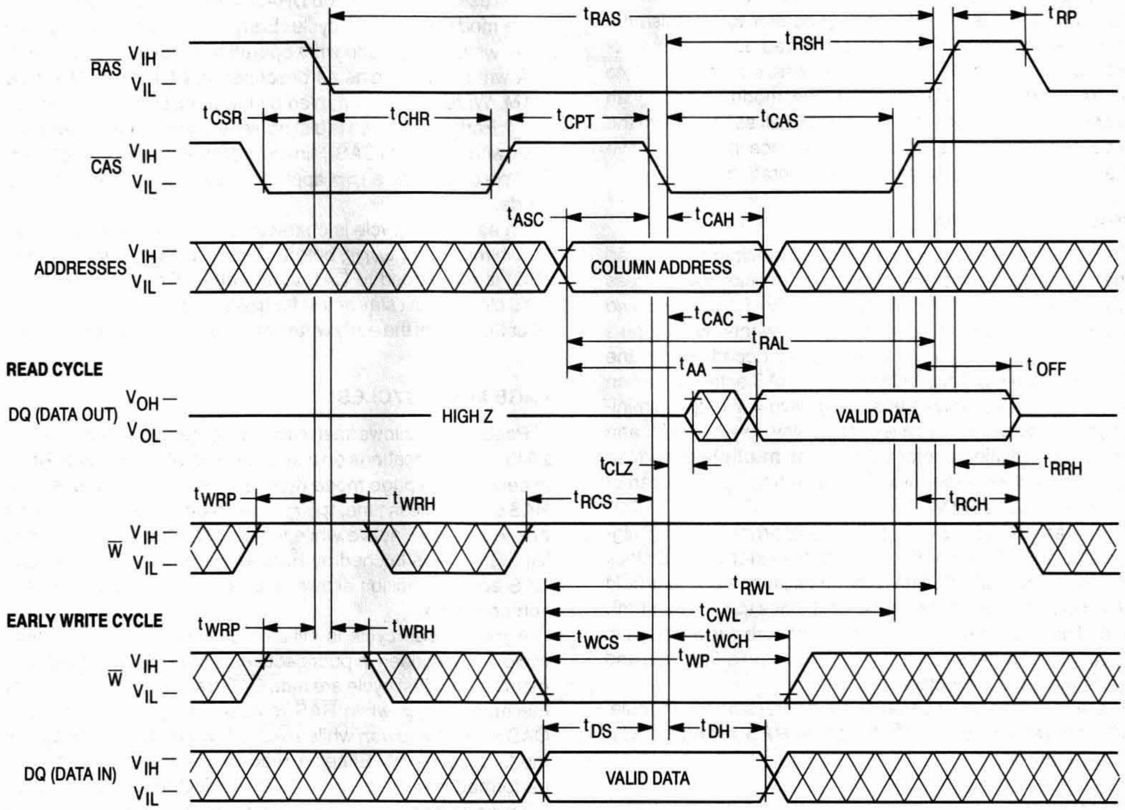
HIDDEN REFRESH CYCLE (READ)


t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$ V_{IH} —
V_{IL} —
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CP}
$\overline{CAS}$ V_{IH} —
V_{IL} —
t_{RAD}
t_{RAL}
t_{ASR}
t_{CAH}
t_{RAH}
t_{ASC}
ADDRESSES V_{IH} —
V_{IL} —
ROW ADDRESS
COLUMN ADDRESS
t_{RCS}
t_{RRH}
t_{WRP}
t_{WRH}
$\overline{W}$ V_{IH} —
V_{IL} —
t_{CAC}
t_{AA}
t_{OFF}
t_{RAC}
DQ (DATA OUT) V_{OH} —
V_{OL} —
VALID DATA
t_{CLZ}

HIDDEN REFRESH CYCLE (EARLY WRITE)


t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$ V_{IH} —
V_{IL} —
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CP}
$\overline{CAS}$ V_{IH} —
V_{IL} —
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES V_{IH} —
V_{IL} —
ROW ADDRESS
COLUMN ADDRESS
t_{RWL}
t_{WRP}
t_{WRH}
t_{WCH}
t_{WCS}
$\overline{W}$ V_{IH} —
V_{IL} —
t_{WP}
t_{DS}
t_{DH}
DQ (DATA IN) V_{IH} —
V_{IL} —
VALID DATA

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



t_{RAS}
t_{RP}
t_{RSH}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CSR}
t_{CHR}
t_{CPT}
t_{CAS}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{ASC}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
COLUMN ADDRESS
t_{CAC}
t_{RAL}
t_{AA}
t_{OFF}
READ CYCLE
DQ (DATA OUT)
V_{OH}
V_{OL}
HIGH Z
VALID DATA
t_{CLZ}
t_{RRH}
t_{WRP}
t_{WRH}
t_{RCS}
t_{RCH}
$\overline{\text{W}}$
V_{IH}
V_{IL}
t_{RWL}
t_{CWL}
EARLY WRITE CYCLE
t_{WRP}
t_{WRH}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{\text{W}}$
V_{IH}
V_{IL}
t_{DS}
t_{DH}
DQ (DATA IN)
V_{IH}
V_{IL}
VALID DATA

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 11-bit address fields. A total of twenty-two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 word locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the module: **$\overline{\text{RAS}}$ only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**.

READ CYCLE

The DRAM may be read with either a "normal" random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window; however, $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ clock active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with either an early write or page mode early write cycle. Early write mode is discussed here, while page mode write operation is covered elsewhere.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early write mode is distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (DQ) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum of t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM94000 require refresh every 16 milliseconds, while refresh time for the MCM9L4000 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM94000, and 124.8 microseconds for the MCM9L4000. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM94000 and 128 milliseconds on the MCM9L4000.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle.

The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{\text{RAS}}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode cycle) as in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read cycle.** Repeat this operation 1024 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, write cycle.** Repeat this operation 1024 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

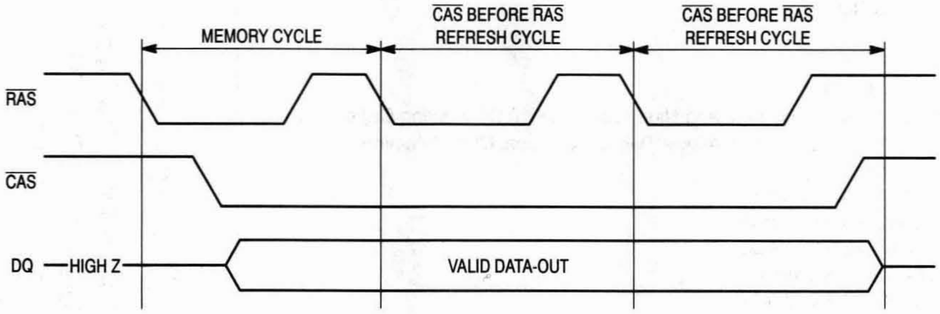


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 94000 / 9L4000 / 94030 X XX

Motorola Memory Prefix — MCM
Part Number — 94000, 9L4000, 94030
Package (AS = SIMM, ASG = Gold SIMM, L = SIP, LH = Low Height SIP, ASC = Industrial Temperature SIMM) — X
Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers —			
MCM94000AS60	MCM94030L60	MCM94000LH60	
MCM94000AS70	MCM94030L70	MCM94000LH70	MCM94000ASC70
MCM94000AS80	MCM94030L80	MCM94000LH80	MCM94000ASC80
MCM9L4000AS60	MCM9L4030L60	MCM9L4000LH60	
MCM9L4000AS70	MCM9L4030L70	MCM9L4000LH70	
MCM9L4000AS80	MCM9L4030L80	MCM9L4000LH80	

NOTE: Contact your Motorola representative for further information on Industrial Temperature Module products.

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM91600
MCM9L1600

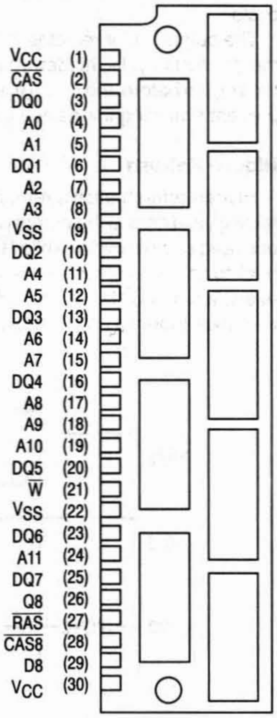
Product Preview

16M x 9 Bit Dynamic Random Access Memory Module

The MCM91600 is a 36M dynamic random access memory (DRAM) module organized as 16,777,218 x 8 bits. The module is a 30-lead single-in-line memory module (SIMM) consisting of nine MCM517400 DRAMs housed in 400 mil J-lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM517400 is a CMOS high-speed dynamic random access memory organized as 16,777,216 one-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh:
  MCM91600 = 32 ms
- Consists of Nine 16M x 1 DRAMs and Nine 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM91600-60 = 60 ns (Max)
  MCM91600-70 = 70 ns (Max)
  MCM91600-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM91600-60 = 5.94 W (Max)
  MCM91600-70 = 4.95 W (Max)
  MCM91600-80 = 4.21 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 99 mW (Max)
  CMOS Levels = 50 mW (Max)
- $\overline{CAS}$ Control for Eight Common I/O Lines
- $\overline{CAS}$ Control for Separate I/O Pair

TOP VIEW

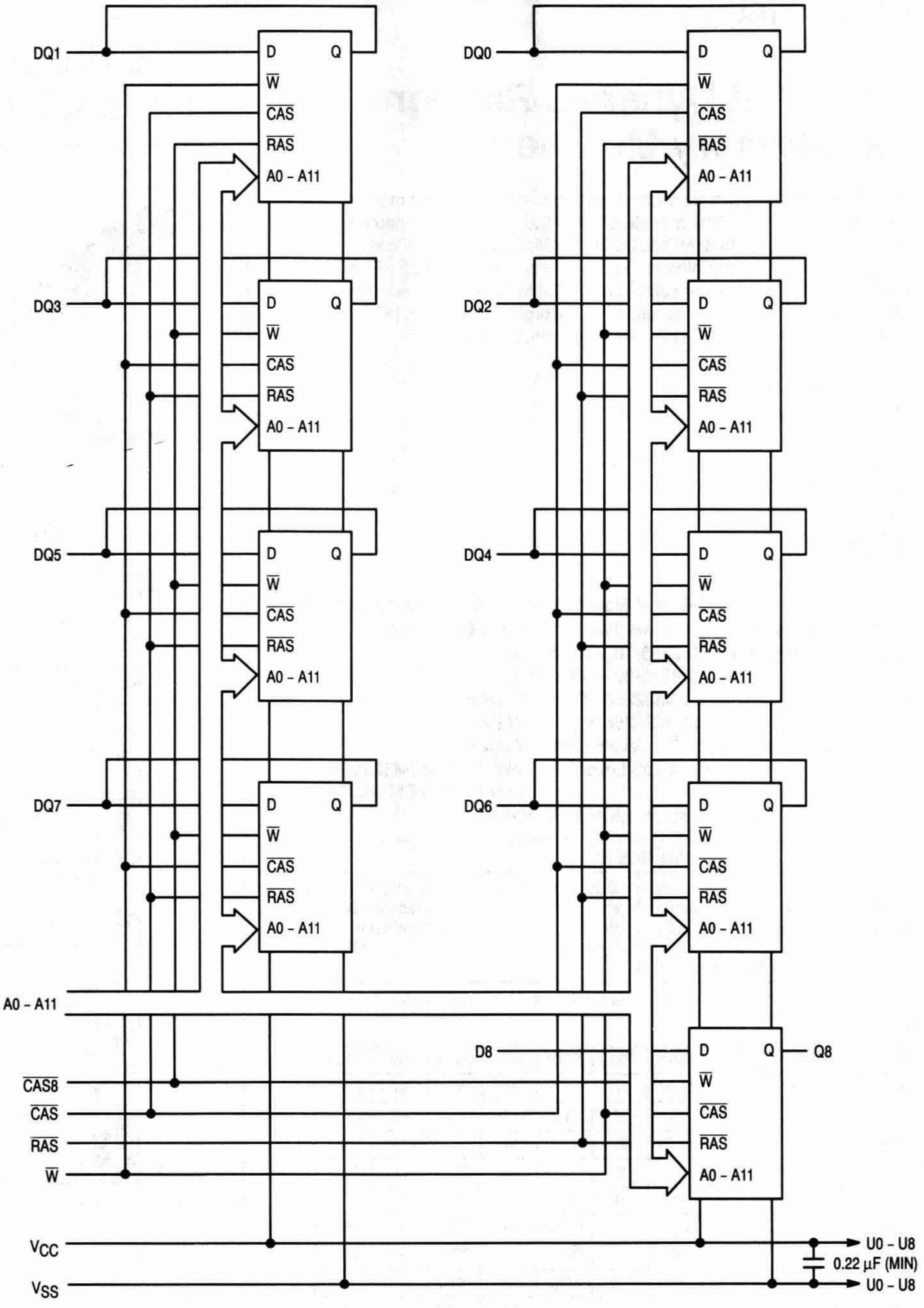


PIN NAMES

A0 – A11	Address Inputs
DQ0 – DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
$\overline{CAS}$, $\overline{CAS8}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

16M x 9 BLOCK DIAGRAM


DQ1
DQ0
DQ3
DQ2
DQ5
DQ4
DQ7
DQ6
D
Q
$\overline{W}$
$\overline{CAS}$
$\overline{RAS}$
A0 - A11
A0 - A11
D8
Q8
$\overline{CAS8}$
$\overline{CAS}$
$\overline{RAS}$
$\overline{W}$
V_{CC}
V_{SS}
U0 - U8
0.22 μF (MIN)
U0 - U8

NOTE: For mechanical data, please see Chapter 10.

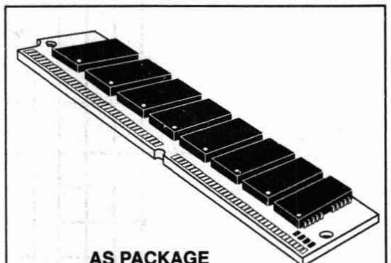
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM32256
MCM32L256

256K x 32 Bit Dynamic Random Access Memory Module

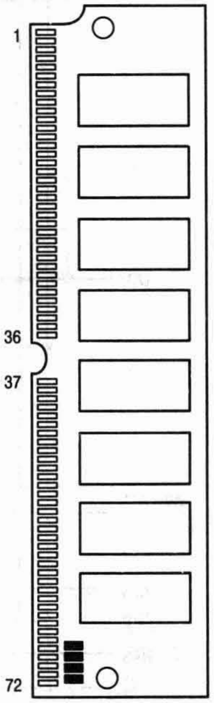
The MCM32256 is an 8M dynamic random access memory (DRAM) module organized as 262,144 x 32 bits. The module is a 72-lead single-in-line memory module (SIMM) consisting of eight MCM514256A DRAMs housed in 20/26 J-lead small outline packages (SOJ) mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM514256A is a 1.0µ CMOS high-speed dynamic random access memory organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM32256 = 8 ms (Max)
  MCM32L256 = 64 ms (Max)
- Consists of Eight 256K x 4 DRAMs and Eight 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM32256-70 = 70 ns (Max)
  MCM32256-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM32256-70 = 3.6 W (Max)
  MCM32256-80 = 3.1 W (Max)
- Low Standby Power Dissipation: TTL Levels = 88 mW (Max)
  CMOS Levels = 44 mW (Max, MCM32256)
  = 8.8 mW (Max, MCM32L256)
- Available in 60 ns Access Time (t_{RAC}): MCM32B256AS60



AS PACKAGE
SIMM MODULE
CASE 866-01

TOP VIEW



PIN NAMES

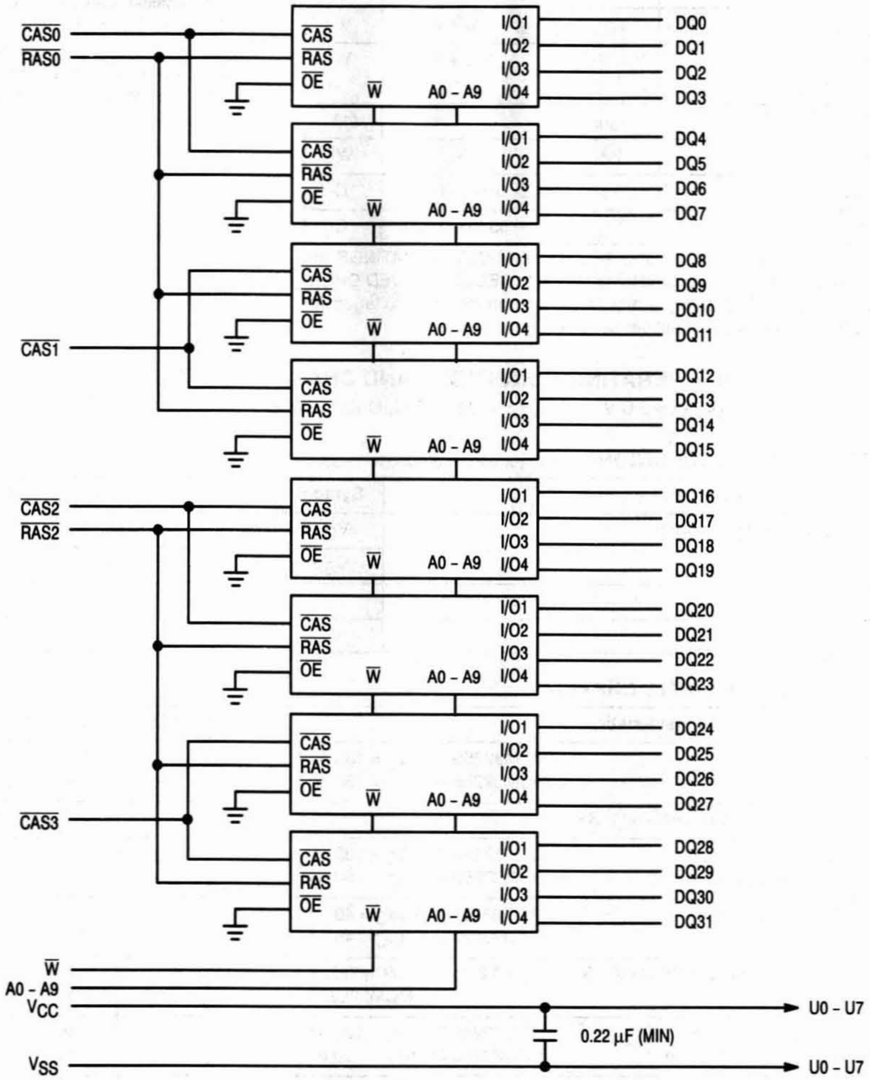
A0 – A8	Address Inputs	DQ0 – DQ31	Data Input/Output
$\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$	Column Address Strobe	PD1 – PD4	Presence Detect
$\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$	Row Address Strobe	$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)	V_{SS}	Ground
NC	No Connection		

All power supply and ground pins must be connected for proper operation of the device.

PIN OUT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{\text{CAS2}}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{\text{CAS3}}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{\text{CAS1}}$	55	DQ11	67	PD1
8	DQ3	20	DQ4	32	NC	44	$\overline{\text{RAS0}}$	56	DQ27	68	PD2
9	DQ19	21	DQ20	33	NC	45	NC	57	DQ12	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{\text{RAS2}}$	46	NC	58	DQ28	70	PD4
11	NC	23	DQ21	35	NC	47	$\overline{\text{W}}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

BLOCK DIAGRAM



CAS0
RAS0
CAS1
CAS2
RAS2
CAS3
CAS
RAS
OE
W
A0 – A9
I/O1
I/O2
I/O3
I/O4
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
W
A0 – A9
VCC
VSS
0.22 µF (MIN)
U0 – U7
U0 – U7

5

PRESENCE DETECT PIN OUT		
Pin Name	**70 ns**	**80 ns**
PD1	V_{SS}	V_{SS}
PD2	NC	NC
PD3	V_{SS}	NC
PD4	NC	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	4.8	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM32256-70, t_{RC} = 130 ns MCM32256-80, t_{RC} = 150 ns	I_{CC1}	— —	640 560	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	16	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles MCM32256-70, t_{RC} = 130 ns MCM32256-80, t_{RC} = 150 ns	I_{CC3}	— —	640 560	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM32256-70, t_{PC} = 40 ns MCM32256-80, t_{PC} = 45 ns	I_{CC4}	— —	480 400	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM32256 MCM32L256	I_{CC5}	— —	8 1.6	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM32256-70, t_{RC} = 130 ns MCM32256-80, t_{RC} = 150 ns	I_{CC6}	— —	640 560	mA	1
V_{CC} Power Supply Current Battery Backup Mode (t_{RC} = 125 µs; $\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$, DQ, A0 – A8 = V_{CC} – 0.2 V or 0.2 V) t_{RAS} = 1 µs MCM32L256 only	I_{CC7}	—	2.4	mA	3
Input Leakage Current ($V_{SS} \leq V_{in} \leq V_{CC}$)	$I_{lkg(I)}$	– 80	+ 80	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \leq V_{out} \leq V_{CC}$)	$I_{lkg(O)}$	– 10	+ 10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.
3. t_{RAS} (max) = 1 µs is applied to refresh of battery backup. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit
Input Capacitance (A0 – A8)	C_{I1}	—	50	pF
Input Capacitance ($\overline{W}$)	C_{I2}	—	66	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I3}	—	38	pF
Input Capacitance ($\overline{CAS0}$ – $\overline{CAS3}$)	C_{I4}	—	24	pF
I/O Capacitance (DQ0 – DQ31)	C_{DQ}	—	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\ \Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM32256-70 MCM32L256-70		MCM32256-80 MCM32L256-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	70	—	80	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	

NOTES: (continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

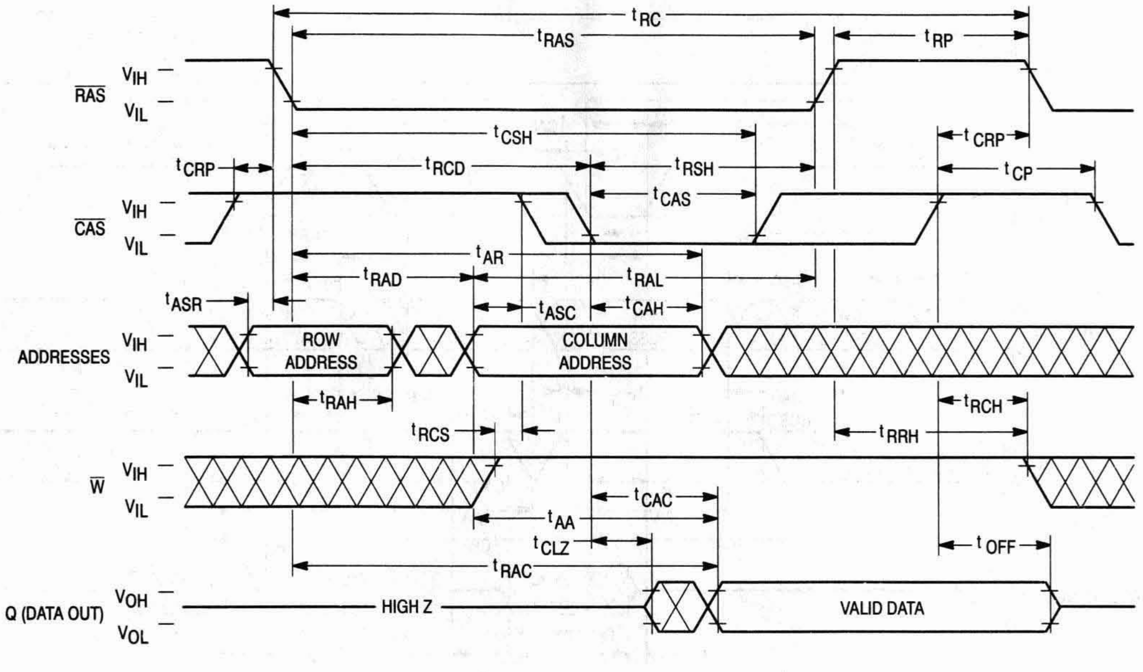
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM32256-70 MCM32L256-70		MCM32256-80 MCM32L256-80			
	Standard	Alternate	Min	Max	Min	Max	Unit	Notes
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	—	60	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	—	15	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	—	60	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	—	60	—	ns	
Refresh Period MCM32256 MCM32L256	t_{RVRV}	t_{RFSH}	— —	8 64	— —	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	ns	

NOTES:

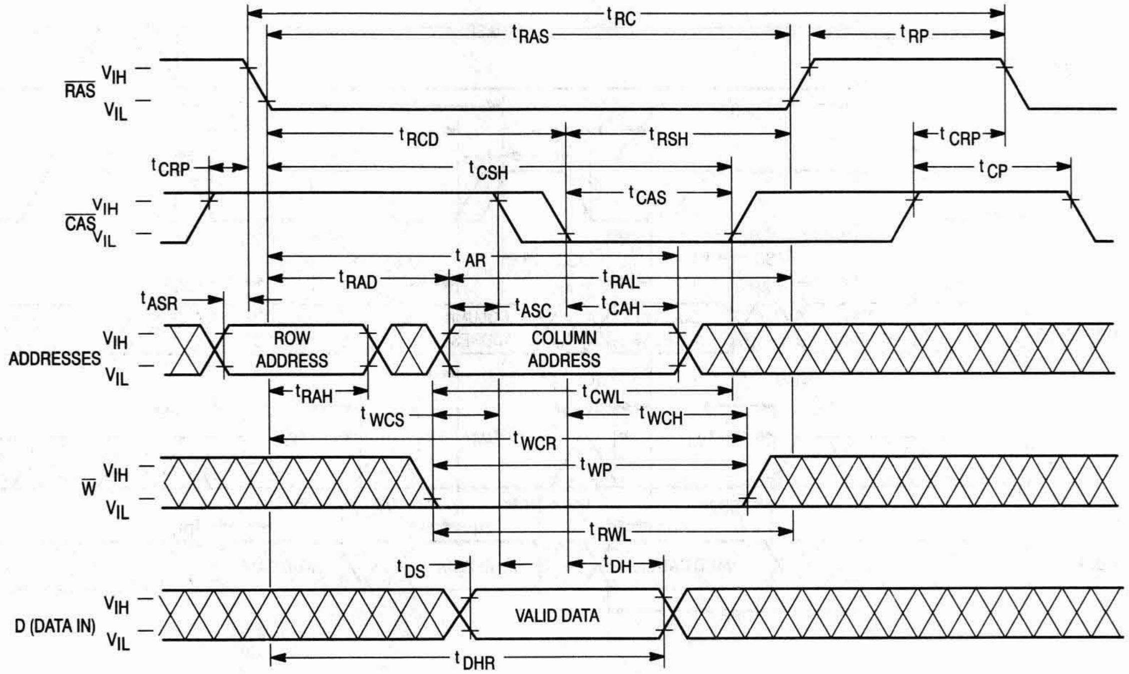
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.

READ CYCLE



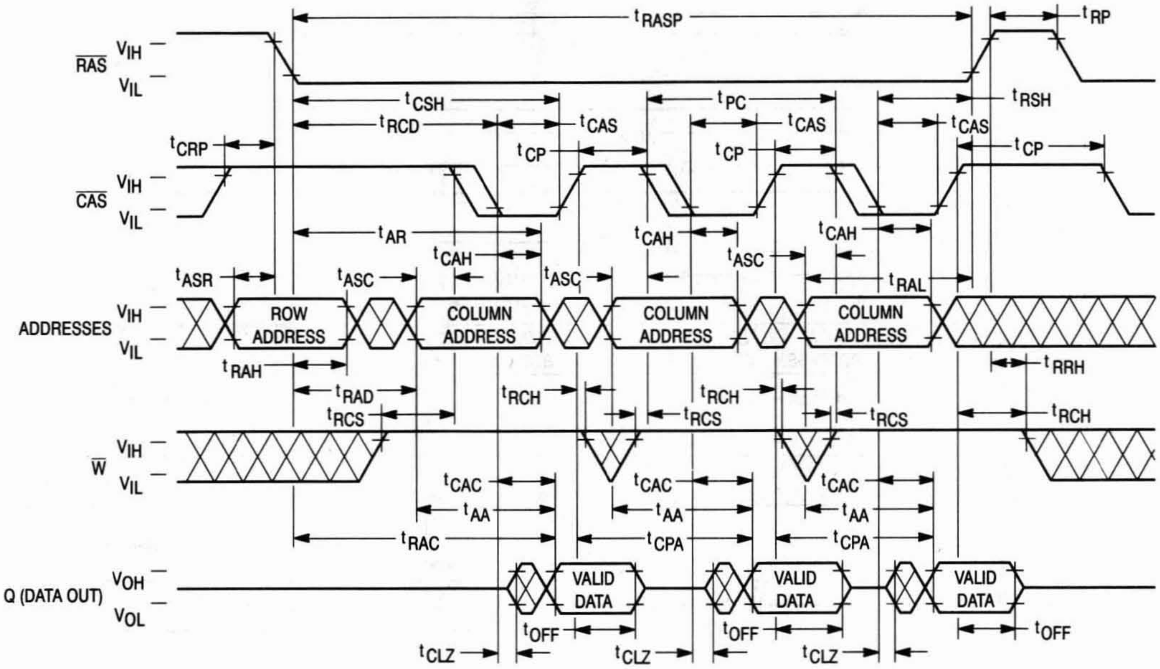
tRC
tRAS
tRP
RAS VIH VIL
tCSH
tCRP
tRCD
tRSH
tCP
tCAS
CAS VIH VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W VIH VIL
tCAC
tAA
tCLZ
tOFF
tRAC
Q (DATA OUT) VOH VOL
HIGH Z
VALID DATA

EARLY WRITE CYCLE

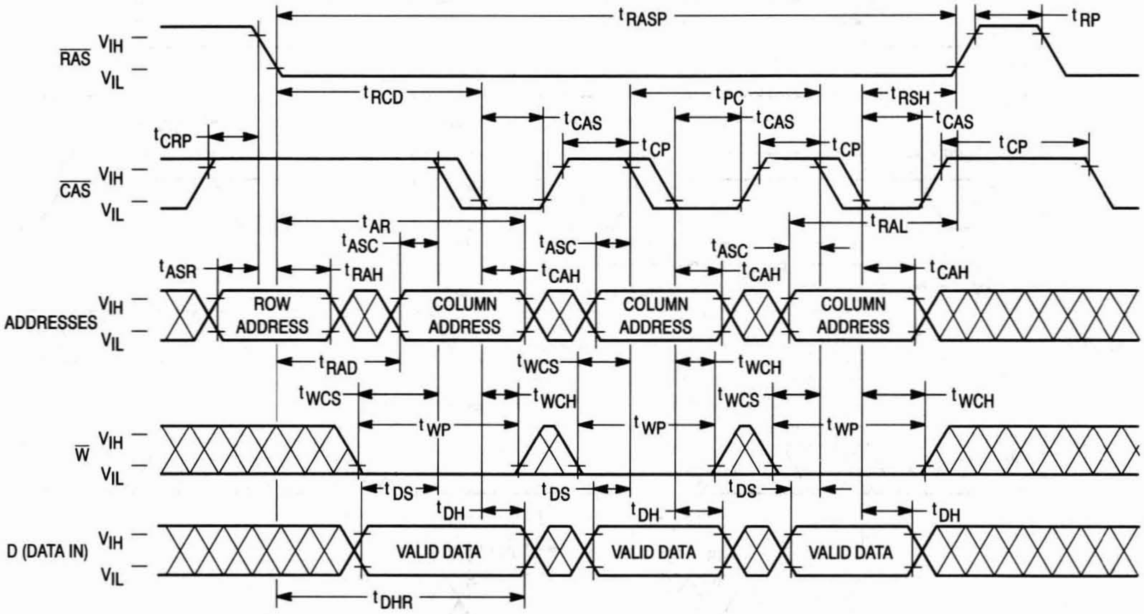


tRC
tRAS
tRP
RAS VIH VIL
tRCD
tRSH
tCRP
tCSH
tCP
tCAS
CAS VIH VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWCR
tWP
W VIH VIL
tRWL
tDS
tDH
D (DATA IN) VIH VIL
VALID DATA
tDHR

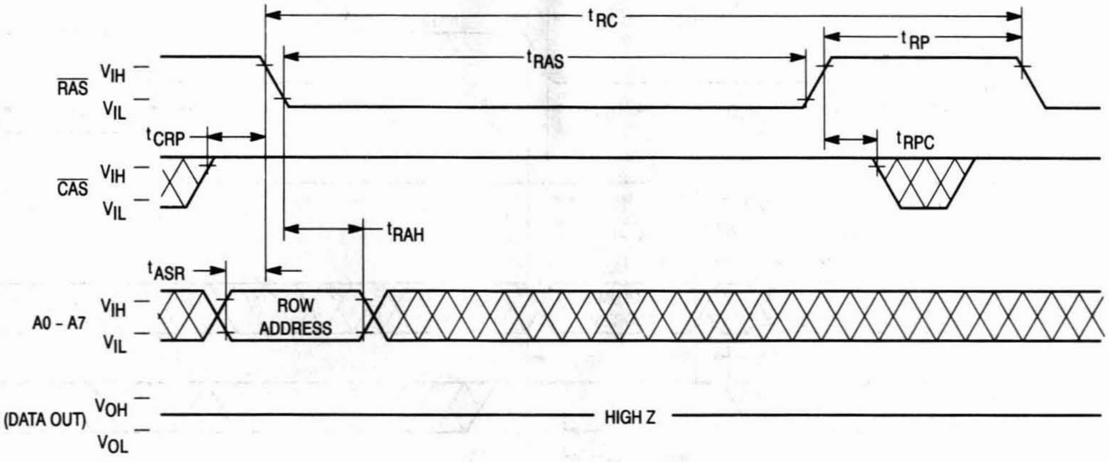
FAST PAGE MODE READ CYCLE


tRASP
tRP
RAS
VIH
VIL
tCSH
tPC
tRSH
tRCD
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCP
CAS
VIH
VIL
tAR
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
tRAL
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAH
tRRH
tRAD
tRCH
tRCH
tRCH
tRCS
tRCS
tRCS
W
VIH
VIL
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
Q (DATA OUT)
VOH
VOL
VALID DATA
VALID DATA
VALID DATA
tOFF
tOFF
tOFF
tCLZ
tCLZ
tCLZ

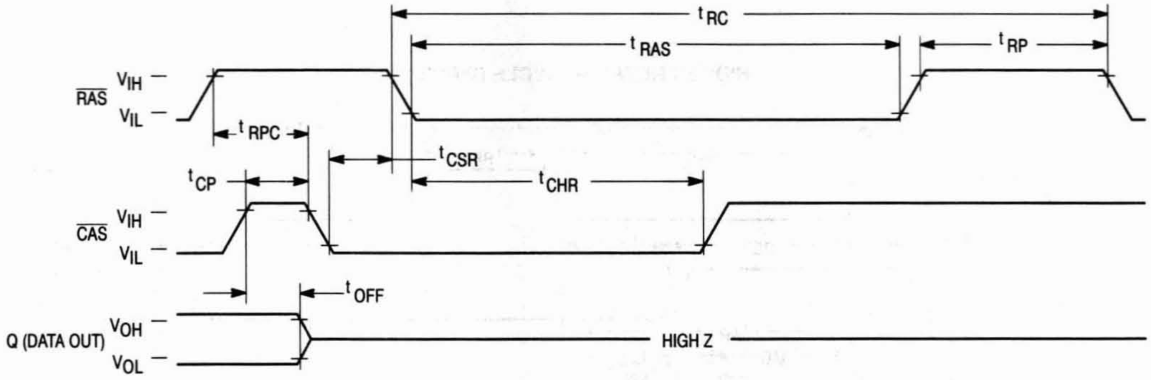
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)


tRASP
tRP
RAS
VIH
VIL
tRCD
tPC
tRSH
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCP
CAS
VIH
VIL
tAR
tRAL
tASC
tASC
tASC
tASR
tRAH
tCAH
tCAH
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tWCS
tWCS
tWCS
tWCH
tWCH
tWCH
tWP
tWP
tWP
W
VIH
VIL
tDS
tDS
tDS
tDH
tDH
tDH
D (DATA IN)
VIH
VIL
VALID DATA
VALID DATA
VALID DATA
tDHR

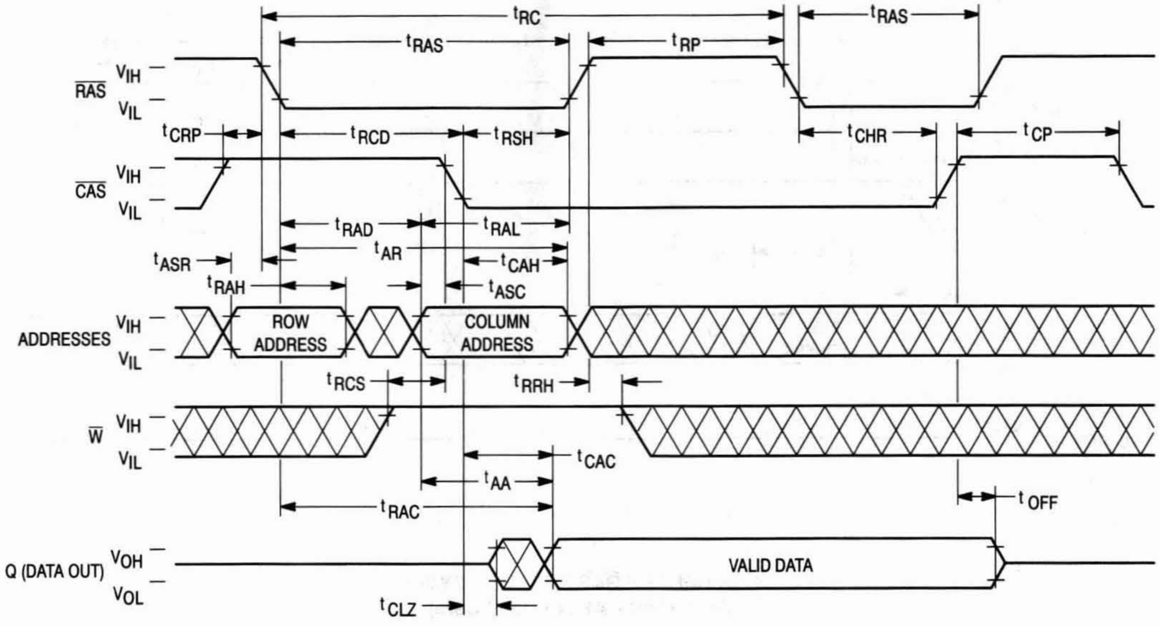
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
($\overline{\text{W}}$ and A8 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
A0 - A7
V_{IH}
V_{IL}
ROW ADDRESS
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

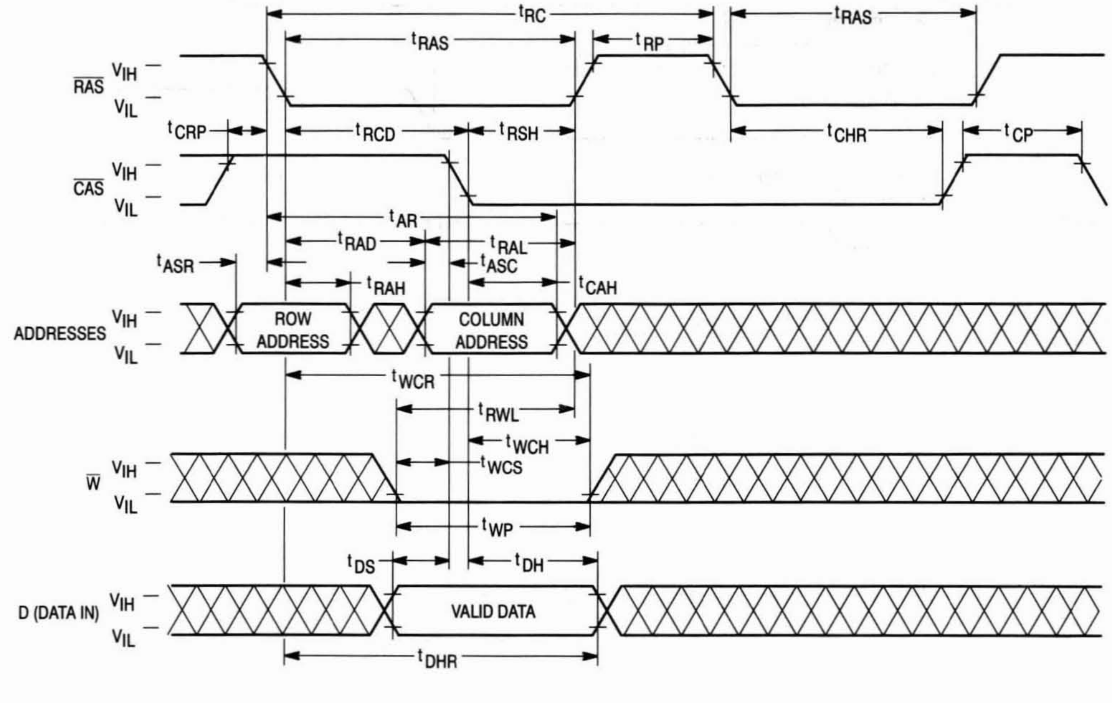
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
($\overline{\text{W}}$ and A0 – A8 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RPC}
t_{CSR}
t_{CP}
t_{CHR}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{OFF}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

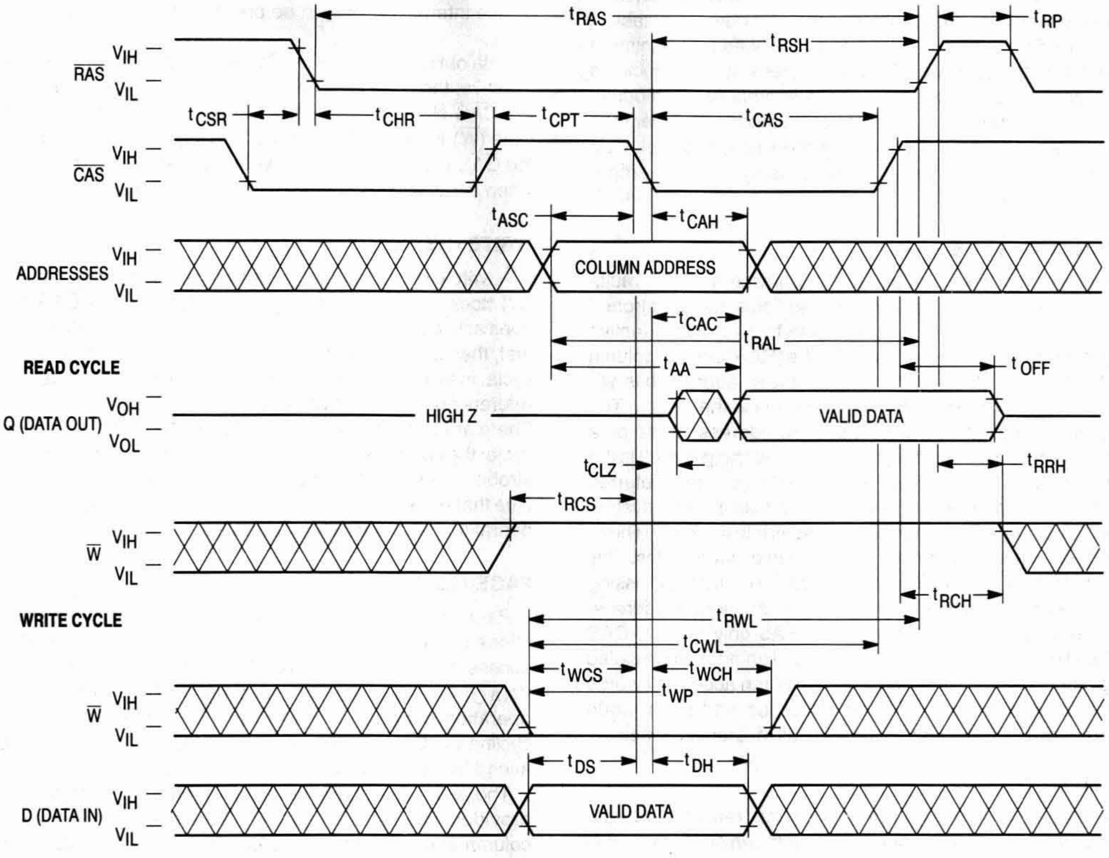
HIDDEN REFRESH CYCLE (READ)


tRC
tRAS
tRP
tRAS
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCP
CAS
VIH
VIL
tRAD
tRAL
tAR
tASR
tCAH
tRAH
tASC
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRCS
tRRH
W
VIH
VIL
tCAC
tAA
tRAC
tOFF
Q (DATA OUT)
VOH
VOL
VALID DATA
tCLZ

HIDDEN REFRESH CYCLE (WRITE)


tRC
tRAS
tRP
tRAS
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCP
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tWCR
tRWL
tWCH
tWCS
W
VIH
VIL
tWP
tDS
tDH
D (DATA IN)
VIH
VIL
VALID DATA
tDHR

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



t_{RAS}
t_{RP}
t_{RSH}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CSR}
t_{CHR}
t_{CPT}
t_{CAS}
$\overline{\text{CAS}}$
t_{ASC}
t_{CAH}
ADDRESSES
COLUMN ADDRESS
t_{CAC}
t_{RAL}
READ CYCLE
t_{AA}
t_{OFF}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z
VALID DATA
t_{CLZ}
t_{RRH}
t_{RCS}
$\overline{\text{W}}$
t_{RCH}
WRITE CYCLE
t_{RWL}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
t_{DS}
t_{DH}
D (DATA IN)
VALID DATA

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the module. During an extended inactive state of the module (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to ensure proper device operation.

ADDRESSING THE RAM

The nine address bus pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of eighteen address bits will decode one of the 262,144 word locations in the device. The column address strobe follows the row address strobe by a specified minimum and maxium time called t_{RCD}, which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up the external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, other variations in addressing the module: the refresh modes ($\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh), and another mode called page mode which allows the user to column access all words within a selected row. The refresh mode and page mode operations are described in more detail in later sections.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, which is covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from the row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at all 512 column locations on a selected row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 10-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In practice, any combination of read and write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the module needs to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the module will also refresh all the words associated with the particular row(s) decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

This refresh cycle is initiated when $\overline{\text{RAS}}$ falls, after $\overline{\text{CAS}}$ has been low (by t_{CSR}). This activates the internal refresh counter, which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{\text{CAS}}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{\text{CAS}}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period (t_{RP}), executing a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. (See Figure 1.)

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read cycle**. Repeat this operation 512 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, write cycle**. Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

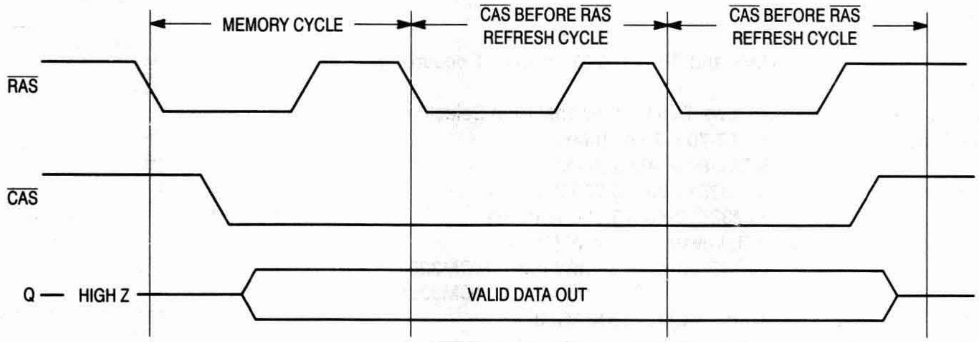


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION

(Order by Full Part Number)

MCM 32256 or 32L256 X XX

Motorola Memory Prefix — MCM
Part Number — 32256 or 32L256
Package (AS = SIMM, ASG = Gold Pad SIMM) — X
Speed (70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers — MCM32256AS70 MCM32256ASG70
MCM32256AS80 MCM32256ASG80

MCM32L256AS70 MCM32L256ASG70
MCM32L256AS80 MCM32L256ASG80

NOTE: Contact your Motorola representative for further information on the 60 ns version of this product.

NOTE: For mechanical data, please see Chapter 10.

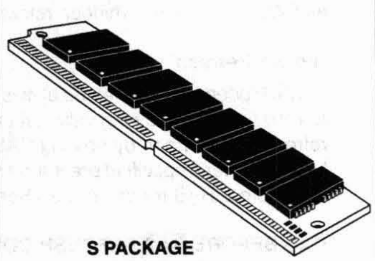
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

512K x 32 Bit Dynamic Random Access Memory Module

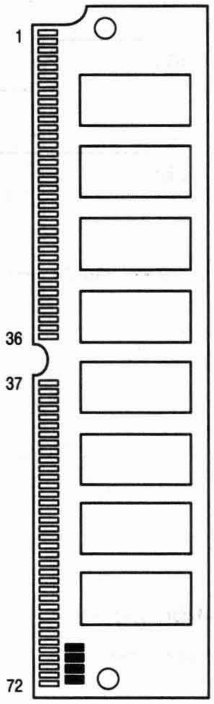
MCM32512
MCM32L512

The MCM32512 is a 16M dynamic random access memory (DRAM) module organized as 524,288 x 32 bits. The module is a 72-lead double-sided single-in-line memory module (SIMM) consisting of sixteen MCM514256A DRAMs housed in 20/26 J-lead small outline packages (SOJ) mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM514256A is a 1.0µ CMOS high-speed dynamic random access memory organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM32512 = 8 ms (Max)
  MCM32L512 = 64 ms (Max)
- Consists of Sixteen 256K x 4 DRAMs and Sixteen 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM32512-70 = 70 ns (Max)
  MCM32512-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM32512-70 = 3.608 W (Max)
  MCM32512-80 = 3.168 W (Max)
- Low Standby Power Dissipation: TTL Levels = 176 mW (Max)
  CMOS Levels = 88 mW (Max, MCM32512)
  = 18 mW (Max, MCM32L512)
- Available in 60 ns Access Time (t_{RAC}): MCM32B512AS60


S PACKAGE
SIMM MODULE
CASE 866-02

TOP VIEW



PIN NAMES

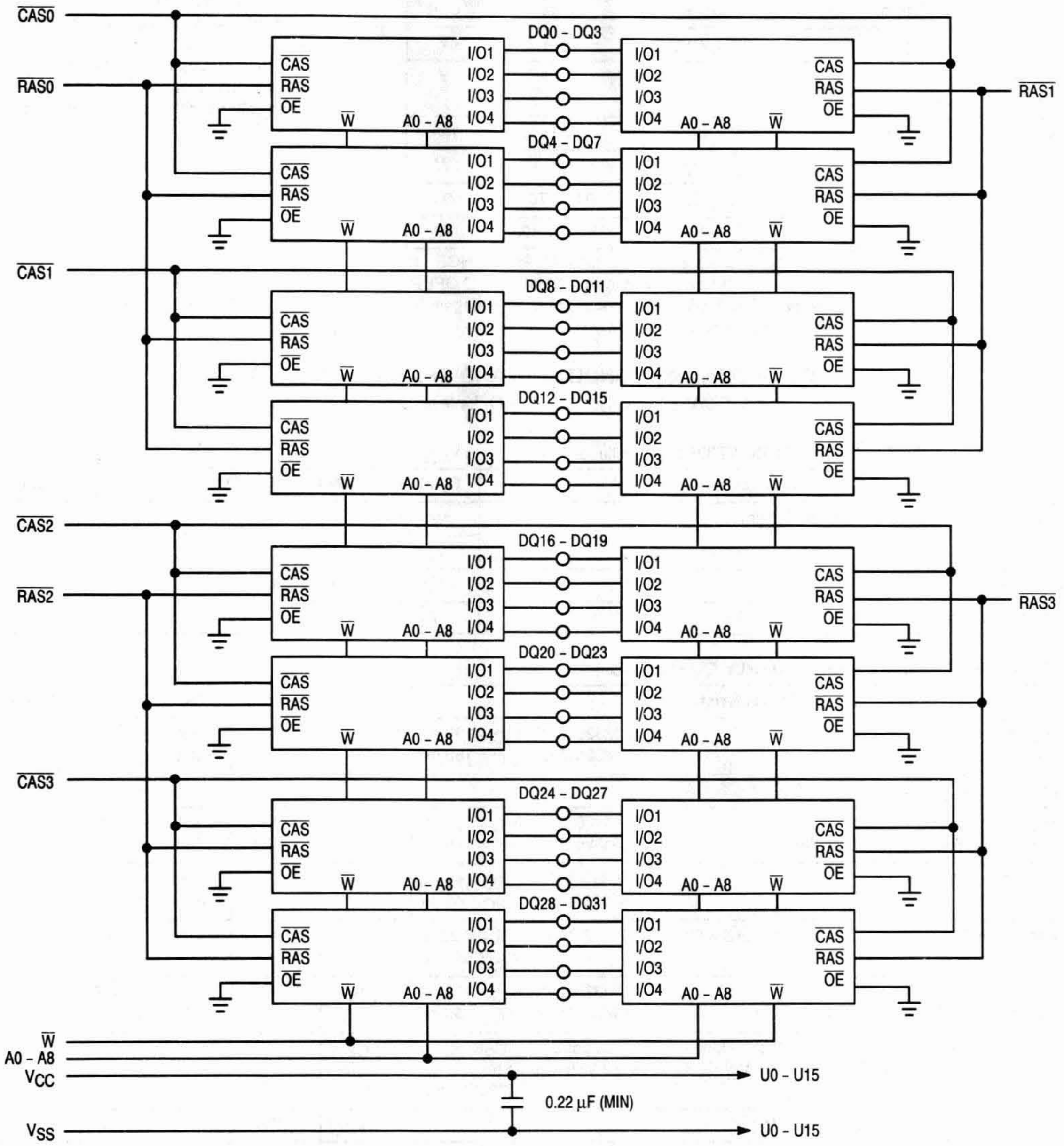
A0 – A8	Address Inputs	DQ0 – DQ31	Data Input/Output
$\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$	Column Address Strobe	PD1 – PD4	Presence Detect
$\overline{\text{RAS0}}$ – $\overline{\text{RAS3}}$	Row Address Strobe	$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)	V_{SS}	Ground
NC	No Connection		

All power supply and ground pins must be connected for proper operation of the device.

PIN OUT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{\text{CAS2}}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{\text{CAS3}}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{\text{CAS1}}$	55	DQ11	67	PD1
8	DQ3	20	DQ4	32	NC	44	$\overline{\text{RAS0}}$	56	DQ27	68	PD2
9	DQ19	21	DQ20	33	$\overline{\text{RAS3}}$	45	$\overline{\text{RAS1}}$	57	DQ12	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{\text{RAS2}}$	46	NC	58	DQ28	70	PD4
11	NC	23	DQ21	35	NC	47	$\overline{\text{W}}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

BLOCK DIAGRAM


CAS0
RAS0
CAS1
CAS2
RAS2
CAS3
RAS1
RAS3
DQ0 - DQ3
DQ4 - DQ7
DQ8 - DQ11
DQ12 - DQ15
DQ16 - DQ19
DQ20 - DQ23
DQ24 - DQ27
DQ28 - DQ31
CAS
RAS
OE
W
A0 - A8
I/O1
I/O2
I/O3
I/O4
W
A0 - A8
VCC
VSS
0.22 µF (MIN)
U0 - U15
U0 - U15

PRESENCE DETECT PIN OUT		
Pin Name	**70 ns**	**80 ns**
PD1	NC	NC
PD2	V_{SS}	V_{SS}
PD3	V_{SS}	NC
PD4	NC	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	4.92	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM32512-70, t_{RC} = 130 ns MCM32512-80, t_{RC} = 150 ns	I_{CC1}	— —	656 576	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	32	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles MCM32512-70, t_{RC} = 130 ns MCM32512-80, t_{RC} = 150 ns	I_{CC3}	— —	656 576	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM32512-70, t_{PC} = 40 ns MCM32512-80, t_{PC} = 45 ns	I_{CC4}	— —	496 416	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM32512 MCM32L512	I_{CC5}	— —	16 3.2	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM32512-70, t_{RC} = 130 ns MCM32512-80, t_{RC} = 150 ns	I_{CC6}	— —	656 576	mA	1
V_{CC} Power Supply Current Battery Backup Mode (t_{RC} = 125 µs; $\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$, DQ, A0 – A8 = V_{CC} – 0.2 V or 0.2 V) t_{RAS} = 1 µs MCM32L512 only	I_{CC7}	—	4.8	mA	3
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 160	160	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.
3. t_{RAS} (max) = 1 µs is applied to refresh of battery backup. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit
Input Capacitance (A0 – A8)	C_{I1}	—	90	pF
Input Capacitance ($\overline{W}$)	C_{I2}	—	122	pF
Input Capacitance ($\overline{RAS0}$ – $\overline{RAS3}$)	C_{I3}	—	38	pF
Input Capacitance ($\overline{CAS0}$ – $\overline{CAS3}$)	C_{I4}	—	38	pF
I/O Capacitance (DQ0 – DQ31)	C_{DQ}	—	24	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\ \Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM32512-70 MCM32L512-70		MCM32512-80 MCM32L512-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	70	—	80	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
$\overline{CAS}$ Hold TIme	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	ns	12

NOTES: (continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

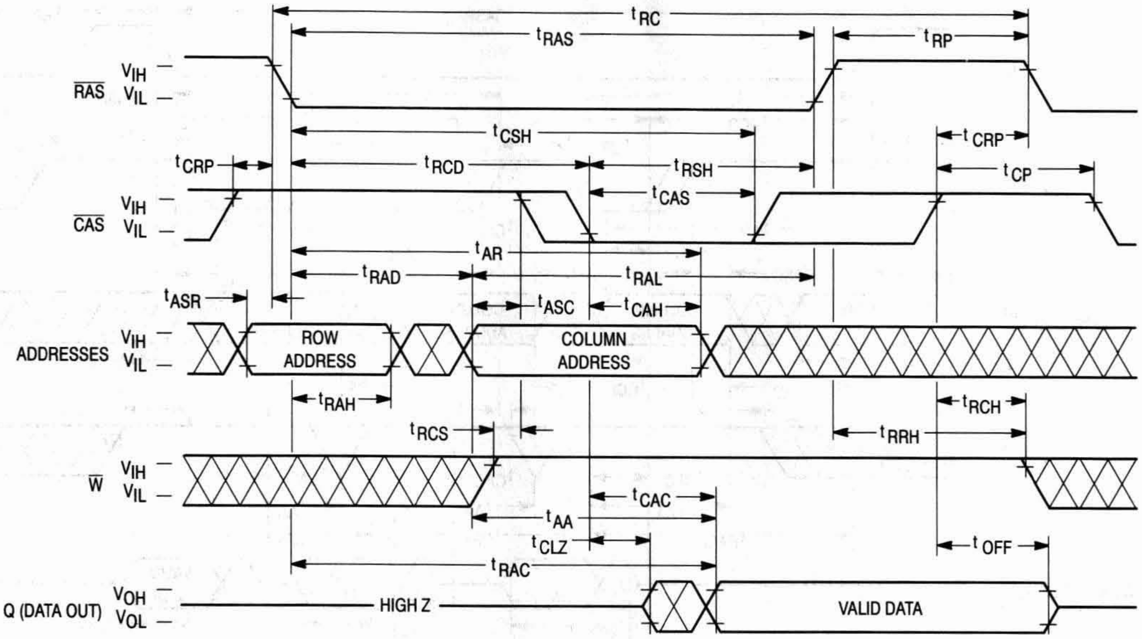
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM32512-70 MCM32L512-70		MCM32512-80 MCM32L512-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
CAS to RAS Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
CAS Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address Hold Time Referenced to RAS	t_{RELAX}	t_{AR}	55	—	60	—	ns	
Column Address to RAS Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to CAS	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to RAS	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to CAS	t_{CELWH}	t_{WCH}	15	—	15	—	ns	
Write Command Hold Time Referenced to RAS	t_{RELWH}	t_{WCR}	55	—	60	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to RAS Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to CAS Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14
Data in Hold Time Referenced to RAS	t_{RELDX}	t_{DHR}	55	—	60	—	ns	
Refresh Period MCM32512 MCM32L512	t_{RVRV}	t_{RFSH}	— —	8 64	— —	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
CAS Setup Time for CAS Before RAS Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
CAS Hold Time for CAS Before RAS Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	ns	
CAS Precharge to CAS Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
CAS Precharge Time for CAS Before RAS Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	ns	
CAS Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	ns	

NOTES:

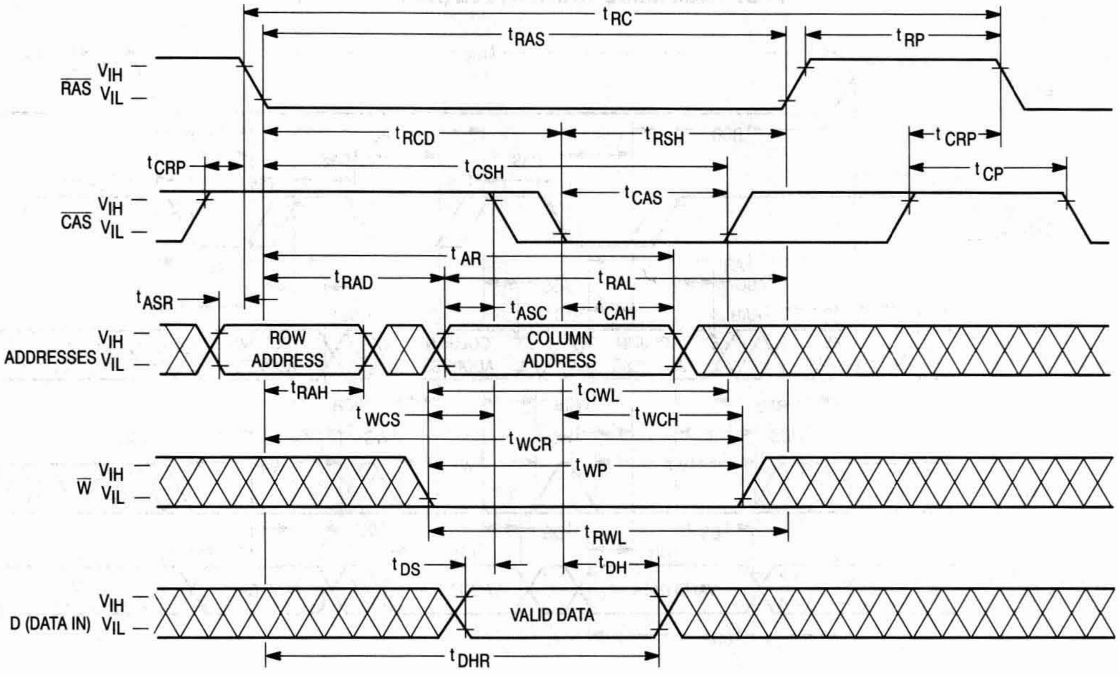
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to CAS leading edge in random write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.
16. To avoid bus contention and potential damage to the module, RAS0 and RAS1 may not be active low simultaneously. Similarly, RAS2 and RAS3 may not be simultaneously active low.

READ CYCLE



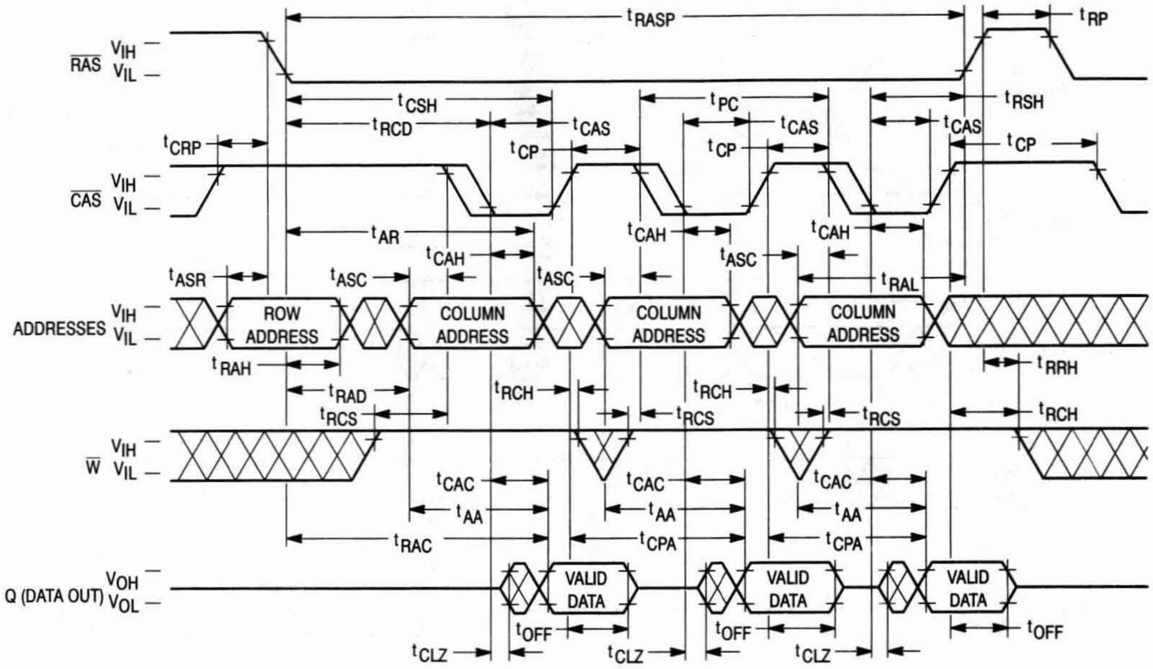
tRC
tRAS
tRP
RAS VIH VIL
tCSH
tCRP
tRCD
tRSH
tCP
tCAS
CAS VIH VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W VIH VIL
tCAC
tAA
tCLZ
tOFF
tRAC
Q (DATA OUT) VOH VOL
HIGH Z
VALID DATA

EARLY WRITE CYCLE



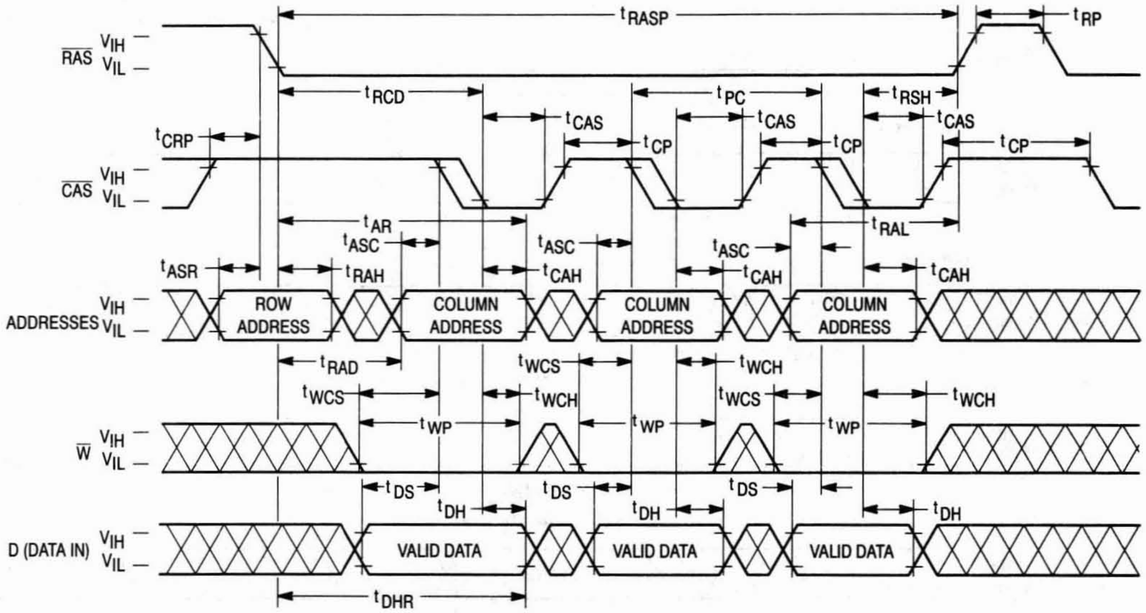
tRC
tRAS
tRP
RAS VIH VIL
tRCD
tRSH
tCRP
tCSH
tCP
tCAS
CAS VIH VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWCR
tWP
W VIH VIL
tRWL
tDS
tDH
D (DATA IN) VIH VIL
VALID DATA
tDHR

FAST PAGE MODE READ CYCLE



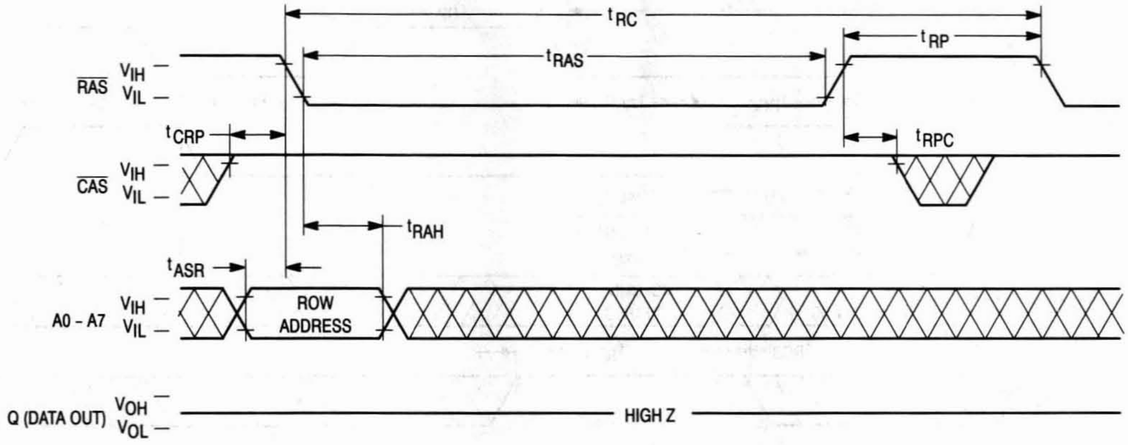
tRASP
tRP
RAS VIH VIL
tCSH
tPC
tRSH
tRCD
tCAS
tCRP
tCP
CAS VIH VIL
tAR
tCAH
tASC
tASR
tRAL
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRRH
tRAD
tRCH
tRCS
W VIH VIL
tCAC
tAA
tRAC
tCPA
Q (DATA OUT) VOH VOL
VALID DATA
tOFF
tCLZ

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

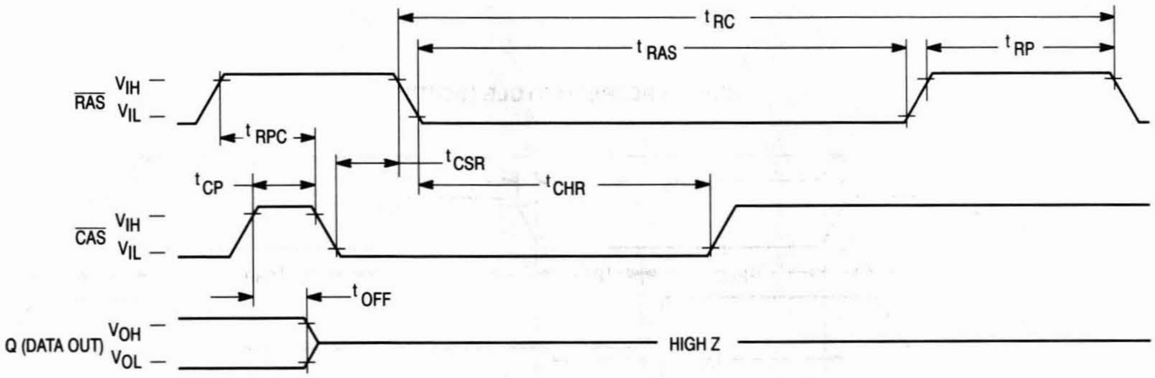


tRASP
tRP
RAS VIH VIL
tRCD
tPC
tRSH
tCAS
tCRP
tCP
CAS VIH VIL
tAR
tASC
tRAL
tASR
tRAH
tCAH
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
tRAD
tWCS
tWCH
tWP
W VIH VIL
tDS
tDH
D (DATA IN) VIH VIL
VALID DATA
tDHR

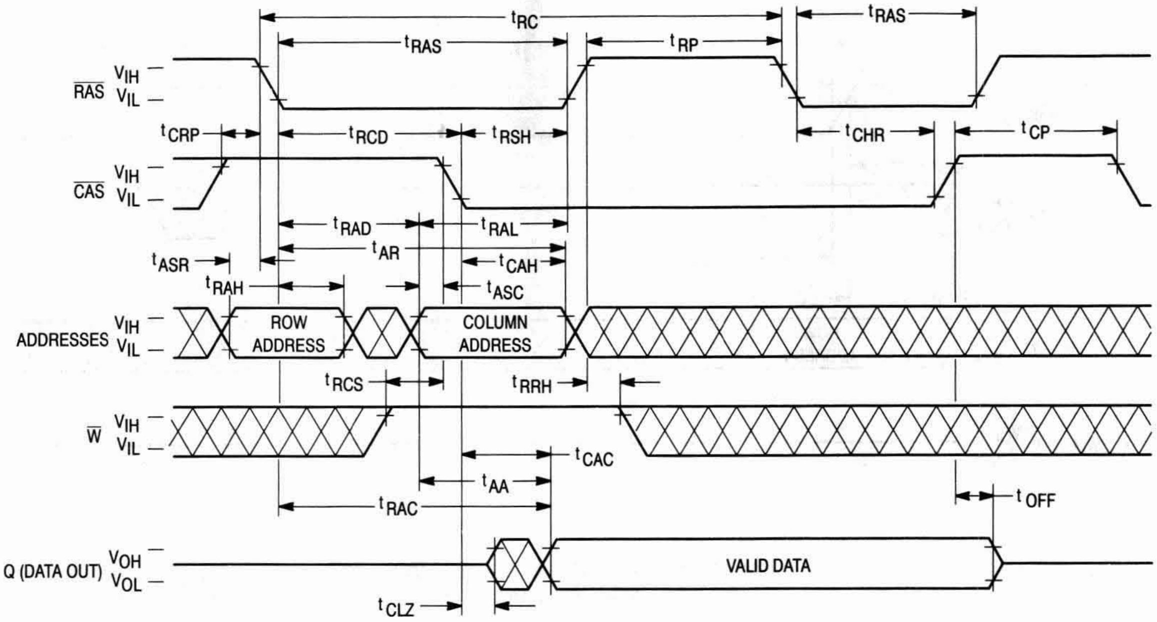
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
($\overline{\text{W}}$ and A8 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$ V_{IH} V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$ V_{IH} V_{IL}
t_{RAH}
t_{ASR}
A0 - A7 V_{IH} V_{IL}
ROW ADDRESS
Q (DATA OUT) V_{OH} V_{OL}
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
($\overline{\text{W}}$ and A0 – A8 are Don't Care)


t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$ V_{IH} V_{IL}
t_{RPC}
t_{CSR}
t_{CP}
t_{CHR}
$\overline{\text{CAS}}$ V_{IH} V_{IL}
t_{OFF}
Q (DATA OUT) V_{OH} V_{OL}
HIGH Z

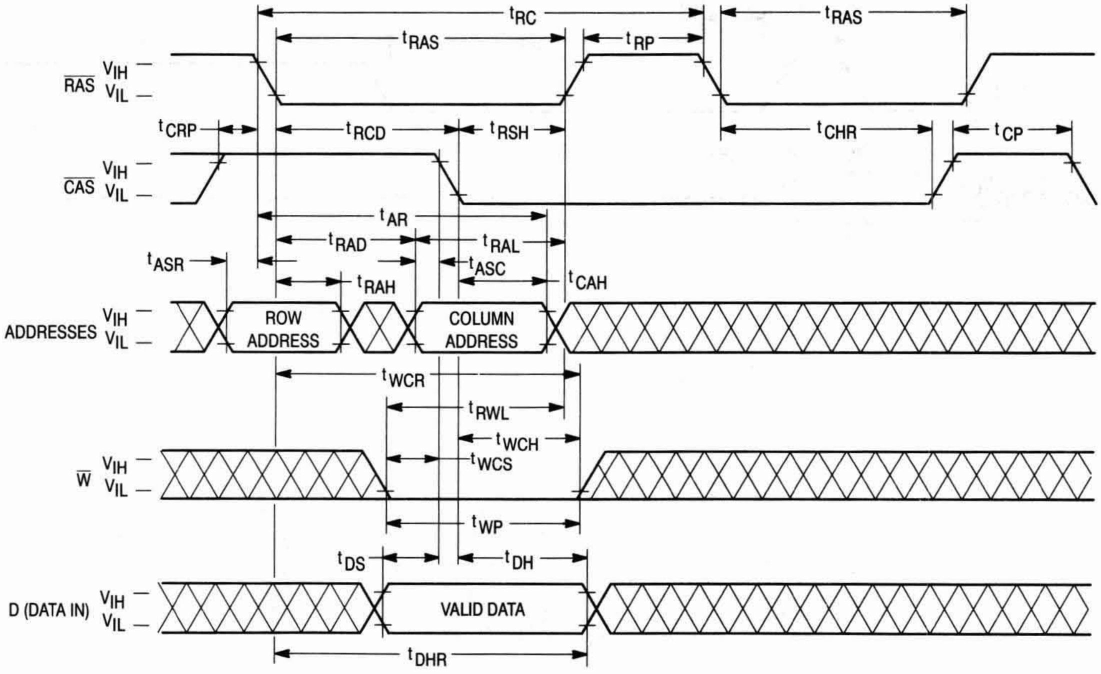
HIDDEN REFRESH CYCLE (READ)



tRC
tRAS
tRAS
tRP
RAS VIH VIL
tCRP
tRCD
tRSH
tCHR
tCP
CAS VIH VIL
tRAD
tRAL
tAR
tASR
tCAH
tRAH
tASC
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
tRCS
tRRH
W VIH VIL
tCAC
tAA
tRAC
tOFF
Q (DATA OUT) VOH VOL
VALID DATA
tCLZ

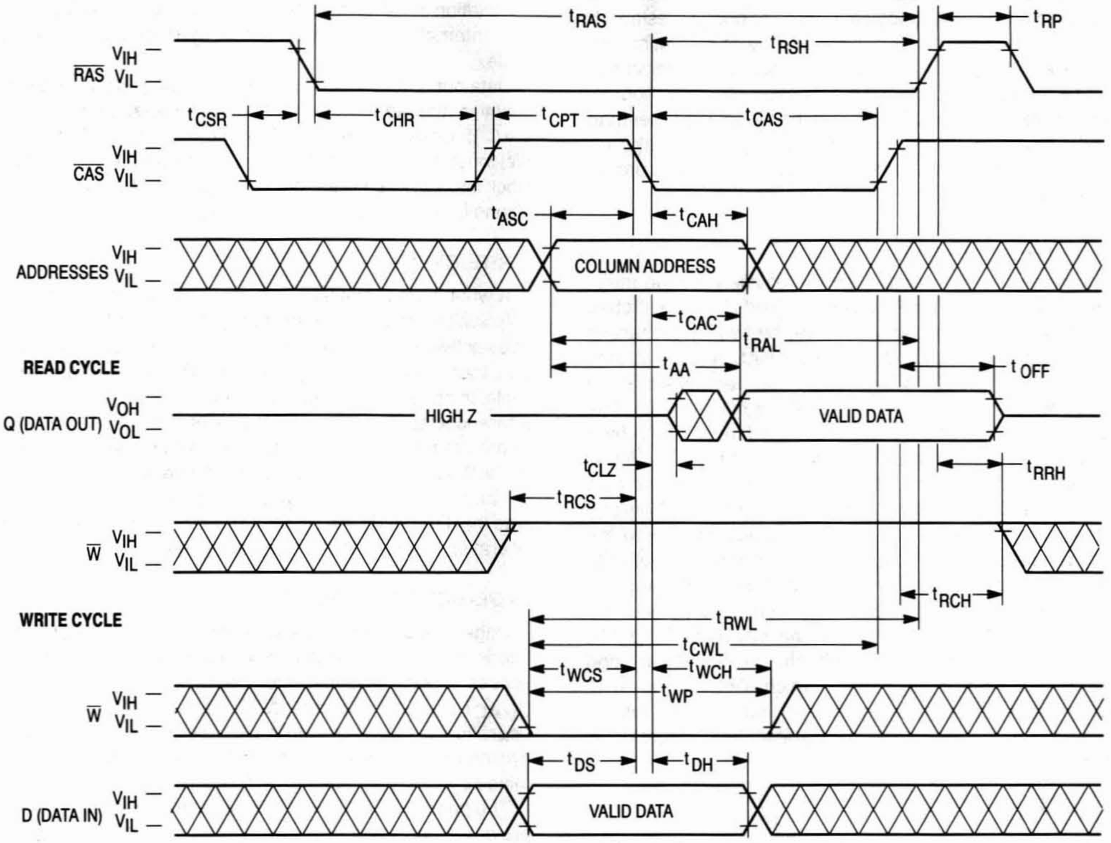
5

HIDDEN REFRESH CYCLE (WRITE)



tRC
tRAS
tRP
tRAS
RAS VIH VIL
tCRP
tRCD
tRSH
tCHR
tCP
CAS VIH VIL
tAR
tRAD
tRAL
tASR
tASC
tRAH
tCAH
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
tWCR
tRWL
tWCH
tWCS
W VIH VIL
tWP
tDS
tDH
D (DATA IN) VIH VIL
VALID DATA
tDHR

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



t_{RAS}
t_{RP}
t_{RSH}
$\overline{RAS}$ V_{IH} V_{IL}
t_{CSR}
t_{CHR}
t_{CPT}
t_{CAS}
$\overline{CAS}$ V_{IH} V_{IL}
t_{ASC}
t_{CAH}
ADDRESSES V_{IH} V_{IL}
COLUMN ADDRESS
t_{CAC}
t_{RAL}
READ CYCLE
t_{AA}
t_{OFF}
Q (DATA OUT) V_{OH} V_{OL}
HIGH Z
VALID DATA
t_{CLZ}
t_{RRH}
t_{RCS}
$\overline{W}$ V_{IH} V_{IL}
t_{RCH}
WRITE CYCLE
t_{RWL}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{W}$ V_{IH} V_{IL}
t_{DS}
t_{DH}
D (DATA IN) V_{IH} V_{IL}
VALID DATA

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the module. During an extended inactive state of the module (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to ensure proper device operation.

ADDRESSING THE RAM

The nine address bus pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of eighteen address bits will decode one of the 524,288 word locations in the device. The column address strobe follows the row address strobe by a specified minimum and maxium time called t_{RCD}, which is the row to column strobe delay. This time interval is also referred to as the multiplex window, which gives flexibility to a system designer to set up the external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, other variations in addressing the module: the refresh modes ($\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh), and another mode called page mode which allows the user to column access all words within a selected row. The refresh mode and page mode operations are described in more detail in later sections.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, which is covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from the row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at all 512 column locations on a selected row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 10-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle (previously described), followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In practice, any combination of read and write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the module needs to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the module will also refresh all the words associated with the particular row(s) decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

This refresh cycle is initiated when $\overline{\text{RAS}}$ falls, after $\overline{\text{CAS}}$ has been low (by t_{CSR}). This activates the internal refresh counter, which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{\text{CAS}}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{\text{CAS}}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period (t_{RP}), executing a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. (See Figure 1.)

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read cycle**. Repeat this operation 512 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, write cycle**. Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

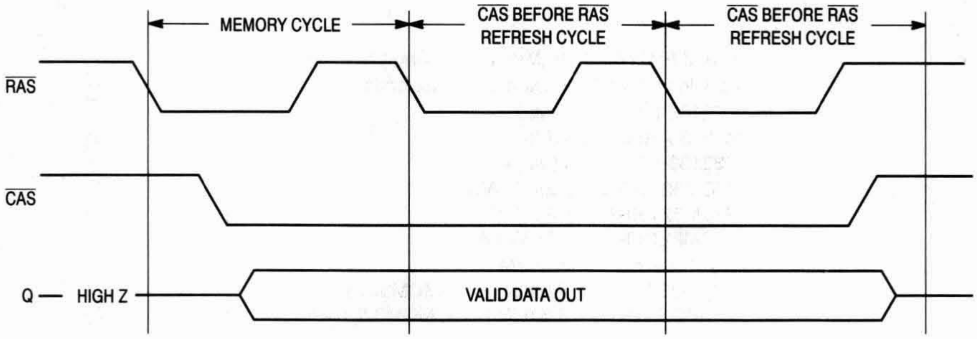

MEMORY CYCLE
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
Q — HIGH Z
VALID DATA OUT

Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 32512 or 32L512 X XX

Motorola Memory Prefix — MCM

Part Number — 32512 or 32L512

Package (AS = SIMM, ASG = Gold Pad SIMM) — X

Speed (70 = 70 ns, 80 = 80 ns, 10 = 100 ns) — XX

Full Part Numbers — MCM32512AS70 MCM32512ASG70
MCM32512AS80 MCM32512ASG80

MCM32L512AS70 MCM32L512ASG70
MCM32L512AS80 MCM32L512ASG80

NOTE: For mechanical data, please see Chapter 10.

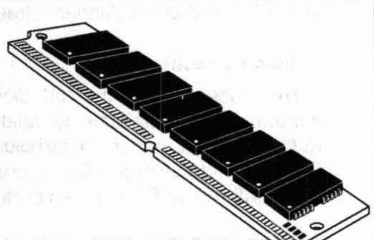
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM32130
MCM32L130

1M x 32 Bit Dynamic Random Access Memory Module

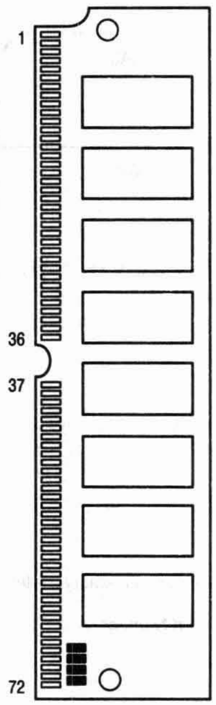
The MCM32130 is a 32M dynamic random access memory (DRAM) module organized as 1,048,576 x 32 bits. The module is a 72-lead single-in-line memory module (SIMM) consisting of eight MCM54400AN DRAMs housed in standard 300 mil SOJ packages mounted on a substrate along with a 0.22 μF (min) decoupling capacitor mounted under each DRAM. The MCM54400AN is a CMOS high speed dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  MCM32130 = 16 ms (Max)
  MCM32L130 = 128 ms (Max)
- Consists of Eight 1M x 4 DRAMs and Eight 0.22 μF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM32130-60 = 60 ns (Max)
  MCM32130-70 = 70 ns (Max)
  MCM32130-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM32130-60 = 5.28 W (Max)
  MCM32130-70 = 4.40 W (Max)
  MCM32130-80 = 3.74 W (Max)
- Low Standby Power Dissipation: TTL Levels = 88 mW (Max)
  CMOS Levels = 44 mW (Max, MCM32130)
  CMOS Levels = 8.8 mW (Max, MCM32L130)



SH PACKAGE
LOW HEIGHT SIMM MODULE
CASE 866-02

TOP VIEW



PIN NAMES

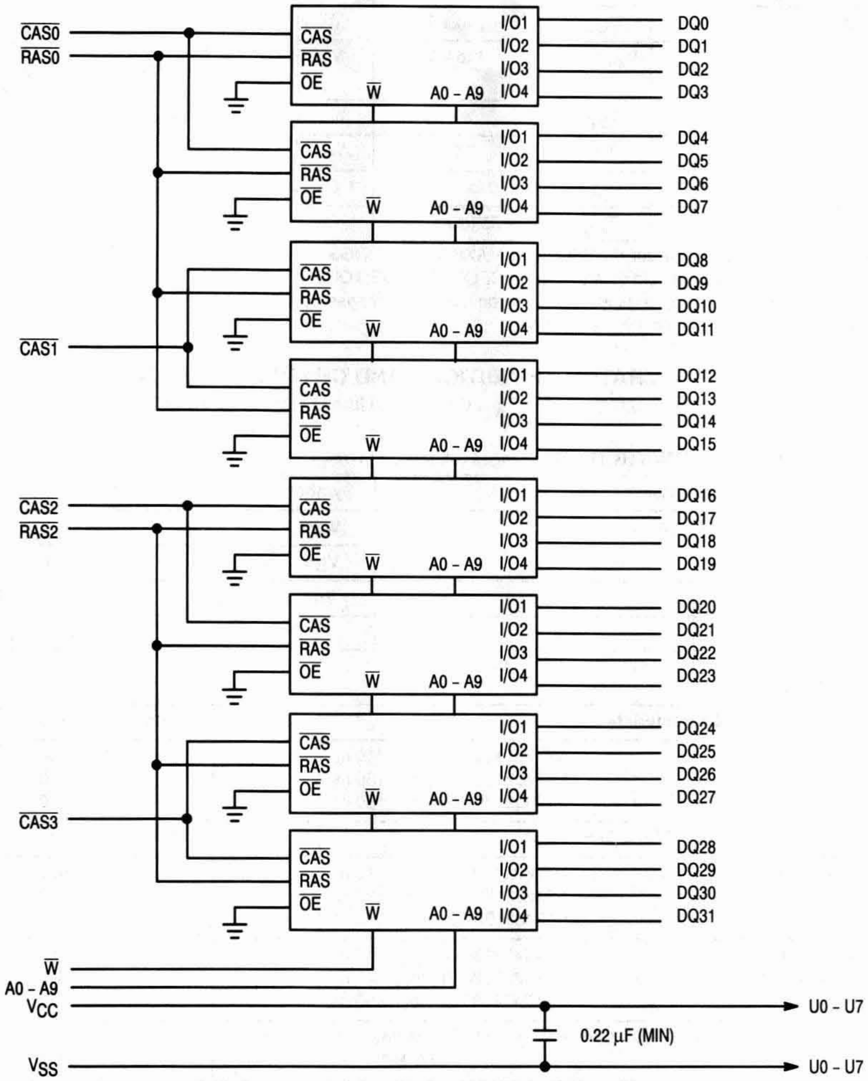
A0 – A9	Address Inputs	DQ0 – DQ31	Data Input/Output
$\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$	Column Address Strobe	PD1 – PD4	Presence Detect
$\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$	Row Address Strobe	$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)	V_{SS}	Ground
NC	No Connection		

All power supply and ground pins must be connected for proper operation of the device.

PIN OUT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{\text{CAS2}}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{\text{CAS3}}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{\text{CAS1}}$	55	DQ11	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{\text{RAS0}}$	56	DQ27	68	PD2
9	DQ19	21	DQ20	33	NC	45	NC	57	DQ12	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{\text{RAS2}}$	46	NC	58	DQ28	70	PD4
11	NC	23	DQ21	35	NC	47	$\overline{\text{W}}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

BLOCK DIAGRAM


CAS0
RAS0
CAS1
CAS2
RAS2
CAS3
CAS
RAS
OE
W
A0 - A9
I/O1
I/O2
I/O3
I/O4
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
W
A0 - A9
VCC
VSS
0.22 µF (MIN)
U0 - U7
U0 - U7

PRESENCE DETECT PIN OUT			
Pin Name	**60 ns**	**70 ns**	**80 ns**
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	7.2	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	MCM32130-60, t_{RC} = 110 ns MCM32130-70, t_{RC} = 130 ns MCM32130-80, t_{RC} = 150 ns	I_{CC1}	— — —	960 800 680	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	16	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles	MCM32130-60, t_{RC} = 110 ns MCM32130-70, t_{RC} = 130 ns MCM32130-80, t_{RC} = 150 ns	I_{CC3}	— — —	960 800 680	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle	MCM32130-60, t_{PC} = 45 ns MCM32130-70, t_{PC} = 45 ns MCM32130-80, t_{PC} = 50 ns	I_{CC4}	— — —	560 560 480	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	MCM32130 MCM32L130	I_{CC5}	— —	8 1.6	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	MCM32130-60, t_{RC} = 110 ns MCM32130-70, t_{RC} = 130 ns MCM32130-80, t_{RC} = 150 ns	I_{CC6}	— — —	960 800 680	mA	1
V_{CC} Power Supply Current Battery Backup Mode (t_{RC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$, DQ, A0 – A9 = V_{CC} – 0.2 V or 0.2 V)	MCM32L130 only	I_{CC7}	—	2.4	mA	1, 3
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)		$I_{lkg(I)}$	– 80	+ 80	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)		$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)		V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Column Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery backup. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE ($f = 1.0$ MHz, $T_A = 25°C$, $V_{CC} = 5$ V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit
Input Capacitance (A0 – A9)	C_{I1}	—	50	pF
Input Capacitance ($\overline{W}$)	C_{I2}	—	66	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I3}	—	38	pF
Input Capacitance ($\overline{CAS0}$ – $\overline{CAS3}$)	C_{I4}	—	24	pF
I/O Capacitance (DQ0 – DQ31)	C_{DQ}	—	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\,\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0\text{ V} \pm 10\%$, $T_A = 0$ to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

	Symbol		MCM32130-60 MCM32L130-60		MCM32130-70 MCM32L130-70		MCM32130-80 MCM32L130-80			
Parameter	**Std**	**Alt**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	50	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	40	—	40	—	45	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	200 k	70	200 k	80	200 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	40	—	45	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	20	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	

NOTES: (continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements $t_T = 5.0$ ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

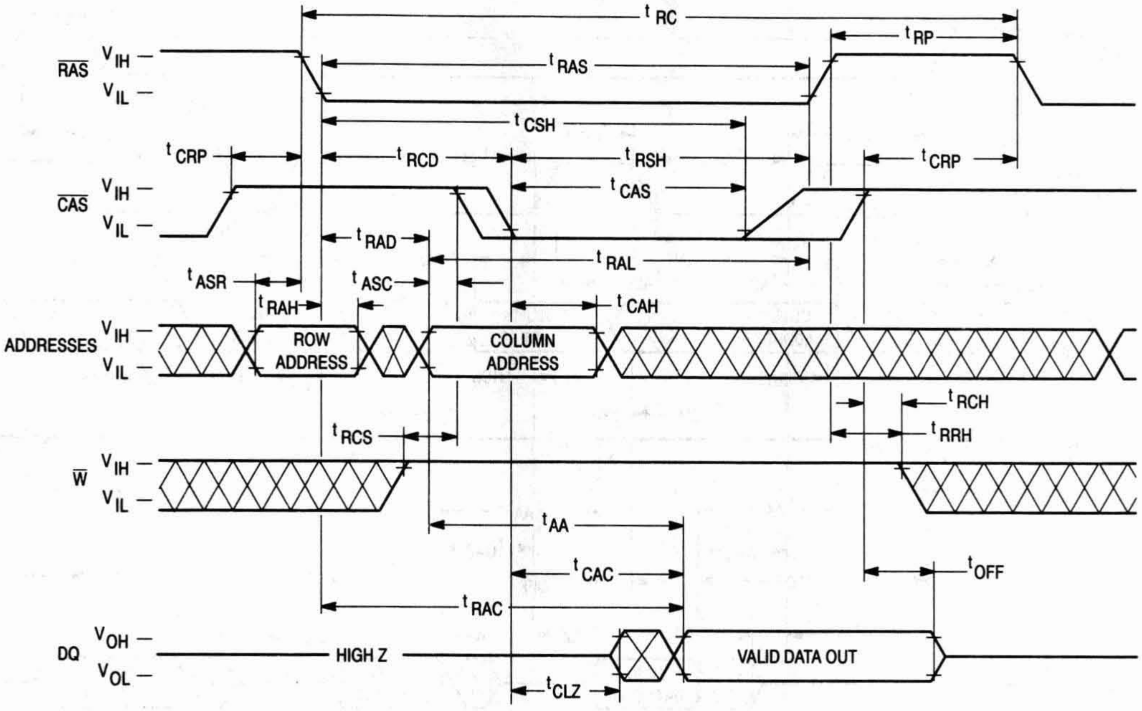
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM32130-60 MCM32L130-60		MCM32130-70 MCM32L130-70		MCM32130-80 MCM32L130-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	14
Refresh Period MCM32130 MCM32L130	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Time	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
Write to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	

NOTES:

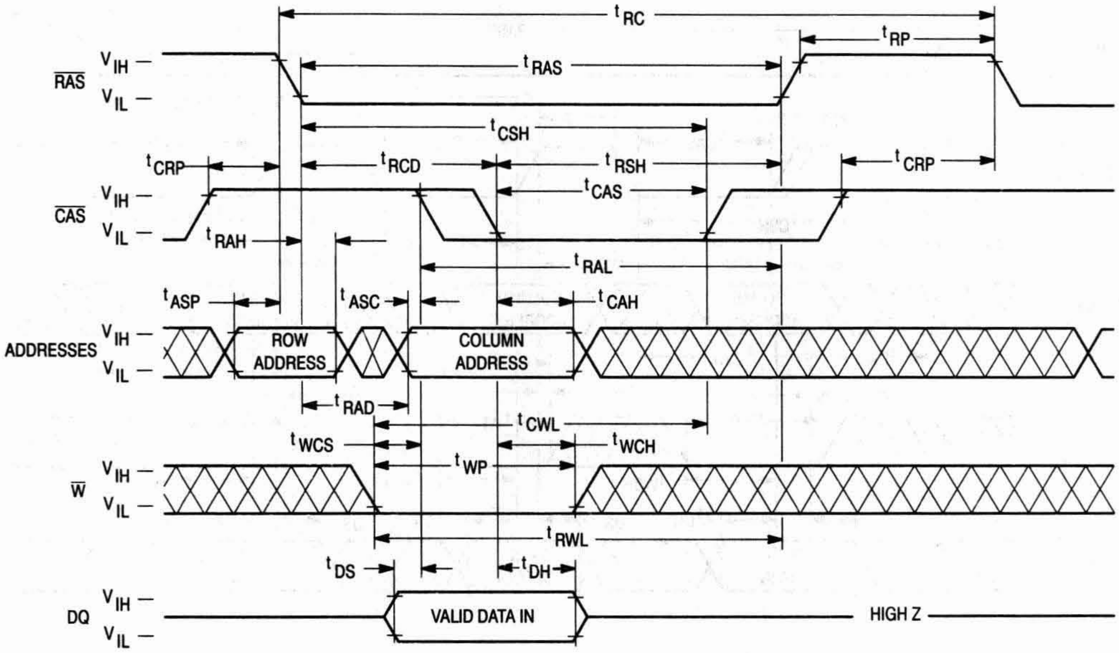
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.

READ CYCLE



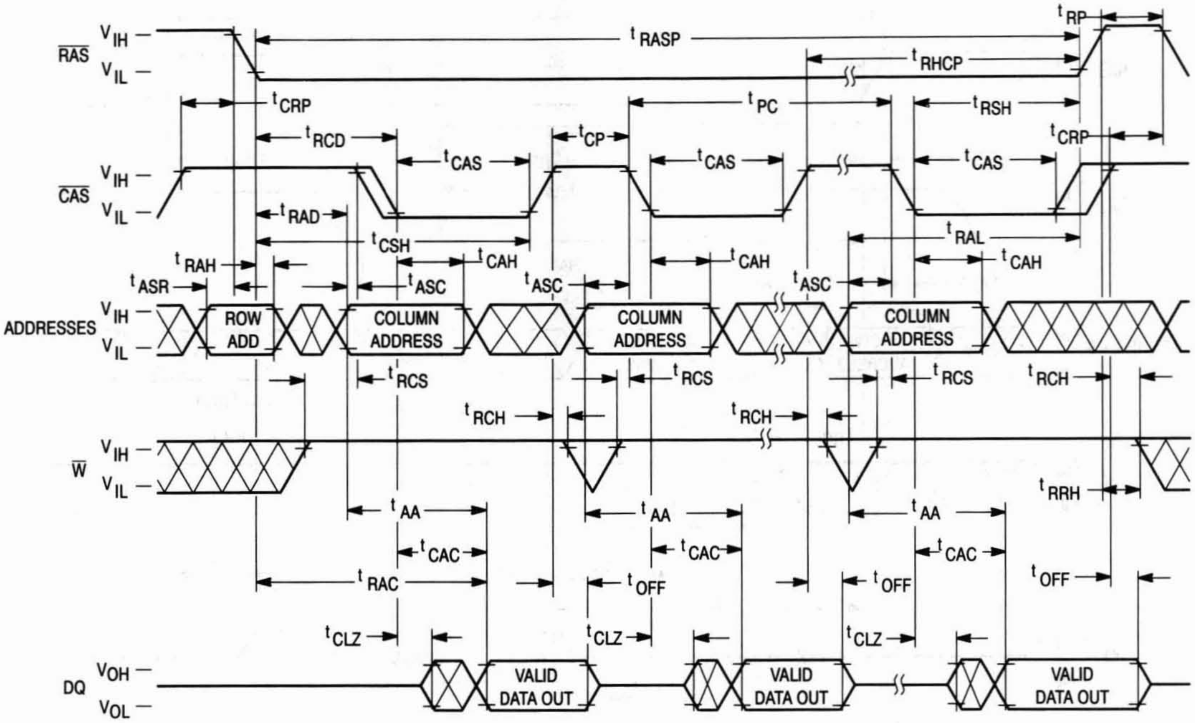
t RC
t RP
RAS
V IH —
V IL —
t RAS
t CSH
t CRP
t RCD
t RSH
t CRP
CAS
V IH —
V IL —
t CAS
t RAD
t RAL
t ASR
t ASC
t RAH
t CAH
ADDRESSES
V IH —
V IL —
ROW ADDRESS
COLUMN ADDRESS
t RCH
t RRH
t RCS
W
V IH —
V IL —
t AA
t CAC
t OFF
t RAC
DQ
V OH —
V OL —
HIGH Z
VALID DATA OUT
t CLZ

EARLY WRITE CYCLE

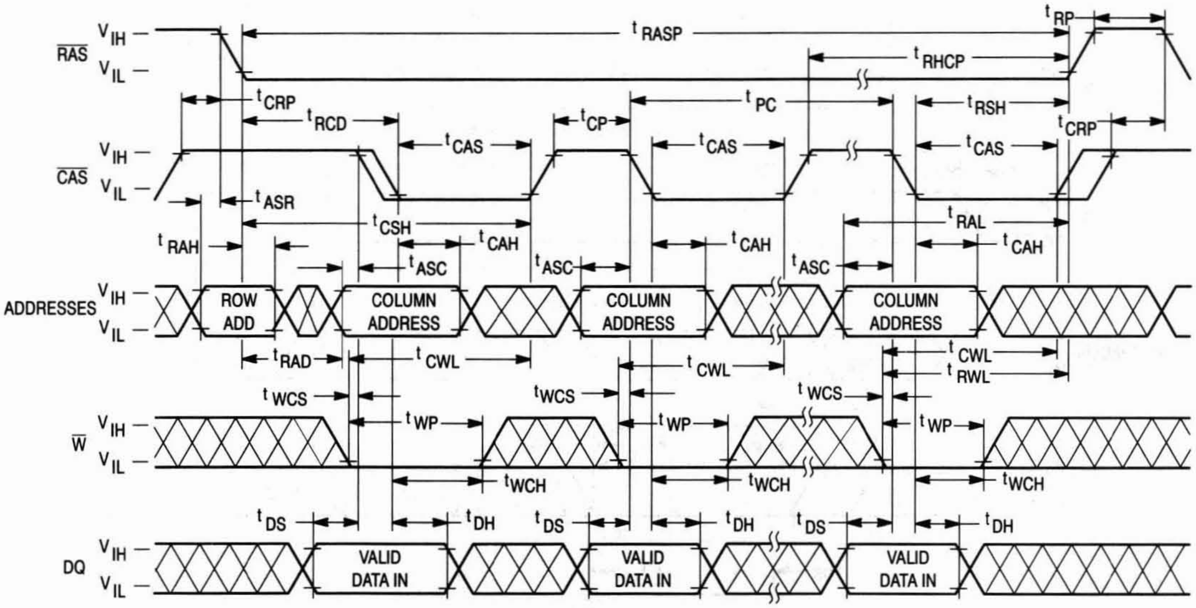


t RC
t RP
RAS
V IH —
V IL —
t RAS
t CSH
t CRP
t RCD
t RSH
t CRP
CAS
V IH —
V IL —
t CAS
t RAH
t RAL
t ASP
t ASC
t CAH
ADDRESSES
V IH —
V IL —
ROW ADDRESS
COLUMN ADDRESS
t RAD
t CWL
t WCS
t WCH
t WP
W
V IH —
V IL —
t RWL
t DS
t DH
DQ
V IH —
V IL —
VALID DATA IN
HIGH Z

FAST PAGE MODE READ CYCLE

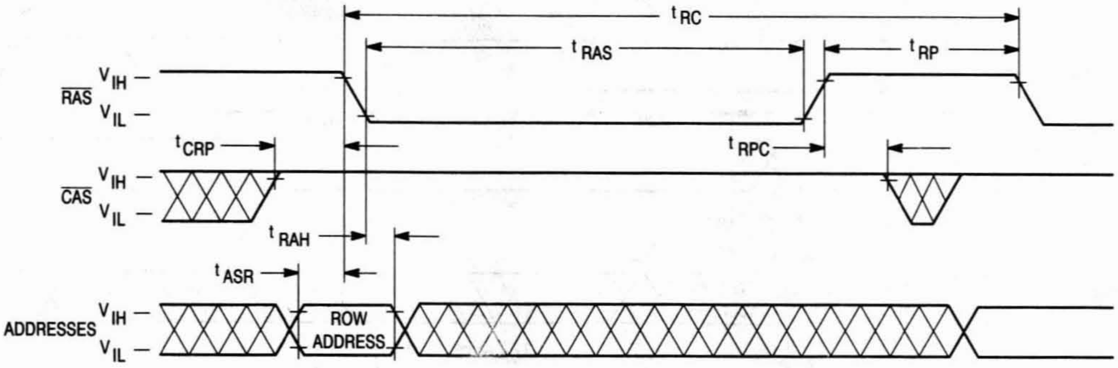

RAS
CAS
ADDRESSES
W
DQ
V IH
V IL
V OH
V OL
t RASP
t RP
t RHCP
t CRP
t PC
t RSH
t RCD
t CP
t CAS
t RAD
t CSH
t RAL
t RAH
t ASR
t CAH
t ASC
ROW ADD
COLUMN ADDRESS
t RCS
t RCH
t RRH
t AA
t CAC
t RAC
t OFF
t CLZ
VALID DATA OUT

FAST PAGE MODE EARLY WRITE CYCLE


RAS
CAS
ADDRESSES
W
DQ
V IH
V IL
t RASP
t RP
t RHCP
t CRP
t RCD
t PC
t RSH
t CP
t CAS
t ASR
t CSH
t RAL
t RAH
t CAH
t ASC
ROW ADD
COLUMN ADDRESS
t RAD
t CWL
t RWL
t WCS
t WP
t WCH
t DS
t DH
VALID DATA IN

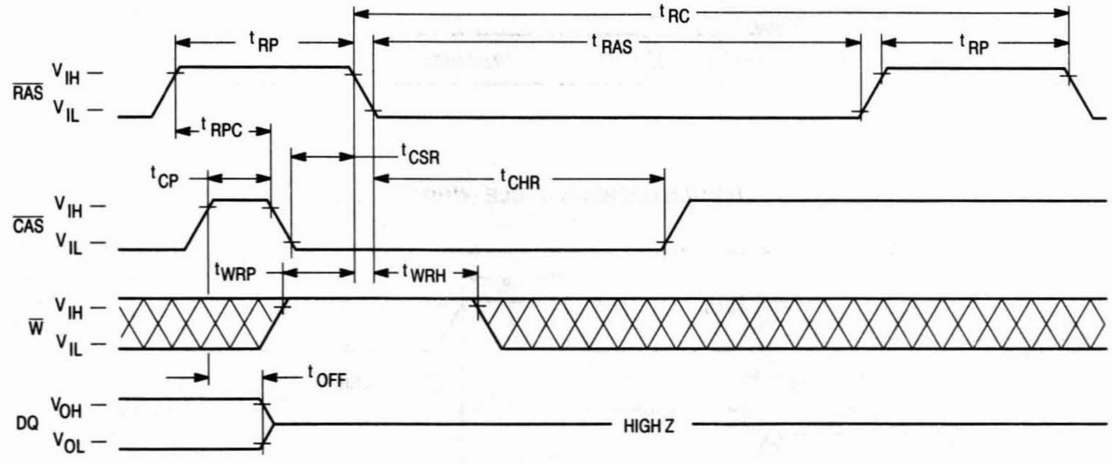
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

($\overline{\text{W}}$ is Don't Care)

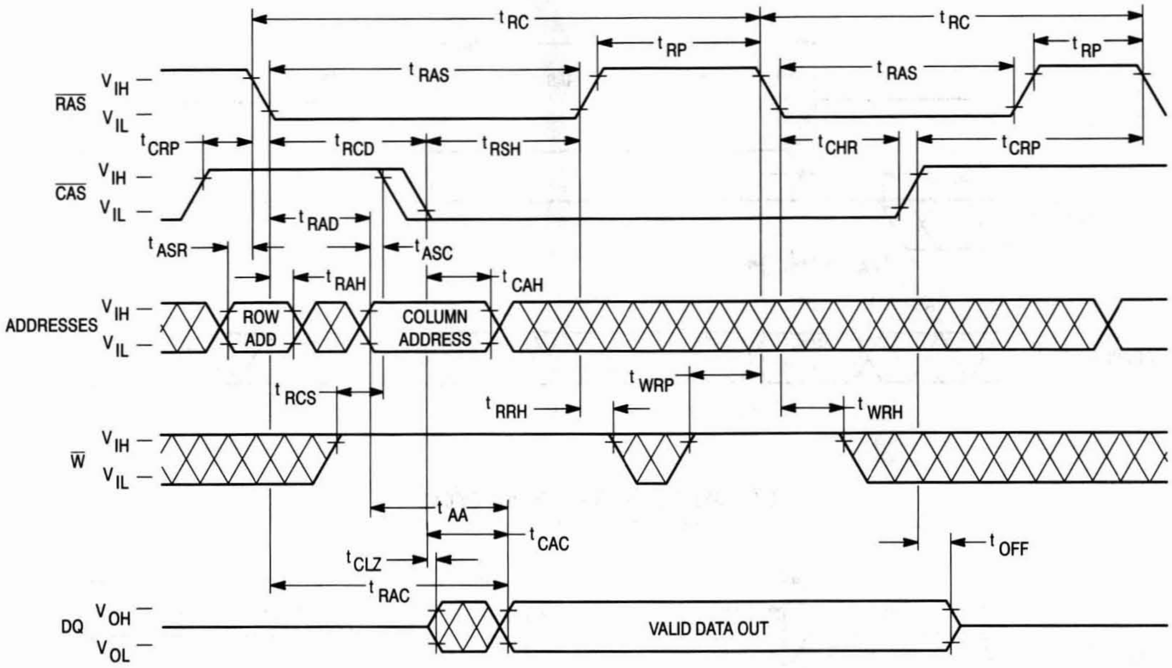

t RC
t RAS
t RP
RAS
V IH
V IL
t CRP
t RPC
CAS
V IH
V IL
t RAH
t ASR
ADDRESSES
V IH
V IL
ROW ADDRESS

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

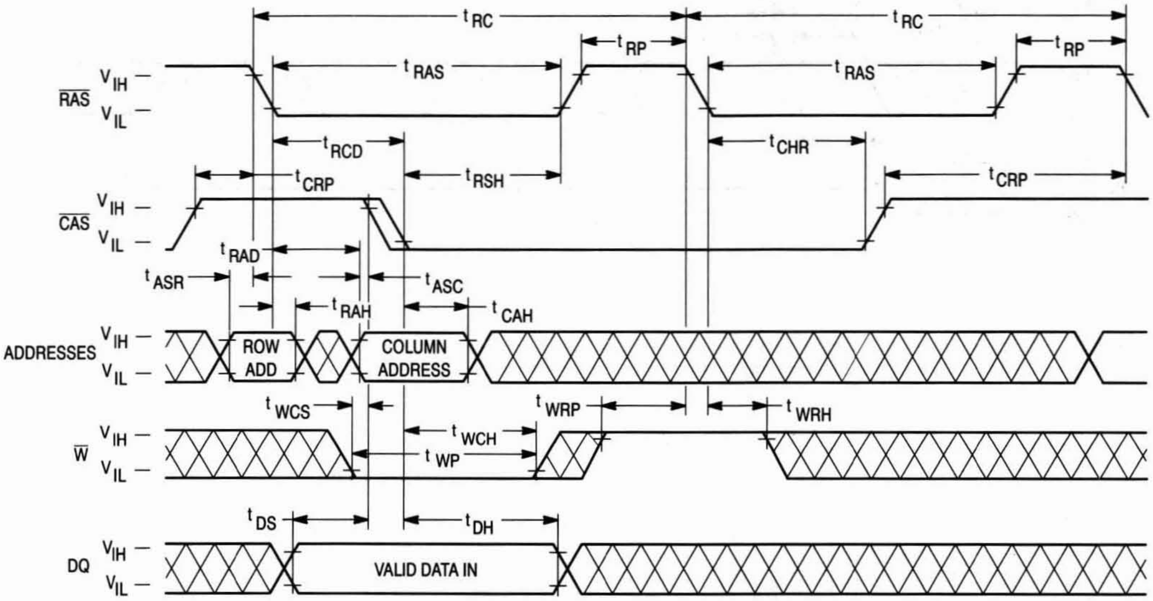
(A0 – A9 are Don't Care)


t RC
t RP
t RAS
t RP
RAS
V IH
V IL
t RPC
t CSR
t CP
t CHR
CAS
V IH
V IL
t WRP
t WRH
W
V IH
V IL
t OFF
DQ
V OH
V OL
HIGH Z

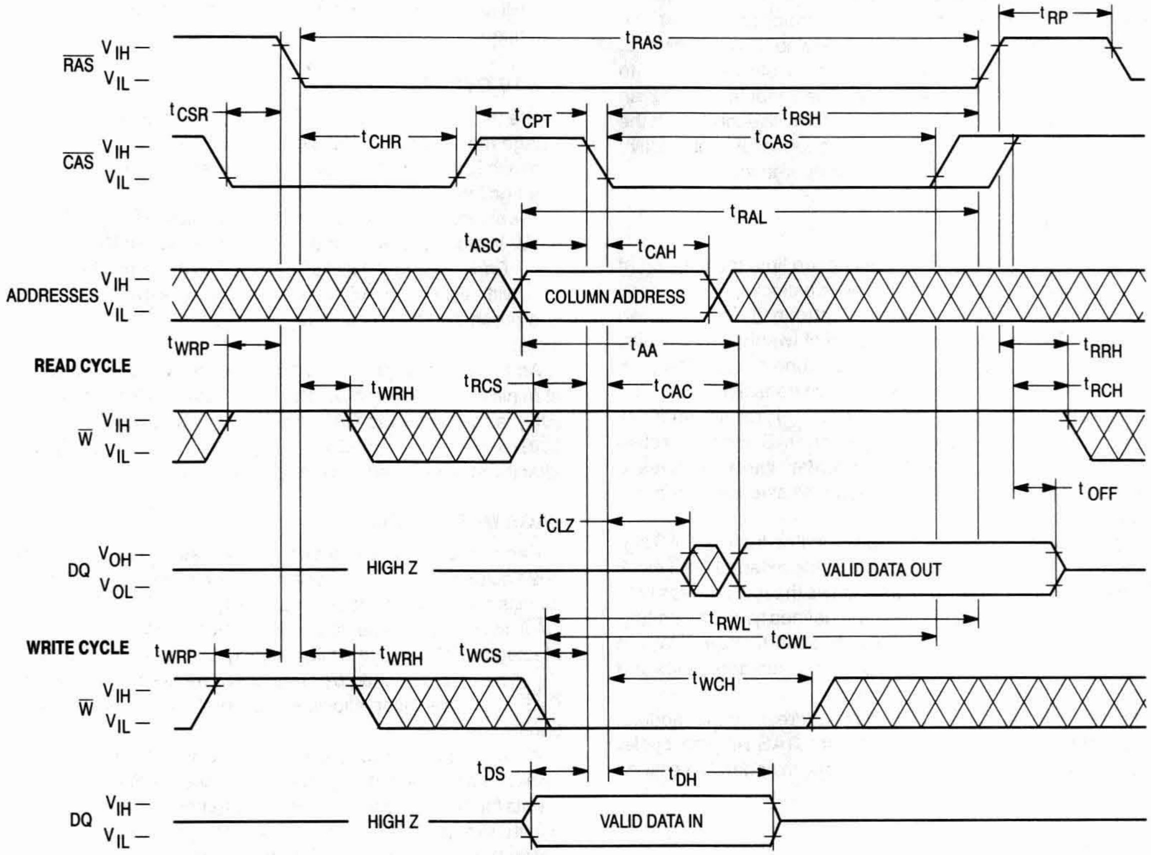
HIDDEN REFRESH CYCLE (READ)


t_{RC}
t_{RC}
t_{RP}
t_{RP}
t_{RAS}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CRP}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADD
COLUMN ADDRESS
t_{RCS}
t_{WRP}
t_{RRH}
t_{WRH}
$\overline{W}$
V_{IH}
V_{IL}
t_{AA}
t_{CAC}
t_{OFF}
t_{CLZ}
t_{RAC}
DQ
V_{OH}
V_{OL}
VALID DATA OUT

HIDDEN REFRESH CYCLE (WRITE)


t_{RC}
t_{RC}
t_{RP}
t_{RP}
t_{RAS}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RCD}
t_{CHR}
t_{RSH}
t_{CRP}
t_{CRP}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADD
COLUMN ADDRESS
t_{WCS}
t_{WRP}
t_{WRH}
t_{WCH}
t_{WP}
$\overline{W}$
V_{IH}
V_{IL}
t_{DS}
t_{DH}
DQ
V_{IH}
V_{IL}
VALID DATA IN

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RP}
t_{RAS}
t_{CSR}
t_{CPT}
t_{RSH}
$\overline{\text{CAS}}$
t_{CHR}
t_{CAS}
t_{RAL}
t_{ASC}
t_{CAH}
ADDRESSES
COLUMN ADDRESS
t_{WRP}
t_{AA}
t_{RRH}
READ CYCLE
t_{WRH}
t_{RCS}
t_{CAC}
t_{RCH}
$\overline{\text{W}}$
t_{OFF}
t_{CLZ}
DQ
V_{OH}
V_{OL}
HIGH Z
VALID DATA OUT
t_{RWL}
t_{CWL}
WRITE CYCLE
t_{WRP}
t_{WRH}
t_{WCS}
t_{WCH}
t_{DS}
t_{DH}
HIGH Z
VALID DATA IN

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 word locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the module: **$\overline{RAS}$ only refresh cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either a "normal" random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. $\overline{CAS}$ controls read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with either an early write or a page mode early write cycle. Early write mode is discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early write mode is distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (DQ) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM32130 require refresh every 16 milliseconds, while refresh time for the MCM32L130 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM32130, and 124.8 microseconds for the MCM32L130. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM32130 and 128 milliseconds on the MCM32L130.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **RAS-only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order actives an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode cycle) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **CAS before RAS refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 1024 test cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 CAS before RAS** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **CAS before RAS refresh counter test, read cycle**. Repeat this operation 1024 times.
3. Select a column address, and write "1" into the cell by performing **CAS before RAS refresh counter test, write cycle**. Repeat this operation 1024 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

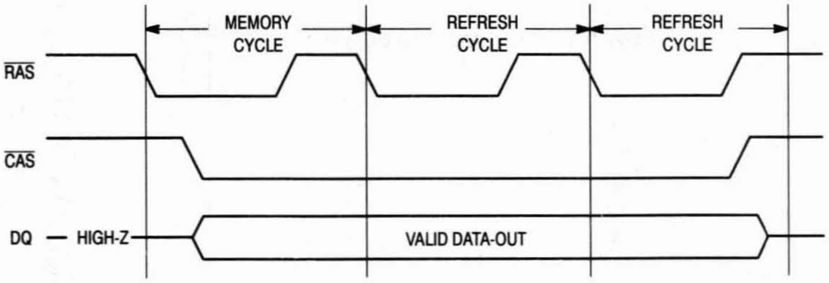


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 32130 or 32L130 X XX

Motorola Memory Prefix — MCM
Part Number — 32130 or 32L130
Package (SH = SIMM, SHG = Gold Pad SIMM, SSH = Very Low Profile SIMM) — X
Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers —
MCM32130SH60 MCM32130SHG60
MCM32130SH70 MCM32130SHG70
MCM32130SH80 MCM32130SHG80

MCM32L130SH60 MCM32L130SHG60
MCM32L130SH70 MCM32L130SHG70
MCM32L130SH80 MCM32L130SHG80

Contact your Motorola representative for further information on the MCM32130SSH profile.

NOTE: For mechanical data, please see Chapter 10.

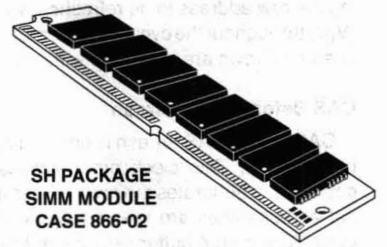
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2M x 32 Bit Dynamic Random Access Memory Module

MCM32230
MCM32L230

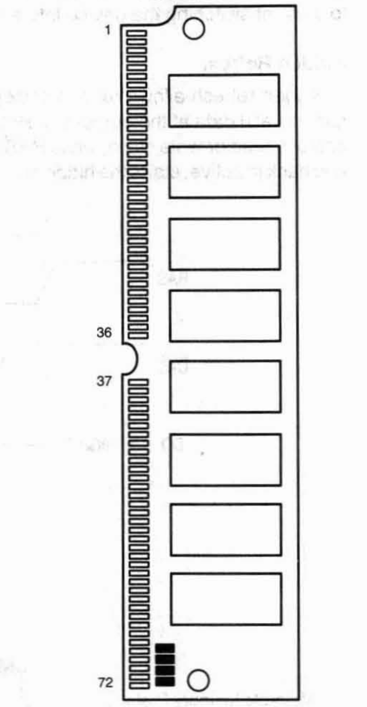
The MCM32230 is a 64M dynamic random access memory (DRAM) module organized as 2,097,152 x 32 bits. The module is a 72-lead double sided single-in-line memory module (SIMM) consisting of sixteen MCM54400AN DRAMs housed in standard 300 mil SOJ packages mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM54400AN is a CMOS high speed, dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$ Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM32230 = 16 ms (Max)
  MCM32L230 = 128 ms (Max)
- Consists of Sixteen 1M x 4 DRAMs and Sixteen 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM32230-60 = 60 ns (Max)
  MCM32230-70 = 70 ns (Max)
  MCM32230-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM32230-60 = 5.37 W (Max)
  MCM32230-70 = 4.49 W (Max)
  MCM32230-80 = 3.83 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 130 W (Max)
  CMOS Levels = 88 mW (Max, MCM32230)
  CMOS Levels = 18 mW (Max, MCM32L230)



SH PACKAGE
SIMM MODULE
CASE 866-02

TOP VIEW



PIN OUT

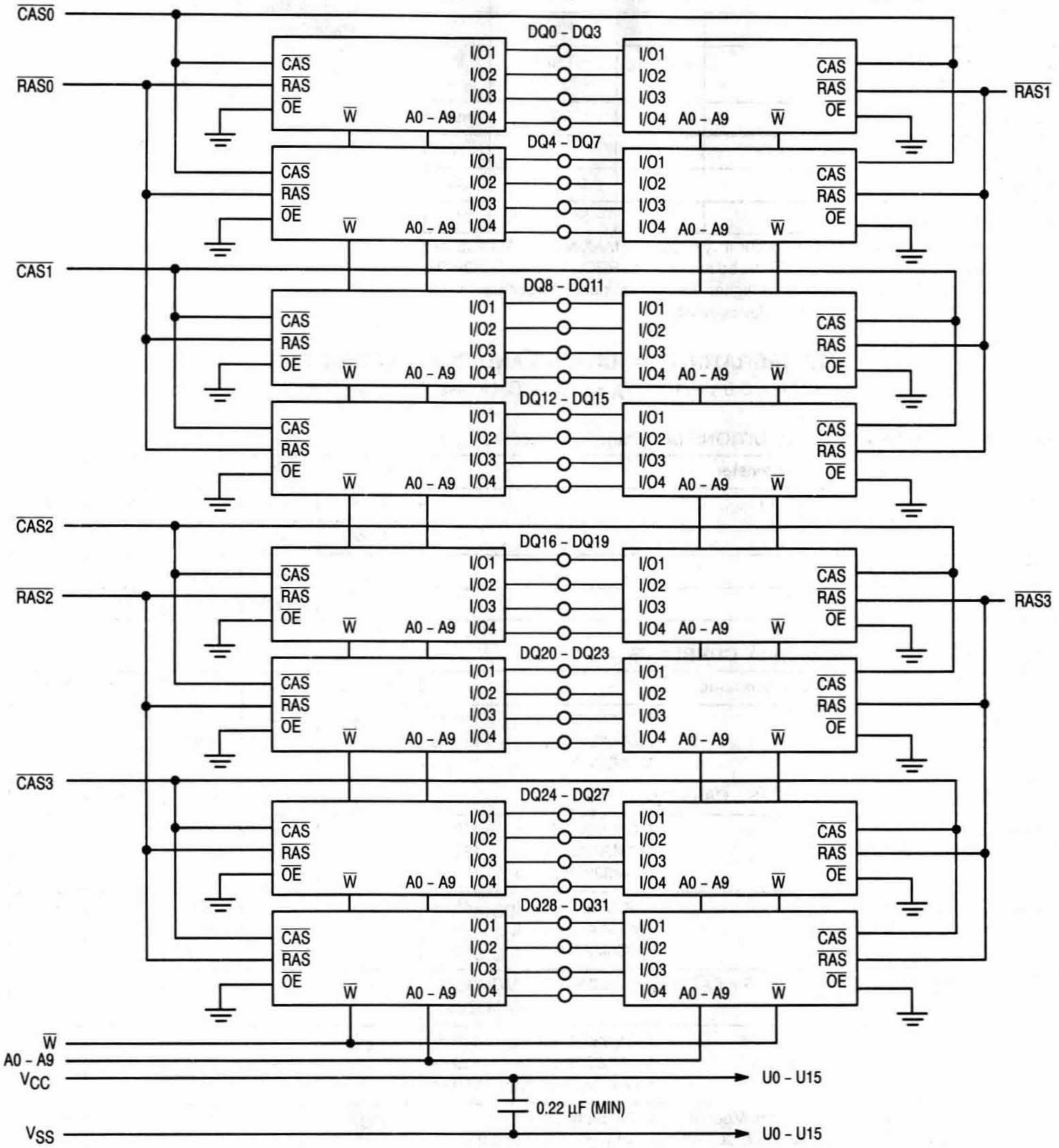
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{\text{CAS2}}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{\text{CAS3}}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{\text{CAS1}}$	55	DQ11	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{\text{RAS0}}$	56	DQ27	68	PD2
9	DQ19	21	DQ20	33	$\overline{\text{RAS3}}$	45	$\overline{\text{RAS1}}$	57	DQ12	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{\text{RAS2}}$	46	NC	58	DQ28	70	PD4
11	NC	23	DQ21	35	NC	47	$\overline{\text{W}}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

PIN NAMES

A0 – A9	Address Inputs
DQ0 – DQ31	Data Input/Output
$\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$	Column Address Strobe
PD1 – PD4	Presence Detect
$\overline{\text{RAS0}}$ – $\overline{\text{RAS3}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

BLOCK DIAGRAM



CAS0
RAS0
CAS1
CAS2
RAS2
CAS3
RAS1
RAS3
DQ0 – DQ3
DQ4 – DQ7
DQ8 – DQ11
DQ12 – DQ15
DQ16 – DQ19
DQ20 – DQ23
DQ24 – DQ27
DQ28 – DQ31
CAS
RAS
OE
W
A0 – A9
I/O1
I/O2
I/O3
I/O4
W
A0 – A9
VCC
VSS
U0 – U15
0.22 µF (MIN)
U0 – U15

PRESENCE DETECT PIN OUT			
Pin Name	**60 ns**	**70 ns**	**80 ns**
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	7.32	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	MCM32230-60, t_{RC} = 110 ns MCM32230-70, t_{RC} = 130 ns MCM32230-80, t_{RC} = 150 ns	I_{CC1}	— — —	976 816 696	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	32	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles	MCM32230-60, t_{RC} = 110 ns MCM32230-70, t_{RC} = 130 ns MCM32230-80, t_{RC} = 150 ns	I_{CC3}	— — —	976 816 696	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle	MCM32230-60, t_{PC} = 45 ns MCM32230-70, t_{PC} = 45 ns MCM32230-80, t_{PC} = 50 ns	I_{CC4}	— — —	576 576 496	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	MCM32230 MCM32L230	I_{CC5}	— —	16 3.2	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	MCM32230-60, t_{RC} = 110 ns MCM32230-70, t_{RC} = 130 ns MCM32230-80, t_{RC} = 150 ns	I_{CC6}	— — —	976 816 696	mA	1
V_{CC} Power Supply Current Battery Backup Mode (t_{RC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$, DQ, A0 – A9 = V_{CC} – 0.2 V or 0.2 V)	MCM32L230 only	I_{CC7}	—	2.4	mA	1, 3
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)		$I_{lkg(I)}$	– 160	160	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)		$I_{lkg(O)}$	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)		V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Column Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery backup. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit	Notes
Input Capacitance (A0 – A9)	C_{I1}	—	90	pF	1
Input Capacitance ($\overline{W}$)	C_{I2}	—	122	pF	1
Input Capacitance ($\overline{RAS0}$ – $\overline{RAS2}$)	C_{I3}	—	38	pF	1
Input Capacitance ($\overline{CAS0}$ – $\overline{CAS3}$)	C_{I4}	—	38	pF	1
I/O Capacitance (DQ0 – DQ31)	C_{DQ}	—	24	pF	1

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\ \Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM32230-60 MCM32L230-60		MCM32230-70 MCM32L230-70		MCM32230-80 MCM32L230-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	50	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	40	—	40	—	45	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	100 k	70	100 k	80	100 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	40	—	45	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	20	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

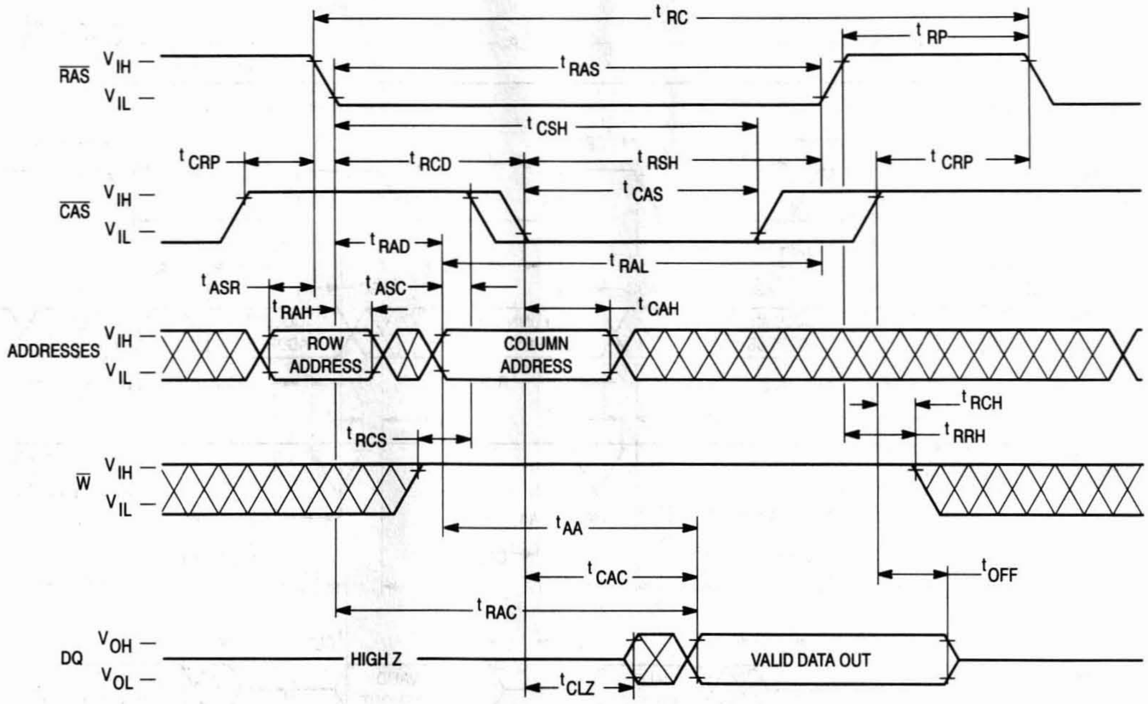
READ AND WRITE CYCLES (Continued)

	Symbol		MCM32230-60 MCM32L230-60		MCM32230-70 MCM32L230-70		MCM32230-80 MCM32L230-80			
Parameter	**Std**	**Alt**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	14
Refresh Period MCM32230 MCM32L230	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	30	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	

NOTES:

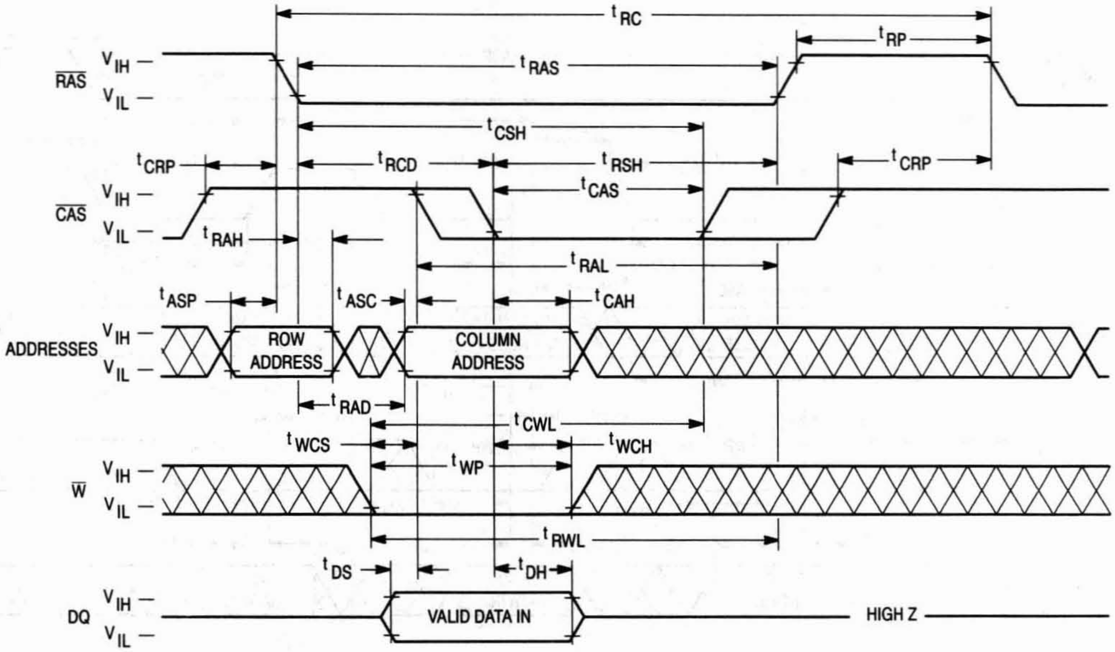
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in late write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), th cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.
16. To avoid bus contention and potential damage to the module, $\overline{RAS0}$ and $\overline{RAS1}$ may not be active low simultaneously. Similarly, $\overline{RAS2}$ and $\overline{RAS3}$ may not be simultaneously active low.

READ CYCLE



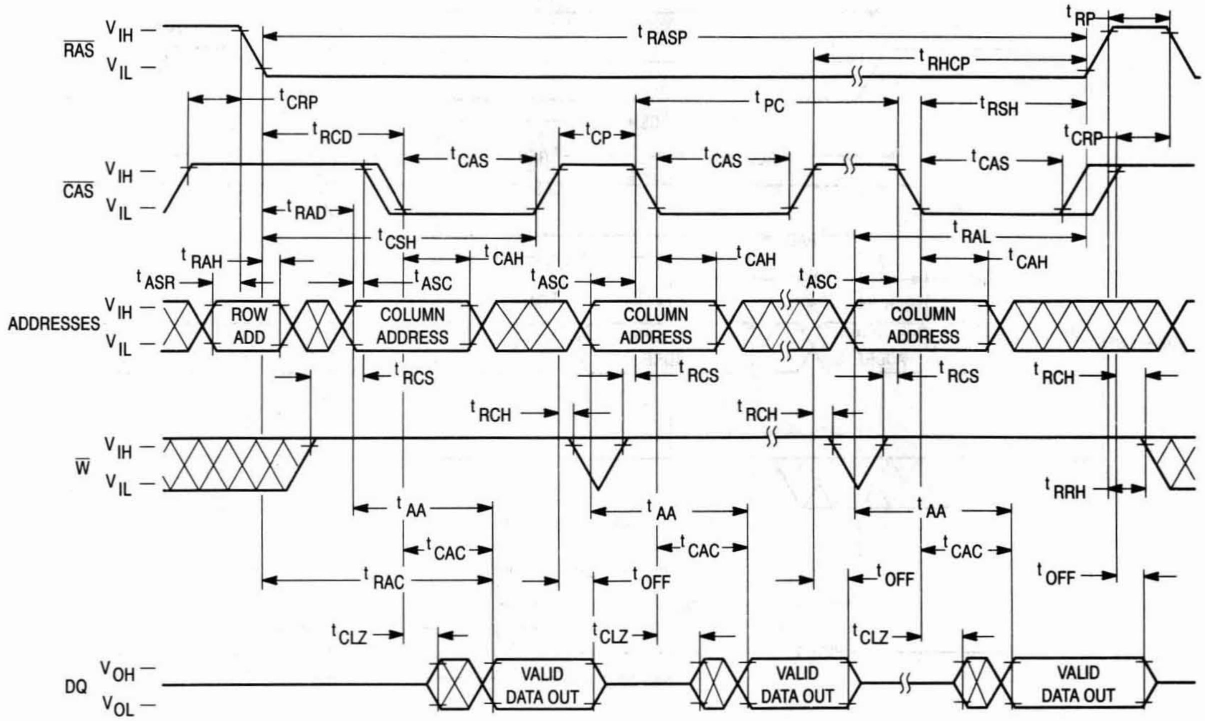
t RC
t RP
RAS
V IH
V IL
t RAS
t CSH
t CRP
t RCD
t RSH
t CRP
CAS
V IH
V IL
t CAS
t RAD
t RAL
t ASR
t ASC
t RAH
t CAH
ADDRESSES
V IH
V IL
ROW ADDRESS
COLUMN ADDRESS
t RCH
t RRH
t RCS
W
V IH
V IL
t AA
t CAC
t OFF
t RAC
DQ
V OH
V OL
HIGH Z
VALID DATA OUT
t CLZ

EARLY WRITE CYCLE

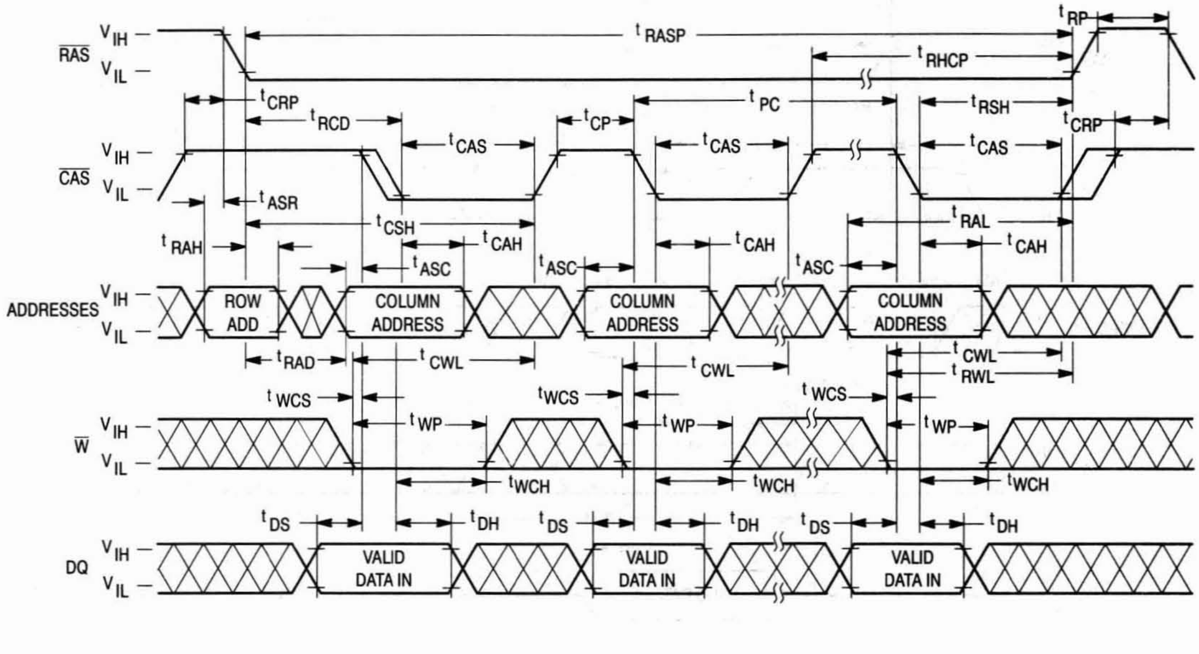


t RC
t RP
RAS
V IH
V IL
t RAS
t CSH
t CRP
t RCD
t RSH
t CRP
CAS
V IH
V IL
t CAS
t RAH
t RAL
t ASP
t ASC
t CAH
ADDRESSES
V IH
V IL
ROW ADDRESS
COLUMN ADDRESS
t RAD
t CWL
t WCS
t WCH
t WP
W
V IH
V IL
t RWL
t DS
t DH
DQ
V IH
V IL
VALID DATA IN
HIGH Z

FAST PAGE MODE READ CYCLE

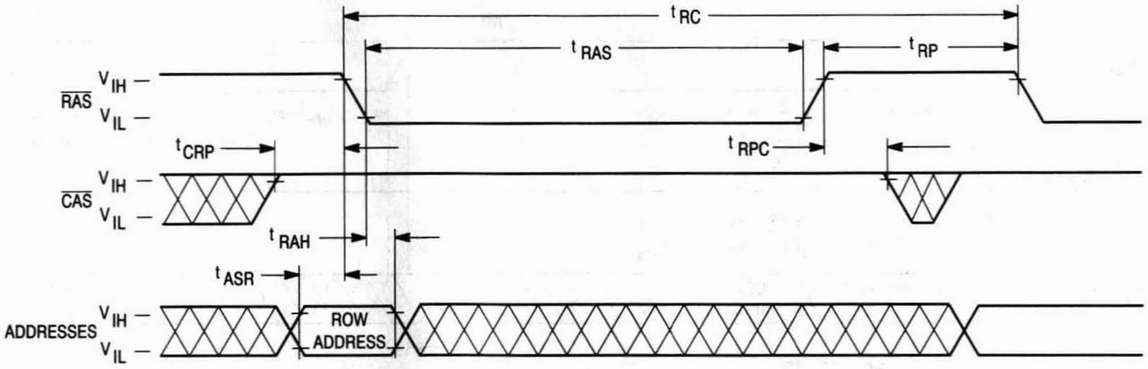

RAS
V IH
V IL
CAS
ADDRESSES
W
DQ
V OH
V OL
t RASP
t RP
t RHCP
t CRP
t PC
t RSH
t RCD
t CP
t CAS
t RAD
t CSH
t RAL
t RAH
t CAH
t ASR
t ASC
ROW ADD
COLUMN ADDRESS
t RCS
t RCH
t RRH
t AA
t CAC
t RAC
t OFF
t CLZ
VALID DATA OUT

FAST PAGE MODE EARLY WRITE CYCLE


RAS
V IH
V IL
CAS
ADDRESSES
W
DQ
t RASP
t RP
t RHCP
t CRP
t PC
t RSH
t RCD
t CP
t CAS
t ASR
t CSH
t RAL
t RAH
t CAH
t ASC
ROW ADD
COLUMN ADDRESS
t RAD
t CWL
t RWL
t WCS
t WP
t WCH
t DS
t DH
VALID DATA IN

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

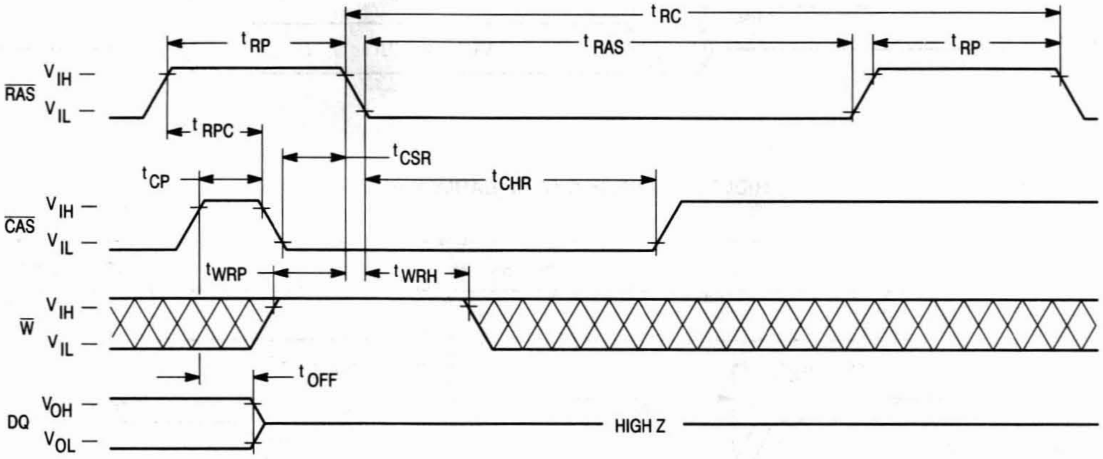
($\overline{\text{W}}$ is Don't Care)



t RC
t RAS
t RP
RAS
V IH
V IL
t CRP
t RPC
CAS
V IH
V IL
t RAH
t ASR
ADDRESSES
V IH
V IL
ROW ADDRESS

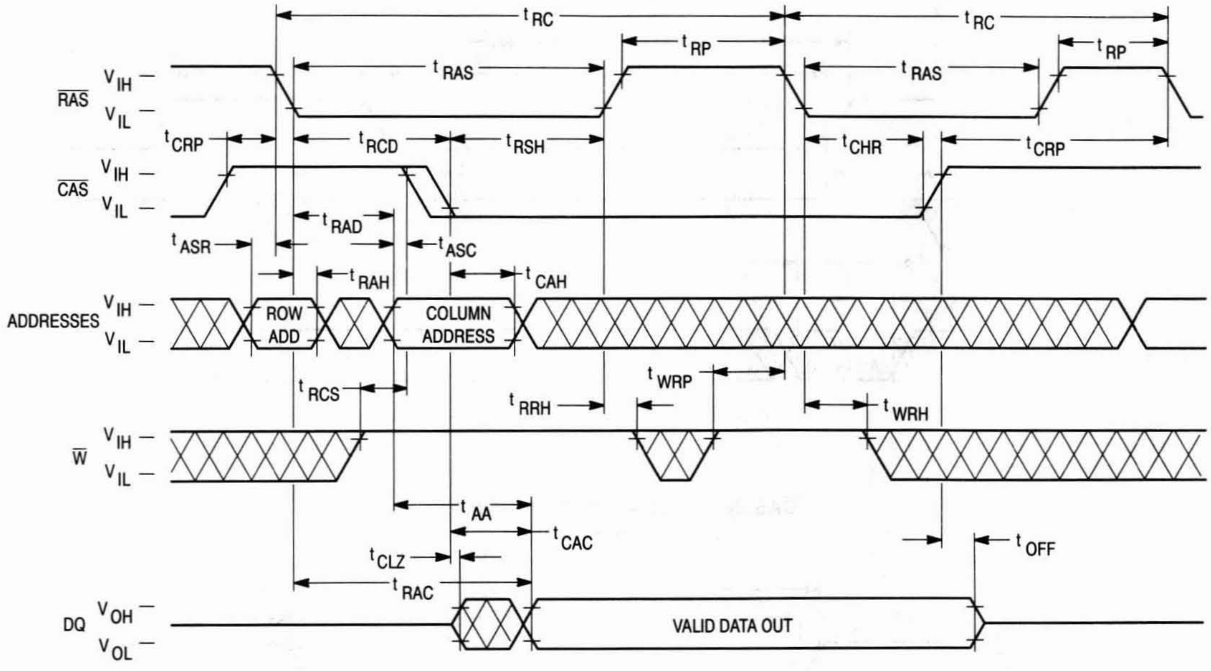
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

(A0 – A9 are Don't Care)



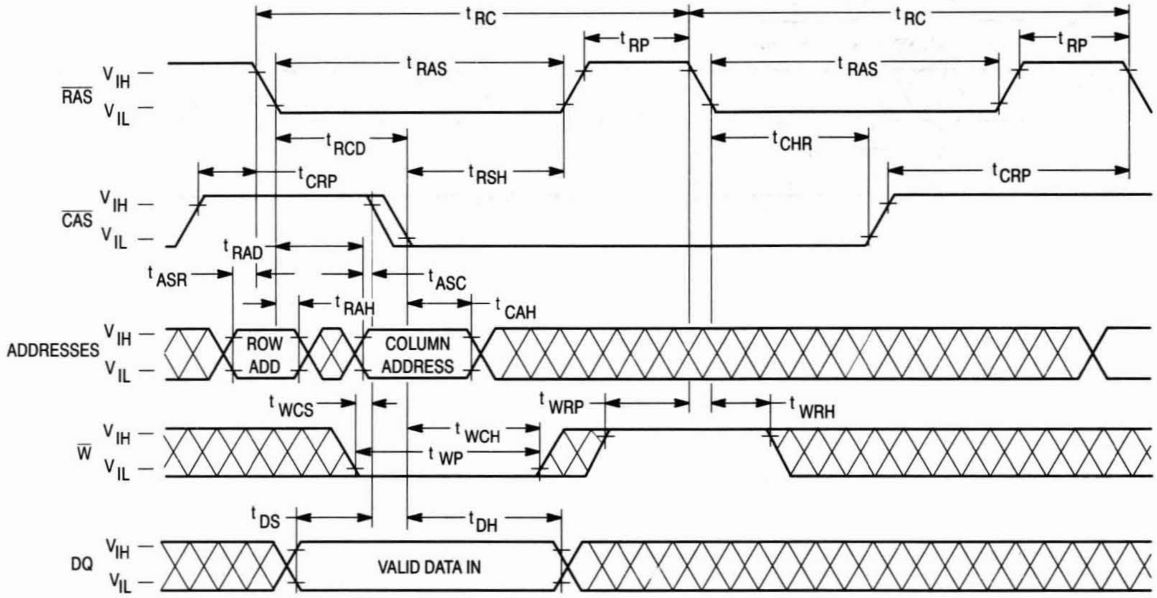
t RC
t RP
t RAS
t RP
RAS
V IH
V IL
t RPC
t CSR
t CP
t CHR
CAS
V IH
V IL
t WRP
t WRH
W
V IH
V IL
t OFF
DQ
V OH
V OL
HIGH Z

HIDDEN REFRESH CYCLE (READ)



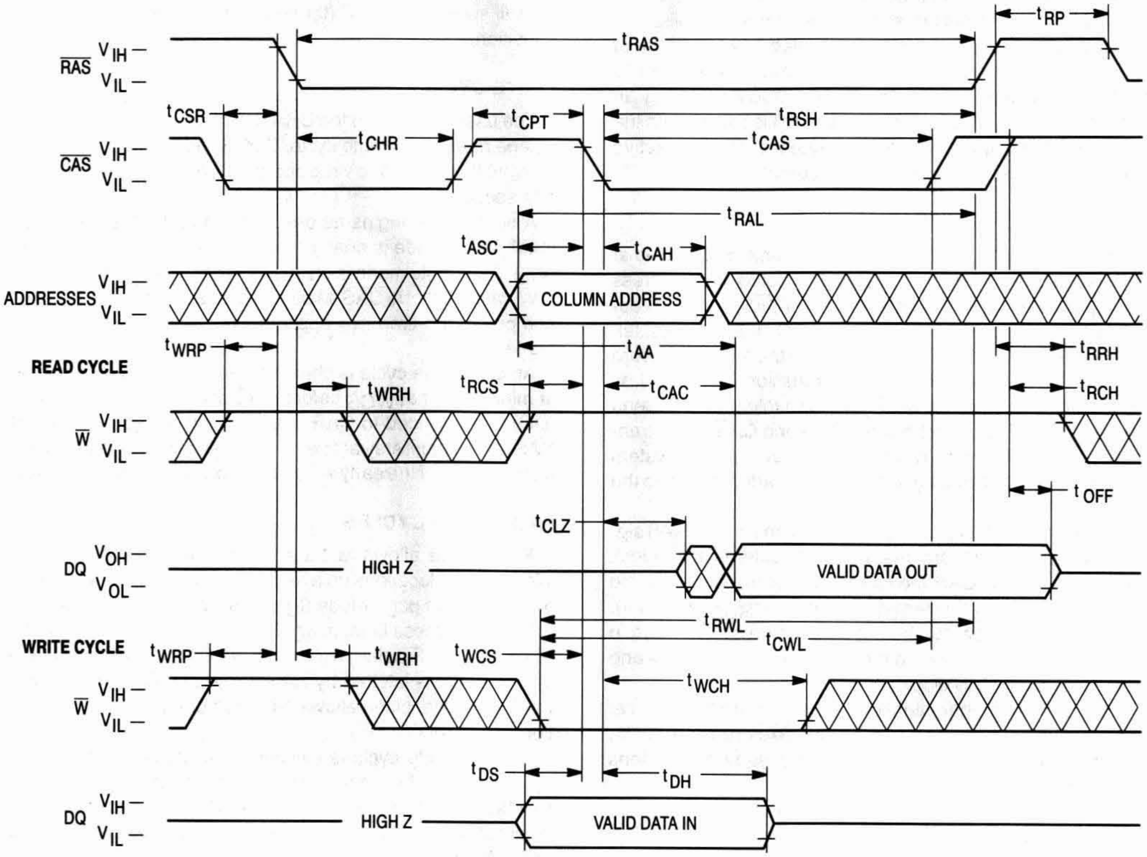
t_{RC}
t_{RC}
t_{RP}
t_{RP}
t_{RAS}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CRP}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADD
COLUMN ADDRESS
t_{RCS}
t_{WRP}
t_{RRH}
t_{WRH}
$\overline{W}$
V_{IH}
V_{IL}
t_{AA}
t_{CAC}
t_{CLZ}
t_{OFF}
t_{RAC}
DQ
V_{OH}
V_{OL}
VALID DATA OUT

HIDDEN REFRESH CYCLE (EARLY WRITE)



t_{RC}
t_{RC}
t_{RP}
t_{RP}
t_{RAS}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RCD}
t_{CHR}
t_{CRP}
t_{RSH}
t_{CRP}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADD
COLUMN ADDRESS
t_{WCS}
t_{WRP}
t_{WRH}
t_{WCH}
t_{WP}
$\overline{W}$
V_{IH}
V_{IL}
t_{DS}
t_{DH}
DQ
V_{IH}
V_{IL}
VALID DATA IN

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE


$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RAS}
t_{RP}
t_{CSR}
t_{CHR}
t_{CPT}
t_{RSH}
t_{CAS}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{RAL}
t_{ASC}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
COLUMN ADDRESS
t_{WRP}
t_{AA}
t_{RRH}
READ CYCLE
t_{WRH}
t_{RCS}
t_{CAC}
t_{RCH}
$\overline{\text{W}}$
V_{IH}
V_{IL}
t_{OFF}
t_{CLZ}
DQ
V_{OH}
V_{OL}
HIGH Z
VALID DATA OUT
t_{RWL}
t_{CWL}
WRITE CYCLE
t_{WRP}
t_{WRH}
t_{WCS}
t_{WCH}
$\overline{\text{W}}$
V_{IH}
V_{IL}
t_{DS}
t_{DH}
DQ
V_{IH}
V_{IL}
HIGH Z
VALID DATA IN

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 word locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the module: **$\overline{\text{RAS}}$ only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either a "normal" random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. $\overline{\text{CAS}}$ controls read access time: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ clock active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with either an early write or a page mode early write cycle. Early write mode is discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early write mode is distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (DQ) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM32230 require refresh every 16 milliseconds, while refresh time for the MCM32L230 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM32230, and 124.8 microseconds for the MCM32L230. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM32230 and 128 milliseconds on the MCM32L230.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decodes. Three other methods of refresh, **RAS-only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure that all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode cycle) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a CAS before RAS refresh counter test. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 1024 test cycles, as indicated by the check data written in each row. See CAS before RAS refresh counter test cycle timing diagram.

The test can be performed only after a minimum of **8 CAS before RAS** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **CAS before RAS refresh counter test, read cycle**. Repeat this operation 1024 times.
3. Select a column address, and write "1" into the cell by performing **CAS before RAS refresh counter test, write cycle**. Repeat this operation 1024 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

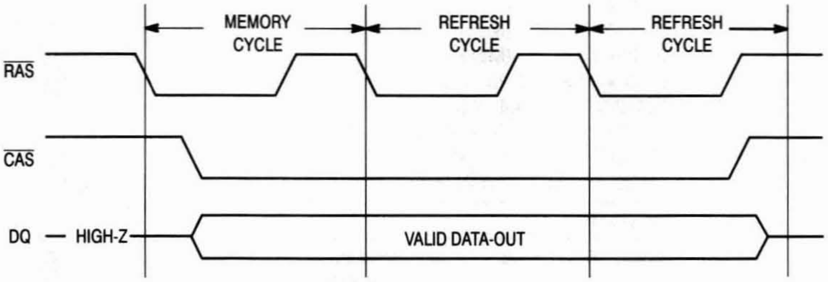


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION

(Order by Full Part Number)

MCM 32230 or 32L230 X XX

Motorola Memory Prefix — MCM
Part Number — 32230 or 32L230
Package (SH = SIMM, SHG = Gold Pad SIMM) — X
Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers —

MCM32230SH60	MCM32230SHG60
MCM32230SH70	MCM32230SHG70
MCM32230SH80	MCM32230SHG80
MCM32L230SH60	MCM32L230SHG60
MCM32L230SH70	MCM32L230SHG70
MCM32L230SH80	MCM32L230SHG80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

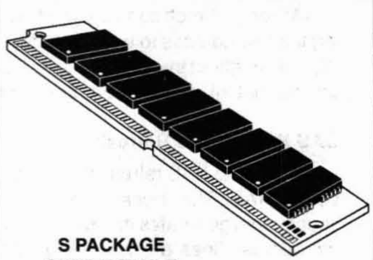
MCM32400

Product Preview

4M x 32 Bit Dynamic Random Access Memory Module

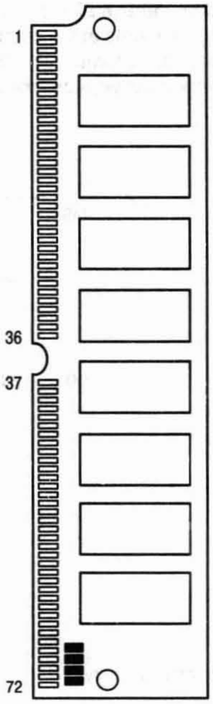
The MCM32400 is a dynamic random access memory (DRAM) module organized as 4,194,304 x 32 bits. The module is a 72-lead single-in-line memory module (SIMM) consisting of eight MCM517400 DRAMs housed in 400 mil J-lead small outline packages (SOJ) mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM517400 is a CMOS high-speed dynamic random access memory organized as 4,194,034 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh:
  MCM32400 = 32 ms
- Consists of Eight 4M x 4 DRAMs and Eight 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM32400-60 = 60 ns (Max)
  MCM32400-70 = 70 ns (Max)
  MCM32400-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM32400-60 = 5.28 W (Max)
  MCM32400-70 = 4.4 W (Max)
  MCM32400-80 = 3.74 W (Max)
- Low Standby Power Dissipation: TTL Levels = 88 mW (Max)
  CMOS Levels = 44 mW (Max)



S PACKAGE
SIMM MODULE
CASE 866-02

TOP VIEW



PIN NAMES

A0 – A10	Address Inputs	DQ0 – DQ31	Data Input/Output
$\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$	Column Address Strobe	PD1 – PD4	Presence Detect
$\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$	Row Address Strobe	$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)	V_{SS}	Ground
NC	No Connection		

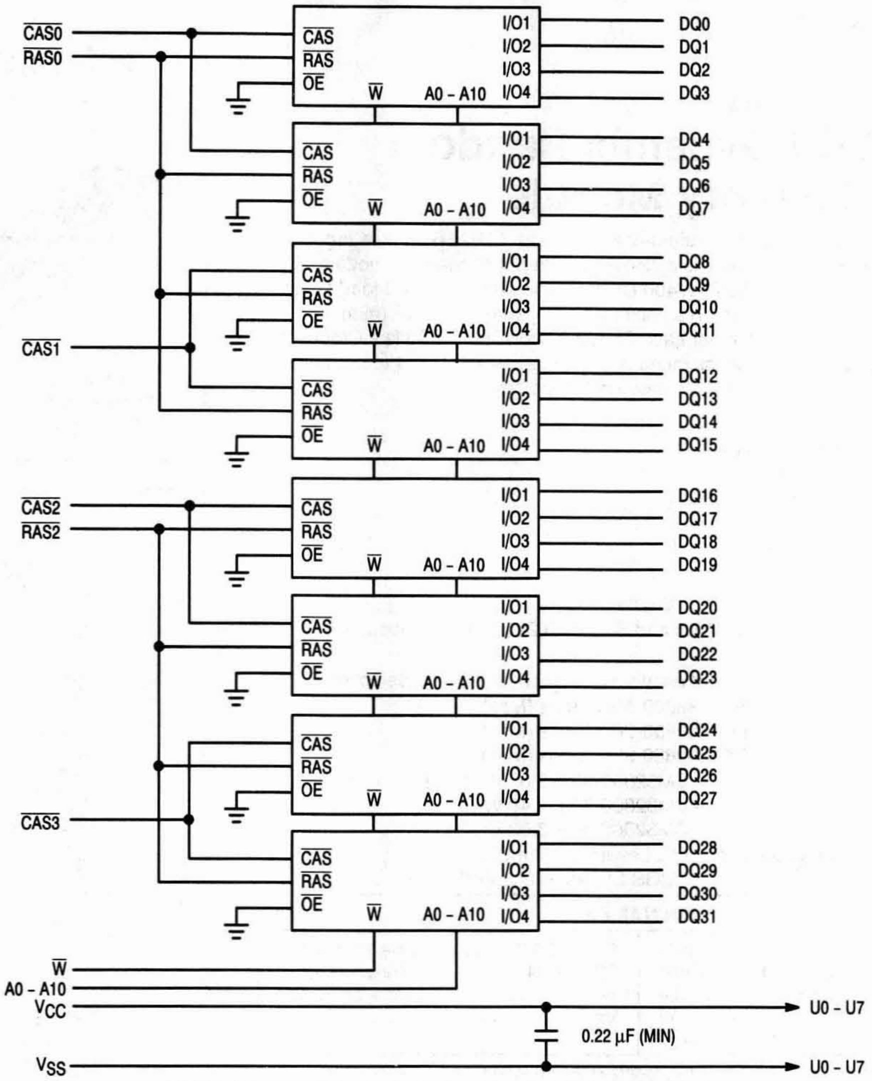
All power supply and ground pins must be connected for proper operation of the device.

PIN ASSIGNMENT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{\text{CAS2}}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{\text{CAS3}}$	54	DQ26	66	NC
7	DQ18	19	A10	31	A8	43	$\overline{\text{CAS1}}$	55	DQ11	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{\text{RAS0}}$	56	DQ27	68	PD2
9	DQ19	21	DQ20	33	NC	45	NC	57	DQ12	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{\text{RAS2}}$	46	NC	58	DQ28	70	PD4
11	NC	23	DQ21	35	NC	47	$\overline{\text{W}}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM


CAS0
RAS0
CAS1
CAS2
RAS2
CAS3
CAS
RAS
OE
W
A0 - A10
I/O1
I/O2
I/O3
I/O4
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
W
A0 - A10
V_{CC}
V_{SS}
U0 - U7
0.22 µF (MIN)
U0 - U7

PRESENCE DETECT PIN OUT			
Pin Name	**60 ns**	**70 ns**	**80 ns**
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	NC	NC	NC
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

ORDERING INFORMATION
(Order by Full Part Number)

MCM 32400 X XX

Motorola Memory Prefix — MCM

Part Number — 32400

Package (S = SIMM, SG = Gold Pad SIMM) — X

Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers —		
	MCM32400S60	MCM32400SG60
	MCM32400S70	MCM32400SG70
	MCM32400S80	MCM32400SG80

NOTE: For mechanical data, please see Chapter 10.

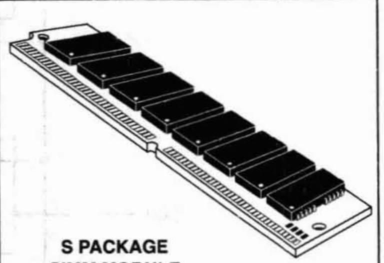
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM32800

Product Preview

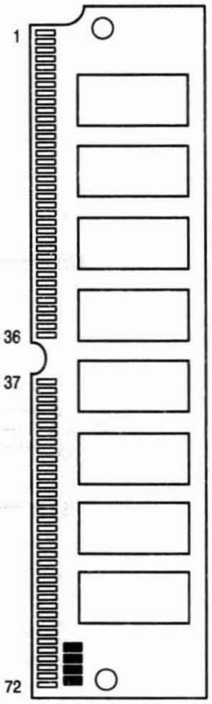
8M x 32 Bit Dynamic Random Access Memory Module

The MCM32800 is a dynamic random access memory (DRAM) module organized as 8,388,608 x 32 bits. The module is a 72-lead single-in-line memory module (SIMM) consisting of sixteen MCM517400 DRAMs housed in 400 mil J-lead small outline packages (SOJ), mounted on a substrate along with a 0.22 μF (min) decoupling capacitor mounted under each DRAM. The MCM517400 is a CMOS high-speed dynamic random access memory organized as 4,194,304 four-bit words and fabricated with CMOS silicon-gate process technology.


S PACKAGE
SIMM MODULE
CASE 866-02

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh: MCM32800 = 32 ms
- Consists of Sixteen 4M x 4 DRAMs and Sixteen 0.22 μF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM32800-60 = 60 ns (Max)
  MCM32800-70 = 70 ns (Max)
  MCM32800-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM32800-60 = 5.37 W (Max)
  MCM32800-70 = 4.49 W (Max)
  MCM32800-80 = 3.83 W (Max)
- Low Standby Power Dissipation: TTL Levels = 176 mW (Max)
  CMOS Levels = 88 mW (Max)

TOP VIEW



PIN NAMES			
A0 – A10	Address Inputs	DQ0 – DQ31	Data Input/Output
$\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$	Column Address Strobe	PD1 – PD4	Presence Detect
$\overline{\text{RAS0}}$ – $\overline{\text{RAS3}}$	Row Address Strobe	$\overline{\text{W}}$	Write Enable
V_{CC}	Power (+ 5 V)	V_{SS}	Ground
NC	No Connection		

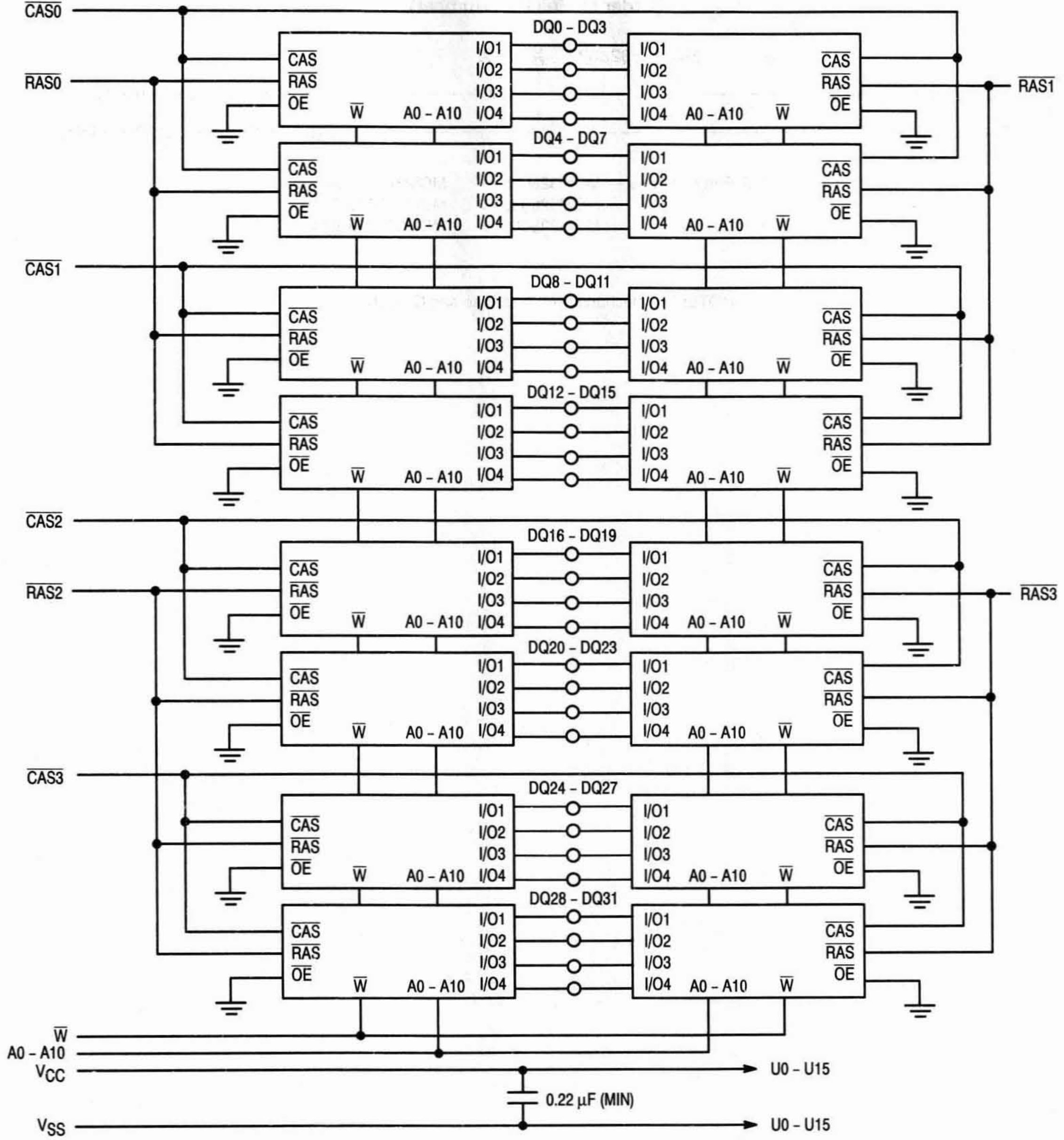
All power supply and ground pins must be connected for proper operation of the device.

PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{\text{CAS2}}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{\text{CAS3}}$	54	DQ26	66	NC
7	DQ18	19	A10	31	A8	43	$\overline{\text{CAS1}}$	55	DQ11	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{\text{RAS0}}$	56	DQ27	68	PD2
9	DQ19	21	DQ20	33	$\overline{\text{RAS3}}$	45	$\overline{\text{RAS1}}$	57	DQ12	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{\text{RAS2}}$	46	NC	58	DQ28	70	PD4
11	NC	23	DQ21	35	NC	47	$\overline{\text{W}}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



CAS0
RAS0
CAS1
CAS2
RAS2
CAS3
RAS1
RAS3
DQ0 - DQ3
DQ4 - DQ7
DQ8 - DQ11
DQ12 - DQ15
DQ16 - DQ19
DQ20 - DQ23
DQ24 - DQ27
DQ28 - DQ31
CAS
RAS
OE
W
A0 - A10
I/O1
I/O2
I/O3
I/O4
W
A0 - A10
VCC
VSS
U0 - U15
0.22 µF (MIN)
U0 - U15

PRESENCE DETECT PIN OUT			
Pin Name	**60 ns**	**70 ns**	**80 ns**
PD1	NC	NC	NC
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

ORDERING INFORMATION
(Order by Full Part Number)

MCM 32800 X XX

Motorola Memory Prefix — MCM

Part Number — 32800

Package (S = SIMM, SG = Gold Pad SIMM) — X

Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers — MCM32800S60 MCM32800SG60
MCM32800S70 MCM32800SG70
MCM32800S80 MCM32800SG80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

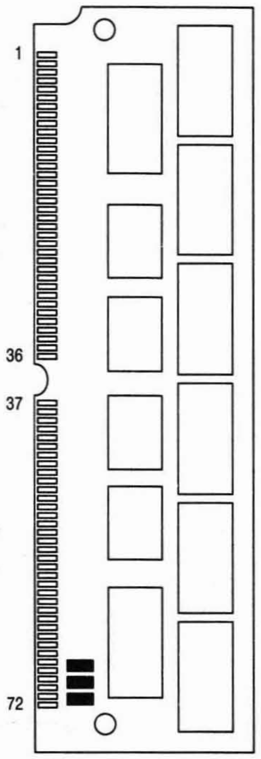
MCM36256

256K x 36 Bit Dynamic Random Access Memory Module

The MCM36256 is a 9M dynamic random access memory (DRAM) module organized as 262,144 x 36 bits. The module is a 72-lead single-in-line memory module (SIMM) consisting of eight MCM514256A DRAMs housed in 20/26 J-lead small outline packages (SOJ) and four CMOS 256K x 1 DRAMs housed in 18-lead PLCC packages, mounted on a substrate along with a 0.22 μF (min) decoupling capacitor mounted under each DRAM. The MCM514256A is a 1.0μ CMOS high-speed dynamic random access memory organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM36256 = 8 ms (Max)
- Consists of Eight 256K x 4 DRAMs, Four 256K x 1 DRAMS, and Twelve 0.22 μF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM36256-70 = 70 ns (Max)
  MCM36256-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM36256-70 = 5.17 W (Max)
  MCM36256-80 = 4.51 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 132 mW (Max)
  CMOS Levels = 66 mW (Max)

S PACKAGE
SIMM MODULE
CASE 866-02



PIN ASSIGNMENTS

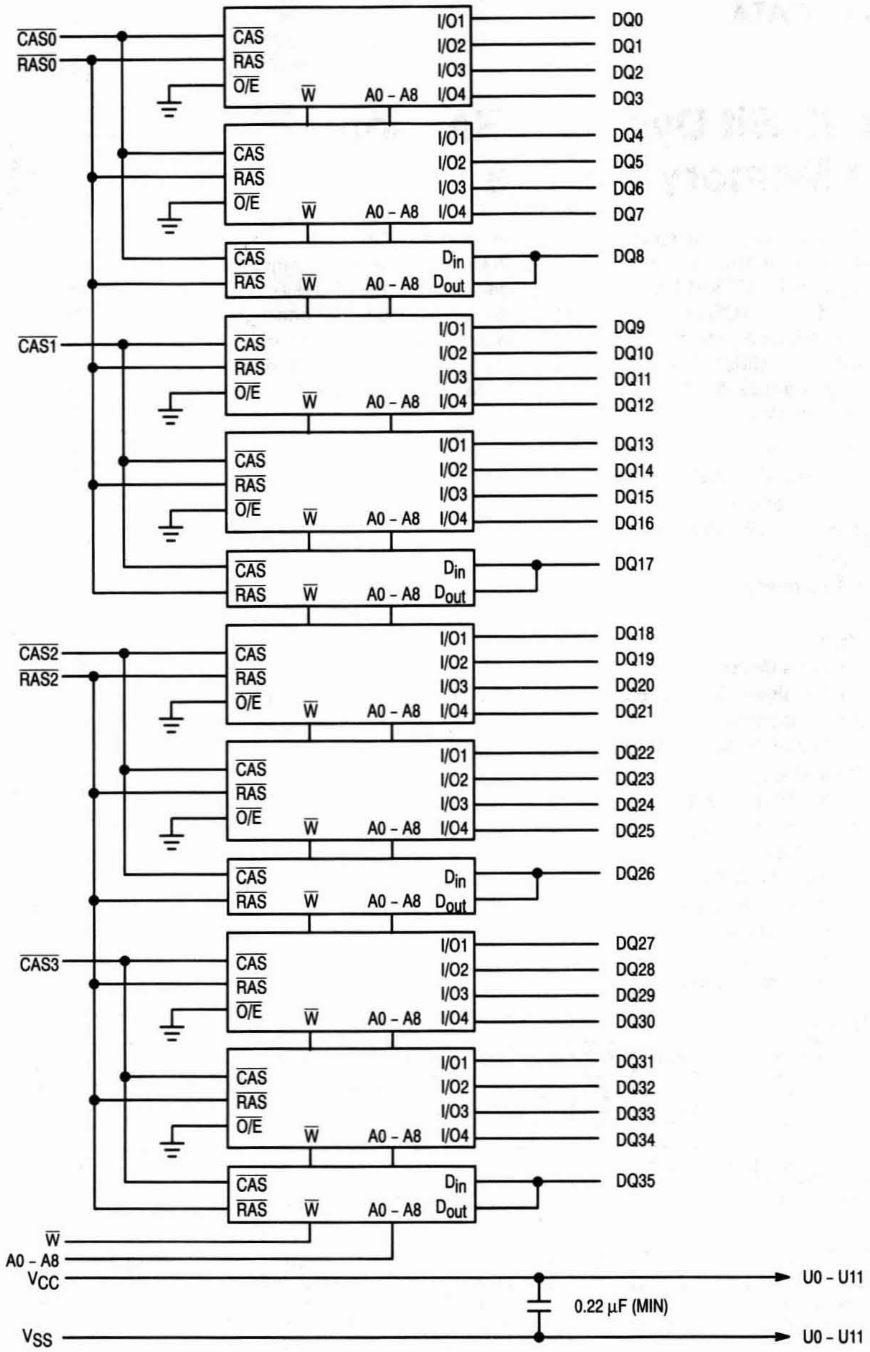
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{\text{CAS2}}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{\text{CAS3}}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{\text{CAS1}}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	NC	44	$\overline{\text{RAS0}}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{\text{RAS2}}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	DQ26	47	$\overline{\text{W}}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

PIN NAMES

A0 – A8	Address Inputs
DQ0 – DQ35	Data Input/Output
$\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$	Column Address Strobe
PD1 – PD4	Presence Detect
$\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

BLOCK DIAGRAM


$\overline{\text{CAS0}}$
$\overline{\text{RAS0}}$
$\overline{\text{CAS1}}$
$\overline{\text{CAS2}}$
$\overline{\text{RAS2}}$
$\overline{\text{CAS3}}$
$\overline{\text{CAS}}$
$\overline{\text{RAS}}$
$\overline{\text{O/E}}$
$\overline{\text{W}}$
A0 – A8
I/O1
I/O2
I/O3
I/O4
D_{in}
D_{out}
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
DQ32
DQ33
DQ34
DQ35
$\overline{\text{W}}$
A0 – A8
V_{CC}
V_{SS}
0.22 µF (MIN)
U0 – U11
U0 – U11

PRESENCE DETECT PIN OUT		
Pin Name	**70 ns**	**80 ns**
PD1	V_{SS}	V_{SS}
PD2	NC	NC
PD3	V_{SS}	NC
PD4	NC	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	7.05	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	MCM36256-70, t_{RC} = 130 ns MCM36256-80, t_{RC} = 150 ns	I_{CC1}	— —	940 820	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	24	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles	MCM36256-70, t_{RC} = 130 ns MCM36256-80, t_{RC} = 150 ns	I_{CC3}	— —	940 820	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle	MCM36256-70, t_{PC} = 40 ns MCM36256-80, t_{PC} = 45 ns	I_{CC4}	— —	680 560	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)		I_{CC5}	—	12	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	MCM36256-70, t_{RC} = 130 ns MCM36256-80, t_{RC} = 150 ns	I_{CC6}	— —	940 820	mA	1
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)		$I_{lkg(I)}$	– 120	+ 120	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)		$I_{lkg(O)}$	– 10	+ 10	µA	
Output High Voltage (I_{OH} = – 5 mA)		V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit
Input Capacitance (A0 – A8)	C_{I1}	—	75	pF
Input Capacitance ($\overline{W}$)	C_{I2}	—	94	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I3}	—	52	pF
Input Capacitance ($\overline{CAS0}$ – $\overline{CAS3}$)	C_{I4}	—	31	pF
I/O Capacitance (DQ0 – DQ7, DQ9 – DQ16, DQ18 – DQ25, DQ27 – DQ34)	C_{DQ1}	—	17	pF
I/O Capacitance (DQ8, DQ17, DQ26, DQ35)	C_{DQ2}	—	22	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\,\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM36256-70		MCM36256-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELAX}	t_{AR}	55	—	60	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13

NOTES: (continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

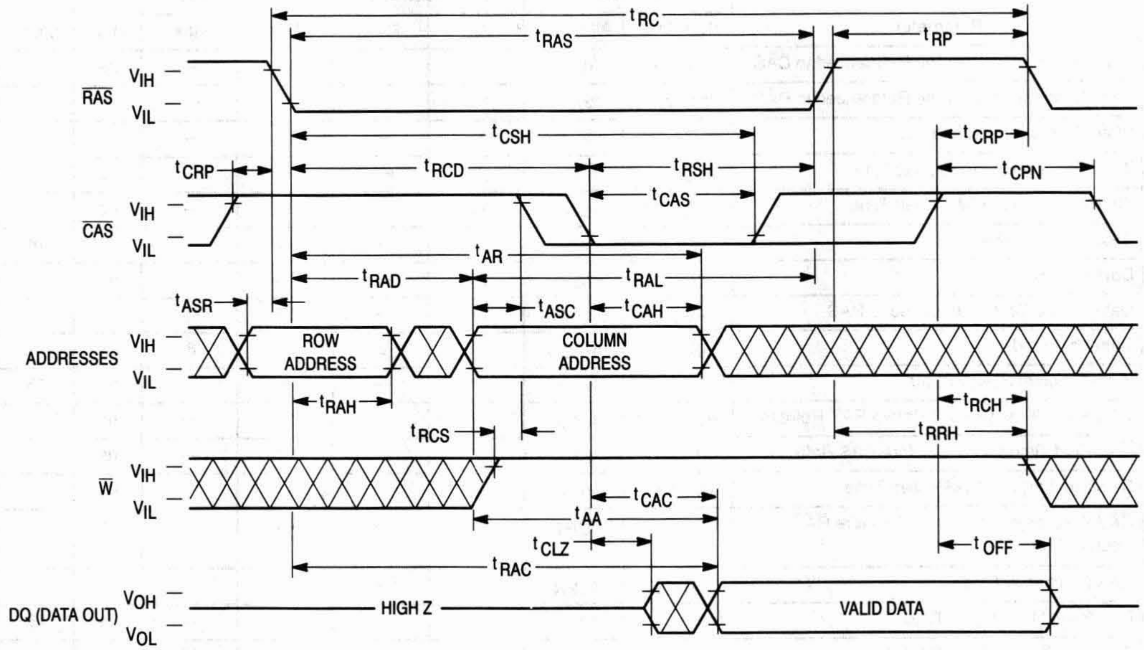
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM36256-70		MCM36256-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	15	—	15	—	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELWH}	t_{WCR}	55	—	60	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	55	—	60	—	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	—	8	—	8	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	ns	
Fast Page Mode Cycle Time	$t_{CELCELP}$	t_{PCP}	45	—	45	—	ns	16
Output Buffer and Turn-Off Delay	t_{CEHQZP}	t_{OFFP}	0	25	0	25	ns	10, 16
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQVP}	t_{CPAP}	—	45	—	45	ns	6, 16

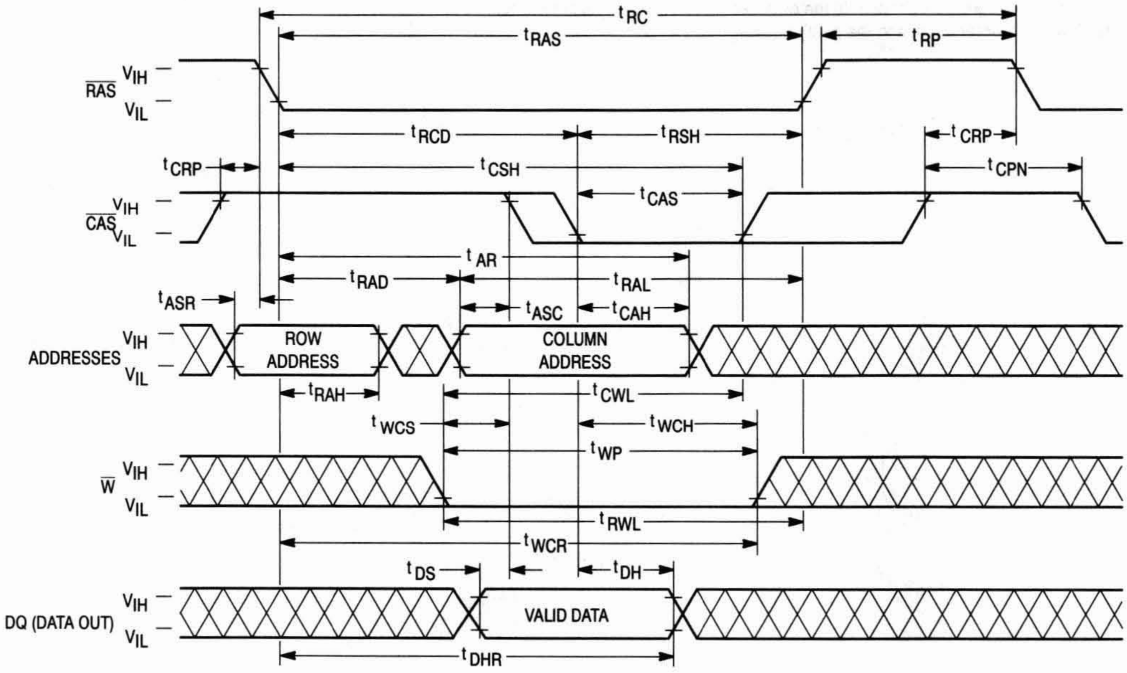
NOTES:

14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.
16. This parameter applies to the parity bits only.

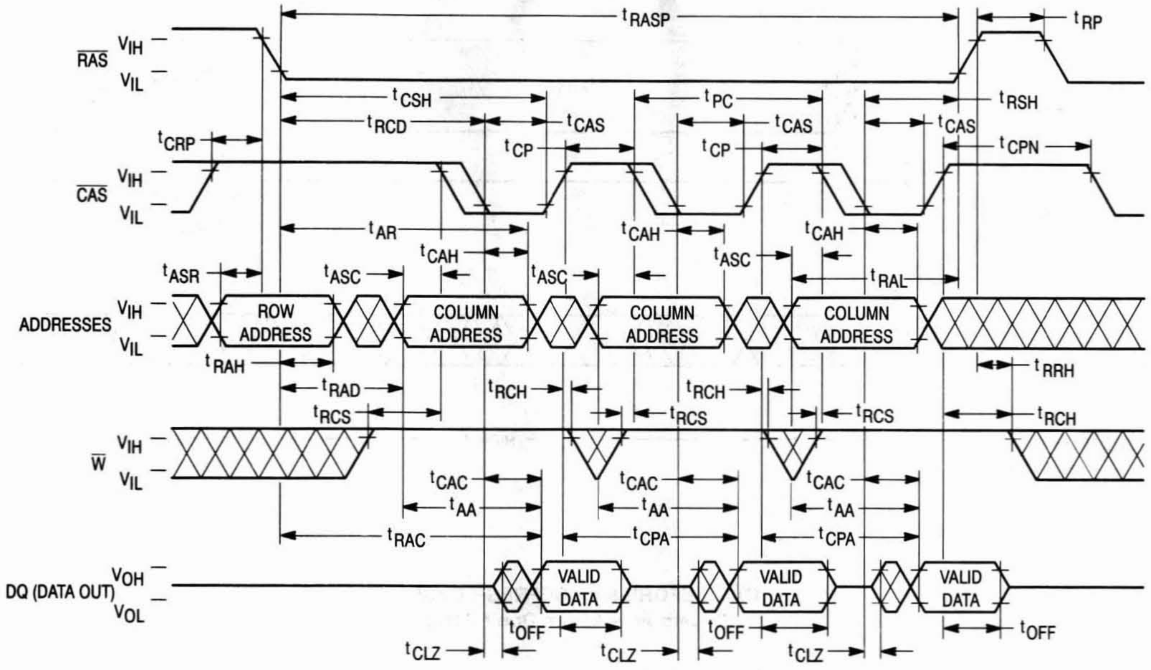
READ CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tCRP
tRCD
tRSH
tCPN
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W
VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
DQ (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA

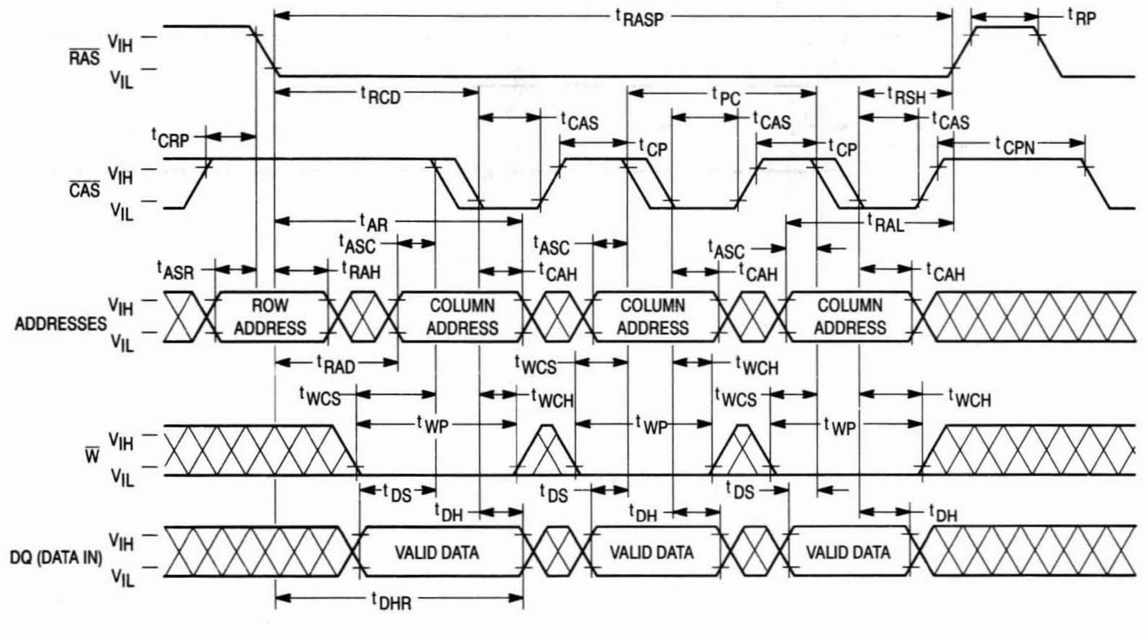
EARLY WRITE CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tRCD
tRSH
tCRP
tCRP
tCSH
tCPN
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWP
W
VIH
VIL
tRWL
tWCR
tDS
tDH
DQ (DATA OUT)
VIH
VIL
VALID DATA
tDHR

FAST PAGE MODE READ CYCLE

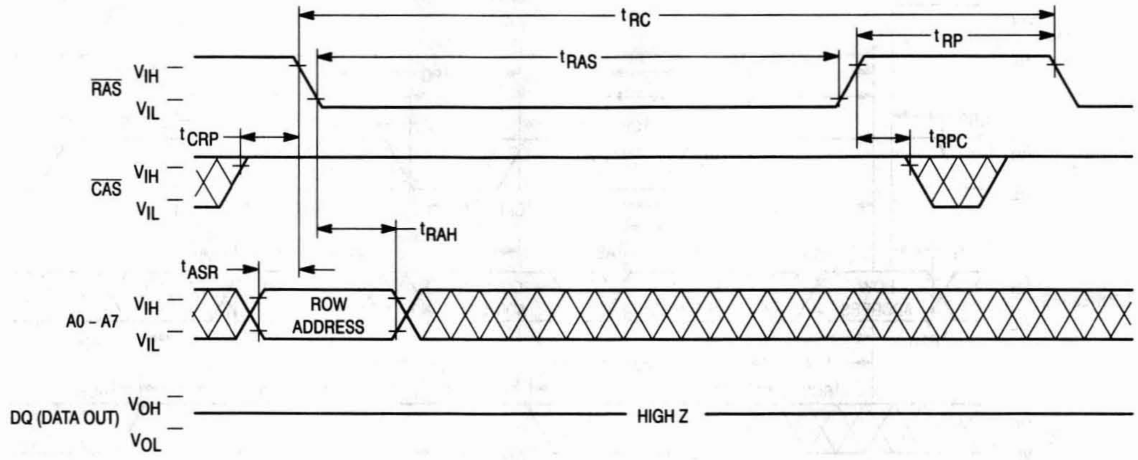

RAS
V_IH
V_IL
CAS
ADDRESSES
W
DQ (DATA OUT)
V_OH
V_OL
t_RASP
t_RP
t_CSH
t_PC
t_RSH
t_RCD
t_CAS
t_CRP
t_CP
t_CPN
t_AR
t_CAH
t_ASR
t_ASC
t_RAL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
t_RAH
t_RAD
t_RCS
t_RCH
t_RRH
t_CAC
t_AA
t_RAC
t_CPA
VALID DATA
VALID DATA
VALID DATA
t_OFF
t_CLZ

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)


RAS
V_IH
V_IL
CAS
ADDRESSES
W
DQ (DATA IN)
t_RASP
t_RP
t_RCD
t_PC
t_RSH
t_CAS
t_CRP
t_CP
t_CPN
t_AR
t_RAL
t_ASC
t_ASR
t_RAH
t_CAH
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
t_RAD
t_WCS
t_WCH
t_WP
t_DS
t_DH
VALID DATA
VALID DATA
VALID DATA
t_DHR

$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

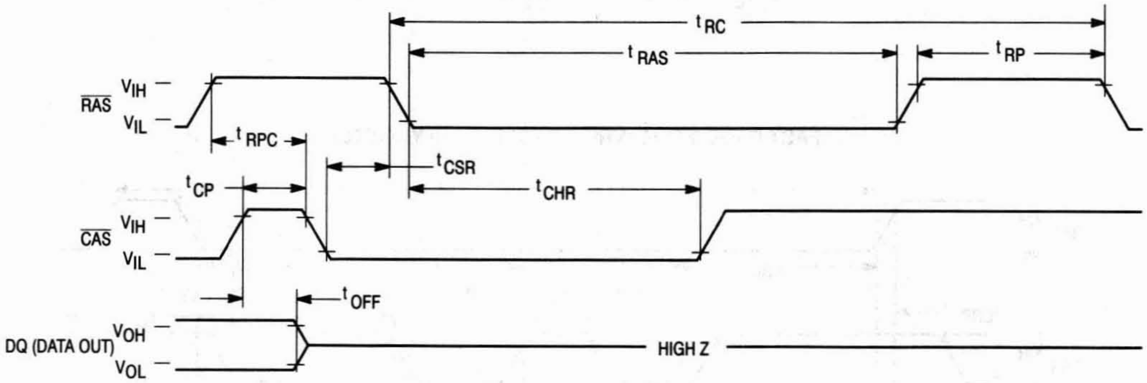
($\overline{\text{W}}$ and A8 are Don't Care)



t_{RC}
t_{RP}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
A0 – A7
V_{IH}
V_{IL}
ROW ADDRESS
DQ (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

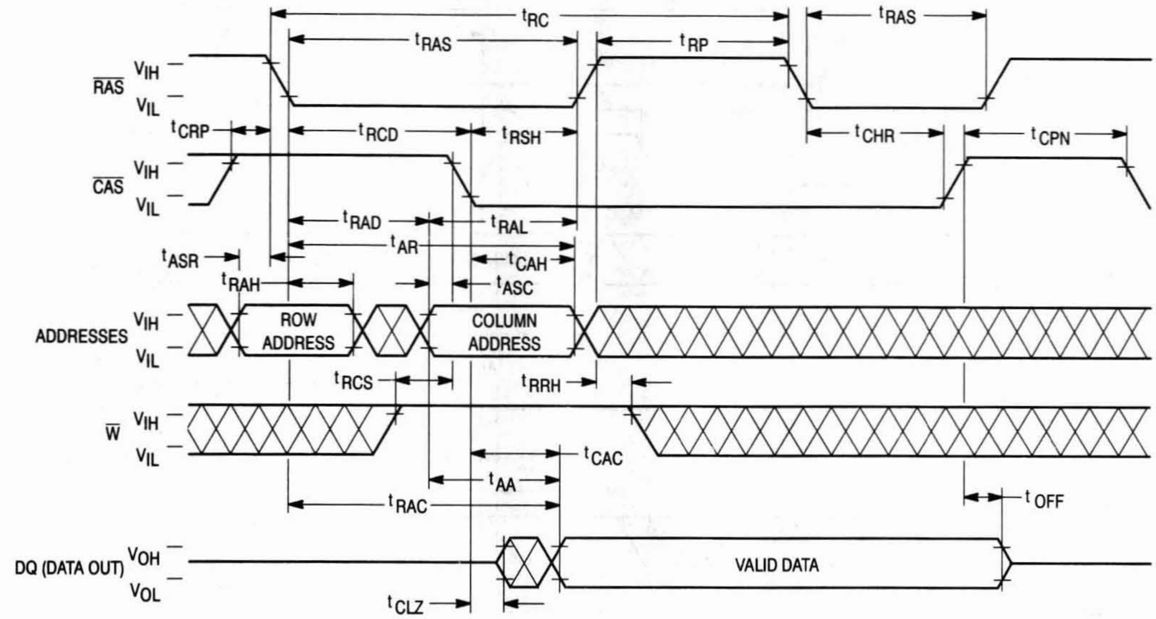
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{W}}$ and A0 – A8 are Don't Care)



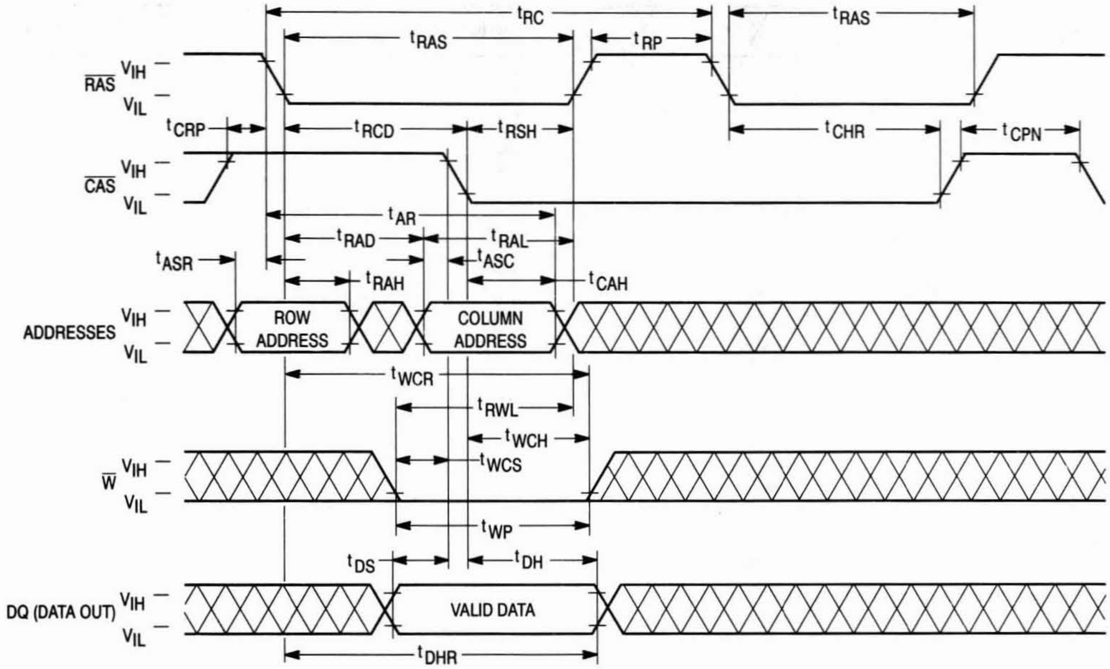
t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RPC}
t_{CSR}
t_{CP}
t_{CHR}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{OFF}
DQ (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

HIDDEN REFRESH CYCLE (READ)



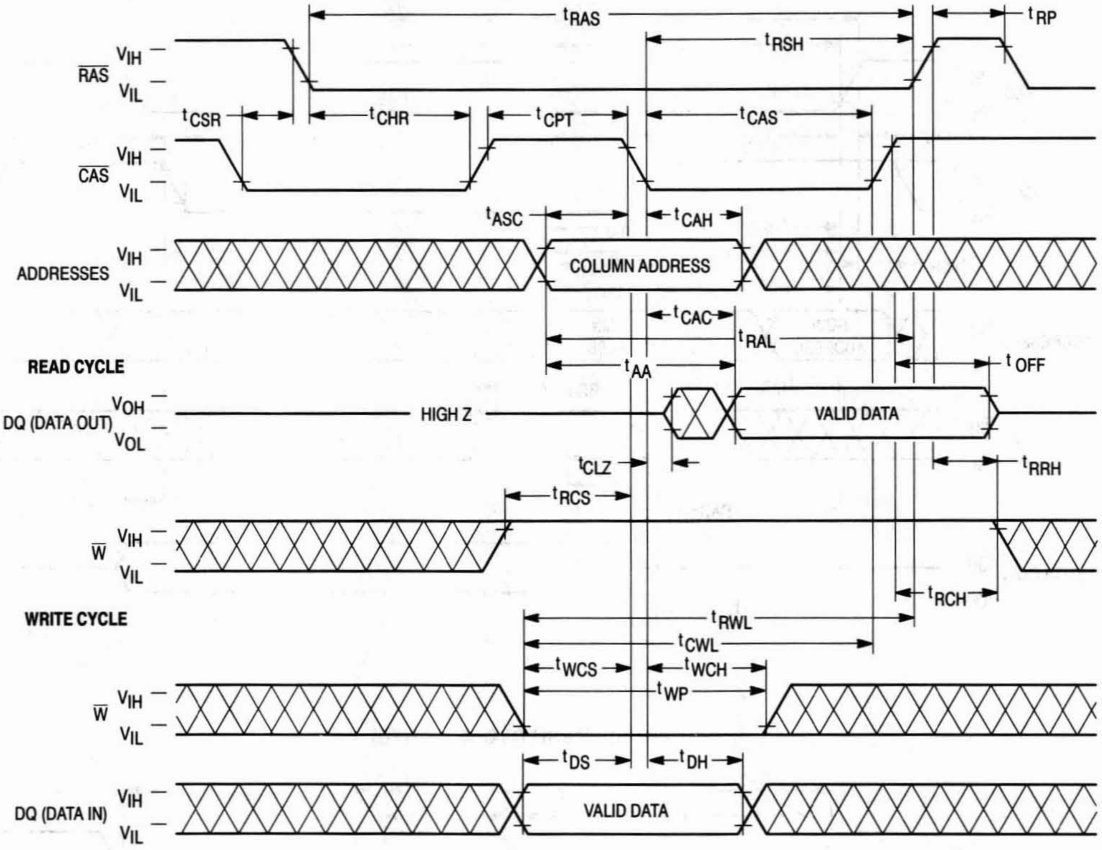
t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CPN}
$\overline{CAS}$
t_{RAD}
t_{RAL}
t_{AR}
t_{CAH}
t_{ASR}
t_{RAH}
t_{ASC}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{RCS}
t_{RRH}
$\overline{W}$
t_{CAC}
t_{AA}
t_{RAC}
t_{OFF}
DQ (DATA OUT)
V_{OH}
V_{OL}
VALID DATA
t_{CLZ}

HIDDEN REFRESH CYCLE (WRITE)



t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CPN}
$\overline{CAS}$
t_{AR}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
t_{WCR}
t_{RWL}
t_{WCH}
t_{WCS}
$\overline{W}$
t_{WP}
t_{DS}
t_{DH}
DQ (DATA OUT)
VALID DATA
t_{DHR}

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



tRAS
tRP
tRSH
$\overline{\text{RAS}}$
VIH
VIL
tCSR
tCHR
tCPT
tCAS
$\overline{\text{CAS}}$
tASC
tCAH
ADDRESSES
COLUMN ADDRESS
tCAC
tRAL
READ CYCLE
tAA
tOFF
DQ (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA
tCLZ
tRRH
tRCS
$\overline{\text{W}}$
tRCH
WRITE CYCLE
tRWL
tCWL
tWCS
tWCH
tWP
tDS
tDH
DQ (DATA IN)
VALID DATA

5

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 word locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This gate feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are two other variations in addressing the module: **$\overline{\text{RAS}}$-only refresh cycle** and **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either a normal random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. $\overline{\text{CAS}}$ controls read access time; $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} after the inactive transition.

WRITE CYCLE

The DRAM may be written by either an early write or a page mode early write cycle. Early write mode is discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early write mode is distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data In (DQ) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 512 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature; therefore, each bit must be periodically refreshed (recharged) to maintain the correct bit state. Bits in the MCM36256 require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM36256. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM36256.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order actives an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read cycle**. Repeat this operation 512 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, write cycle**. Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

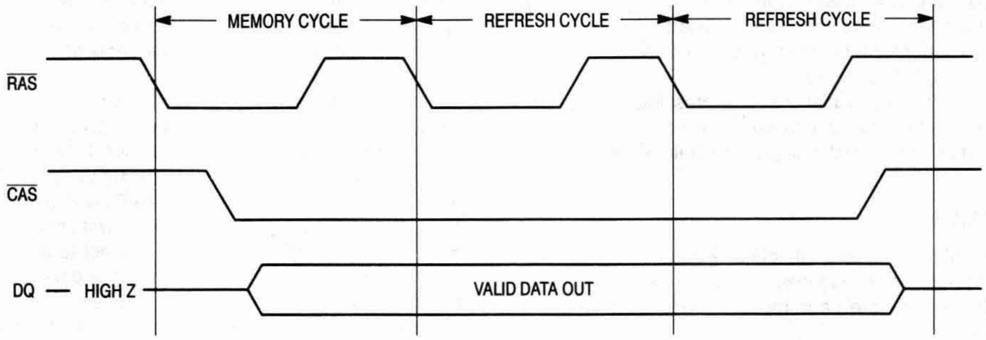


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION

(Order by Full Part Number)

MCM 36256 X XX

Motorola Memory Prefix — MCM
Part Number — 36256
Package (S = SIMM, SG = Gold Pad SIMM) — X
Speed (70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers — MCM36256S70 MCM36256SG70
MCM36256S80 MCM36256SG80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

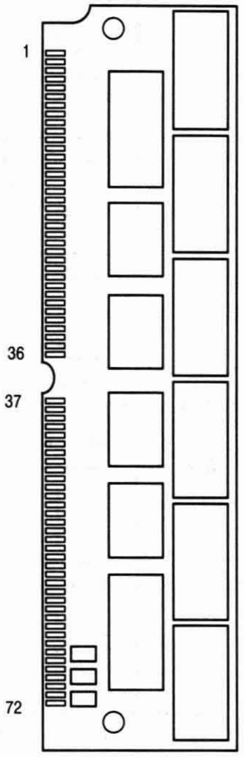
MCM36512

512K x 36 Bit Dynamic Random Access Memory Module

The MCM36512 is an 18M dynamic random access memory (DRAM) module organized as 524,288 x 36 bits. The module is a 72-lead double-sided single-in-line memory module (SIMM) consisting of sixteen MCM514256A DRAMs housed in 20/26 J-lead small outline packages (SOJ) and eight CMOS 256K x 1 DRAMs housed in 18-lead PLCC packages, mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM514256A is a 1.0µ CMOS high-speed dynamic random access memory organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh: MCM36512 = 8 ms (Max)
- Consists of Sixteen 256K x 4 DRAMs, Eight 256K x 1 DRAMs, and Twenty Four 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM36512-70 = 70 ns (Max)
  MCM36512-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM36512-70 = 5.302 W (Max)
  MCM36512-80 = 4.642 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 264 mW (Max)
  CMOS Levels = 132 mW (Max)

S PACKAGE
SIMM MODULE
CASE 866-02



PIN ASSIGNMENTS

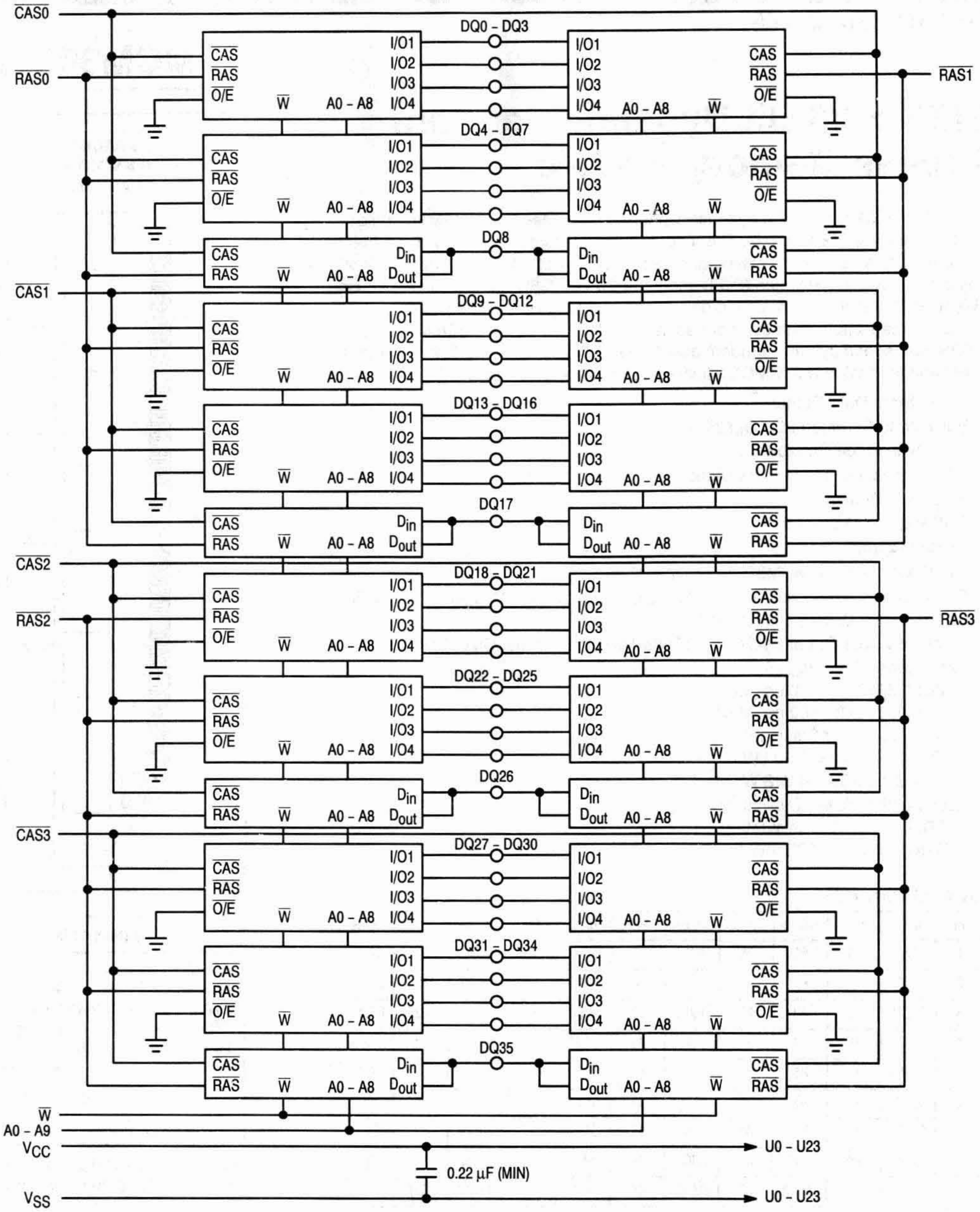
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	NC	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

PIN NAMES

A0 – A8	Address Inputs
DQ0 – DQ35	Data Input/Output
$\overline{CAS0}$ – $\overline{CAS3}$	Column Address Strobe
PD1 – PD4	Presence Detect
$\overline{RAS0}$ – $\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

BLOCK DIAGRAM


$\overline{CAS0}$
$\overline{RAS0}$
$\overline{CAS1}$
$\overline{CAS2}$
$\overline{RAS2}$
$\overline{CAS3}$
$\overline{RAS1}$
$\overline{RAS3}$
DQ0 - DQ3
DQ4 - DQ7
DQ8
DQ9 - DQ12
DQ13 - DQ16
DQ17
DQ18 - DQ21
DQ22 - DQ25
DQ26
DQ27 - DQ30
DQ31 - DQ34
DQ35
$\overline{CAS}$
$\overline{RAS}$
$\overline{O/E}$
$\overline{W}$
A0 - A8
I/O1
I/O2
I/O3
I/O4
D_{in}
D_{out}
$\overline{W}$
A0 - A9
V_{CC}
V_{SS}
0.22 µF (MIN)
U0 - U23
U0 - U23

PRESENCE DETECT PIN OUT		
Pin Name	**70 ns**	**80 ns**
PD1	NC	NC
PD2	V_{SS}	V_{SS}
PD3	V_{SS}	NC
PD4	NC	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	7.23	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM36512-70, t_{RC} = 130 ns MCM36512-80, t_{RC} = 150 ns	I_{CC1}	— —	964 844	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	48	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles MCM36512-70, t_{RC} = 130 ns MCM36512-80, t_{RC} = 150 ns	I_{CC3}	— —	964 844	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM36512-70, t_{PC} = 40 ns MCM36512-80, t_{PC} = 45 ns	I_{CC4}	— —	704 584	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	24	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM36512-70, t_{RC} = 130 ns MCM36512-80, t_{RC} = 150 ns	I_{CC6}	— —	964 844	mA	1
Input Leakage Current ($V_{SS} \leq V_{in} \leq V_{CC}$)	$I_{lkg(I)}$	– 240	240	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \leq V_{out} \leq V_{CC}$)	$I_{lkg(O)}$	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit
Input Capacitance (A0 – A8)	C_{I1}	—	138	pF
Input Capacitance ($\overline{\text{W}}$)	C_{I2}	—	178	pF
Input Capacitance ($\overline{\text{RAS0}}$ – $\overline{\text{RAS3}}$)	C_{I3}	—	52	pF
Input Capacitance ($\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$)	C_{I4}	—	52	pF
I/O Capacitance (DQ0 – DQ7, DQ9 – DQ16, DQ18 – DQ25, DQ27 – DQ34)	C_{DQ1}	—	24	pF
I/O Capacitance (DQ8, DQ17, DQ26, DQ35)	C_{DQ2}	—	34	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\,\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM36512-70		MCM36512-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold TIme	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	ns	12

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

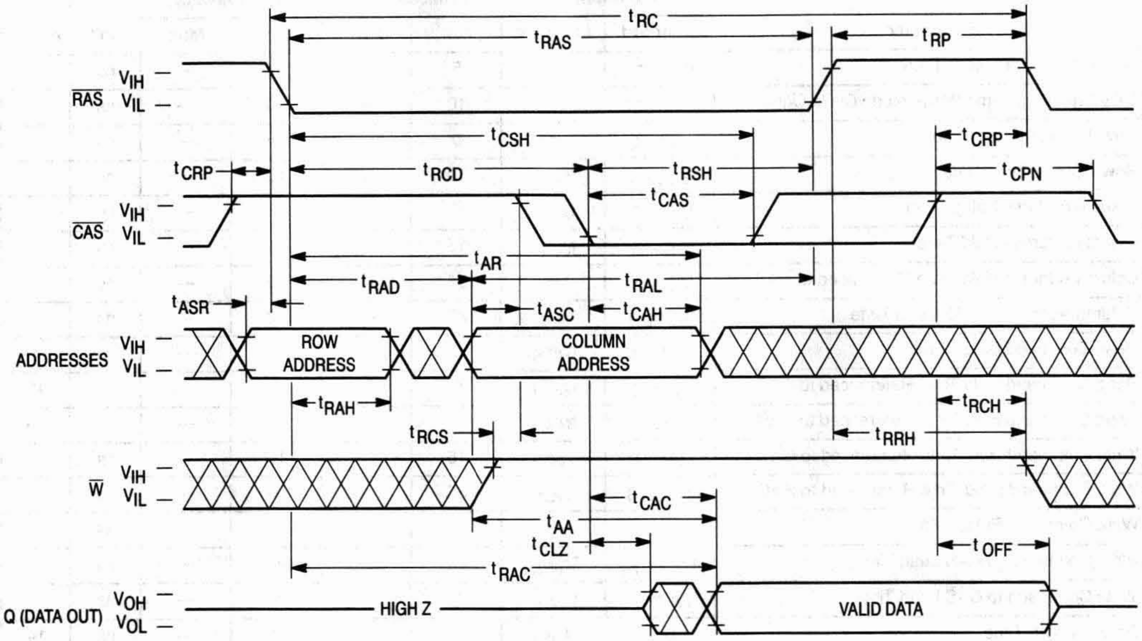
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM36512-70		MCM36512-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELAX}	t_{AR}	55	—	60	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	15	—	15	—	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELWH}	t_{WCR}	55	—	60	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	55	—	60	—	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	—	8	—	8	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	ns	
Fast Page Mode Cycle Time	$t_{CELCELP}$	t_{PCP}	45	—	45	—	ns	17
Output Buffer and Turn–Off Delay	t_{CEHQZP}	t_{OFFP}	0	25	0	25	ns	10,17
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQVP}	t_{CPAP}		45		45	ns	6,17

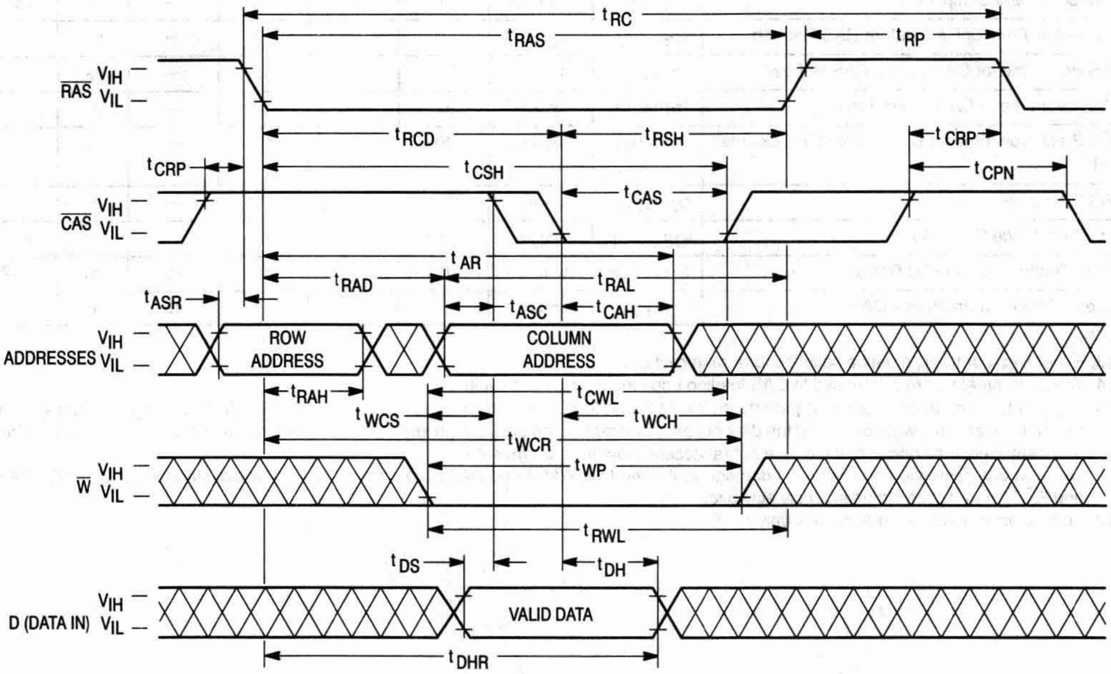
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.
16. To avoid bus contention and potential damage to the module, $\overline{\text{RAS0}}$ and $\overline{\text{RAS1}}$ may not be active low simultaneously. Similarly, $\overline{\text{RAS2}}$ and $\overline{\text{RAS3}}$ may not be simultaneously active low.
17. This parameter applies to parity bits only.

READ CYCLE


tRC
tRAS
tRP
RAS VIH
VIL
tCSH
tCRP
tCRP
tRCD
tRSH
tCPN
tCAS
CAS VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
Q (DATA OUT) VOH
VOL
HIGH Z
VALID DATA

EARLY WRITE CYCLE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tRAS
tRP
RAS VIH
VIL
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tCRP
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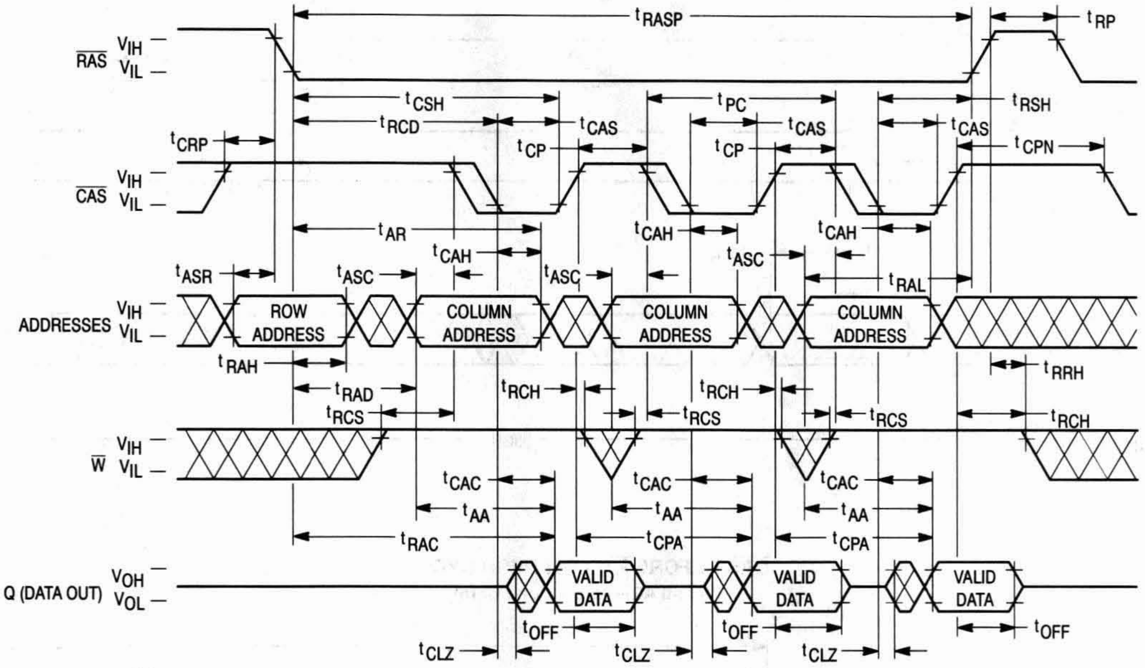
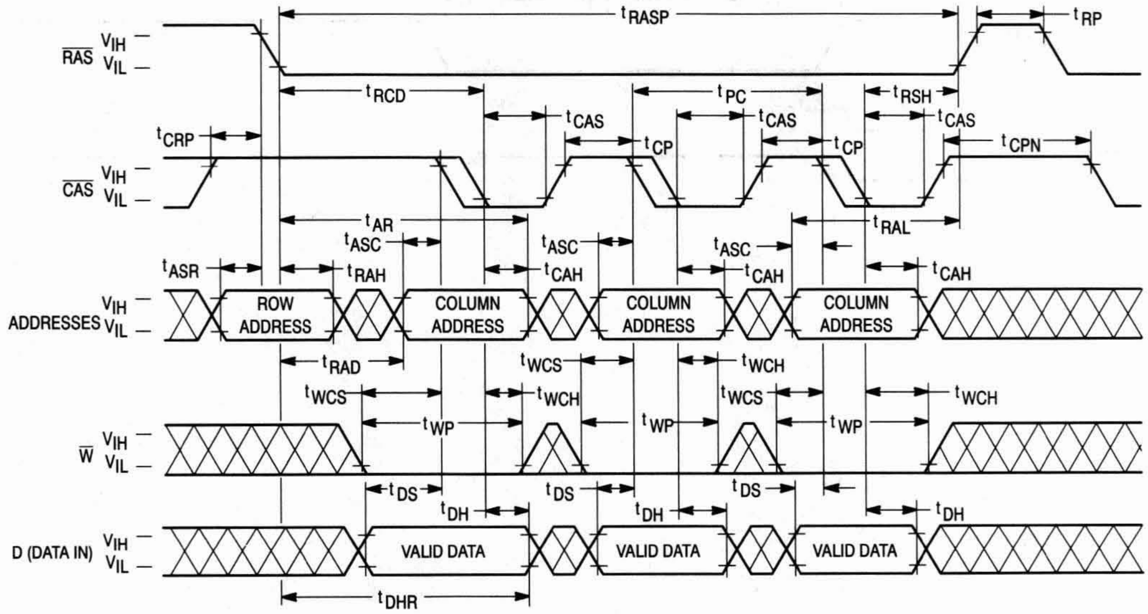
tCSH
tCPN
tCAS
CAS VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWCR
tWP
W VIH
VIL
tRWL
tDS
tDH
D (DATA IN) VIH
VIL
VALID DATA
tDHR

FAST PAGE MODE READ CYCLE

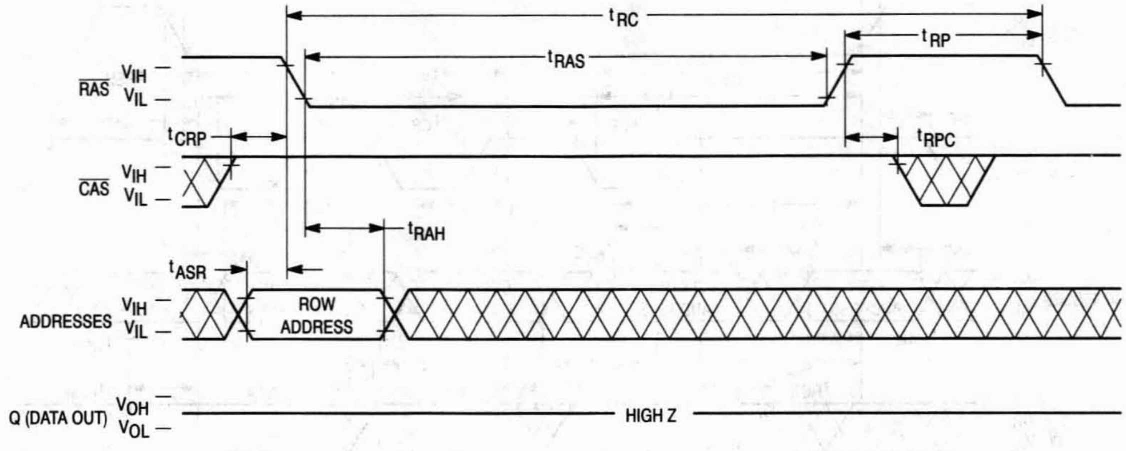

RAS VIH VIL
CAS VIH VIL
ADDRESSES VIH VIL
W VIH VIL
Q (DATA OUT) VOH VOL
tRASP
tRP
tCSH
tPC
tRSH
tRCD
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCPN
tAR
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
tRAL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAH
tRRH
tRAD
tRCH
tRCH
tRCH
tRCS
tRCS
tRCS
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
VALID DATA
VALID DATA
VALID DATA
tOFF
tOFF
tOFF
tCLZ
tCLZ
tCLZ

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)


RAS VIH VIL
CAS VIH VIL
ADDRESSES VIH VIL
W VIH VIL
D (DATA IN) VIH VIL
tRASP
tRP
tRCD
tPC
tRSH
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCPN
tAR
tRAL
tASC
tASC
tASC
tASR
tRAH
tCAH
tCAH
tCAH
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tWCS
tWCS
tWCS
tWCH
tWCH
tWCH
tWP
tWP
tWP
tDS
tDS
tDS
tDH
tDH
tDH
VALID DATA
VALID DATA
VALID DATA
tDHR

$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

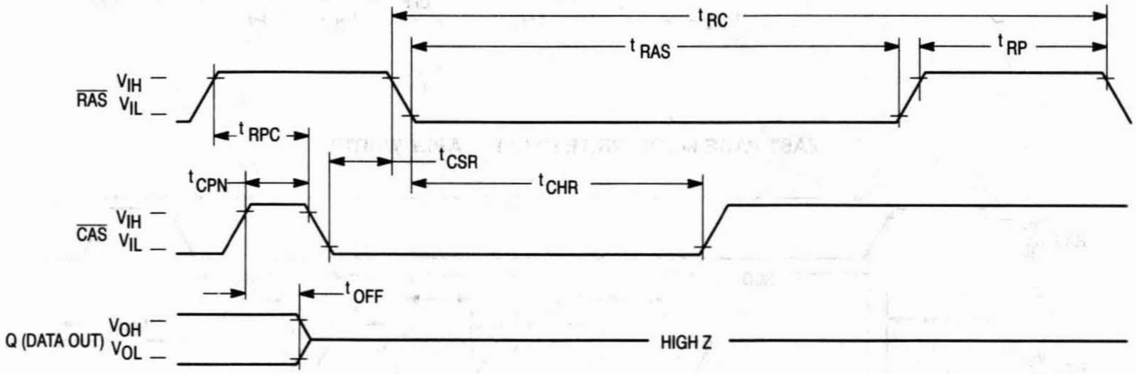
($\overline{\text{W}}$ and A9 are Don't Care)



t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

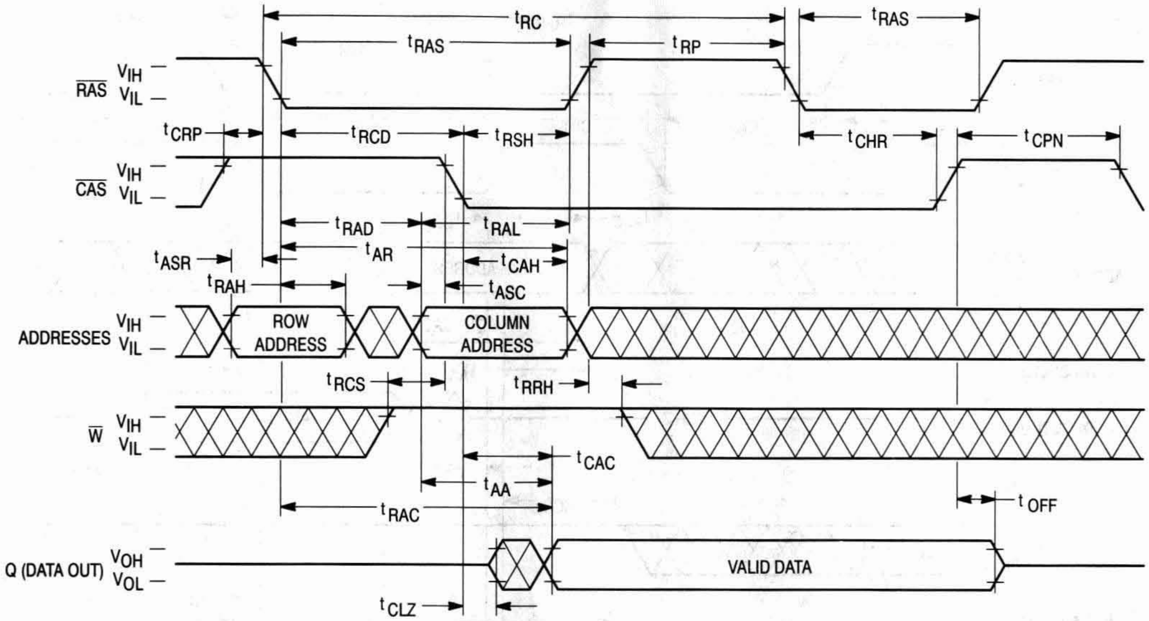
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{W}}$ and A0 – A9 are Don't Care)

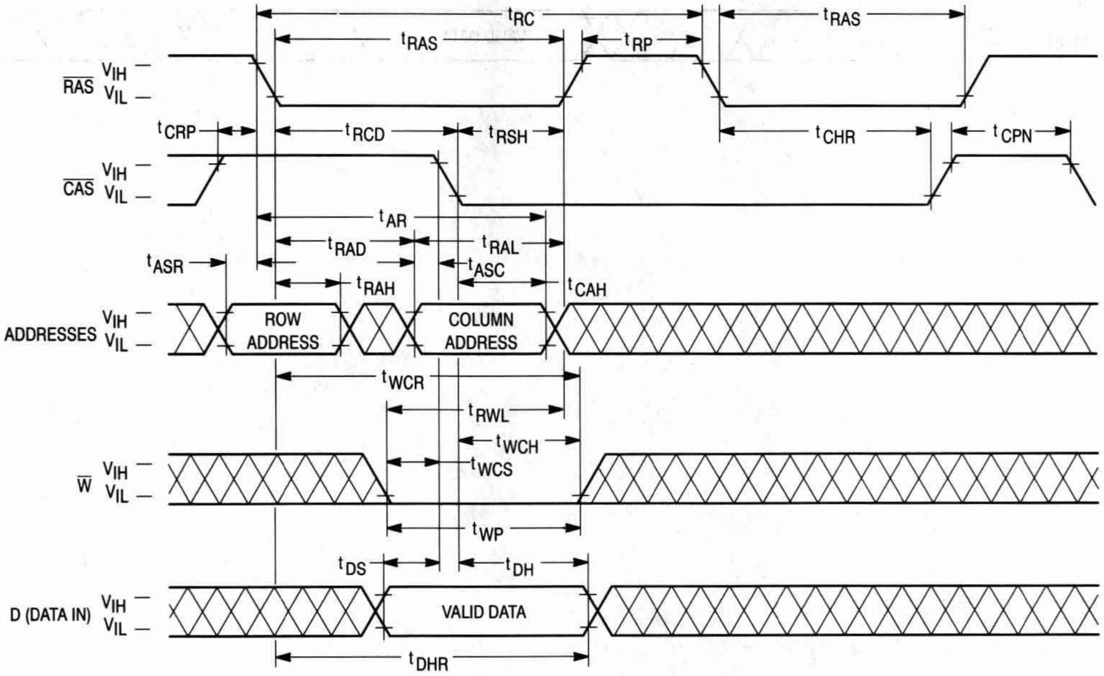


t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RPC}
t_{CSR}
t_{CPN}
t_{CHR}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{OFF}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

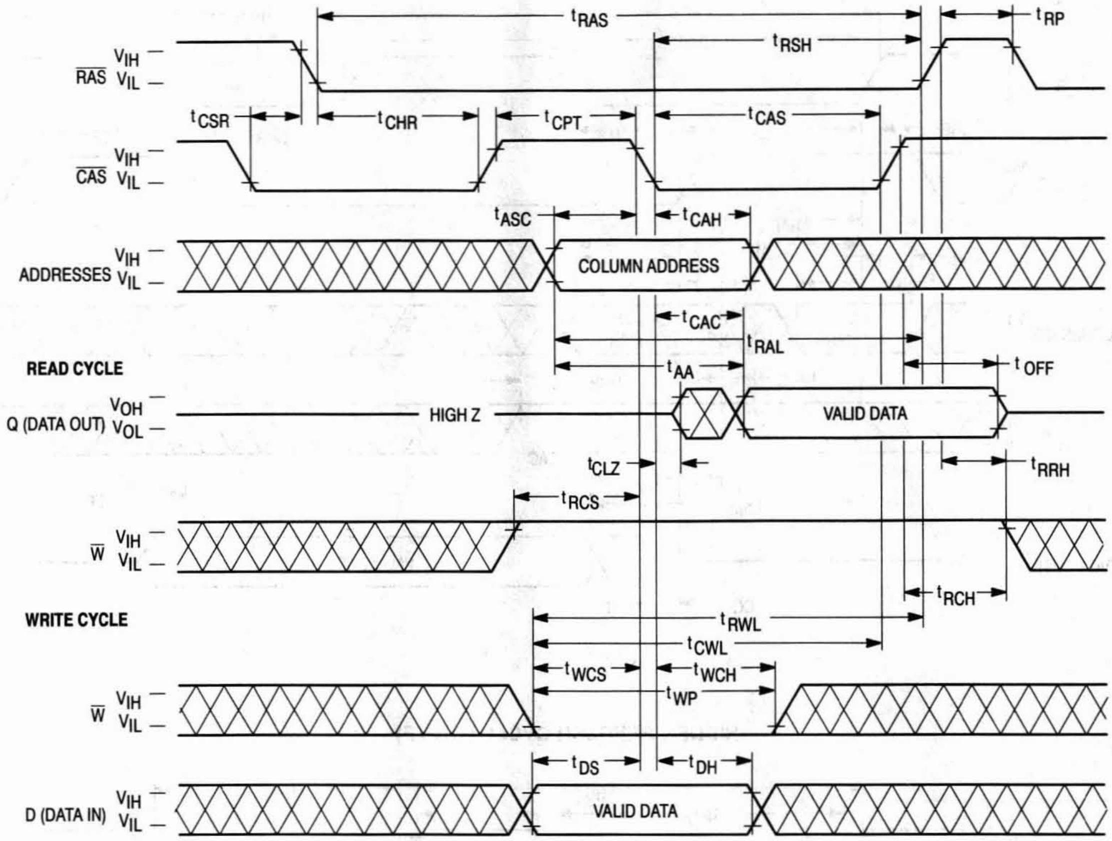
HIDDEN REFRESH CYCLE (READ)


t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$ V_{IH} V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CPN}
$\overline{CAS}$ V_{IH} V_{IL}
t_{RAD}
t_{RAL}
t_{AR}
t_{ASR}
t_{CAH}
t_{RAH}
t_{ASC}
ADDRESSES V_{IH} V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{RCS}
t_{RRH}
$\overline{W}$ V_{IH} V_{IL}
t_{CAC}
t_{AA}
t_{RAC}
t_{OFF}
Q (DATA OUT) V_{OH} V_{OL}
VALID DATA
t_{CLZ}

HIDDEN REFRESH CYCLE (WRITE)


t_{RC}
t_{RAS}
t_{RP}
t_{RAS}
$\overline{RAS}$ V_{IH} V_{IL}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CPN}
$\overline{CAS}$ V_{IH} V_{IL}
t_{AR}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES V_{IH} V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{WCR}
t_{RWL}
t_{WCH}
t_{WCS}
$\overline{W}$ V_{IH} V_{IL}
t_{WP}
t_{DS}
t_{DH}
D (DATA IN) V_{IH} V_{IL}
VALID DATA
t_{DHR}

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE


tRAS
tRP
tRSH
VIH
RAS VIL
tCSR
tCHR
tCPT
tCAS
VIH
CAS VIL
tASC
tCAH
VIH
ADDRESSES VIL
COLUMN ADDRESS
tCAC
tRAL
READ CYCLE
tAA
tOFF
VOH
Q (DATA OUT) VOL
HIGH Z
VALID DATA
tCLZ
tRRH
tRCS
VIH
W VIL
tRCH
WRITE CYCLE
tRWL
tCWL
tWCS
tWCH
tWP
VIH
W VIL
tDS
tDH
VIH
D (DATA IN) VIL
VALID DATA

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 word locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gate feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are two other variations in addressing the module: **$\overline{RAS}$-only refresh cycle** and **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either a normal random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. $\overline{CAS}$ controls read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} after the inactive transition.

WRITE CYCLE

The DRAM may be written by either an early write or a page mode early write cycle. Early write mode is discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early write mode is distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data In (DQ) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 512 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically refreshed (recharged) to maintain the correct bit state. Bits in the MCM36512 require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM36512. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM36512.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read cycle**. Repeat this operation 512 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, write cycle**. Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

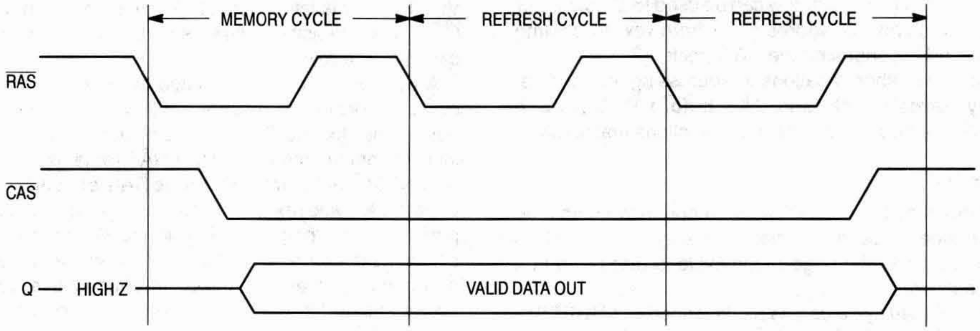


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION

(Order by Full Part Number)

MCM 36512 X XX

Motorola Memory Prefix — MCM
Part Number — 36512
Package (S = SIMM, SG = Gold Pad SIMM) — X
Speed (70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers — MCM36512S70 MCM36512SG70
MCM36512S80 MCM36512SG80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

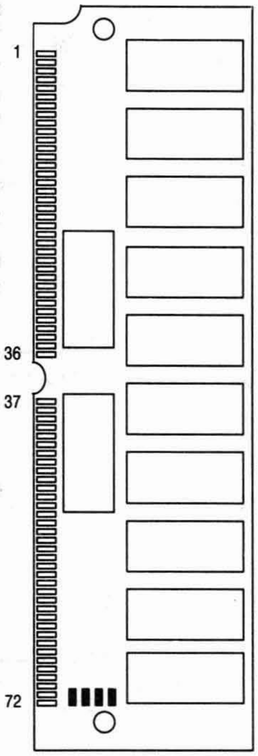
MCM36100
MCM36L100

1M x 36 Bit Dynamic Random Access Memory Module

The MCM36100 is a 36M dynamic random access memory (DRAM) module organized as 1,048,576 x 36 bits. The module is a 72-lead single-in-line memory module (SIMM) consisting of eight MCM54400A DRAMs housed in standard 300 mil SOJ packages and four CMOS 1M x 1 DRAMs housed in 20/26 lead SOJ packages, mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM54400A is a CMOS high-speed dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  MCM36100 = 16 ms (Max)
  MCM36L100 = 128 ms (Max)
- Consists of Eight 1M x 4 DRAMs, Four 1M x 1 DRAMs, and Twelve 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM36100-70 = 70 ns (Max)
  MCM36100-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM36100-70 = 6.16 W (Max)
  MCM36100-80 = 5.28 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 132 mW (Max)
  CMOS Levels = 66 mW (Max, MCM36100)
  = 13.2 mW (Max, MCM36L100)

S PACKAGE
SIMM MODULE
CASE 866A-02



PIN OUT

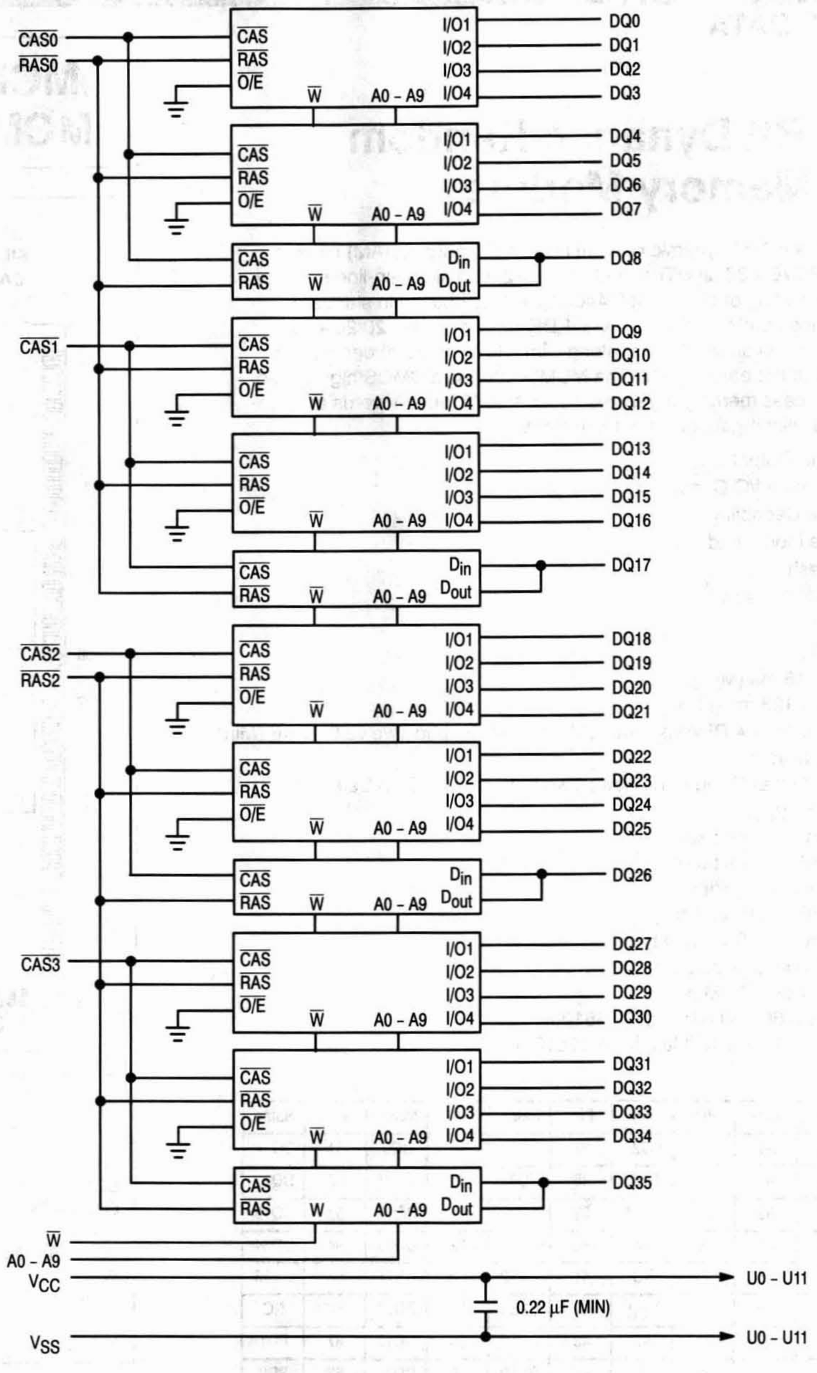
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

PIN NAMES

A0 – A9	Address Inputs
DQ0 – DQ35	Data Input/Output
$\overline{CAS0}$ – $\overline{CAS3}$	Column Address Strobe
PD1 – PD4	Presence Detect
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

BLOCK DIAGRAM



CAS0
RAS0
CAS1
CAS2
RAS2
CAS3
CAS
RAS
O/E
W
A0 – A9
I/O1
I/O2
I/O3
I/O4
Din
Dout
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
DQ32
DQ33
DQ34
DQ35
W
A0 – A9
VCC
VSS
0.22 µF (MIN)
U0 – U11
U0 – U11

PRESENCE DETECT PIN OUT		
Pin Name	**70 ns**	**80 ns**
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}
PD3	V_{SS}	NC
PD4	NC	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	8.4	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	MCM36100-70, t_{RC} = 130 ns MCM36100-80, t_{RC} = 150 ns	I_{CC1}	— —	1120 960	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	24	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles	MCM36100-70, t_{RC} = 130 ns MCM36100-80, t_{RC} = 150 ns	I_{CC3}	— —	1120 960	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle	MCM36100-70, t_{PC} = 45 ns MCM36100-80, t_{PC} = 50 ns	I_{CC4}	— —	800 680	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	MCM36100 MCM36L100	I_{CC5}	— —	12 2.4	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	MCM36100-70, t_{RC} = 130 ns MCM36100-80, t_{RC} = 150 ns	I_{CC6}	— —	1120 960	mA	1
V_{CC} Power Supply Current Battery Backup Mode (t_{RC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$, DQ, A0 – A9 = V_{CC} – 0.2 V or 0.2 V)	MCM36L100 only	I_{CC7}	—	3.6	mA	1, 3
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)		$I_{lkg(I)}$	– 120	+ 120	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)		$I_{lkg(O)}$	– 10	+ 10	µA	
Output High Voltage (I_{OH} = – 5 mA)		V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery backup. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit
Input Capacitance (A0 – A9)	C_{I1}	—	70	pF
Input Capacitance ($\overline{\text{W}}$)	C_{I2}	—	94	pF
Input Capacitance ($\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$)	C_{I3}	—	52	pF
Input Capacitance ($\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$)	C_{I4}	—	31	pF
I/O Capacitance (DQ0 – DQ7, DQ9 – DQ16, DQ18 – DQ25, DQ27 – DQ34)	C_{DQ1}	—	17	pF
I/O Capacitance (DQ8, DQ17, DQ26, DQ35)	C_{DQ2}	—	22	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\,\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM36100–70 MCM36L100-70		MCM36100–80 MCM36L100-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	50	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	40	—	45	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10 k	80	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100 k	80	100 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	45	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

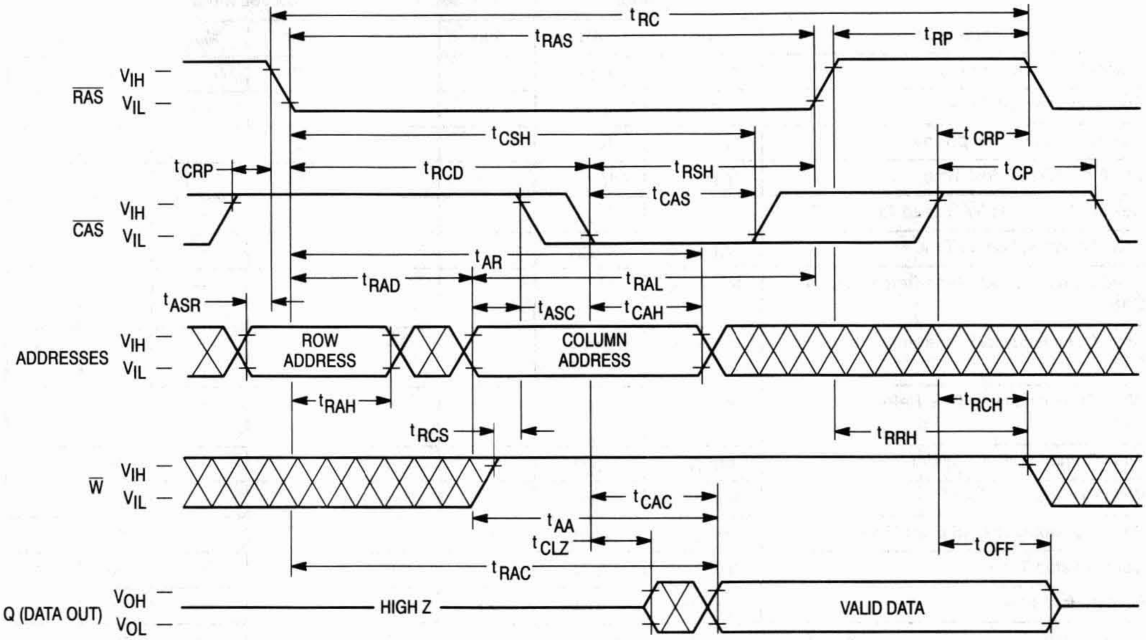
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM36100-70 MCM36L100-70		MCM36100-80 MCM36L100-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14
Refresh Period MCM36100 MCM36L100	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Time	t_{CEHCEL}	t_{CPT}	40	—	40	—	ns	
Write to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	$t_{RELREH(P)}$	t_{RASPP}	70	100 k	80	100 k	ns	16
$\overline{\text{CAS}}$ Precharge Time	$t_{CEHCEL(P)}$	t_{CPNP}	10	—	10	—	ns	16

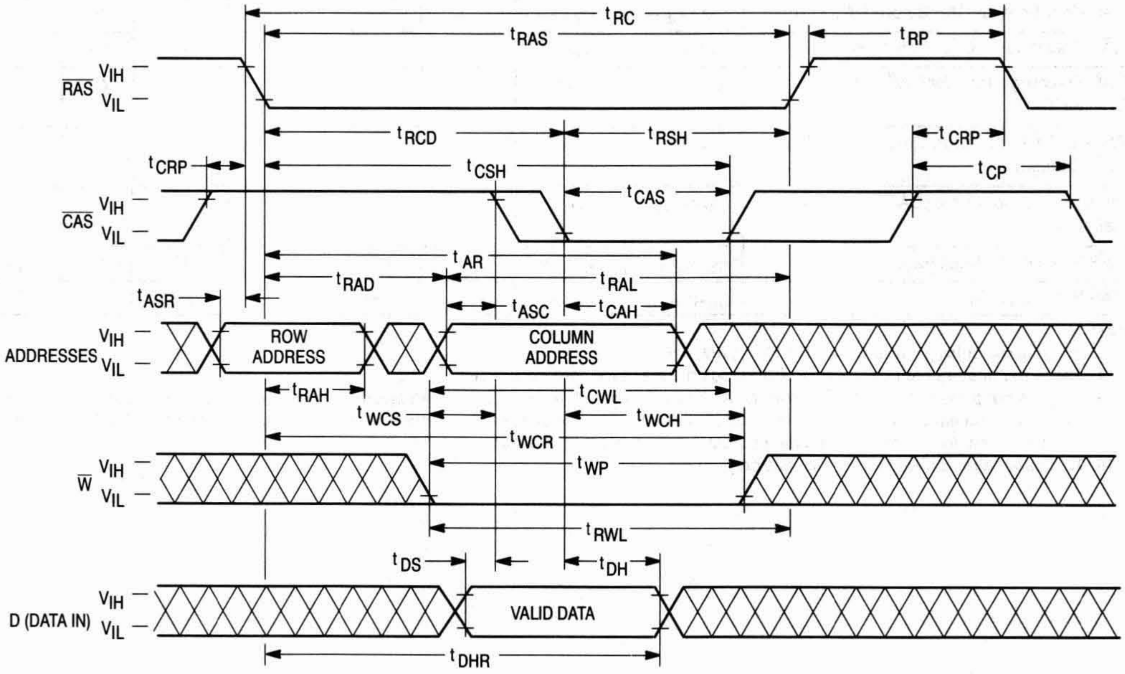
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.
16. This parameter applies to the parity bits only.

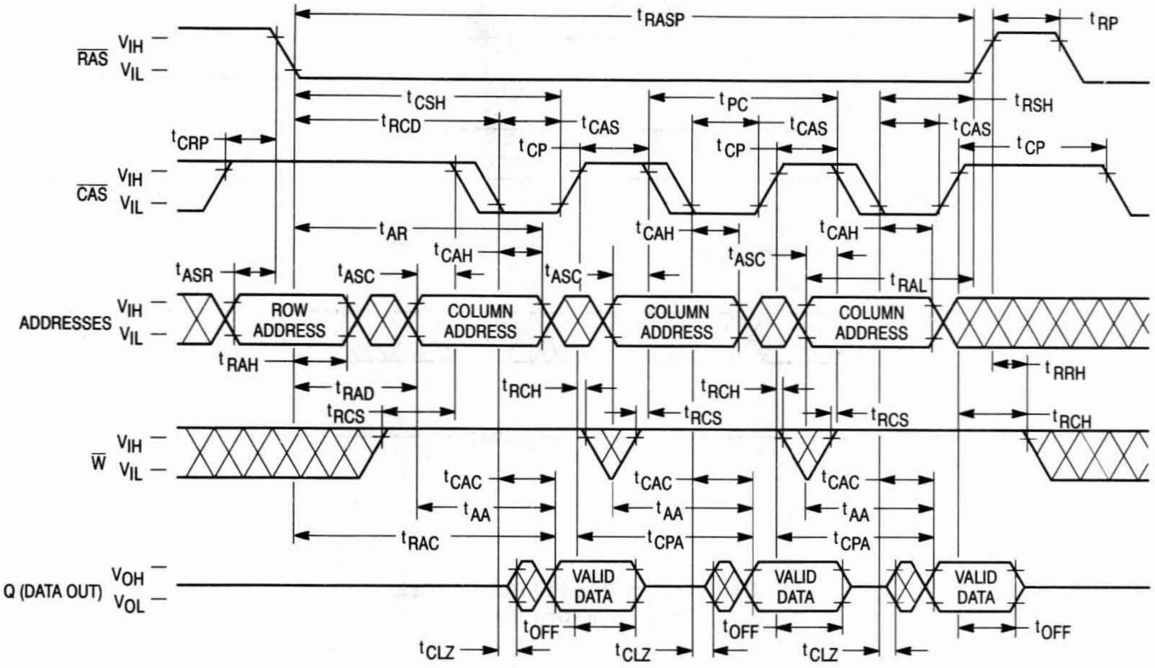
READ CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCAS
tCP
CAS
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W
tCAC
tAA
tCLZ
tOFF
tRAC
Q (DATA OUT)
VOH
VOL
HIGH Z
VALID DATA

EARLY WRITE CYCLE

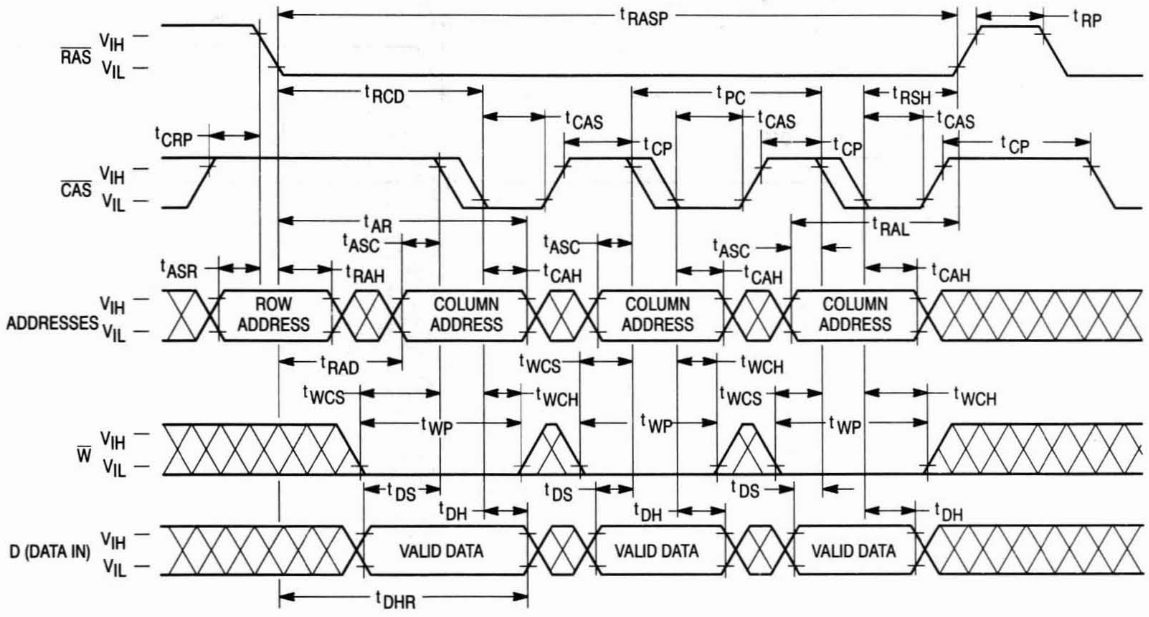

tRC
tRAS
tRP
RAS
VIH
VIL
tRCD
tRSH
tCRP
tCSH
tCP
tCAS
CAS
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWCR
tWP
W
tRWL
tDS
tDH
D (DATA IN)
VALID DATA
tDHR

FAST PAGE MODE READ CYCLE



RAS
VIH
VIL
CAS
VIH
VIL
ADDRESSES
VIH
VIL
W
VIH
VIL
Q (DATA OUT)
VOH
VOL
tRASP
tRP
tCSH
tPC
tRSH
tRCD
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCP
tAR
tCAH
tCAH
tCAH
tASC
tASR
tASC
tASC
tRAL
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAH
tRRH
tRAD
tRCH
tRCH
tRCS
tRCS
tRCS
tRCH
tCAC
tCAC
tCAC
tAA
tAA
tAA
tRAC
tCPA
tCPA
VALID DATA
VALID DATA
VALID DATA
tOFF
tOFF
tOFF
tCLZ
tCLZ
tCLZ

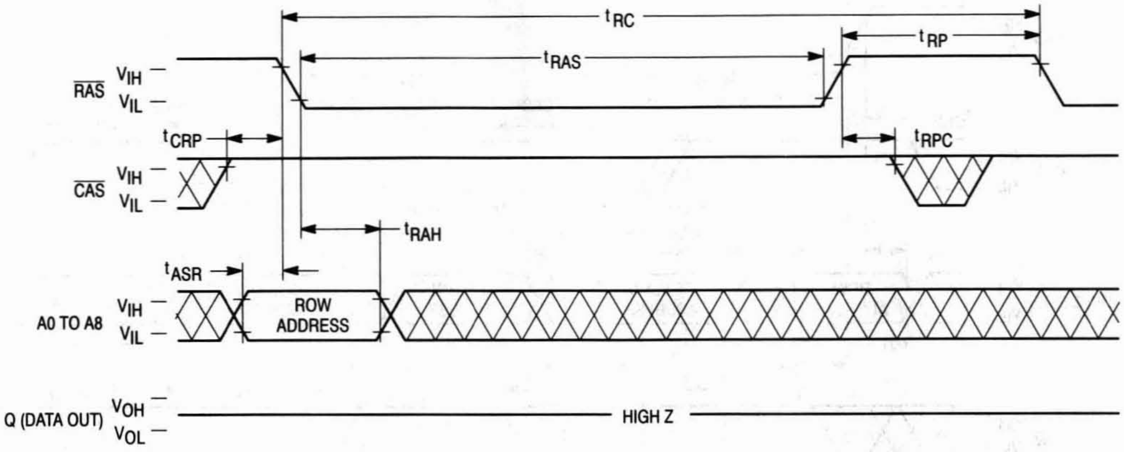
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



RAS
VIH
VIL
CAS
VIH
VIL
ADDRESSES
VIH
VIL
W
VIH
VIL
D (DATA IN)
VIH
VIL
tRASP
tRP
tRCD
tPC
tRSH
tCAS
tCAS
tCAS
tCRP
tCP
tCP
tCP
tAR
tRAL
tASC
tASC
tASC
tASR
tRAH
tCAH
tCAH
tCAH
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tWCS
tWCH
tWCS
tWCH
tWCS
tWCH
tWP
tWP
tWP
tDS
tDS
tDS
tDH
tDH
tDH
VALID DATA
VALID DATA
VALID DATA
tDHR

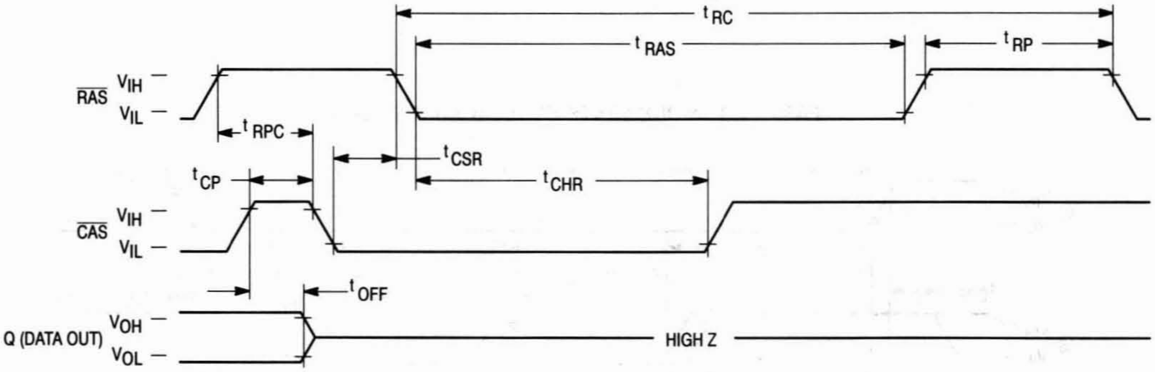
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

($\overline{\text{W}}$ and A9 are Don't Care)

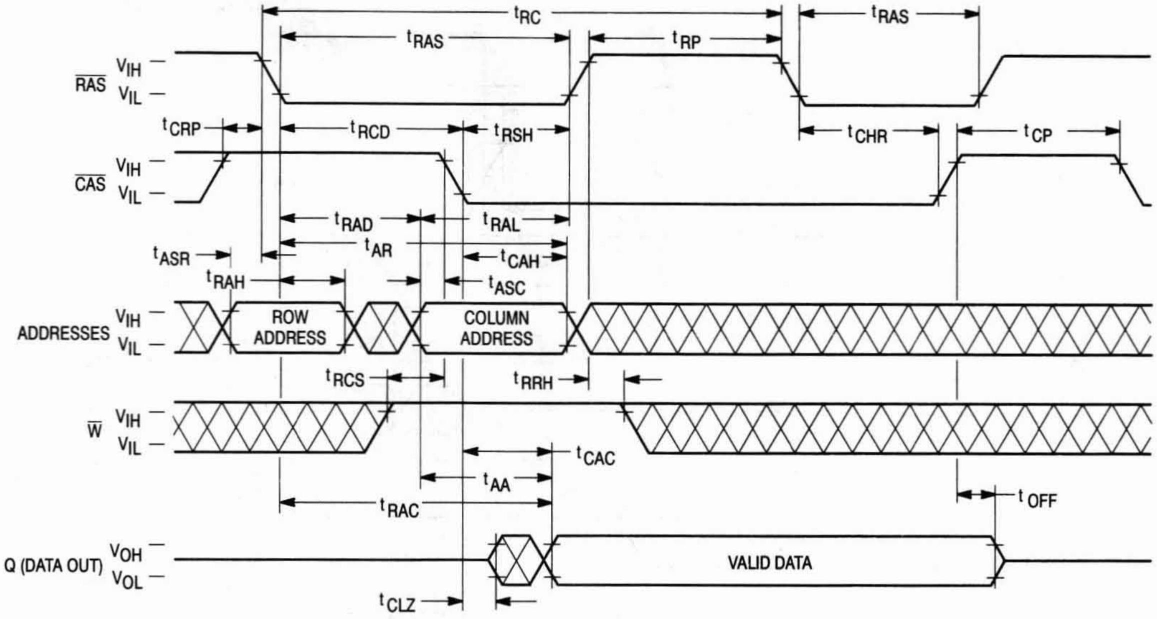

t RC
t RAS
t RP
RAS
VIH
VIL
t CRP
t RPC
CAS
VIH
VIL
t RAH
t ASR
A0 TO A8
VIH
VIL
ROW ADDRESS
Q (DATA OUT)
VOH
VOL
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

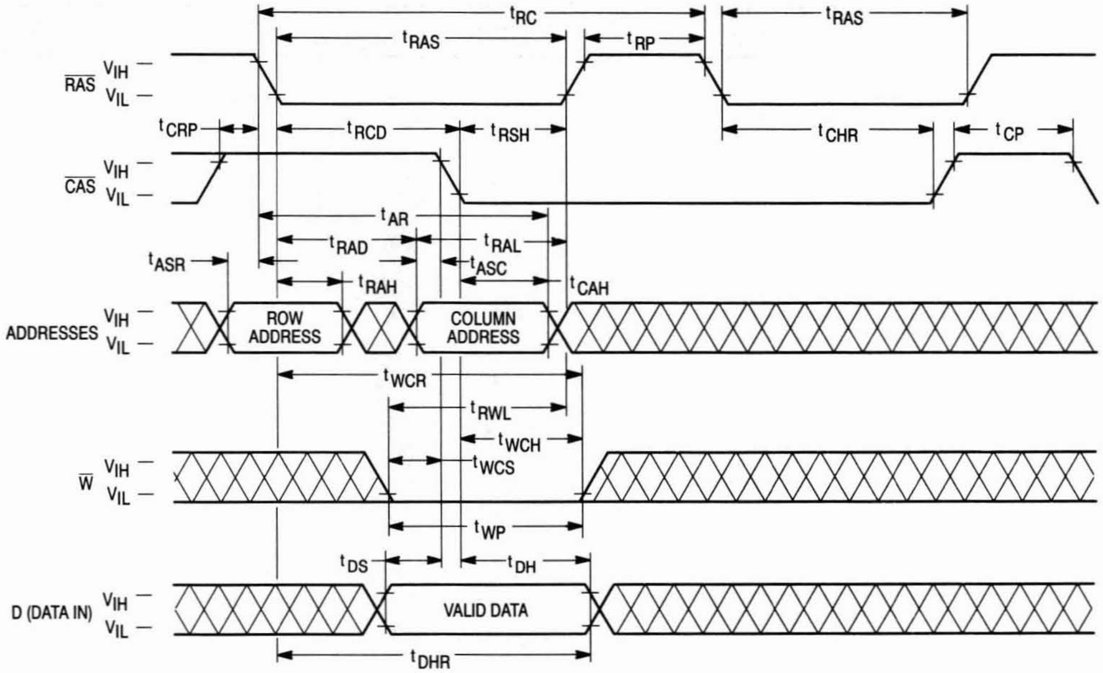
(A0 – A9 are Don't Care)


t RC
t RAS
t RP
RAS
VIH
VIL
t RPC
t CSR
t CP
t CHR
CAS
VIH
VIL
t OFF
Q (DATA OUT)
VOH
VOL
HIGH Z

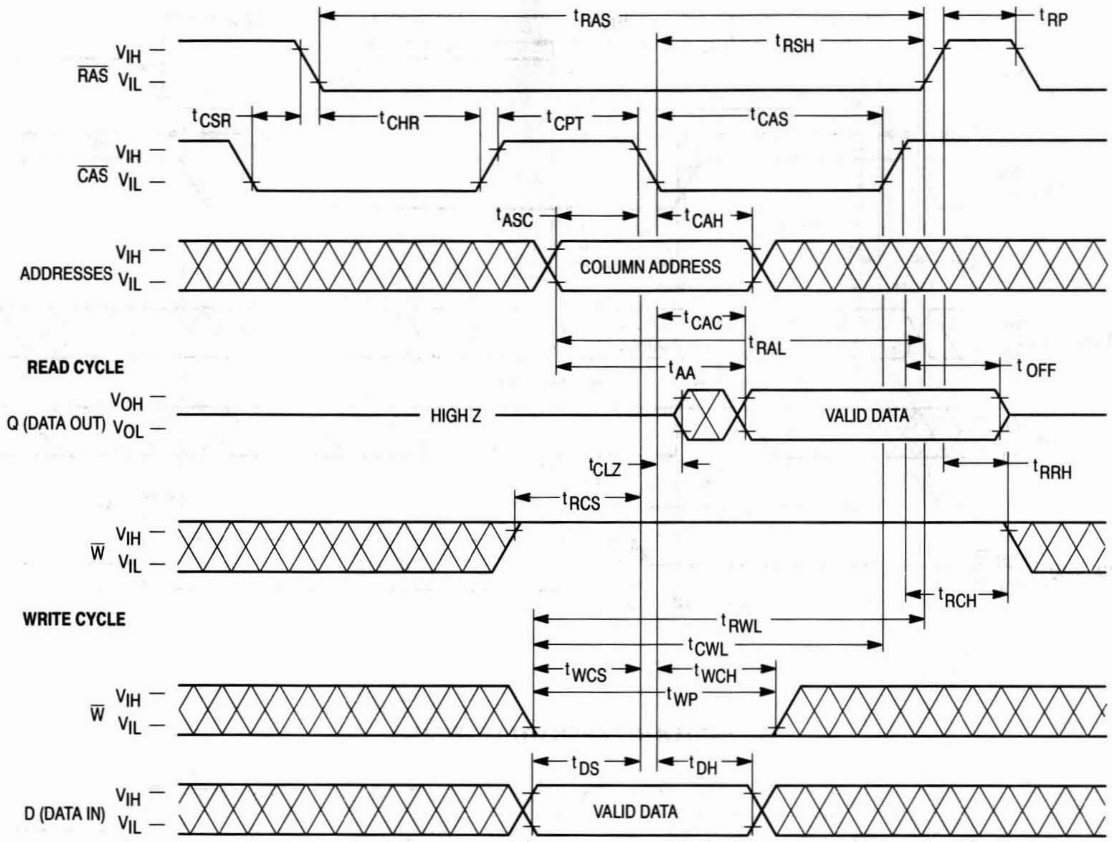
HIDDEN REFRESH CYCLE (READ)


tRC
tRAS
tRP
tRAS
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCP
CAS
VIH
VIL
tRAD
tRAL
tAR
tASR
tCAH
tRAH
tASC
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRCS
tRRH
W
VIH
VIL
tCAC
tAA
tRAC
tOFF
Q (DATA OUT)
VOH
VOL
VALID DATA
tCLZ

HIDDEN REFRESH CYCLE (WRITE)


tRC
tRAS
tRP
tRAS
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCP
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tWCR
tRWL
tWCH
tWCS
W
VIH
VIL
tWP
tDS
tDH
D (DATA IN)
VIH
VIL
VALID DATA
tDHR

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



t_{RAS}
t_{RP}
t_{RSH}
V_{IH}
$\overline{\text{RAS}}$ V_{IL}
t_{CSR}
t_{CHR}
t_{CPT}
t_{CAS}
V_{IH}
$\overline{\text{CAS}}$ V_{IL}
t_{ASC}
t_{CAH}
V_{IH}
ADDRESSES V_{IL}
COLUMN ADDRESS
t_{CAC}
t_{RAL}
READ CYCLE
t_{AA}
t_{OFF}
V_{OH}
Q (DATA OUT) V_{OL}
HIGH Z
VALID DATA
t_{CLZ}
t_{RRH}
t_{RCS}
V_{IH}
$\overline{W}$ V_{IL}
t_{RCH}
WRITE CYCLE
t_{RWL}
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
V_{IH}
$\overline{W}$ V_{IL}
t_{DS}
t_{DH}
V_{IH}
D (DATA IN) V_{IL}
VALID DATA

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 4 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 word locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the module: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either a "normal" random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. $\overline{\text{CAS}}$ controls read access time; $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{\text{CAS}}$ clock active transition (t_{CAC}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for minimum times of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the $\overline{\text{CAS}}$ clock is active. When the $\overline{\text{CAS}}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with either an early write or a page mode early write cycle. Early write mode is discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early write mode is distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS} and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (DQ) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM36100 require refresh every 16 milliseconds, while refresh time for the MCM36L100 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM36100, and 124.8 microseconds for the MCM36L100. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM36100 and 128 milliseconds on the MCM36L100.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

This refresh cycle is initiated when $\overline{\text{RAS}}$ falls after $\overline{\text{CAS}}$ has been low (by t_{CSR}). This activates the internal refresh counter, which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{\text{CAS}}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{\text{CAS}}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period (t_{RP}), executing a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. (See Figure 1.)

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 1024 test cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read cycle**. Repeat this operation 1024 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, write cycle**. Repeat this operation 1024 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

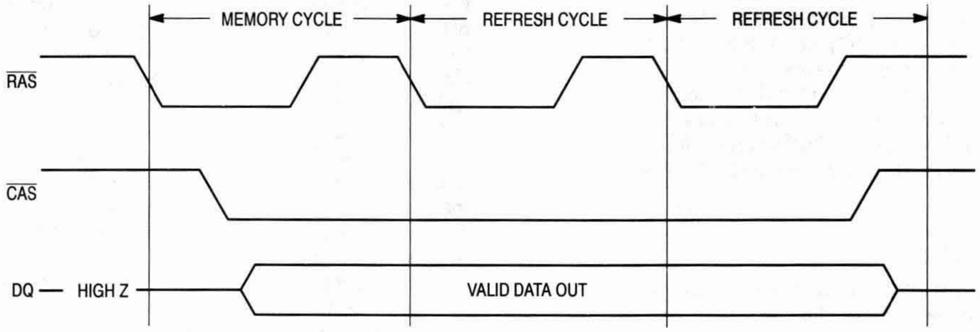


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION

(Order by Full Part Number)

MCM 36100 or 36L100 X XX

Motorola Memory Prefix — MCM
Part Number — 36100 or 36L100
X — Package (AS = SIMM, ASG = Gold Pad SIMM)
XX — Speed (70 = 70 ns, 80 = 80 ns)

Full Part Numbers —		
	MCM36100AS70	MCM36100ASG70
	MCM36100AS80	MCM36100ASG80
	MCM36L100AS70	MCM36L100ASG70
	MCM36L100AS80	MCM36L100ASG80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

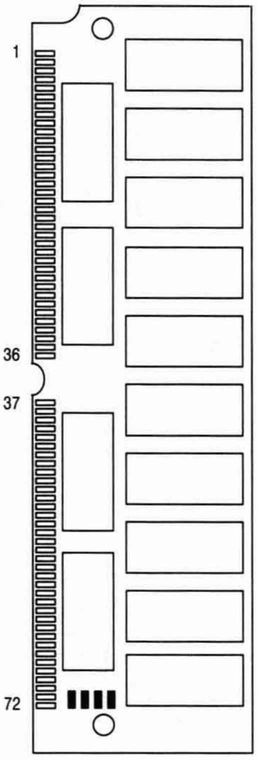
MCM36200
MCM36L200

2M x 36 Bit Dynamic Random Access Memory Module

The MCM36200 is a 72M dynamic random access memory (DRAM) module organized as 2,097,152 x 36 bits. The module is a double-sided 72-lead single-in-line memory module (SIMM) consisting of sixteen MCM54400 DRAMs housed in standard 300 mil SOJ packages and eight CMOS 1M x 1 DRAMs housed in 20/26 lead SOJ packages, mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM54400 is a CMOS high speed dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  MCM36200 = 16 ms (Max)
  MCM36L200 = 128 ms (Max)
- Consists of Sixteen 1M x 4 DRAMs, Eight 1M x 1 DRAMs, and Twenty Four 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM36200-70 = 70 ns (Max)
  MCM36200-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM36200-70 = 6.30 W (Max)
  MCM36200-80 = 5.42 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 264 mW (Max)
  CMOS Levels= 132 mW (Max, MCM36200)
  = 27 mW (Max, MCM36L200)

AS PACKAGE
SIMM MODULE
CASE 866A-02



PIN ASSIGNMENTS

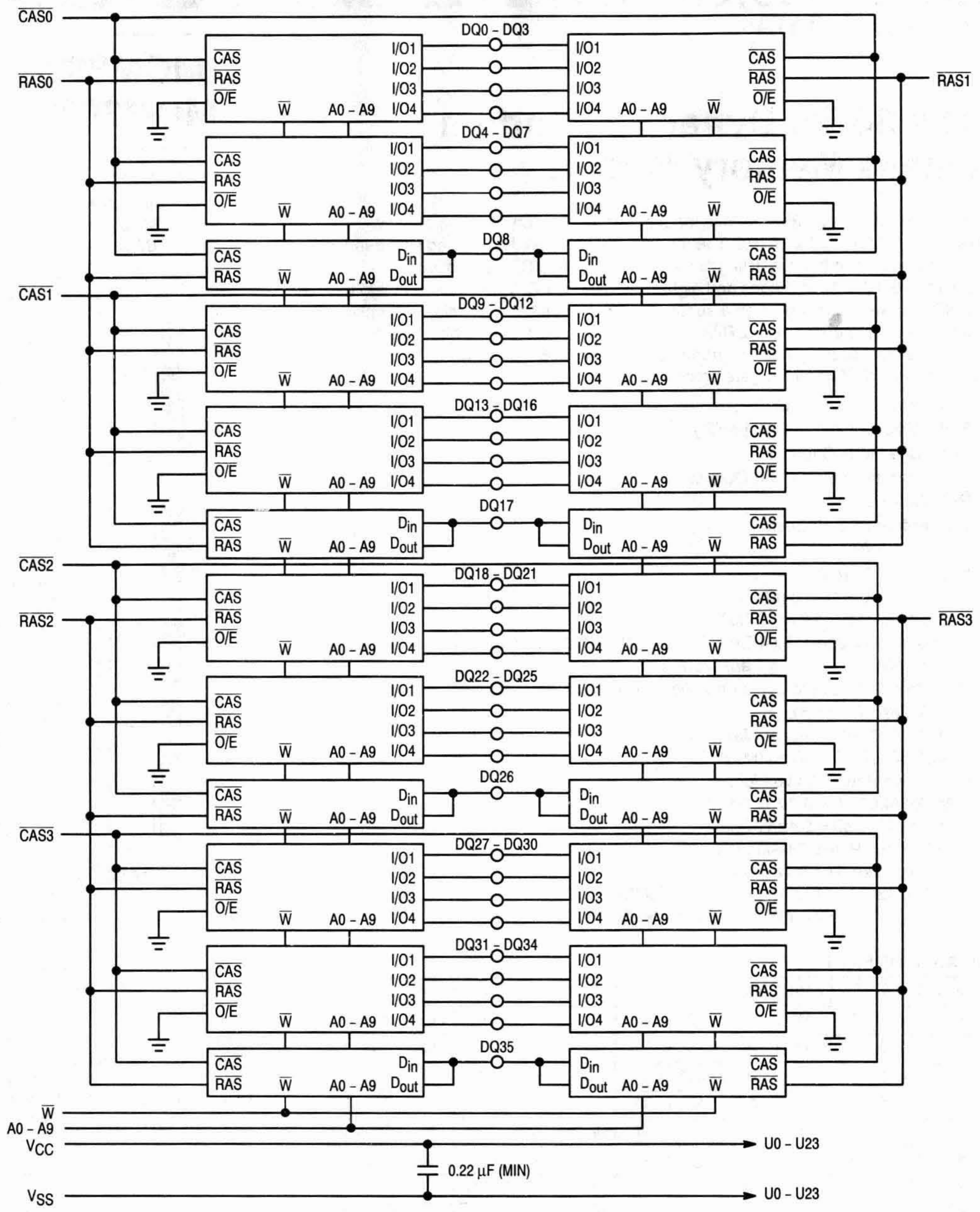
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

PIN NAMES

A0 – A9	Address Inputs
DQ0 – DQ35	Data Input/Output
$\overline{CAS0}$ – $\overline{CAS3}$	Column Address Strobe
PD1 – PD4	Presence Detect
$\overline{RAS0}$ – $\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

BLOCK DIAGRAM


CAS0
RAS0
CAS1
CAS2
RAS2
CAS3
RAS1
RAS3
DQ0 – DQ3
DQ4 – DQ7
DQ8
DQ9 – DQ12
DQ13 – DQ16
DQ17
DQ18 – DQ21
DQ22 – DQ25
DQ26
DQ27 – DQ30
DQ31 – DQ34
DQ35
CAS
RAS
O/E
W
A0 – A9
I/O1
I/O2
I/O3
I/O4
Din
Dout
W
A0 – A9
VCC
VSS
0.22 µF (MIN)
U0 – U23
U0 – U23

PRESENCE DETECT PIN OUT		
Pin Name	**70 ns**	**80 ns**
PD1	NC	NC
PD2	NC	NC
PD3	V_{SS}	NC
PD4	NC	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	10.1	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM36200-70, t_{RC} = 130 ns MCM36200-80, t_{RC} = 150 ns	I_{CC1}	— —	1144 984	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	48	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles MCM36200-70, t_{RC} = 130 ns MCM36200-80, t_{RC} = 150 ns	I_{CC3}	— —	1144 984	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM36200-70, t_{PC} = 45 ns MCM36200-80, t_{PC} = 45 ns	I_{CC4}	— —	824 704	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM36200 MCM36L200	I_{CC5}	— —	24 8	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM36200-70, t_{RC} = 130 ns MCM36200-80, t_{RC} = 150 ns	I_{CC6}	— —	1144 984	mA	1
VCC Power Supply Current Battery Backup Mode (t_{RC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$, DQ, A0 – A9 = V_{CC} – 0.2 V or 0.2 V) MCM36L200 only	I_{CC7}	—	7.2	mA	3
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 240	240	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.
3. t_{RAS} (max) = 1 µs is applied to refresh of battery backup. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE

Characteristic	Symbol	Min	Max	Unit
Input Capacitance (A0 – A9)	C_{I1}	—	130	pF
Input Capacitance ($\overline{\text{W}}$)	C_{I2}	—	178	pF
Input Capacitance ($\overline{\text{RAS0}}$ – $\overline{\text{RAS2}}$)	C_{I3}	—	52	pF
Input Capacitance ($\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$)	C_{I4}	—	52	pF
I/O Capacitance (DQ0 – DQ7, DQ9 – DQ16, DQ18 – DQ25, DQ27 – DQ34)	C_{DQ1}	—	24	pF
I/O Capacitance (DQ8, DQ17, DQ26, DQ35)	C_{DQ2}	—	34	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\ \Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM36200-70 MCM36L200-70		MCM36200-80 MCM36L200-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	ns	6
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	50	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	70	—	80	ns	7, 8
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	ns	7, 10
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	40	—	45	ns	7
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold TIme	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	45	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	ns	12
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	ns	13

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. To avoid bus contention and potential damage to the module, $\overline{\text{RAS0}}$ and $\overline{\text{RAS1}}$ may not be active low simultaneously. Similarly, $\overline{\text{RAS2}}$ and $\overline{\text{RAS3}}$ may not be simultaneously active low.
6. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
7. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \le t_{RCD}$ (max).
9. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
10. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

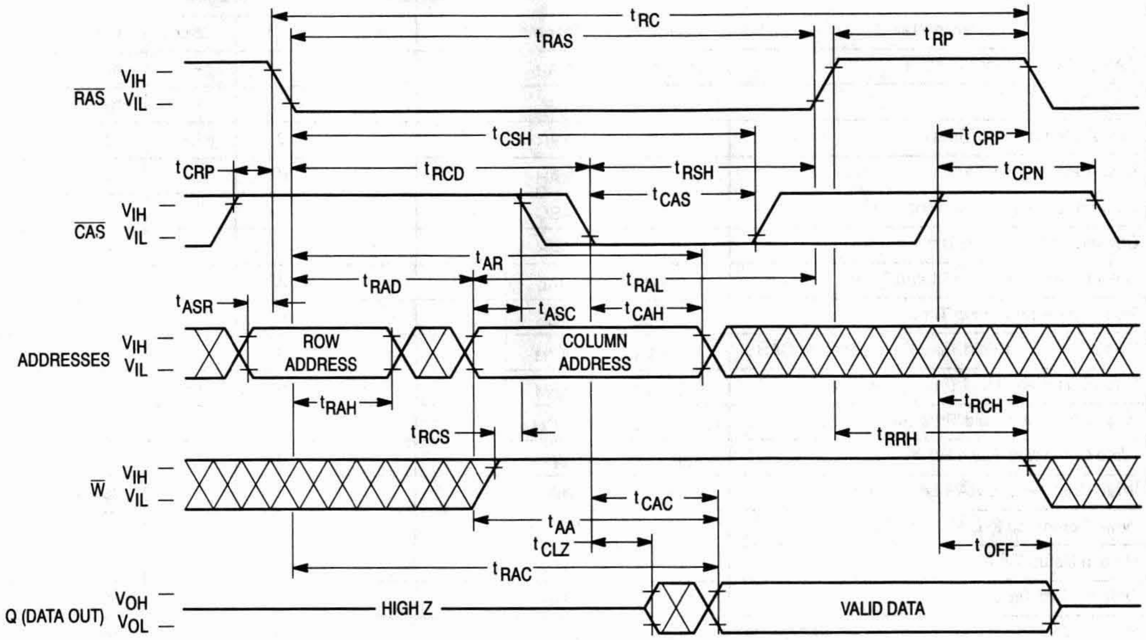
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM36200-70 MCM36L200-70		MCM36200-80 MCM36L200-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CELREL}	t_{CRP}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	14
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	14
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	15
Refresh Period MCM36200 MCM36L200	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	16
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	ns	
Write to $\overline{\text{RAS}}$ Precharge Time for ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	ns	
Write to $\overline{\text{RAS}}$ Hold Time for ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	$t_{RELREH(P)}$	t_{RPC}	70	100,000	80	100,000	ns	17
$\overline{\text{CAS}}$ Precharge Time	$t_{CEHCEL(P)}$	t_{CPN}	10	—	10	—	ns	17

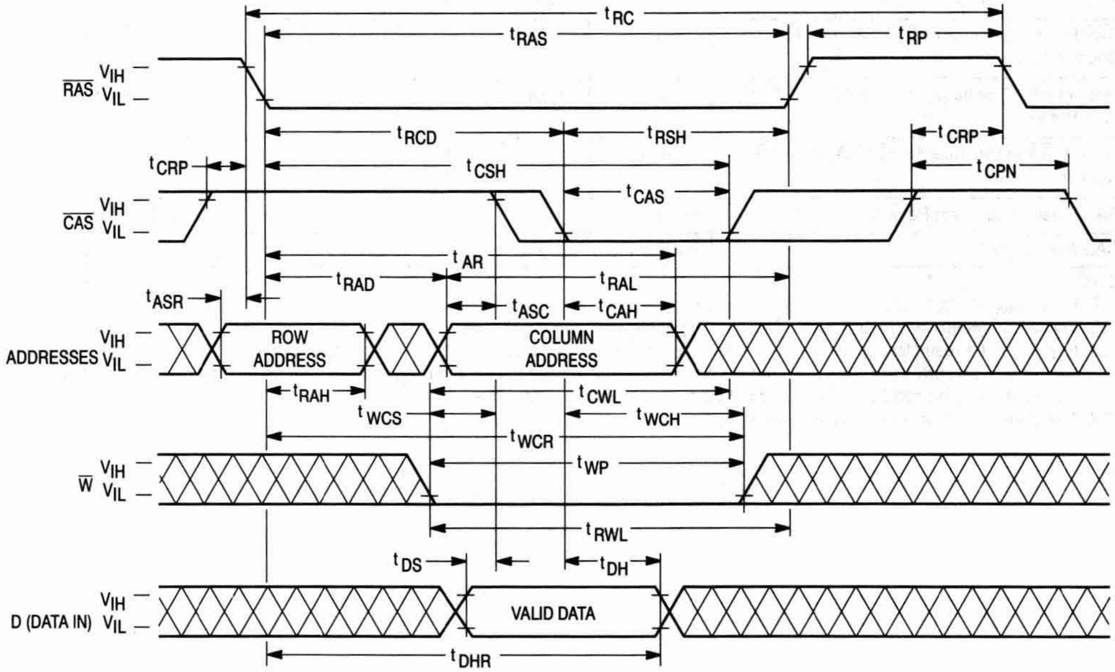
NOTES:

14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles.
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.
17. This parameter applies to the parity bits only.

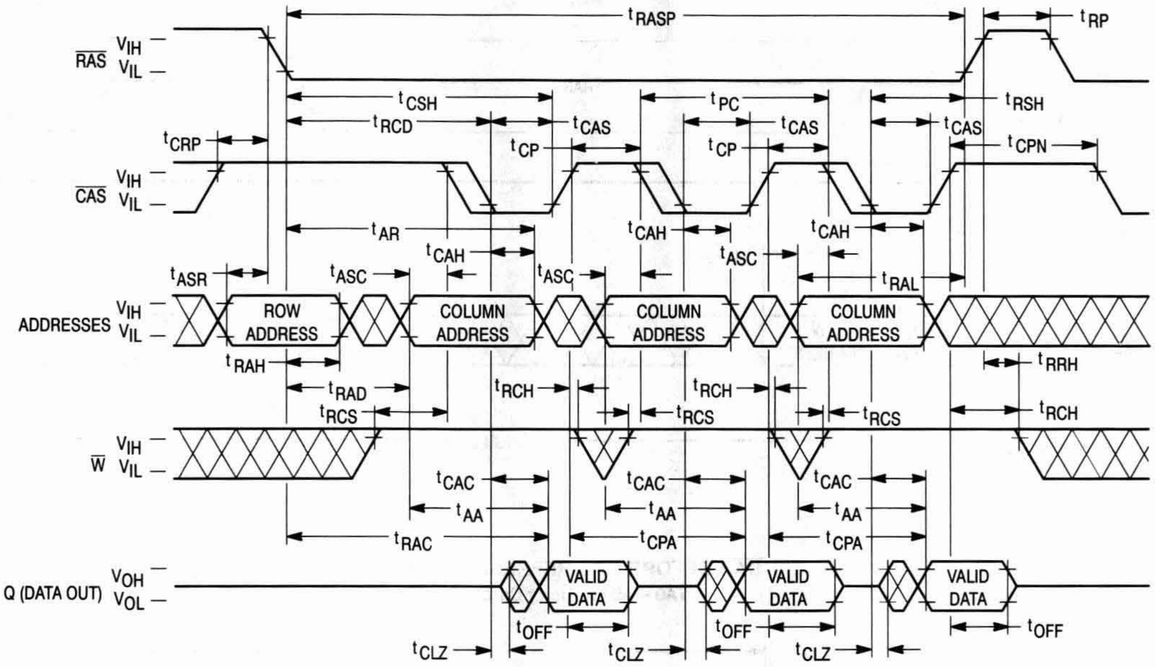
READ CYCLE


tRC
tRAS
tRP
RAS VIH
VIL
tCSH
tCRP
tCRP
tRCD
tRSH
tCPN
tCAS
CAS VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tRCH
tRCS
tRRH
W VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
Q (DATA OUT) VOH
VOL
HIGH Z
VALID DATA

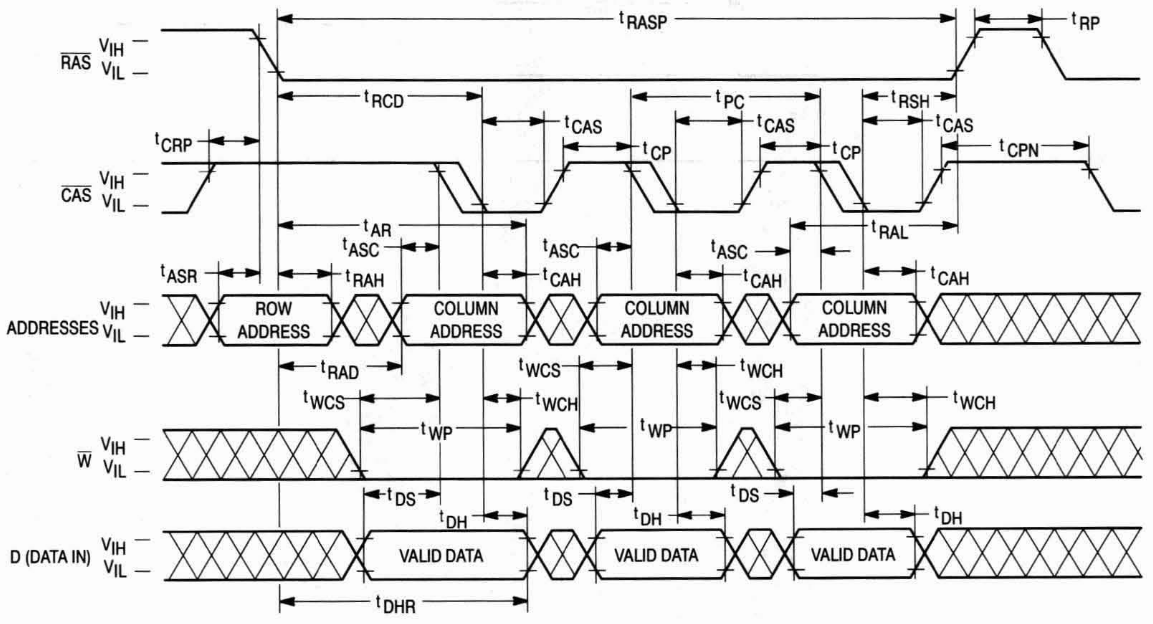
EARLY WRITE CYCLE


tRC
tRAS
tRP
RAS VIH
VIL
tRCD
tRSH
tCRP
tCRP
tCSH
tCPN
tCAS
CAS VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tCAH
ADDRESSES VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAH
tCWL
tWCS
tWCH
tWCR
tWP
W VIH
VIL
tRWL
tDS
tDH
D (DATA IN) VIH
VIL
VALID DATA
tDHR

FAST PAGE MODE READ CYCLE

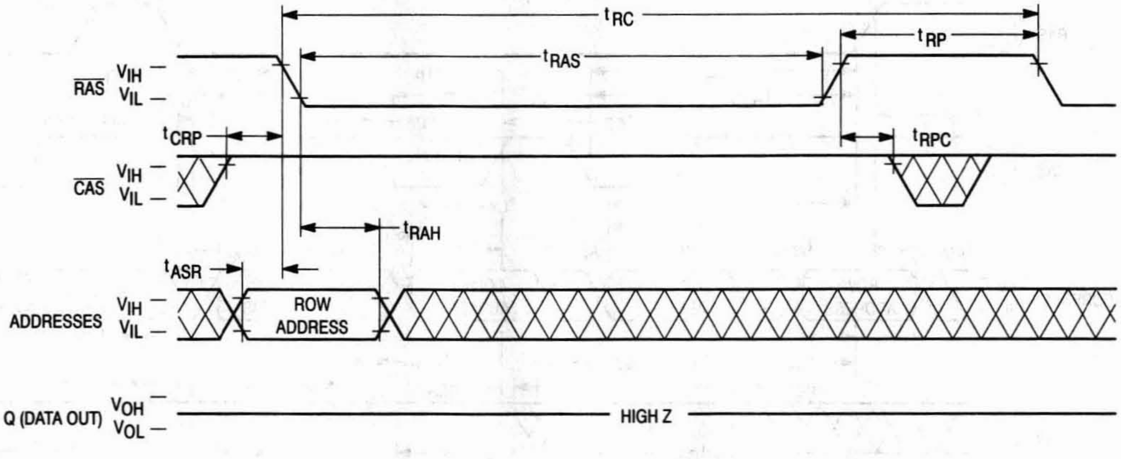

t_{RASP}
t_{RP}
$\overline{RAS}$ V_{IH} V_{IL}
t_{CSH}
t_{PC}
t_{RSH}
t_{RCD}
t_{CAS}
t_{CAS}
t_{CAS}
t_{CRP}
t_{CP}
t_{CP}
t_{CPN}
$\overline{CAS}$ V_{IH} V_{IL}
t_{AR}
t_{CAH}
t_{CAH}
t_{CAH}
t_{ASC}
t_{ASC}
t_{ASC}
t_{ASR}
t_{RAL}
ADDRESSES V_{IH} V_{IL}
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
t_{RAH}
t_{RRH}
t_{RAD}
t_{RCH}
t_{RCH}
t_{RCS}
t_{RCS}
t_{RCS}
t_{RCH}
$\overline{W}$ V_{IH} V_{IL}
t_{CAC}
t_{CAC}
t_{CAC}
t_{AA}
t_{AA}
t_{AA}
t_{RAC}
t_{CPA}
t_{CPA}
Q (DATA OUT) V_{OH} V_{OL}
VALID DATA
VALID DATA
VALID DATA
t_{OFF}
t_{OFF}
t_{OFF}
t_{CLZ}
t_{CLZ}
t_{CLZ}

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)


t_{RASP}
t_{RP}
$\overline{RAS}$ V_{IH} V_{IL}
t_{RCD}
t_{PC}
t_{RSH}
t_{CAS}
t_{CAS}
t_{CAS}
t_{CRP}
t_{CP}
t_{CP}
t_{CPN}
$\overline{CAS}$ V_{IH} V_{IL}
t_{AR}
t_{RAL}
t_{ASC}
t_{ASC}
t_{ASC}
t_{ASR}
t_{RAH}
t_{CAH}
t_{CAH}
t_{CAH}
ADDRESSES V_{IH} V_{IL}
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
t_{RAD}
t_{WCS}
t_{WCH}
t_{WCS}
t_{WCH}
t_{WCS}
t_{WCH}
t_{WP}
t_{WP}
t_{WP}
$\overline{W}$ V_{IH} V_{IL}
t_{DS}
t_{DS}
t_{DS}
t_{DH}
t_{DH}
t_{DH}
D (DATA IN) V_{IH} V_{IL}
VALID DATA
VALID DATA
VALID DATA
t_{DHR}

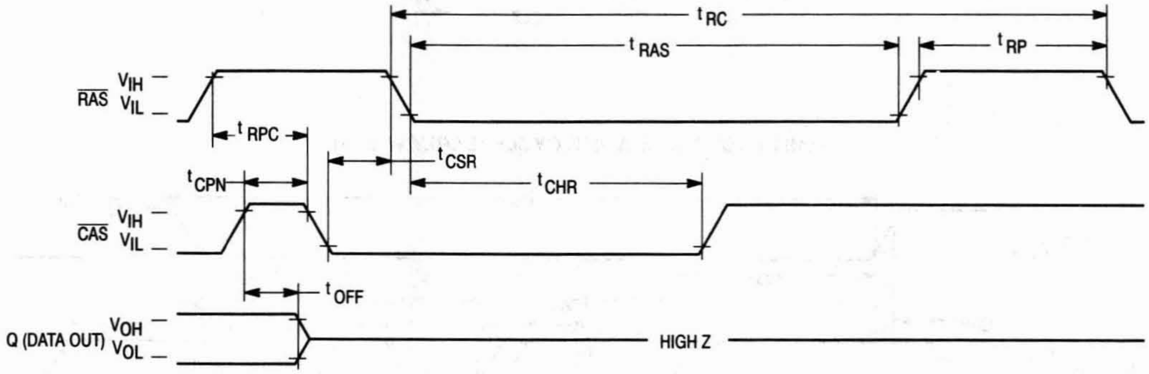
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

($\overline{\text{W}}$ and A9 are Don't Care)

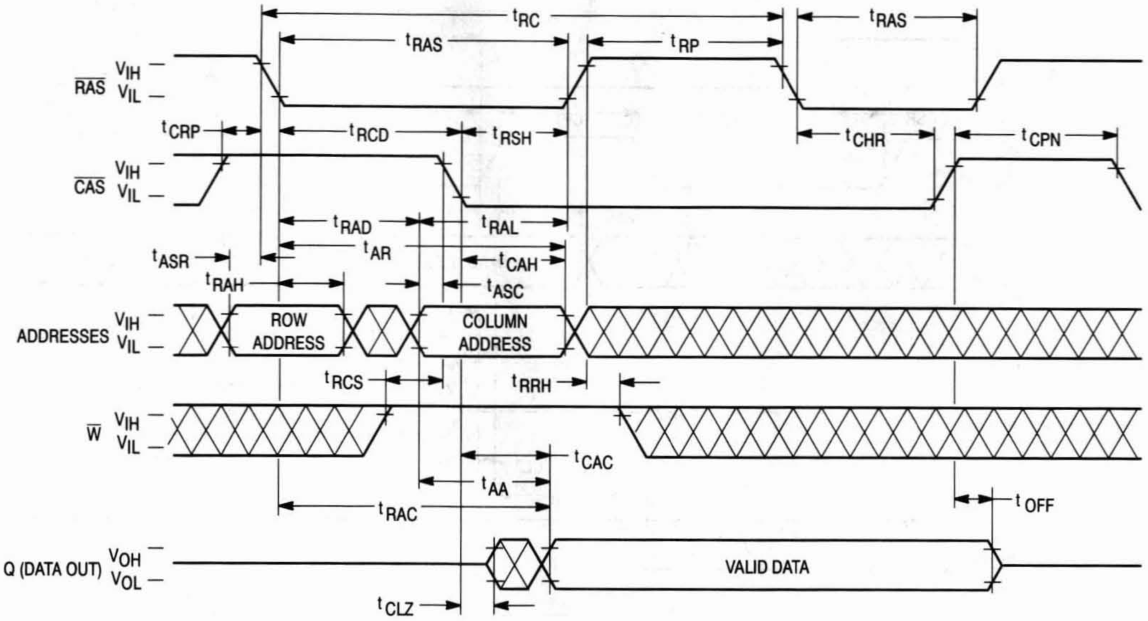

t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

(A0 – A9 are Don't Care)

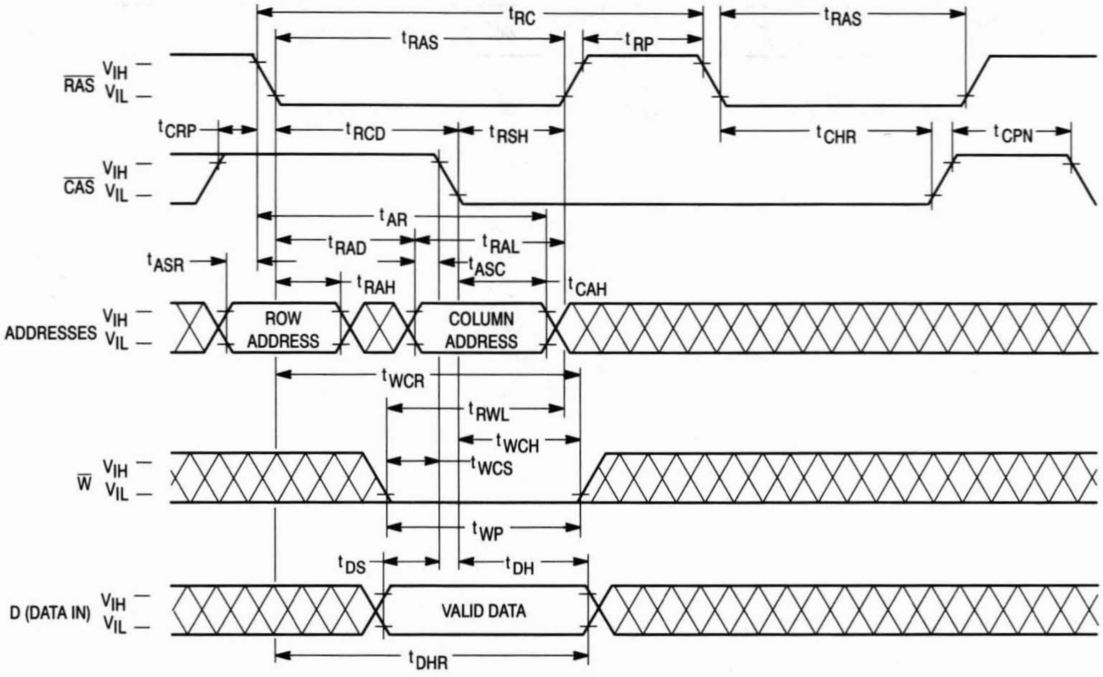

t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RPC}
t_{CSR}
t_{CPN}
t_{CHR}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{OFF}
Q (DATA OUT)
V_{OH}
V_{OL}
HIGH Z

HIDDEN REFRESH CYCLE (READ)



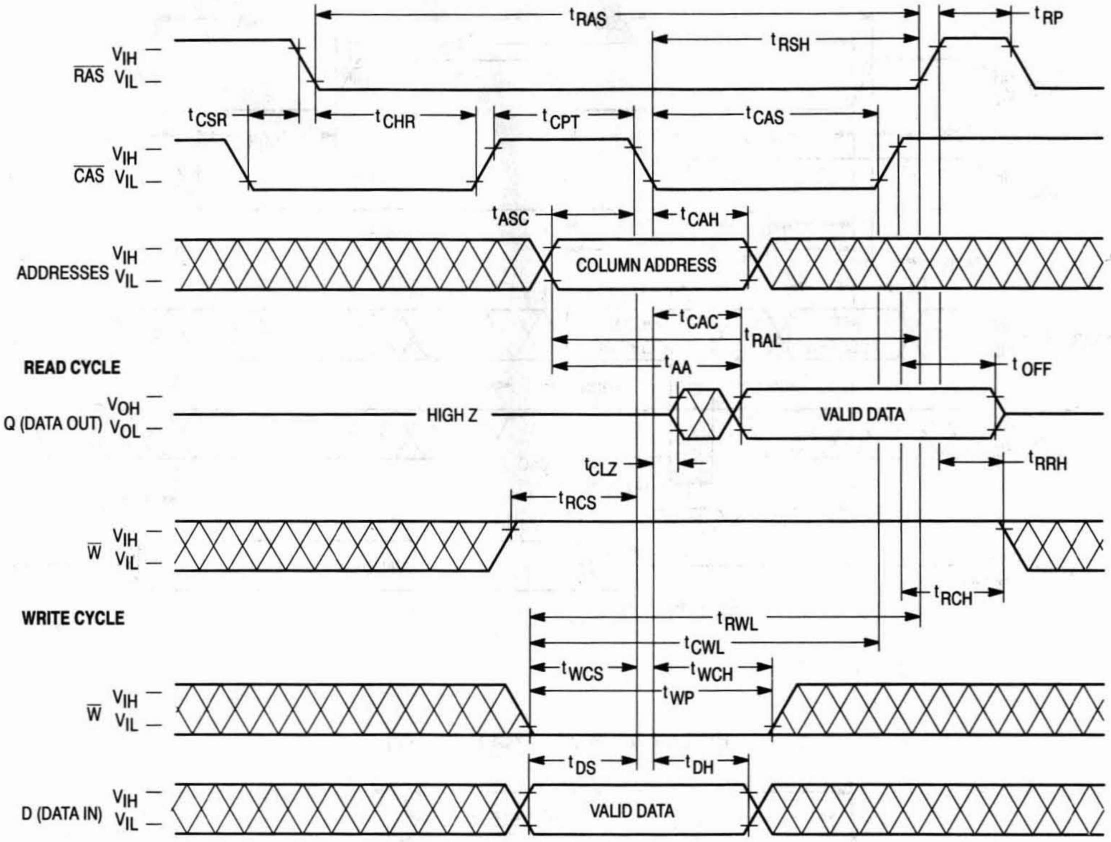
tRC
tRAS
tRP
tRAS
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCPN
CAS
VIH
VIL
tRAD
tRAL
tAR
tCAH
tASR
tRAH
tASC
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRCS
tRRH
W
VIH
VIL
tCAC
tAA
tRAC
tOFF
Q (DATA OUT)
VOH
VOL
VALID DATA
tCLZ

HIDDEN REFRESH CYCLE (WRITE)



tRC
tRAS
tRP
tRAS
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCPN
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tWCR
tRWL
tWCH
tWCS
W
VIH
VIL
tWP
tDS
tDH
D (DATA IN)
VIH
VIL
VALID DATA
tDHR

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



tRAS
tRP
tRSH
$\overline{\text{RAS}}$ VIH VIL
tCSR
tCHR
tCPT
tCAS
$\overline{\text{CAS}}$ VIH VIL
tASC
tCAH
ADDRESSES VIH VIL
COLUMN ADDRESS
tCAC
tRAL
READ CYCLE
tAA
tOFF
Q (DATA OUT) VOH VOL
HIGH Z
VALID DATA
tCLZ
tRRH
tRCS
$\overline{\text{W}}$ VIH VIL
tRCH
WRITE CYCLE
tRWL
tCWL
tWCS
tWCH
tWP
$\overline{\text{W}}$ VIH VIL
tDS
tDH
D (DATA IN) VIH VIL
VALID DATA

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the module. During an extended inactive state of the module (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to ensure proper device operation.

ADDRESSING THE RAM

The ten address bus pins on the device are time multiplexed with two separate 10-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of twenty address bits will decode one of the 2,097,152 word locations in the module. The column address strobe follows the row address strobe by a specified minimum and maximum time called t_{RCD}, which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up the external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the module. One is the $\overline{RAS}$-only refresh cycle (described later) where a 9-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A9 is not required for refresh. The other variation, page mode, allows the user to column access all words within a selected row. (See **PAGE-MODE CYCLES** section).

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, which is covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access from the $\overline{CAS}$ clock active transition (t_{CAC}) will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from the row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum period for the $\overline{RAS}$ clock (t_{RAS}) and the minimum period for the $\overline{CAS}$ clock (t_{CAS}). The $\overline{RAS}$ clock must stay inactive for the minimum time (t_{RP}). The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive mode (t_{RCH}).

WRITE CYCLE

A write cycle is similar to a read cycle except that the write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at all 1024 column locations on a selected row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 10-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, (previously described) followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In practice, any combination of read and write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the module needs to be refreshed at least once every 16 milliseconds. This is accomplished by sequentially cycling through the 1024 row address locations every 16 milliseconds (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the module will also refresh all the words associated with the particular row(s) decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 1024 row addresses every 16 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

This refresh cycle is initiated when $\overline{\text{RAS}}$ falls, after $\overline{\text{CAS}}$ has been low (by t_{CSR}). This activates the internal refresh counter, which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{\text{CAS}}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{\text{CAS}}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period (t_{RP}), executing a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. (See Figure 1.)

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 1024 test cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read cycle**. Repeat this operation 1024 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, write cycle**. Repeat this operation 1024 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

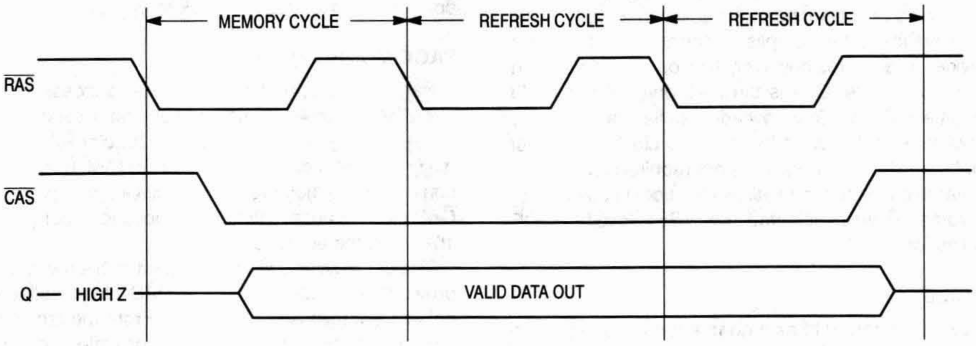


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION

(Order by Full Part Number)

MCM 36200 or 36L200 X XX

Motorola Memory Prefix — MCM
Part Number — 36200 or 36L200
Package (AS = SIMM, ASG = Gold Pad SIMM) — X
Speed (70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers — MCM36200AS70 MCM36200ASG70
MCM36200AS80 MCM36200ASG80

MCM36L200AS70 MCM36L200ASG70
MCM36L200AS80 MCM36L200ASG80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM36400

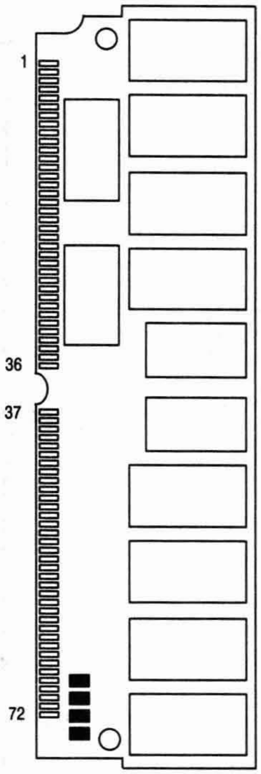
Product Preview

4M x 36 Bit Dynamic Random Access Memory Module

The MCM36400 is a dynamic random access memory (DRAM) module organized as 4,194,304 x 36 bits. The module is a 72-lead single-in-line memory module (SIMM) consisting of eight MCM517400 DRAMs, housed in 400 mil J-lead small outline packages (SOJ), and four MCM54100AN DRAMs housed in 300 mil J-lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM517400 is a CMOS high-speed dynamic random access memory organized as 4,194,304 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh: MCM36400 = 32 ms
- Consists of Eight 4M x 4 DRAMs, Four 4M x 1 DRAMs, and Twelve 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM36400-60 = 60 ns (Max)
  MCM36400-70 = 70 ns (Max)
  MCM36400-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM36400-60 = 7.92 W (Max)
  MCM36400-70 = 6.6 W (Max)
  MCM36400-80 = 5.61 W (Max)
- Low Standby Power Dissipation: TTL Levels = 132 mW (Max)
  CMOS Levels = 66 mW (Max)

S PACKAGE
SIMM MODULE
TOP VIEW



PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{\text{CAS2}}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{\text{CAS3}}$	54	DQ29	66	NC
7	DQ20	19	A10	31	A8	43	$\overline{\text{CAS1}}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{\text{RAS0}}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{\text{RAS2}}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	DQ26	47	$\overline{\text{W}}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

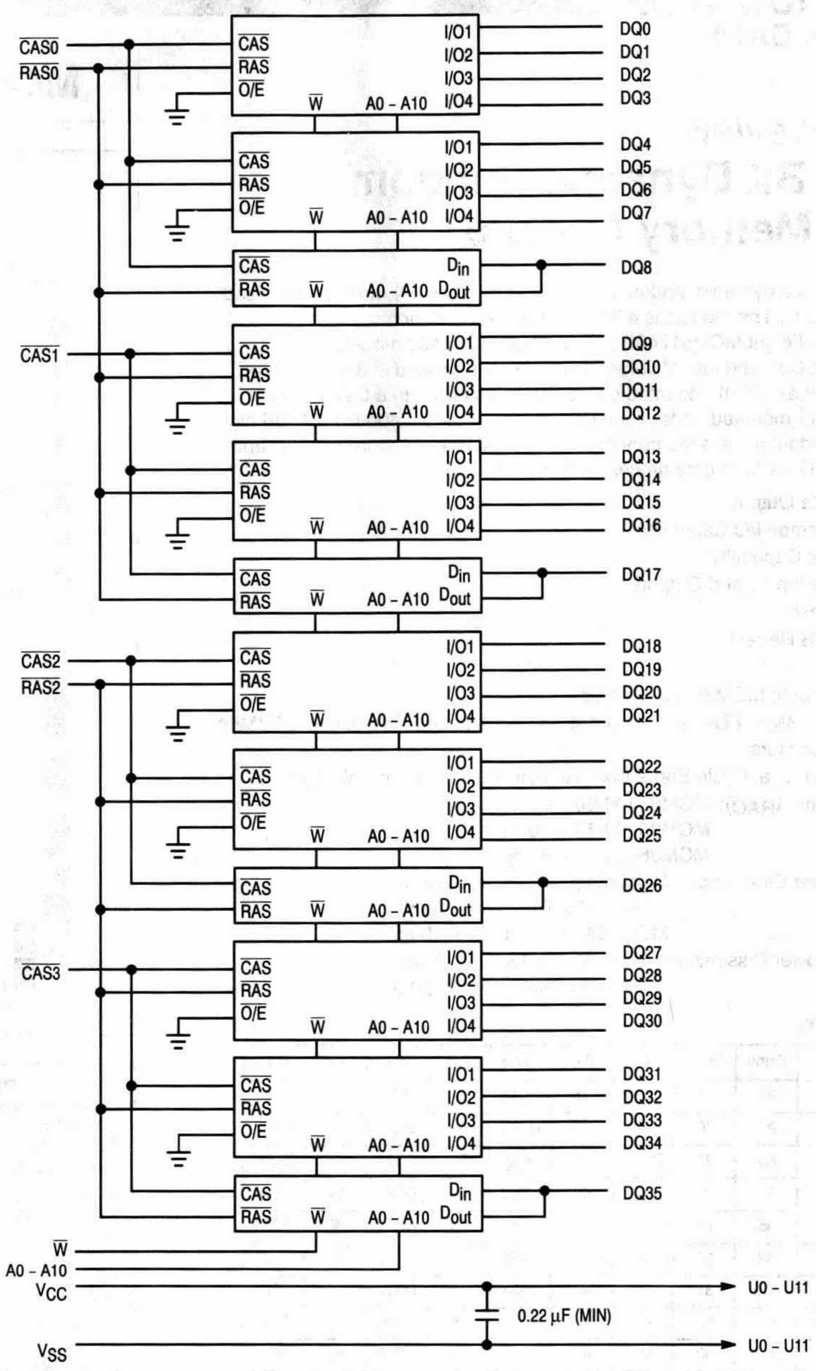
PIN NAMES

A0 – A10	Address Inputs
DQ0 – DQ35	Data Input/Output
$\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$	Column Address Strobe
PD1 – PD4	Presence Detect
$\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM


$\overline{CAS0}$
$\overline{RAS0}$
$\overline{CAS1}$
$\overline{CAS2}$
$\overline{RAS2}$
$\overline{CAS3}$
$\overline{CAS}$
$\overline{RAS}$
$\overline{O/E}$
$\overline{W}$
A0 – A10
I/O1
I/O2
I/O3
I/O4
D_{in}
D_{out}
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
DQ32
DQ33
DQ34
DQ35
$\overline{W}$
A0 – A10
V_{CC}
V_{SS}
0.22 µF (MIN)
U0 – U11
U0 – U11

PRESENCE DETECT PIN OUT			
Pin Name	**60 ns**	**70 ns**	**80 ns**
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	NC	NC	NC
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

ORDERING INFORMATION
(Order by Full Part Number)

MCM 36400 X XX

Motorola Memory Prefix — MCM

Part Number — 36400

Package (S = SIMM, SG = Gold Pad SIMM) — X

Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers —		
	MCM36400S60	MCM36400SG60
	MCM36400S70	MCM36400SG70
	MCM36400S80	MCM36400SG80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM36800

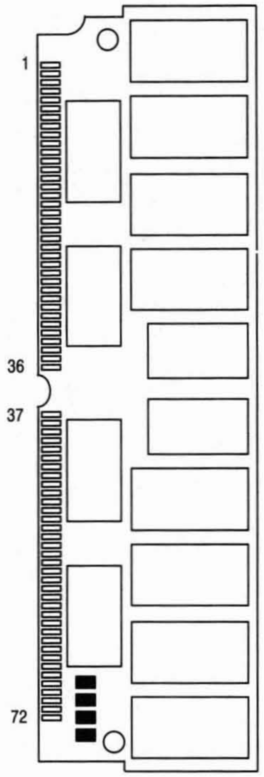
Product Preview

8M x 36 Bit Dynamic Random Access Memory Module

The MCM36800 is a dynamic random access memory (DRAM) module organized as 8,388,608 x 36 bits. The module is a 72-lead single-in-line memory module (SIMM) consisting of sixteen MCM517400 DRAMs, housed in 400 mil J-lead small outline packages (SOJ), and eight MCM54100AN DRAMs housed in 300 mil J-lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM517400 is a CMOS high-speed dynamic random access memory organized as 4,194,304 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh: MCM36800 = 32 ms
- Consists of Sixteen 4M x 4 DRAMs, Eight 4M x 1 DRAMs, and Twenty-Four 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM36800-60 = 60 ns (Max)
  MCM36800-70 = 70 ns (Max)
  MCM36800-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM36800-60 = 8.06 W (Max)
  MCM36800-70 = 6.74 W (Max)
  MCM36800-80 = 5.75 W (Max)
- Low Standby Power Dissipation: TTL Levels = 264 mW (Max)
  CMOS Levels = 132 mW (Max)

S PACKAGE
SIMM MODULE
TOP VIEW



PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{\text{CAS2}}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{\text{CAS3}}$	54	DQ29	66	NC
7	DQ20	19	A10	31	A8	43	$\overline{\text{CAS1}}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{\text{RAS0}}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{\text{RAS3}}$	45	$\overline{\text{RAS1}}$	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{\text{RAS2}}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	DQ26	47	$\overline{\text{W}}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

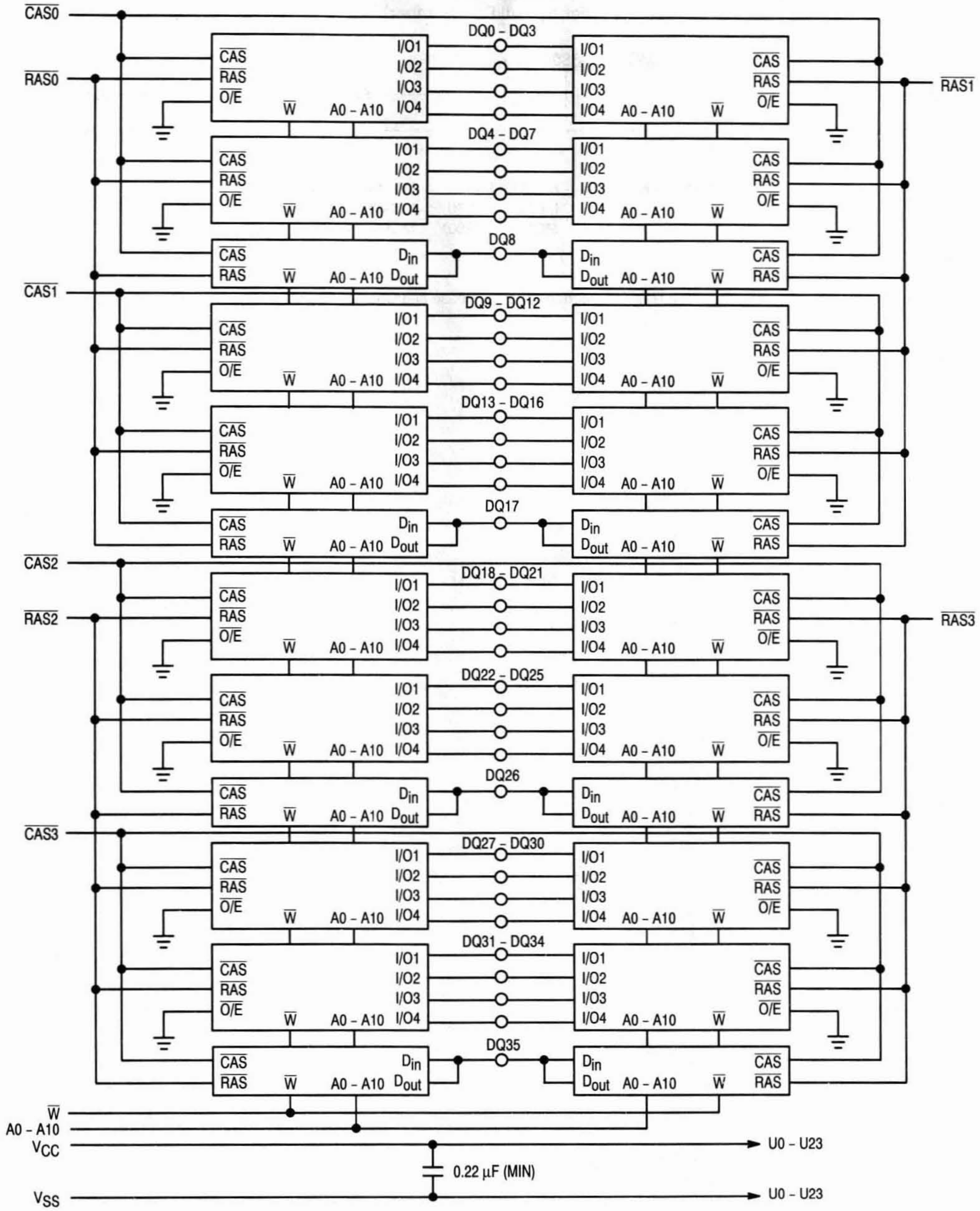
PIN NAMES

A0 – A10	Address Inputs
DQ0 – DQ35	Data Input/Output
$\overline{\text{CAS0}}$ – $\overline{\text{CAS3}}$	Column Address Strobe
PD1 – PD4	Presence Detect
$\overline{\text{RAS0}}$ – $\overline{\text{RAS3}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM


CAS0
RAS0
CAS1
CAS2
RAS2
CAS3
RAS1
RAS3
DQ0 – DQ3
DQ4 – DQ7
DQ8
DQ9 – DQ12
DQ13 – DQ16
DQ17
DQ18 – DQ21
DQ22 – DQ25
DQ26
DQ27 – DQ30
DQ31 – DQ34
DQ35
CAS
RAS
O/E
W
A0 – A10
I/O1
I/O2
I/O3
I/O4
Din
Dout
W
A0 – A10
VCC
VSS
0.22 µF (MIN)
U0 – U23
U0 – U23

PRESENCE DETECT PIN OUT			
Pin Name	**60 ns**	**70 ns**	**80 ns**
PD1	NC	NC	NC
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

ORDERING INFORMATION
(Order by Full Part Number)

MCM 36800 X XX

Motorola Memory Prefix — MCM
Part Number — 36800
Package (S = SIMM, SG = Gold Pad SIMM) — X
Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers — MCM36800S60 MCM36800SG60
MCM36800S70 MCM36800SG70
MCM36800S80 MCM36800SG80

NOTE: For mechanical data, please see Chapter 10.

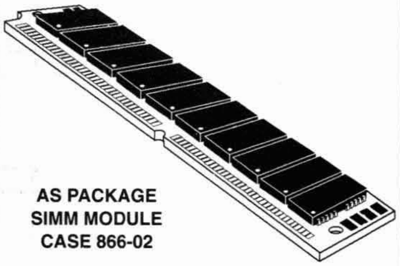
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM40256
MCM40L256

256K x 40 Bit Dynamic Random Access Memory Module
for Error Correction Applications

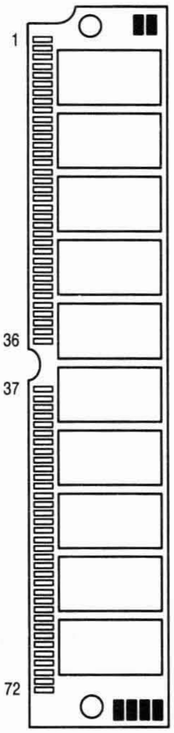
The MCM40256 and MCM40L256 are 10M dynamic random access memory (DRAM) modules organized as 262,144 x 40 bits. The module is a 72-lead single-in-line memory module (SIMM) consisting of ten MCM514256A DRAMs housed in 20/26 J-lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM514256A is a 1.0µ CMOS high-speed dynamic random access memory organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh: MCM40256 = 8 ms (Max)
  MCM40L256 = 64 ms (Max)
- Consists of Ten 256K x 4 DRAMs, and Ten 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM40256-60 = 60 ns (Max)
  MCM40256-70 = 70 ns (Max)
  MCM40256-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM40200-60 = 4.95 W (Max)
  MCM40256-70 = 4.40 W (Max)
  MCM40256-80 = 3.85 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 110 mW (Max)
  CMOS Levels = 55 mW (Max, MCM40256)
  = 11 mW (Max, MCM40L256)



AS PACKAGE
SIMM MODULE
CASE 866-02

TOP VIEW



PIN NAMES

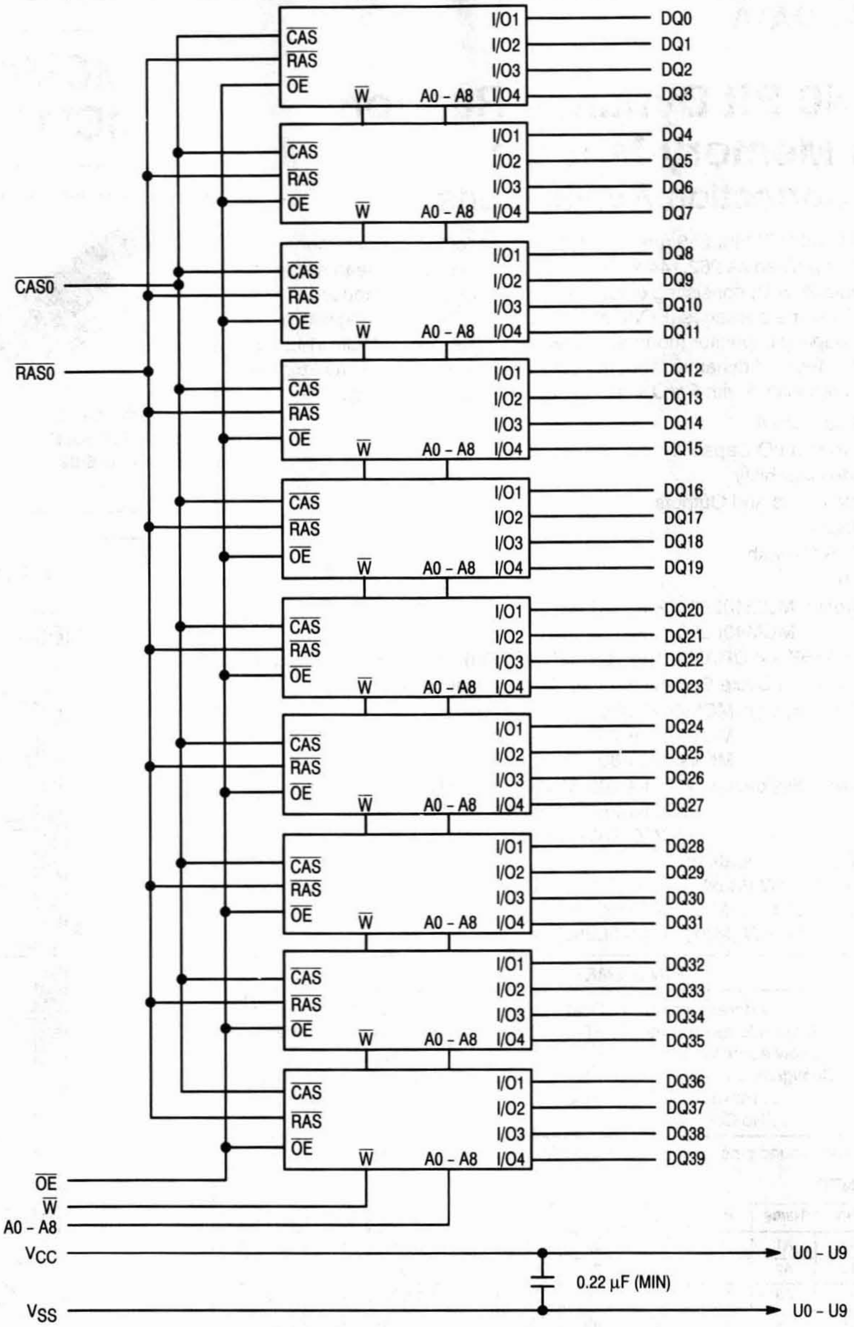
A0 – A8	Address Inputs	DQ0 – DQ39	Data Input/Output
$\overline{\text{CAS0}}$	Column Address Strobe	PD1 – PD5	Presence Detect
$\overline{\text{RAS0}}$	Row Address Strobe	$\overline{\text{W}}$	Read/Write Input
$\overline{\text{X40}}$	Configuration Detection	$\overline{\text{OE}}$	Output Enable
V_{CC}	Power (+ 5 V)	V_{SS}	Ground
NC	No Connection		

All power supply and ground pins must be connected for proper operation of the device.

PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	NC	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{\text{OE}}$	31	A8	43	NC	55	DQ28	67	PD1
8	DQ6	20	DQ8	32	NC	44	$\overline{\text{RAS0}}$	56	DQ29	68	PD2
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ30	69	PD3
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD4
11	PD5	23	DQ11	35	DQ17	47	$\overline{\text{W}}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	$\overline{\text{X40}}$	60	DQ32	72	V_{SS}

256K x 40 BLOCK DIAGRAM


CAS
RAS
OE
W
A0 - A8
I/O1
I/O2
I/O3
I/O4
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
DQ32
DQ33
DQ34
DQ35
DQ36
DQ37
DQ38
DQ39
CAS0
RAS0
OE
W
A0 - A8
VCC
VSS
0.22 µF (MIN)
U0 - U9
U0 - U9

PRESENCE DETECT PIN OUT			
Pin Name	**60 ns**	**70 ns**	**80 ns**
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	NC	NC	NC
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}
PD5	NC	NC	NC
$\overline{\text{X40}}$	V_{SS}	V_{SS}	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	6.75	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	MCM40256-60, t_{RC} = 110 ns MCM40256-70, t_{RC} = 130 ns MCM40256-80, t_{RC} = 150 ns	I_{CC1}	— — —	900 800 700	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	20	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles	MCM40256-60, t_{RC} = 110 ns MCM40256-70, t_{RC} = 130 ns MCM40256-80, t_{RC} = 150 ns	I_{CC3}	— — —	900 800 700	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle	MCM40256-60, t_{PC} = 40 ns MCM40256-70, t_{PC} = 40 ns MCM40256-80, t_{PC} = 45 ns	I_{CC4}	— — —	600 600 500	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	MCM40256 MCM40L256	I_{CC5}	— —	10 2	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	MCM40256-60, t_{RC} = 110 ns MCM40256-70, t_{RC} = 130 ns MCM40256-80, t_{RC} = 150 ns	I_{CC6}	— — —	900 800 700	mA	1
V_{CC} Power Supply Current Battery Backup Mode (t_{RC} = 125 μs; $\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$, DQ, A0 – A8 = V_{CC} – 0.2 V or 0.2 V) t_{RAS} = 1 μs	MCM40L256 only	I_{CC7}	—	3.0	mA	3
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)		$I_{lkg(I)}$	– 100	100	μA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)		$I_{lkg(O)}$	– 10	+ 10	μA	
Output High Voltage (I_{OH} = – 5 mA)		V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.
3. t_{RAS} (max) = 1 μs is applied to refresh of battery back-up. t_{RAS} (max) = 10 μs is applied to functional operating.

CAPACITANCE ($f = 1.0$ MHz, $T_A = 25°C$, $V_{CC} = 5$ V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit
Input Capacitance (A0 – A8)	C_{I1}	—	60	pF
Input Capacitance ($\overline{\text{W}}$, $\overline{\text{OE}}$, $\overline{\text{CAS0}}$, $\overline{\text{RAS0}}$)	C_{I2}	—	80	pF
I/O Capacitance (DQ0 – DQ39)	C_{DQ1}	—	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\ \Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0\ V \pm 10\%$, $T_A = 0$ to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM40256-60 MCM40L256-60		MCM40256-70 MCM40L256-70		MCM40256-80 MCM40L256-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RMW}	165	—	185	—	205	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	40	—	45	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRMW}	95	—	95	—	100	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6, 9
Access Time from $\overline{\text{CAS}}$ Precharge	t_{CEHQV}	t_{CPA}	—	35	—	35	—	40	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge (Page Mode Cycle Only)	t_{CELREH}	t_{RHCP}	35	—	35	—	40	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	11

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements $t_T = 5.0$ ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$ and -40 to $+85°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) and/or t_{GZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM40256-60 MCM40L256-60		MCM40256-70 MCM40L256-70		MCM40256-80 MCM40L256-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELAX}	t_{AR}	50	—	55	—	60	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELWH}	t_{WCR}	45	—	55	—	60	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	14
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	50	—	55	—	60	—	ns	
Refresh Period MCM40256 MCM40L256	t_{RVRV}	t_{RFSH}	— —	8 64	— —	8 64	— —	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	50	—	ns	15
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	90	—	100	—	110	—	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	60	—	65	—	70	—	ns	15
$\overline{\text{CAS}}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	65	—	65	—	70	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	ns	

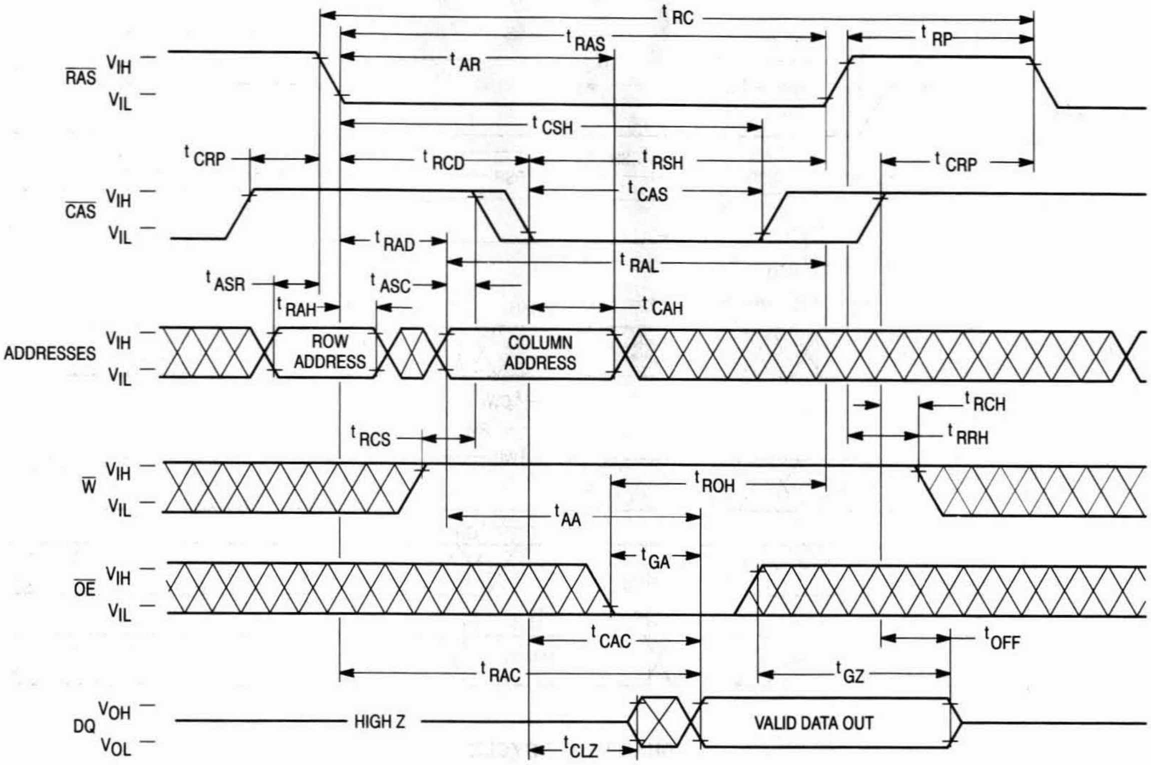
NOTES: (continued)

12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in delayed write or read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

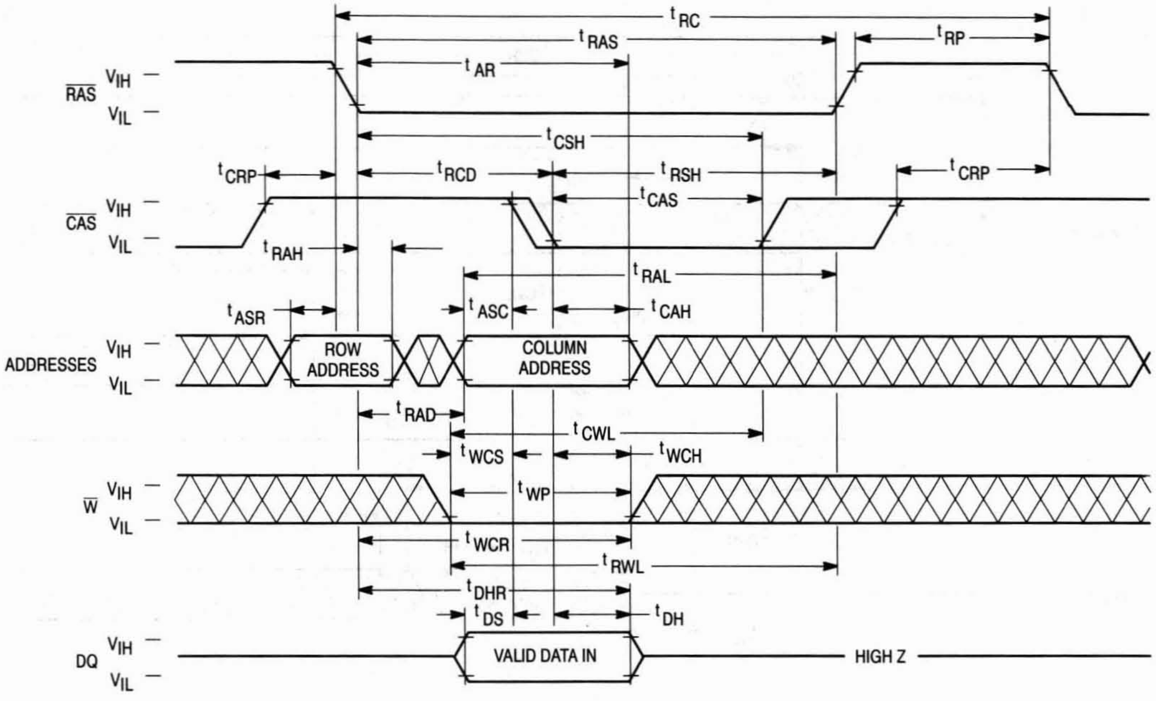
Parameter	Symbol		MCM40256-60 MCM40L256-60		MCM40256-70 MCM40L256-70		MCM40256-80 MCM40L256-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{OE}}$	t_{GLREH}	t_{ROH}	10	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	20	—	20	ns	
$\overline{\text{OE}}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	20	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{\text{OE}}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	20	ns	10
$\overline{\text{OE}}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	20	—	ns	

READ CYCLE



tRC
tRAS
tRP
tAR
RAS VIH VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS VIH VIL
tRAD
tRAL
tASR
tASC
tRAH
tCAH
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
tRCH
tRCS
tRRH
W VIH VIL
tROH
tAA
tGA
OE VIH VIL
tCAC
tOFF
tRAC
tGZ
DQ VOH VOL
HIGH Z
VALID DATA OUT
tCLZ

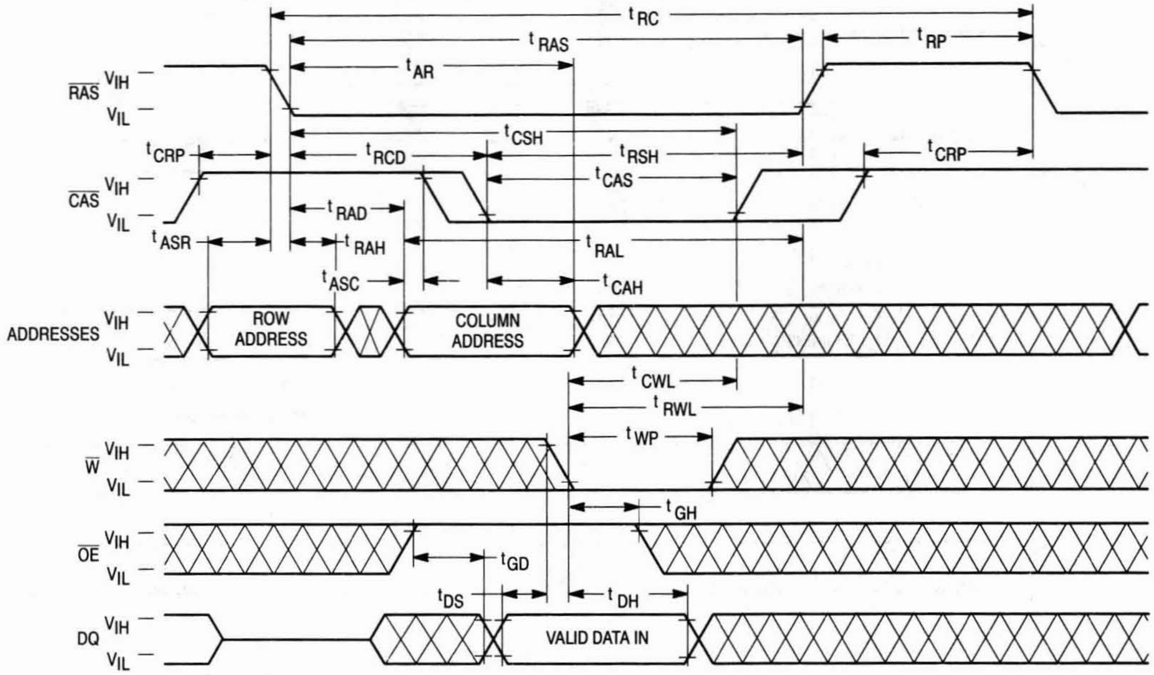
EARLY WRITE CYCLE



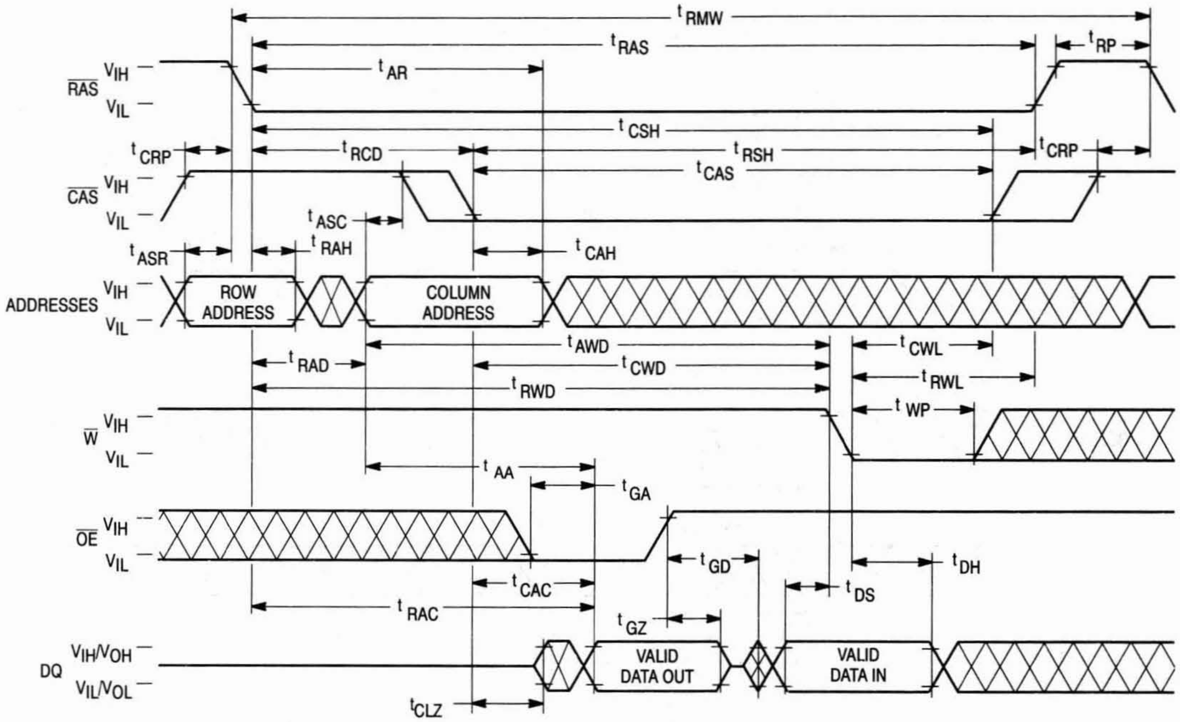
tRC
tRAS
tRP
tAR
RAS VIH VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS VIH VIL
tRAH
tRAL
tASR
tASC
tCAH
ADDRESSES VIH VIL
ROW ADDRESS
COLUMN ADDRESS
tRAD
tCWL
tWCS
tWCH
W VIH VIL
tWP
tWCR
tRWL
tDHR
tDS
tDH
DQ VIH VIL
VALID DATA IN
HIGH Z

5

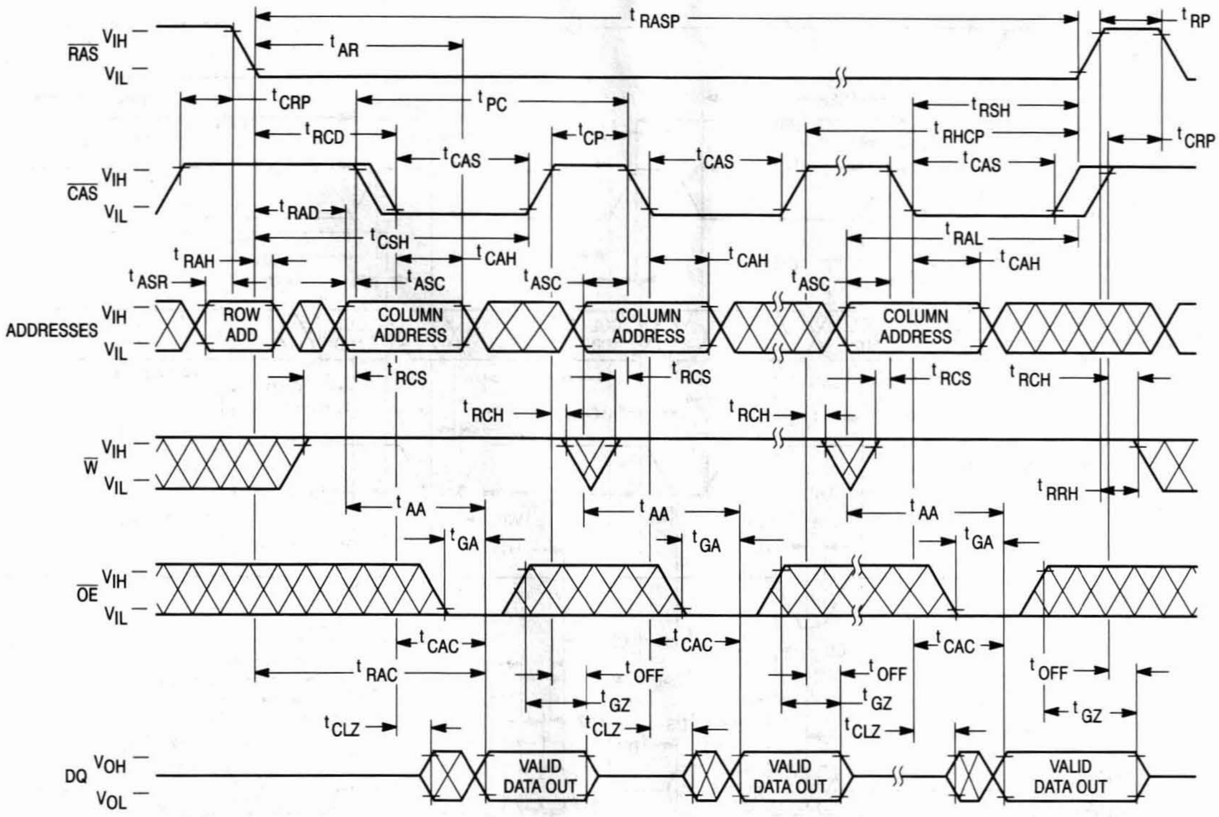
$\overline{\text{OE}}$ CONTROLLED LATE WRITE CYCLE


t RC
t RAS
t AR
t RP
RAS
VIH
VIL
t CSH
t CRP
t RCD
t RSH
t CRP
CAS
VIH
VIL
t CAS
t RAD
t ASR
t RAH
t RAL
t ASC
t CAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
t CWL
t RWL
t WP
W
VIH
VIL
t GH
OE
VIH
VIL
t GD
t DS
t DH
DQ
VIH
VIL
VALID DATA IN

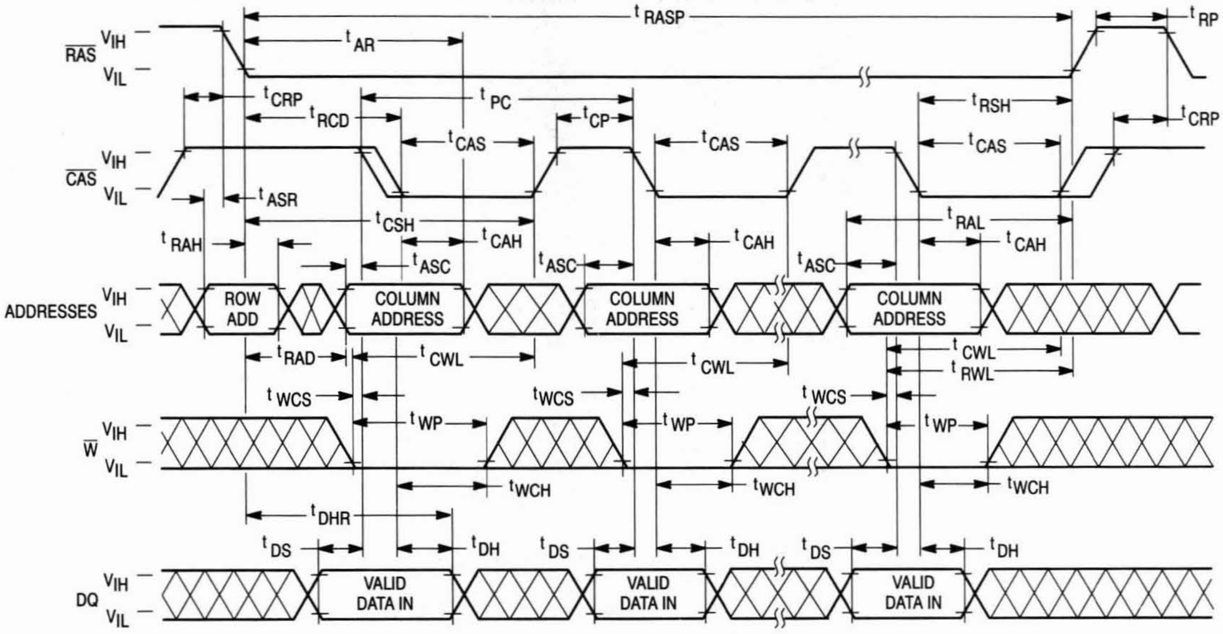
READ-WRITE CYCLE


t RMW
t RAS
t RP
t AR
RAS
VIH
VIL
t CSH
t CRP
t RCD
t RSH
t CRP
CAS
VIH
VIL
t CAS
t ASC
t ASR
t RAH
t CAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
t AWD
t CWL
t RAD
t CWD
t RWL
t RWD
t WP
W
VIH
VIL
t AA
t GA
OE
VIH
VIL
t GD
t CAC
t DS
t DH
t RAC
t GZ
DQ
VIH/VOH
VIL/VOL
VALID DATA OUT
VALID DATA IN
tCLZ

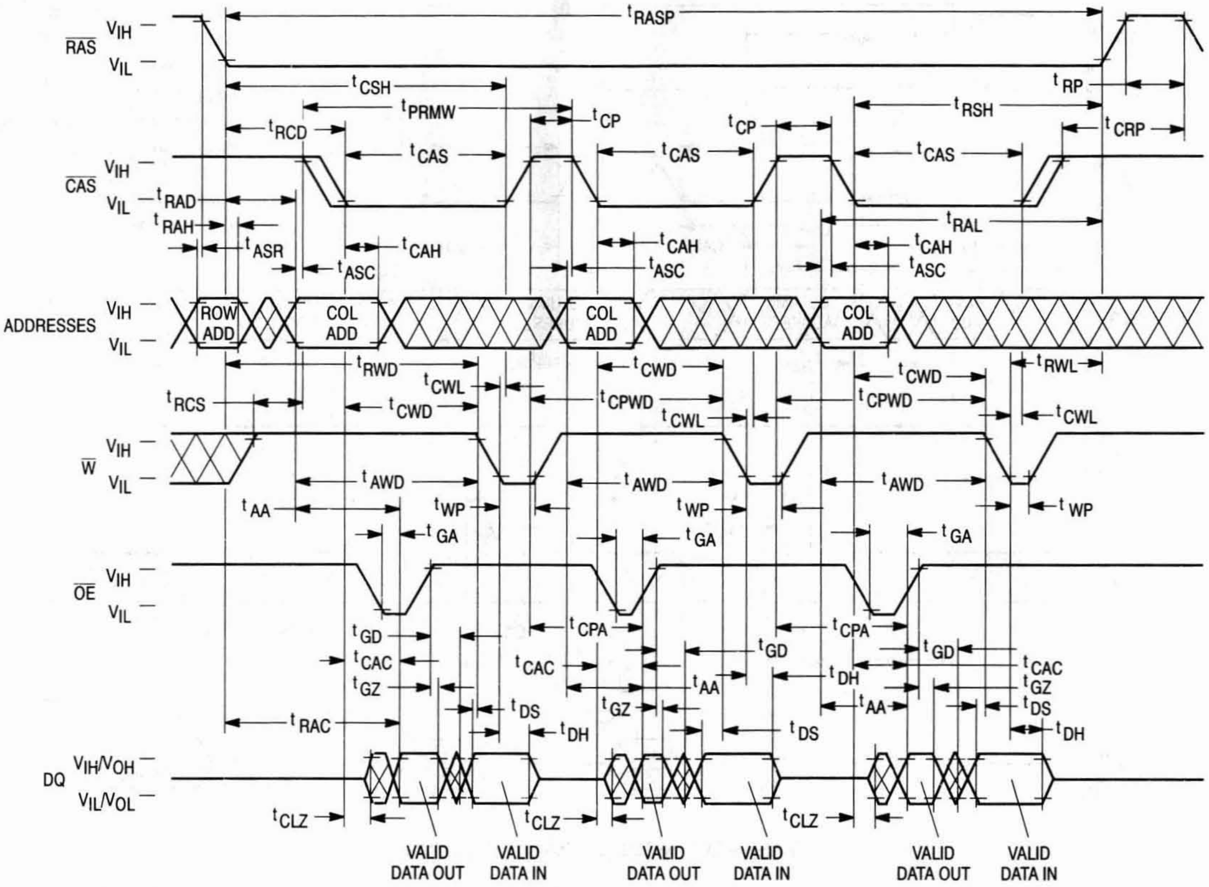
FAST PAGE MODE READ CYCLE


RAS
CAS
ADDRESSES
W
OE
DQ
VIH
VIL
VOH
VOL
tRASP
tRP
tAR
tCRP
tPC
tRSH
tRCD
tCP
tRHCP
tCAS
tRAD
tCSH
tRAL
tRAH
tCAH
tASR
tASC
ROW ADD
COLUMN ADDRESS
tRCS
tRCH
tRRH
tAA
tGA
tCAC
tRAC
tOFF
tGZ
tCLZ
VALID DATA OUT

FAST PAGE MODE EARLY-WRITE CYCLE

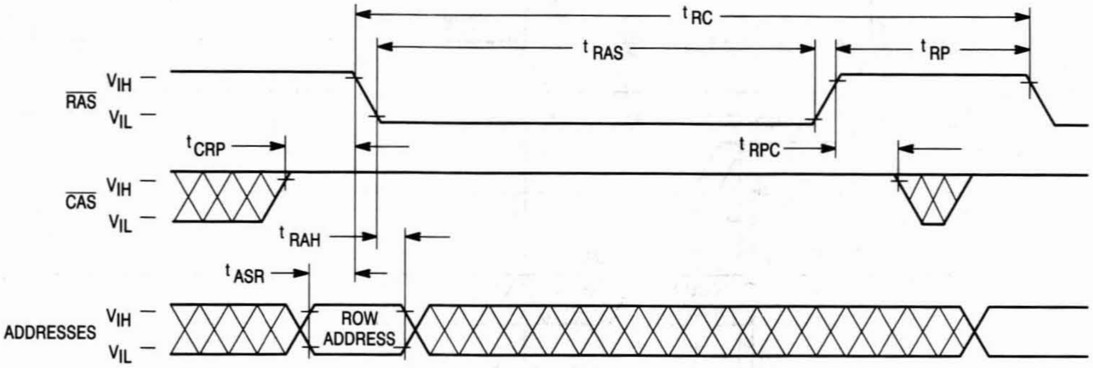

RAS
CAS
ADDRESSES
W
DQ
VIH
VIL
tRASP
tRP
tAR
tCRP
tPC
tRCD
tCP
tRSH
tCAS
tASR
tCSH
tRAL
tRAH
tCAH
tASC
ROW ADD
COLUMN ADDRESS
tRAD
tCWL
tRWL
tWCS
tWP
tWCH
tDHR
tDS
tDH
VALID DATA IN

FAST PAGE MODE READ-WRITE CYCLE


RAS
VIH
VIL
CAS
ADDRESSES
W
OE
DQ
VIH/VOH
VIL/VOL
tRASP
tCSH
tPRMW
tRCD
tCP
tRSH
tRP
tCRP
tCAS
tRAD
tRAH
tASR
tCAH
tASC
tRAL
ROW ADD
COL ADD
tRWD
tCWL
tCWD
tCPWD
tRWL
tRCS
tAWD
tAA
tWP
tGA
tGD
tCAC
tGZ
tCPA
tDH
tDS
tRAC
tCLZ
VALID DATA OUT
VALID DATA IN

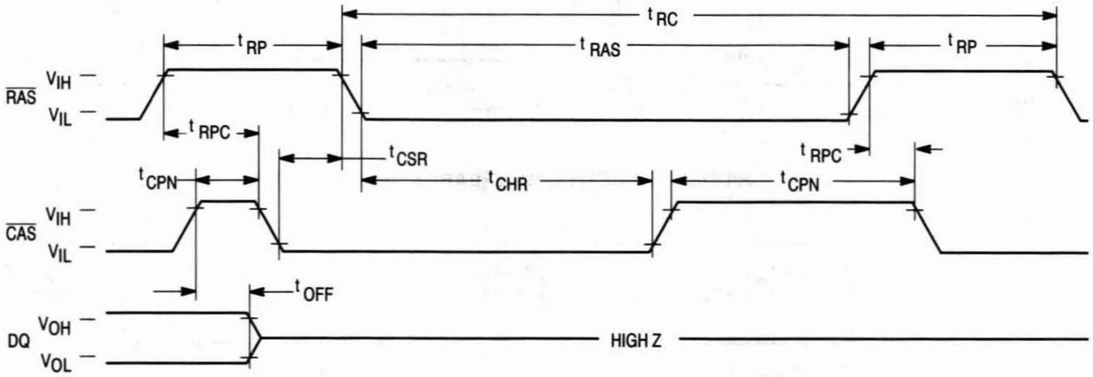
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

($\overline{\text{W}}$ and $\overline{\text{OE}}$ are Don't Care)

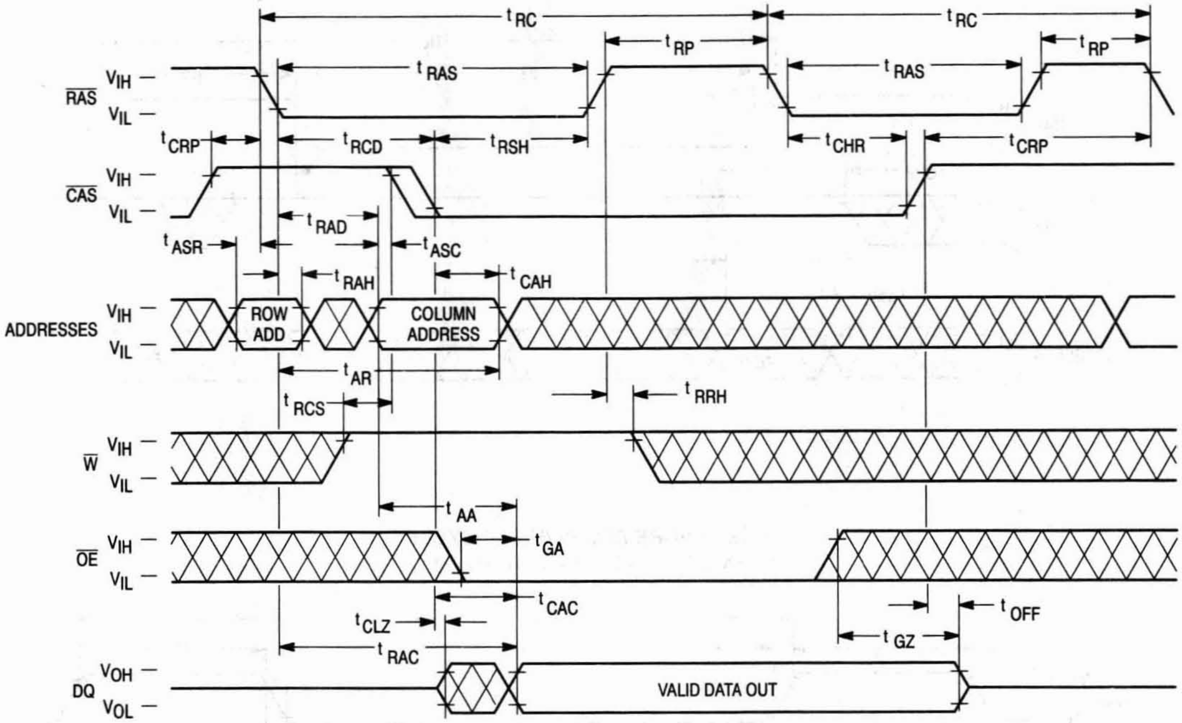

t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAH}
t_{ASR}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{W}}$, $\overline{\text{OE}}$, and A0 – A8 are Don't Care)

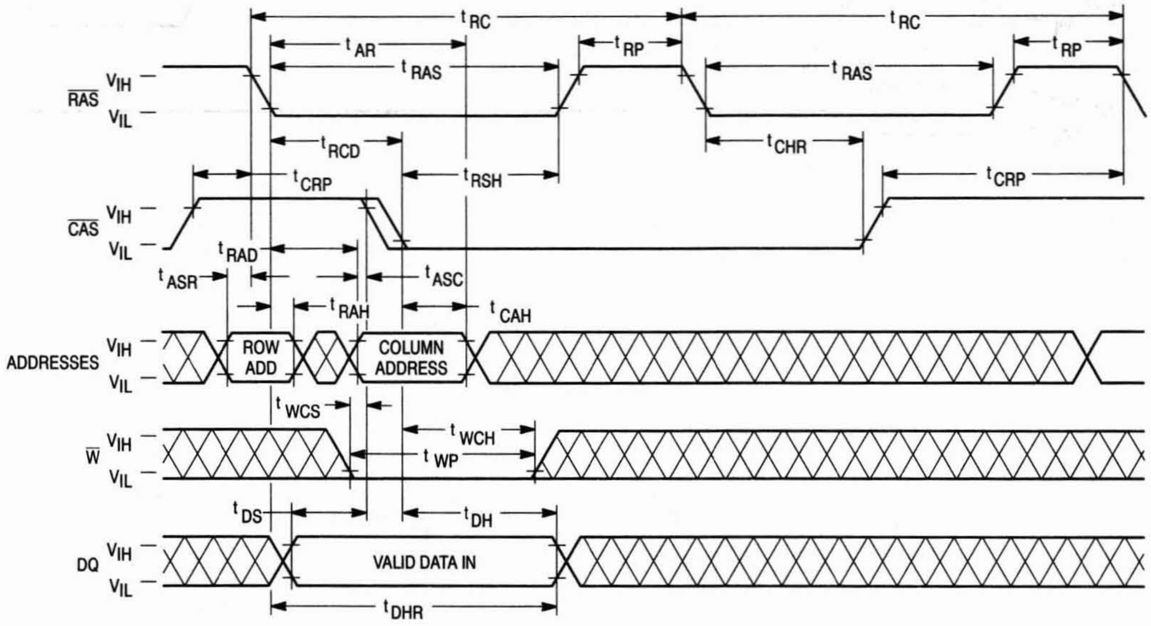

t_{RC}
t_{RP}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{RPC}
t_{CSR}
t_{RPC}
t_{CPN}
t_{CHR}
t_{CPN}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{OFF}
DQ
V_{OH}
V_{OL}
HIGH Z

HIDDEN REFRESH CYCLE (READ)



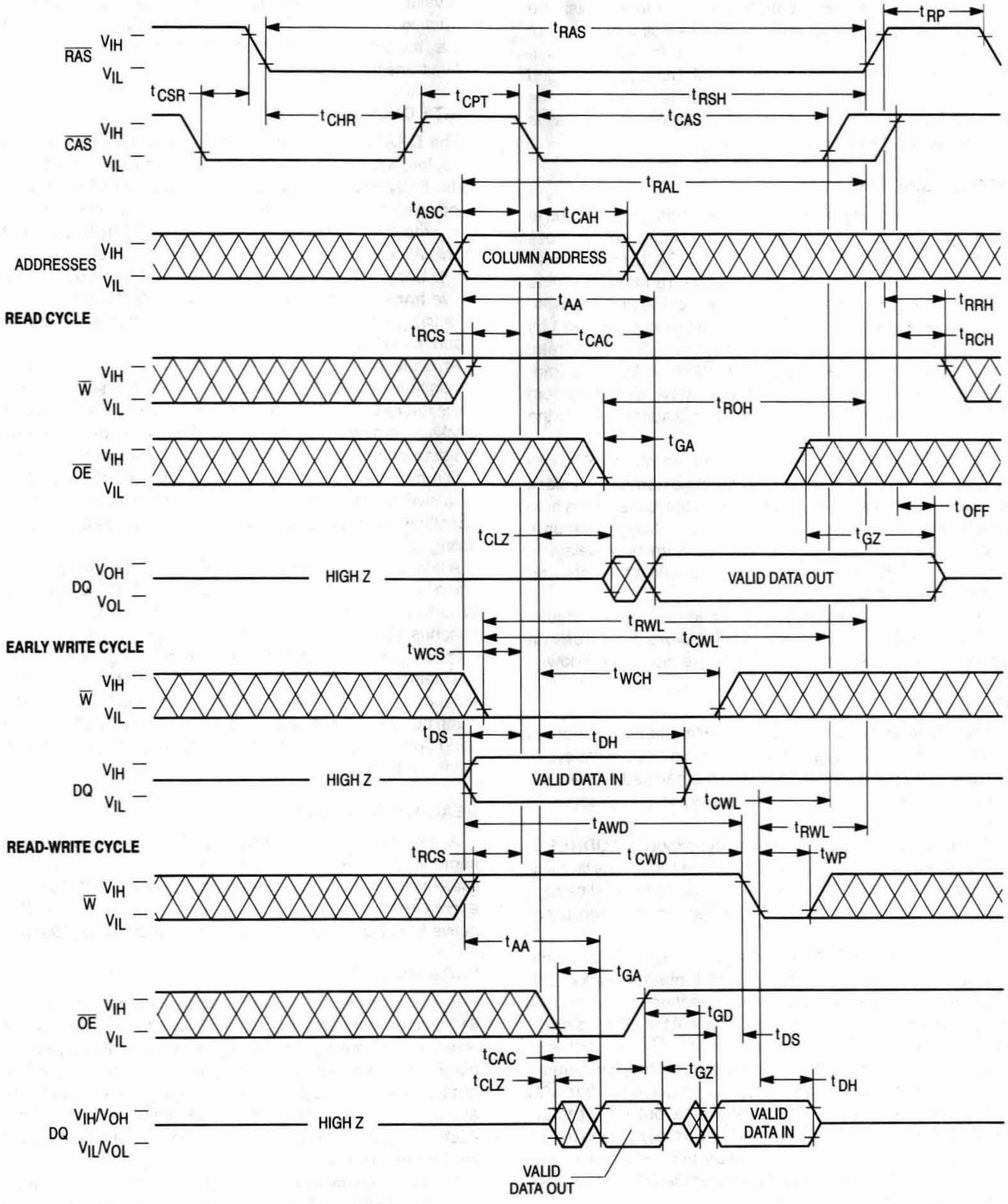
t RC
t RC
t RP
t RP
t RAS
t RAS
RAS
VIH
VIL
t CRP
t RCD
t RSH
t CHR
t CRP
CAS
VIH
VIL
t RAD
t ASR
t ASC
t RAH
t CAH
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
t AR
t RCS
t RRH
W
VIH
VIL
t AA
OE
VIH
VIL
t GA
t CAC
t CLZ
t OFF
t GZ
t RAC
DQ
VOH
VOL
VALID DATA OUT

HIDDEN REFRESH CYCLE (EARLY WRITE)



t RC
t RC
t AR
t RP
t RP
t RAS
t RAS
RAS
VIH
VIL
t RCD
t CHR
t CRP
t RSH
t CRP
CAS
VIH
VIL
t RAD
t ASR
t ASC
t RAH
t CAH
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
t WCS
t WCH
t WP
W
VIH
VIL
t DS
t DH
DQ
VIH
VIL
VALID DATA IN
t DHR

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE


$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RAS}
t_{RP}
t_{CSR}
t_{CHR}
t_{CPT}
t_{RSH}
t_{CAS}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{RAL}
t_{ASC}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
COLUMN ADDRESS
READ CYCLE
t_{AA}
t_{RRH}
t_{RCS}
t_{CAC}
t_{RCH}
$\overline{\text{W}}$
V_{IH}
V_{IL}
t_{ROH}
t_{GA}
$\overline{\text{OE}}$
V_{IH}
V_{IL}
t_{OFF}
t_{CLZ}
t_{GZ}
DQ
V_{OH}
V_{OL}
HIGH Z
VALID DATA OUT
t_{RWL}
t_{CWL}
EARLY WRITE CYCLE
t_{WCS}
t_{WCH}
$\overline{\text{W}}$
V_{IH}
V_{IL}
t_{DS}
t_{DH}
DQ
V_{IH}
V_{IL}
HIGH Z
VALID DATA IN
t_{CWL}
t_{AWD}
t_{RWL}
READ-WRITE CYCLE
t_{RCS}
t_{CWD}
t_{WP}
$\overline{\text{W}}$
V_{IH}
V_{IL}
t_{AA}
t_{GA}
$\overline{\text{OE}}$
V_{IH}
V_{IL}
t_{GD}
t_{DS}
t_{CAC}
t_{GZ}
t_{CLZ}
t_{DH}
DQ
V_{IH}/V_{OH}
V_{IL}/V_{OL}
HIGH Z
VALID DATA IN
VALID DATA OUT

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 word locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This gate feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are two other variations in addressing the module: **$\overline{\text{RAS}}$-only refresh cycle** and **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: normal random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{\text{CAS}}$ and output enable ($\overline{\text{OE}}$) control read access time: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum and $\overline{\text{OE}}$ must be active t_{RAC}-t_{GA} (both minimum) after $\overline{\text{RAS}}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{\text{OE}}$ active transition does not occur in time, read access time is determined by either the $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ clocks are active. When either the $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The DRAM may be written with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data In (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data out buffers disabled, effectively disabling $\overline{\text{OE}}$.

A late write cycle (referred to as $\overline{\text{OE}}$ controlled write) occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + t_T) \leq t_{RAS}$, if timing minimums ($t_{RCD}$, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but Q may be indeterminate — see note 15 of AC Operating Conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 512 column locations on a selected row of the dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically refreshed (recharged) to maintain the correct bit state. Bits in the MCM40256 require refresh every 8 milliseconds while refresh time for the MCM40L256 is 64 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM40256 and 124.8 microseconds for the MCM40L256. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM40256 and 64 milliseconds on the MCM40L256.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other mehtods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

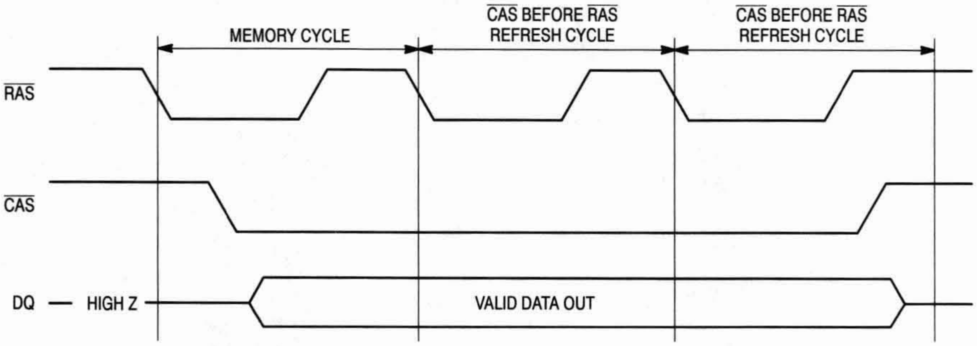


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM **40256 or 40L256** **X** **XX**

Motorola Memory Prefix — MCM

Part Number — 40256 or 40L256

Package (AS = SIMM, ASG = Gold Pad SIMM) — X

Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers —		
	MCM40256AS60	MCM40256ASG60
	MCM40256AS70	MCM40256ASG70
	MCM40256AS80	MCM40256ASG80
	MCM40L256AS60	MCM40L256ASG60
	MCM40L256AS70	MCM40L256ASG70
	MCM40L256AS80	MCM40L256ASG80

NOTE: For mechanical data, please see Chapter 10.

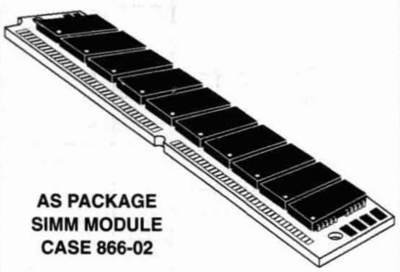
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM40512
MCM40L512

512K x 40 Bit Dynamic Random Access Memory Module
for Error Correction Applications

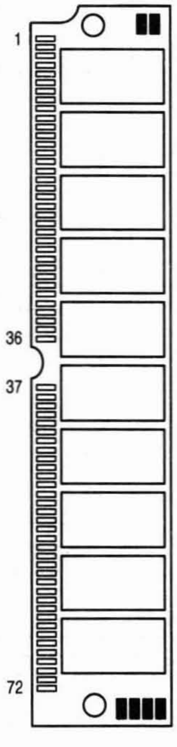
The MCM40512 and MCM40L512 are 20M dynamic random access memory (DRAM) modules organized as 524,288 x 40 bits. The module is a double-sided 72-lead single-in-line memory module (SIMM) consisting of twenty MCM514256A DRAMs housed in 20/26 J-lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM514256A is a 1.0µ CMOS high-speed dynamic random access memory organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh: MCM40512 = 8 ms (Max)
  MCM40L512 = 64 ms (Max)
- Consists of Twenty 256K x 4 DRAMs, and Twenty 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM40512-60 = 60 ns (Max)
  MCM40512-70 = 70 ns (Max)
  MCM40512-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM40512-60 = 5.06 W (Max)
  MCM40512-70 = 4.51 W (Max)
  MCM40512-80 = 3.96 W (Max)
- Low Standby Power Dissipation: TTL Levels = 220 mW (Max)
  CMOS Levels = 110 mW (Max, MCM40512)
  = 22 mW (Max, MCM40L512)



AS PACKAGE
SIMM MODULE
CASE 866-02

TOP VIEW



PIN NAMES

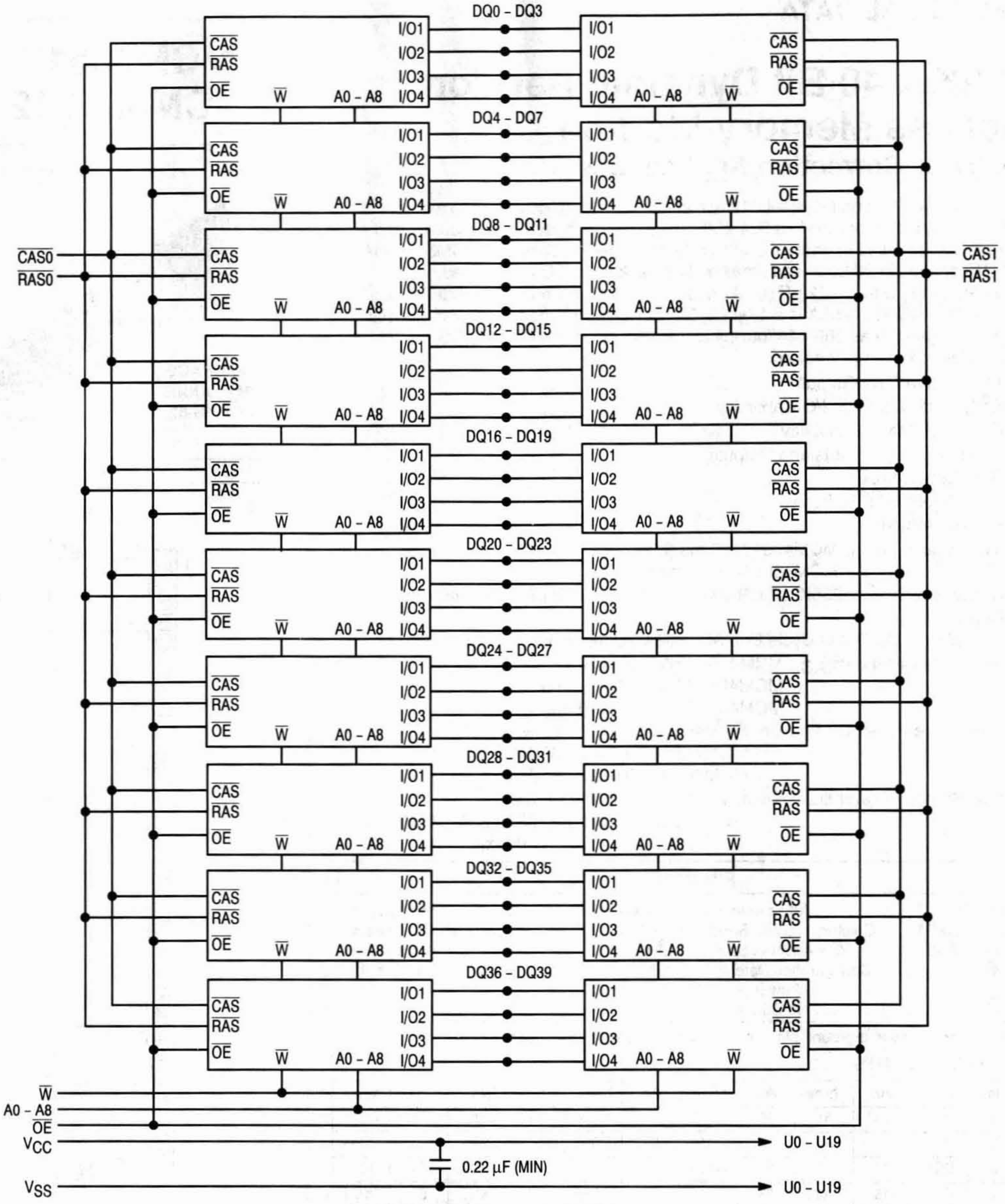
A0 – A8	Address Inputs	DQ0 – DQ39	Data Input/Output
$\overline{\text{CAS0}}$, $\overline{\text{CAS1}}$	Column Address Strobe	PD1 – PD5	Presence Detect
$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$	Row Address Strobe	$\overline{\text{W}}$	Read/Write Input
$\overline{\text{X40}}$	Configuration Detection	$\overline{\text{OE}}$	Output Enable
V_{CC}	Power (+ 5 V)	V_{SS}	Ground
NC	No Connection		

All power supply and ground pins must be connected for proper operation of the device.

PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	NC	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{\text{OE}}$	31	A8	43	$\overline{\text{CAS1}}$	55	DQ28	67	PD1
8	DQ6	20	DQ8	32	NC	44	$\overline{\text{RAS0}}$	56	DQ29	68	PD2
9	DQ7	21	DQ9	33	NC	45	$\overline{\text{RAS1}}$	57	DQ30	69	PD3
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD4
11	PD5	23	DQ11	35	DQ17	47	$\overline{\text{W}}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	$\overline{\text{X40}}$	60	DQ32	72	V_{SS}

512K x 40 BLOCK DIAGRAM


DQ0 – DQ3
DQ4 – DQ7
DQ8 – DQ11
DQ12 – DQ15
DQ16 – DQ19
DQ20 – DQ23
DQ24 – DQ27
DQ28 – DQ31
DQ32 – DQ35
DQ36 – DQ39
I/O1
I/O2
I/O3
I/O4
CAS
RAS
OE
W
A0 – A8
CAS0
RAS0
CAS1
RAS1
W
A0 – A8
OE
VCC
VSS
0.22 µF (MIN)
U0 – U19
U0 – U19

PRESENCE DETECT PIN OUT			
Pin Name	**60 ns**	**70 ns**	**80 ns**
PD1	NC	NC	NC
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}
PD5	NC	NC	NC
$\overline{X40}$	V_{SS}	V_{SS}	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	6.9	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	MCM40512-60, t_{RC} = 110 ns MCM40512-70, t_{RC} = 130 ns MCM40512-80, t_{RC} = 150 ns	I_{CC1}	— — —	920 820 720	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	40	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles	MCM40512-60, t_{RC} = 110 ns MCM40512-70, t_{RC} = 130 ns MCM40512-80, t_{RC} = 150 ns	I_{CC3}	— — —	920 820 720	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle	MCM40512-60, t_{PC} = 40 ns MCM40512-70, t_{PC} = 40 ns MCM40512-80, t_{PC} = 45 ns	I_{CC4}	— — —	620 620 520	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	MCM40512 MCM40L512	I_{CC5}	— —	20 4	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	MCM40512-60, t_{RC} = 110 ns MCM40512-70, t_{RC} = 130 ns MCM40512-80, t_{RC} = 150 ns	I_{CC6}	— — —	920 820 720	mA	1
V_{CC} Power Supply Current Battery Backup Mode (t_{RC} = 125 µs; $\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$, DQ, A0 – A8 = V_{CC} – 0.2 V or 0.2 V) t_{RAS} = 1 µs	MCM40L512 only	I_{CC7}	—	6.0	mA	3
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)		$I_{lkg(I)}$	– 200	200	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)		$I_{lkg(O)}$	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)		V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.
3. t_{RAS} (max) = 1 µs is applied to refresh of battery back-up. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit
Input Capacitance (A0 – A8)	C_{I1}	—	110	pF
Input Capacitance ($\overline{\text{W}}$, $\overline{\text{OE}}$)	C_{I2}	—	150	pF
Input Capacitance ($\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{CAS0}}$, $\overline{\text{CAS1}}$)	C_{I3}	—	80	pF
I/O Capacitance (DQ0 – DQ39)	C_{DQ1}	—	24	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\ \Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C and – 40 to + 85°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

	Symbol		MCM40512-60 MCM40L512-60		MCM40512-70 MCM40L512-70		MCM40512-80 MCM40L512-80			
Parameter	Std	Alt	Min	Max	Min	Max	Min	Max	Unit	Notes
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RMW}	165	—	185	—	205	—	ns	6
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	40	—	45	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRMW}	95	—	95	—	100	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	7, 8
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	7, 10
Access Time from $\overline{\text{CAS}}$ Precharge	t_{CEHQV}	t_{CPA}	—	35	—	35	—	40	ns	7
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge (Page Mode Cycle Only)	t_{CELREH}	t_{RHCP}	35	—	35	—	40	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	12

NOTES: (continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. To avoid bus contention and potential damage to the module, $\overline{\text{RAS0}}$ and $\overline{\text{RAS1}}$ may not be active low simultaneously.
6. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C and – 40 to + 85°C) is ensured.
7. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
11. t_{OFF} (max) and/or t_{GZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM40512-60 MCM40L512-60		MCM40512-70 MCM40L512-70		MCM40512-80 MCM40L512-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	13
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELAX}	t_{AR}	50	—	55	—	60	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	14
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	14
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELWH}	t_{WCR}	45	—	55	—	60	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	15
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{RELDX}	t_{DHR}	50	—	55	—	60	—	ns	
Refresh Period MCM40512 MCM40L512	t_{RVRV}	t_{RFSH}	— —	8 64	— —	8 64	— —	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	16
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	50	—	ns	16
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	90	—	100	—	110	—	ns	16
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	60	—	65	—	70	—	ns	16
$\overline{\text{CAS}}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	65	—	65	—	70	—	ns	16

NOTES:

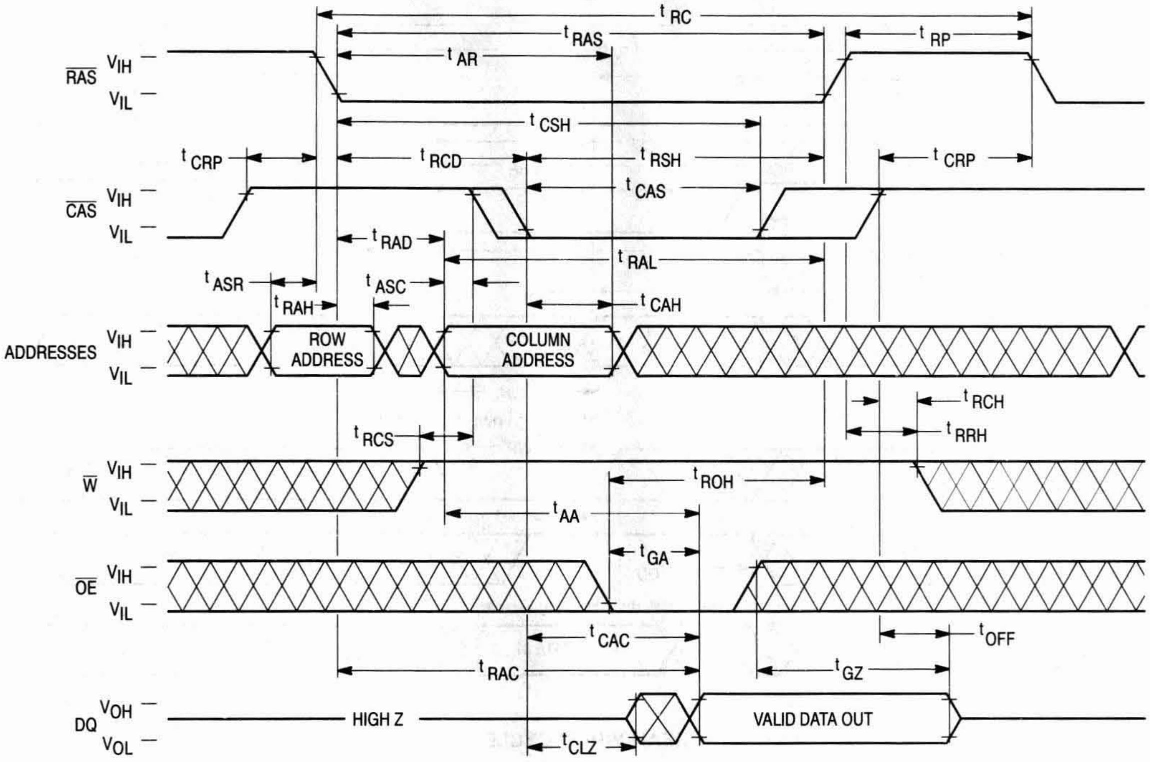
(continued)

13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in delayed write or read-write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ AND WRITE CYCLES (Continued)

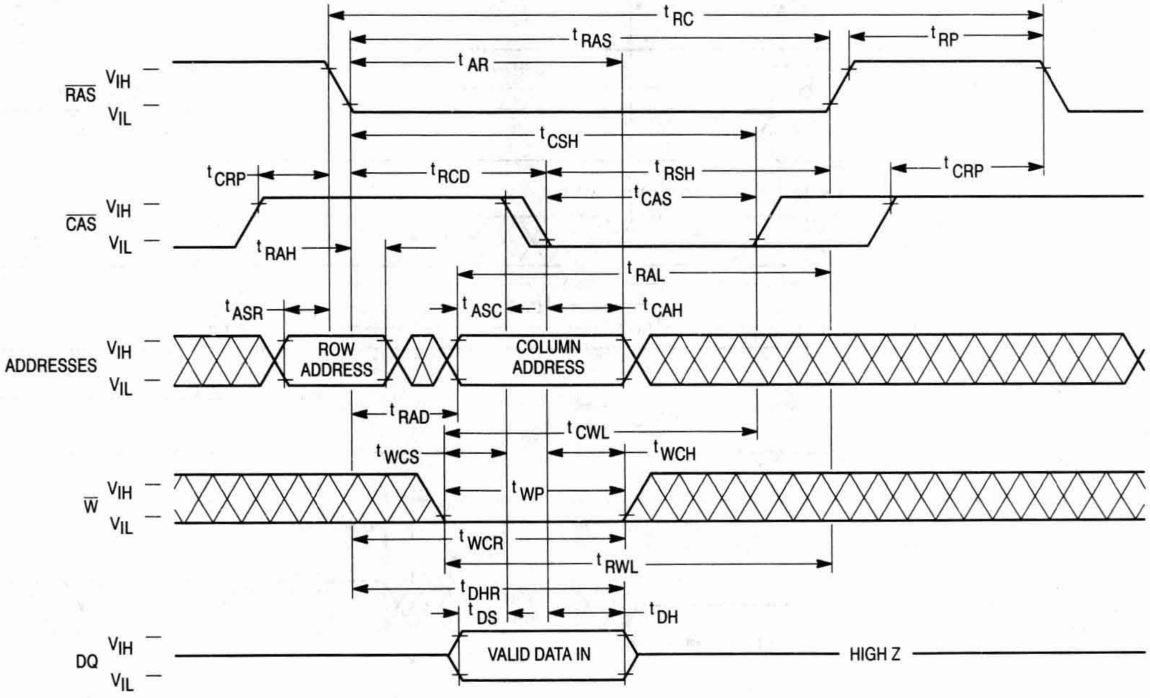
Parameter	Symbol		MCM40512-60 MCM40L512-60		MCM40512-70 MCM40L512-70		MCM40512-80 MCM40L512-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{OE}}$	t_{GLREH}	t_{ROH}	10	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	20	—	20	ns	
$\overline{\text{OE}}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	20	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{\text{OE}}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	20	ns	11
$\overline{\text{OE}}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	20	—	ns	

READ CYCLE



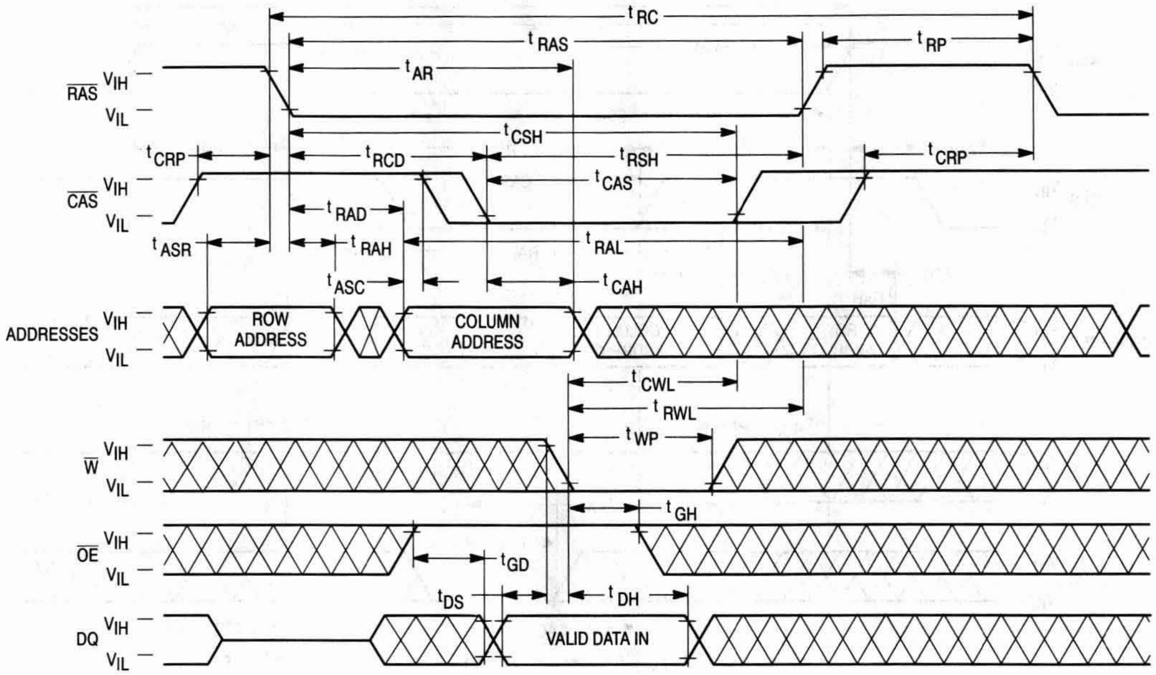
t RC
t RAS
t RP
t AR
RAS
VIH
VIL
t CSH
t CRP
t RCD
t RSH
t CRP
CAS
VIH
VIL
t CAS
t RAD
t RAL
t ASR
t ASC
t RAH
t CAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
t RCH
t RRH
t RCS
W
VIH
VIL
t ROH
t AA
t GA
OE
VIH
VIL
t CAC
t OFF
t RAC
t GZ
DQ
VOH
VOL
HIGH Z
VALID DATA OUT
t CLZ

EARLY WRITE CYCLE



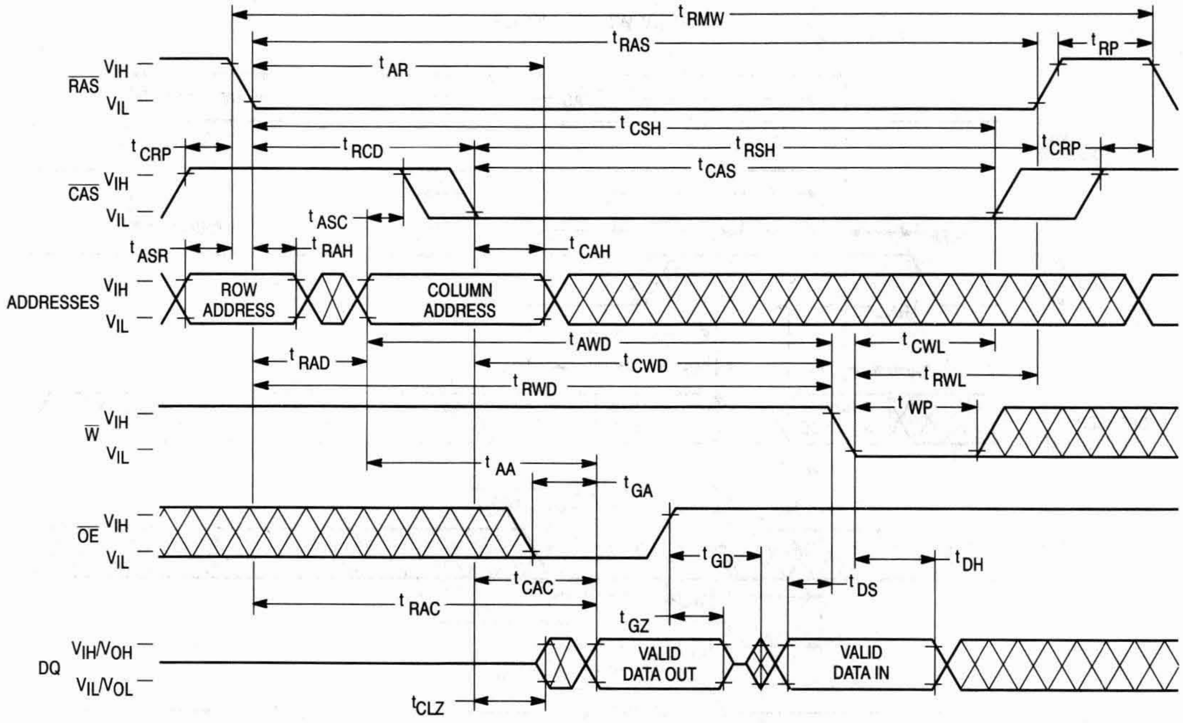
t RC
t RAS
t RP
t AR
RAS
VIH
VIL
t CSH
t CRP
t RCD
t RSH
t CRP
t CAS
CAS
VIH
VIL
t RAH
t RAL
t ASR
t ASC
t CAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
t RAD
t CWL
t WCS
t WCH
W
VIH
VIL
t WP
t WCR
t RWL
t DHR
t DS
t DH
DQ
VIH
VIL
VALID DATA IN
HIGH Z

$\overline{\text{OE}}$ CONTROLLED LATE WRITE CYCLE



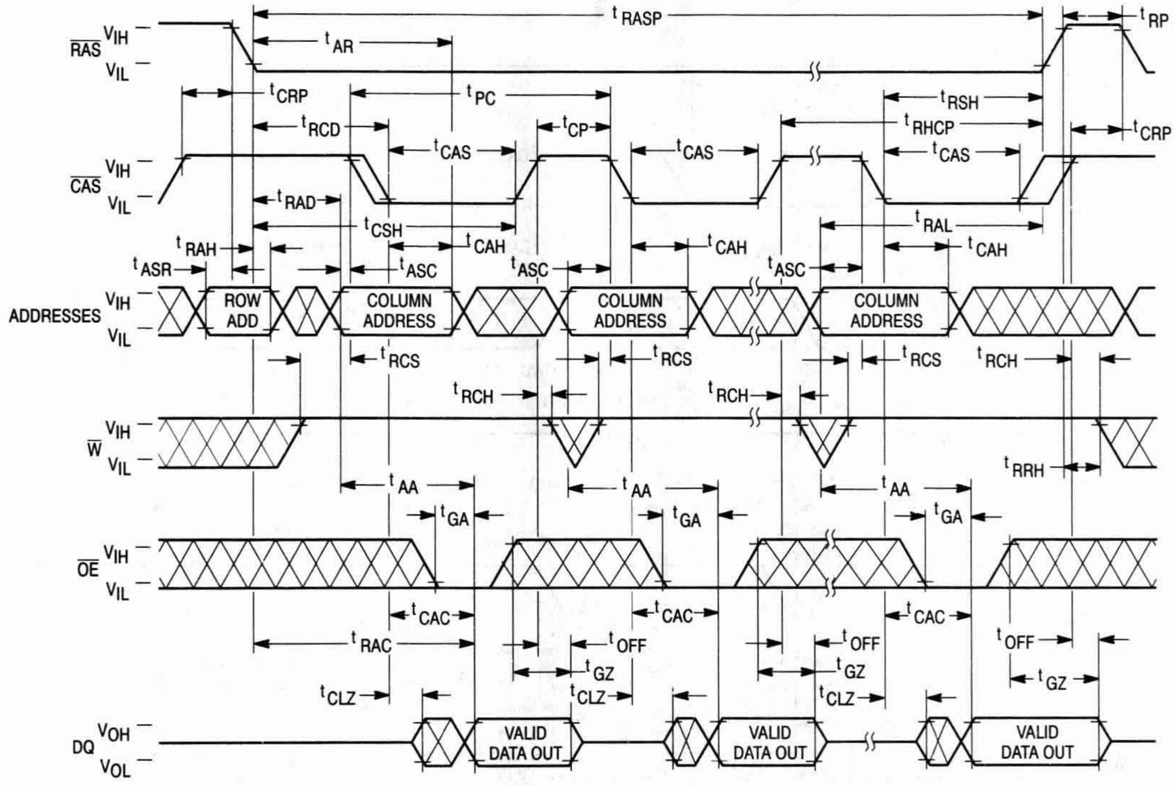
tRC
tRAS
tRP
tAR
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tRAD
tASR
tRAH
tRAL
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tCWL
tRWL
tWP
W
VIH
VIL
tGH
OE
VIH
VIL
tGD
tDS
tDH
DQ
VIH
VIL
VALID DATA IN

READ-WRITE CYCLE



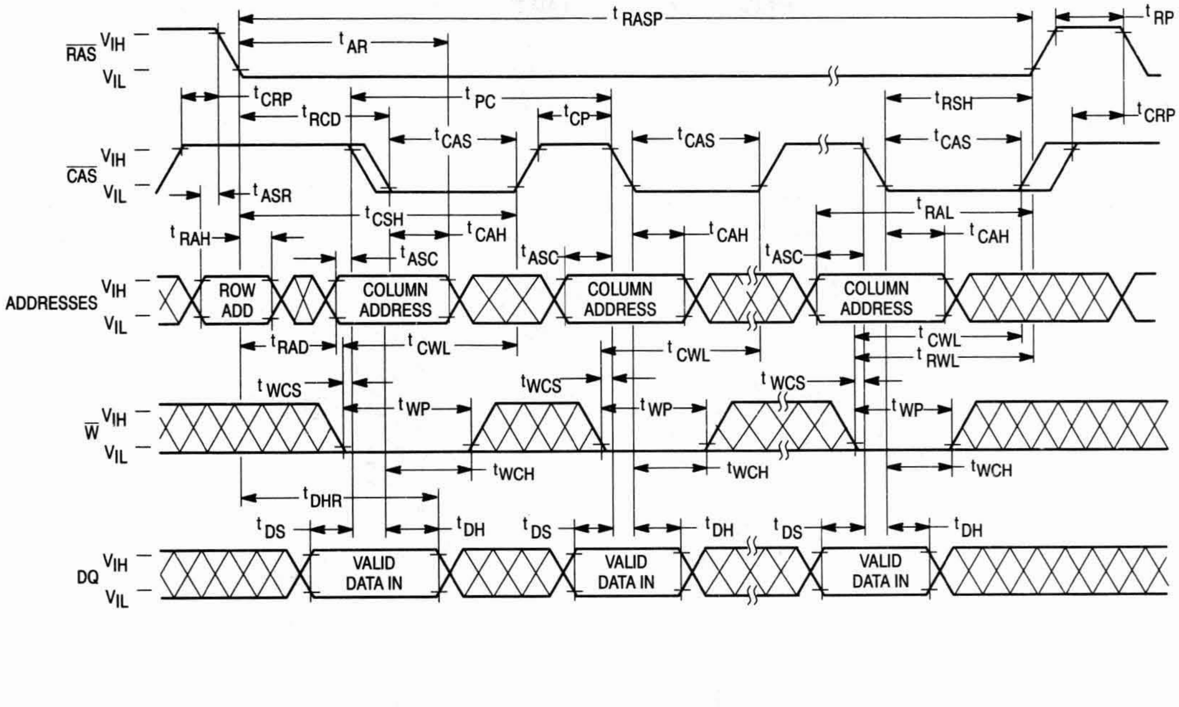
tRMW
tRAS
tRP
tAR
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tASC
tASR
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tAWD
tCWL
tRAD
tCWD
tRWL
tRWD
tWP
W
VIH
VIL
tAA
tGA
OE
VIH
VIL
tGD
tDH
tCAC
tDS
tRAC
tGZ
DQ
VIH/VOH
VIL/VOL
VALID DATA OUT
VALID DATA IN
tCLZ

FAST PAGE MODE READ CYCLE



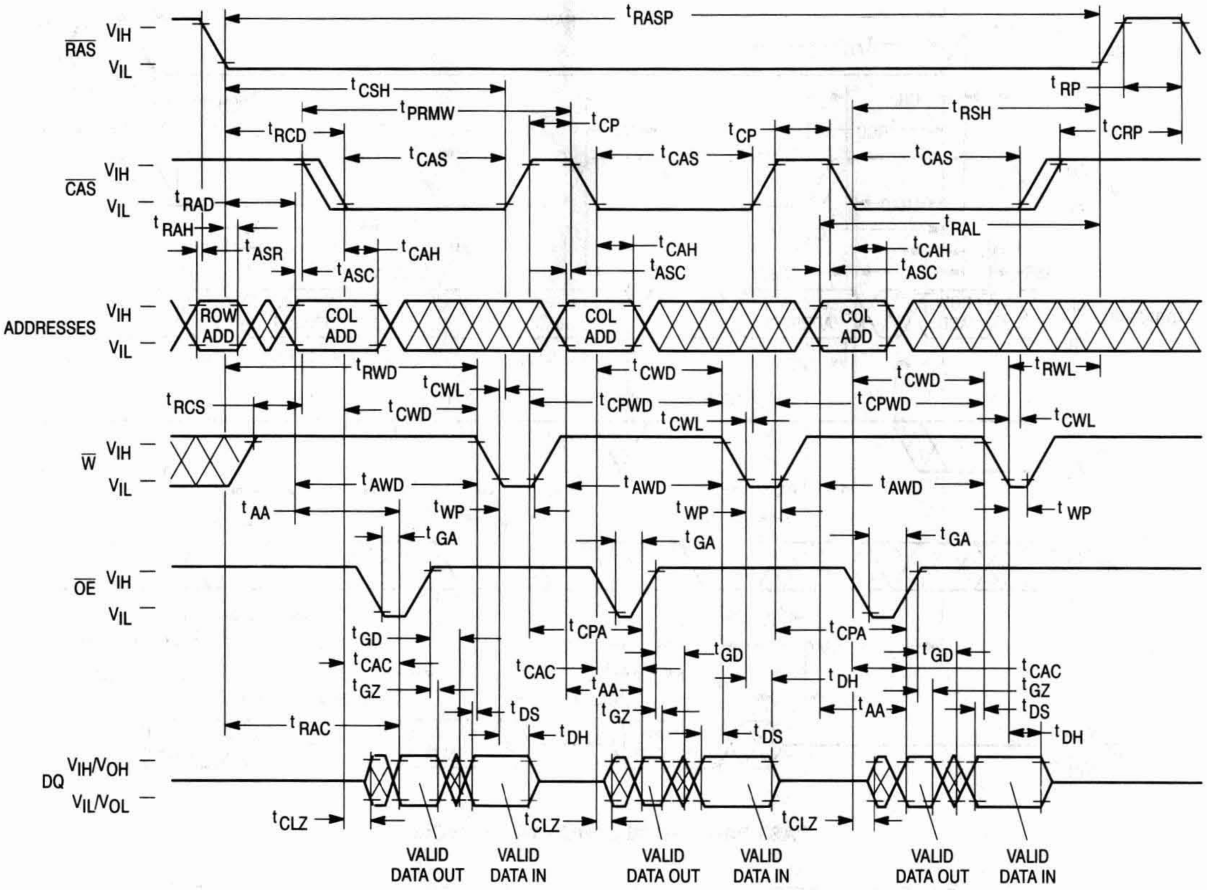
RAS
VIH
VIL
CAS
ADDRESSES
W
OE
DQ
VOH
VOL
tRASP
tRP
tAR
tCRP
tPC
tRSH
tRCD
tCP
tRHCP
tCAS
tRAD
tRAL
tCSH
tRAH
tCAH
tASR
tASC
ROW ADD
COLUMN ADDRESS
tRCS
tRCH
tRRH
tAA
tGA
tCAC
tRAC
tOFF
tGZ
tCLZ
VALID DATA OUT

FAST PAGE MODE EARLY-WRITE CYCLE



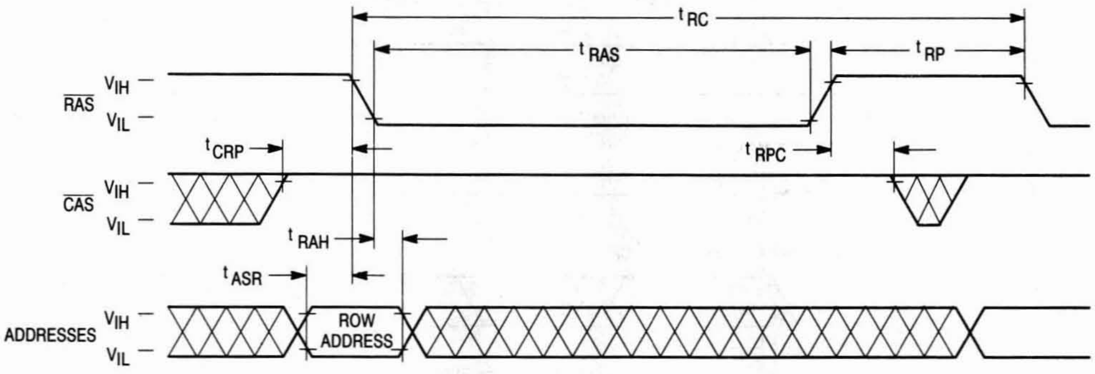
RAS
VIH
VIL
CAS
ADDRESSES
W
DQ
tRASP
tRP
tAR
tCRP
tPC
tRCD
tCP
tRSH
tCAS
tASR
tCSH
tRAL
tRAH
tCAH
tASC
ROW ADD
COLUMN ADDRESS
tRAD
tCWL
tRWL
tWCS
tWP
tWCH
tDHR
tDS
tDH
VALID DATA IN

FAST PAGE MODE READ-WRITE CYCLE


RAS
VIH
VIL
tRASP
tCSH
tPRMW
tRCD
tCP
tCAS
tRSH
tRP
tCRP
CAS
tRAD
tRAH
tASR
tCAH
tASC
tRAL
ADDRESSES
ROW ADD
COL ADD
tRWD
tCWL
tCWD
tRCS
tCPWD
tRWL
W
tAWD
tAA
tWP
tGA
OE
tGD
tCAC
tGZ
tCPA
tDH
tDS
tRAC
DQ
VIH/VOH
VIL/VOL
tCLZ
VALID DATA OUT
VALID DATA IN

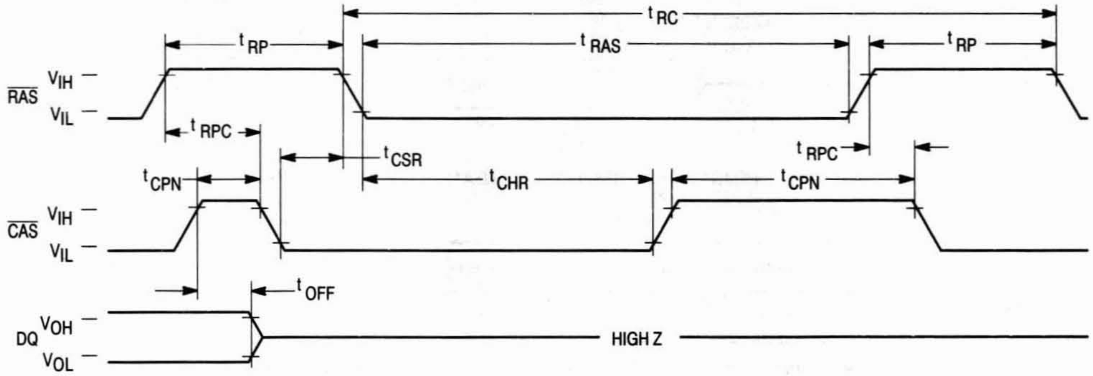
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

($\overline{\text{W}}$ and $\overline{\text{OE}}$ are Don't Care)

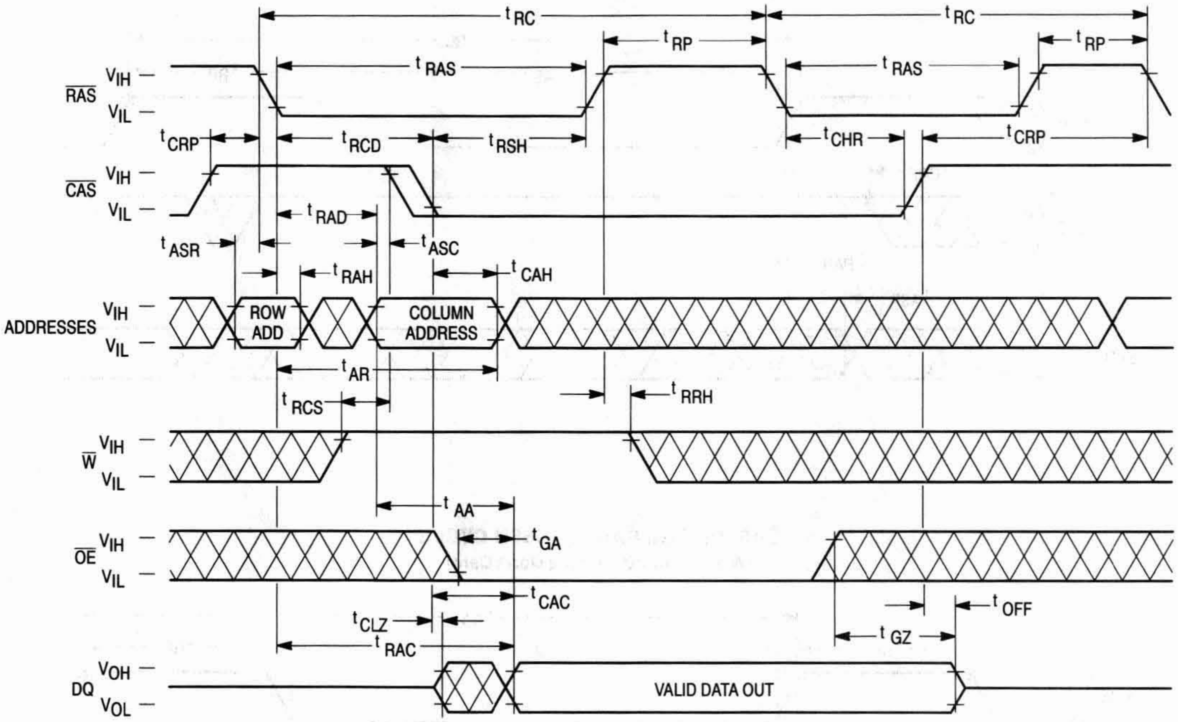

t_{RC}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{CRP}
t_{RPC}
$\overline{\text{CAS}}$
t_{RAH}
t_{ASR}
ADDRESSES
ROW ADDRESS

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{W}}$, $\overline{\text{OE}}$, and A0 – A8 are Don't Care)

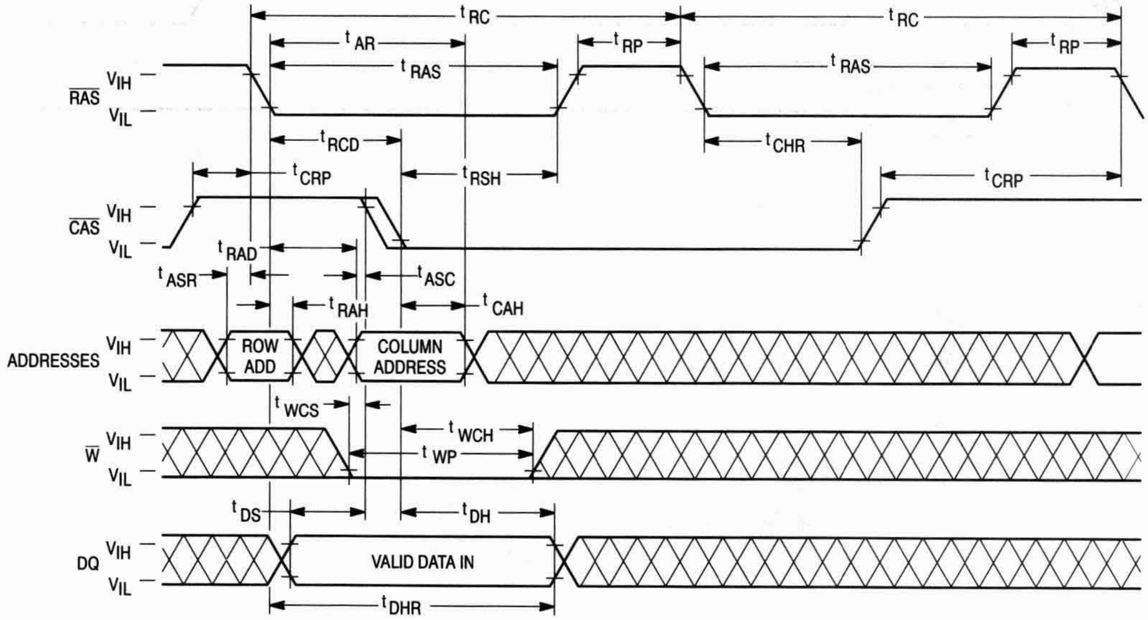

t_{RC}
t_{RP}
t_{RAS}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RPC}
t_{CSR}
t_{RPC}
t_{CPN}
t_{CHR}
t_{CPN}
$\overline{\text{CAS}}$
t_{OFF}
DQ
V_{OH}
V_{OL}
HIGH Z

HIDDEN REFRESH CYCLE (READ)



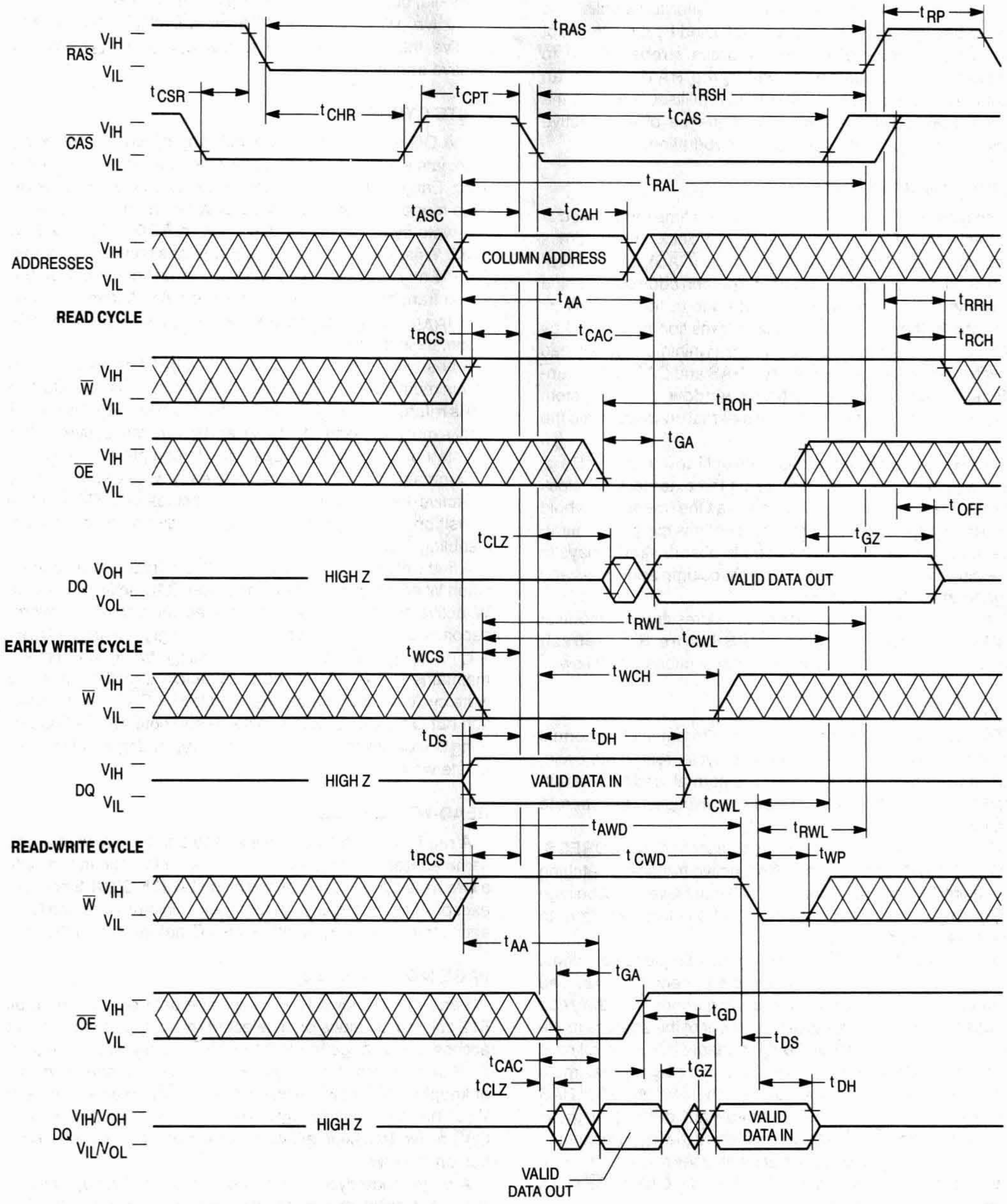
tRC
tRC
tRP
tRP
tRAS
tRAS
RAS
VIH
VIL
tCRP
tRCD
tRSH
tCHR
tCRP
CAS
VIH
VIL
tRAD
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
tAR
tRCS
tRRH
W
VIH
VIL
tAA
tGA
OE
VIH
VIL
tCAC
tCLZ
tOFF
tRAC
tGZ
DQ
VOH
VOL
VALID DATA OUT

HIDDEN REFRESH CYCLE (EARLY WRITE)



tRC
tRC
tAR
tRP
tRP
tRAS
tRAS
RAS
VIH
VIL
tRCD
tCHR
tCRP
tRSH
tCRP
CAS
VIH
VIL
tRAD
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
tWCS
tWCH
tWP
W
VIH
VIL
tDS
tDH
DQ
VIH
VIL
VALID DATA IN
tDHR

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE


$\overline{RAS}$
V_{IH}
V_{IL}
t_{RAS}
t_{RP}
t_{CSR}
t_{CHR}
t_{CPT}
t_{RSH}
$\overline{CAS}$
t_{CAS}
t_{RAL}
t_{ASC}
t_{CAH}
ADDRESSES
COLUMN ADDRESS
READ CYCLE
t_{AA}
t_{RRH}
t_{RCS}
t_{CAC}
t_{RCH}
$\overline{W}$
t_{ROH}
t_{GA}
$\overline{OE}$
t_{OFF}
t_{CLZ}
t_{GZ}
DQ
V_{OH}
V_{OL}
HIGH Z
VALID DATA OUT
t_{RWL}
EARLY WRITE CYCLE
t_{CWL}
t_{WCS}
t_{WCH}
t_{DS}
t_{DH}
VALID DATA IN
t_{AWD}
READ-WRITE CYCLE
t_{CWD}
t_{WP}
t_{GD}
V_{IH}/V_{OH}
V_{IL}/V_{OL}
VALID DATA IN
VALID DATA OUT

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 bit locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gate feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are two other variations in addressing the module: **$\overline{RAS}$-only refresh cycle** and **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: normal random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{CAS}$ and output enable ($\overline{OE}$) control read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum and $\overline{OE}$ must be active t_{RAC}-t_{GA} (both minimum) after $\overline{RAS}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{OE}$ active transition does not occur in time, read access time is determined by either the $\overline{CAS}$ or $\overline{OE}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CAS}$ and $\overline{OE}$ clocks are active. When either the $\overline{CAS}$ or $\overline{OE}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The DRAM may be written with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data In (D) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data out buffers disabled, effectively disabling $\overline{OE}$.

A late write cycle (referred to as $\overline{OE}$ controlled write) occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + t_T$) $\leq t_{RAS}$, if timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition but Q may be indeterminate — see note 15 of AC Operating Conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} minimum after the $\overline{CAS}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 512 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically refreshed (recharged) to maintain the correct bit state. Bits in the MCM40512 require refresh every 8 milliseconds while refresh time for the MCM40L512 is 64 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM40512 and 124.8 microseconds for the MCM40L512. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM40512 and 64 milliseconds on the MCM40L512.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **RAS-only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1).

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **eight CAS before RAS** initialization cycles. Test procedure:

1. Write “0”s into all memory cells with normal write mode.
2. Select a column address, read “0” out and write “1” into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 512 times.
3. Read the “1”s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read “1” out and write “0” into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 512 times.
5. Read “0”s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

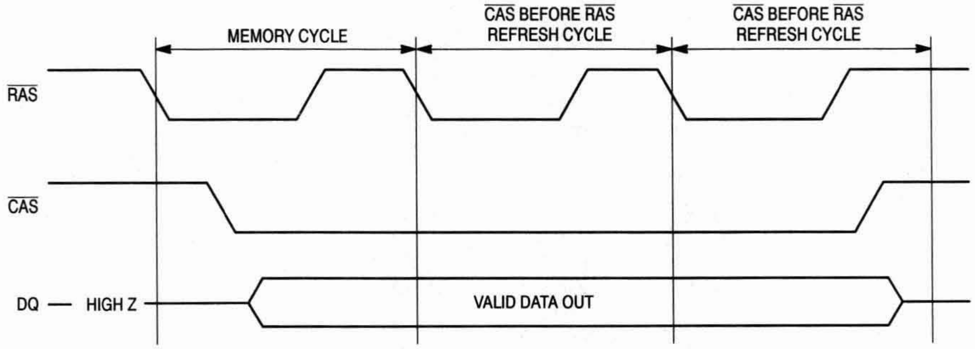


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 40512 or 40L512 X XX

Motorola Memory Prefix — MCM

Part Number — 40512 or 40L512

Package (AS = SIMM, ASG = Gold Pad SIMM) — X

Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers —	MCM40512AS60	MCM40512ASG60
	MCM40512AS70	MCM40512ASG70
	MCM40512AS80	MCM40L12ASG80
	MCM40L512AS60	MCM40L512ASG60
	MCM40L512AS70	MCM40L512ASG70
	MCM40L512AS80	MCM40L512ASG80

NOTE: For mechanical data, please see Chapter 10.

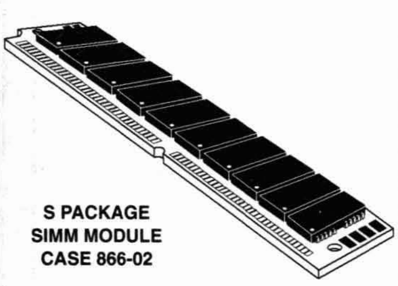
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM40100
MCM40L100

1M x 40 Bit Dynamic Random Access Memory Module
for Error Correction Applications

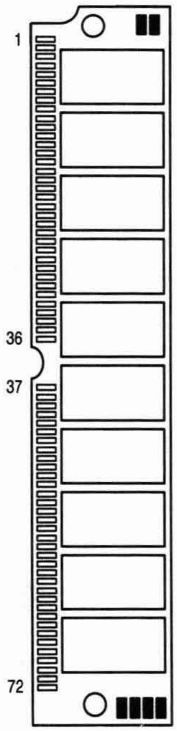
The MCM40100 and MCM40L100 are 40M dynamic random access memory (DRAM) modules organized as 1,048,576 x 40 bits. The module is a 72-lead single-in-line memory module (SIMM) consisting of ten MCM54400AN DRAMs housed in 20/26 J-lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM54400AN is a CMOS high-speed dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM40100 = 16 ms (Max)
  MCM40L100 = 128 ms (Max)
- Consists of Ten 1M x 4 DRAMs, and Ten 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM40100-60 = 60 ns (Max)
  MCM40100-70 = 70 ns (Max)
  MCM40100-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM40100-60 = 6.60 W (Max)
  MCM40100-70 = 5.50 W (Max)
  MCM40100-80 = 4.68 W (Max)
- Low Standby Power Dissipation: TTL Levels = 110 mW (Max)
  CMOS Levels = 55 mW (Max, MCM40100)
  = 11 mW (Max, MCM40L100)



S PACKAGE
SIMM MODULE
CASE 866-02

TOP VIEW



PIN NAMES

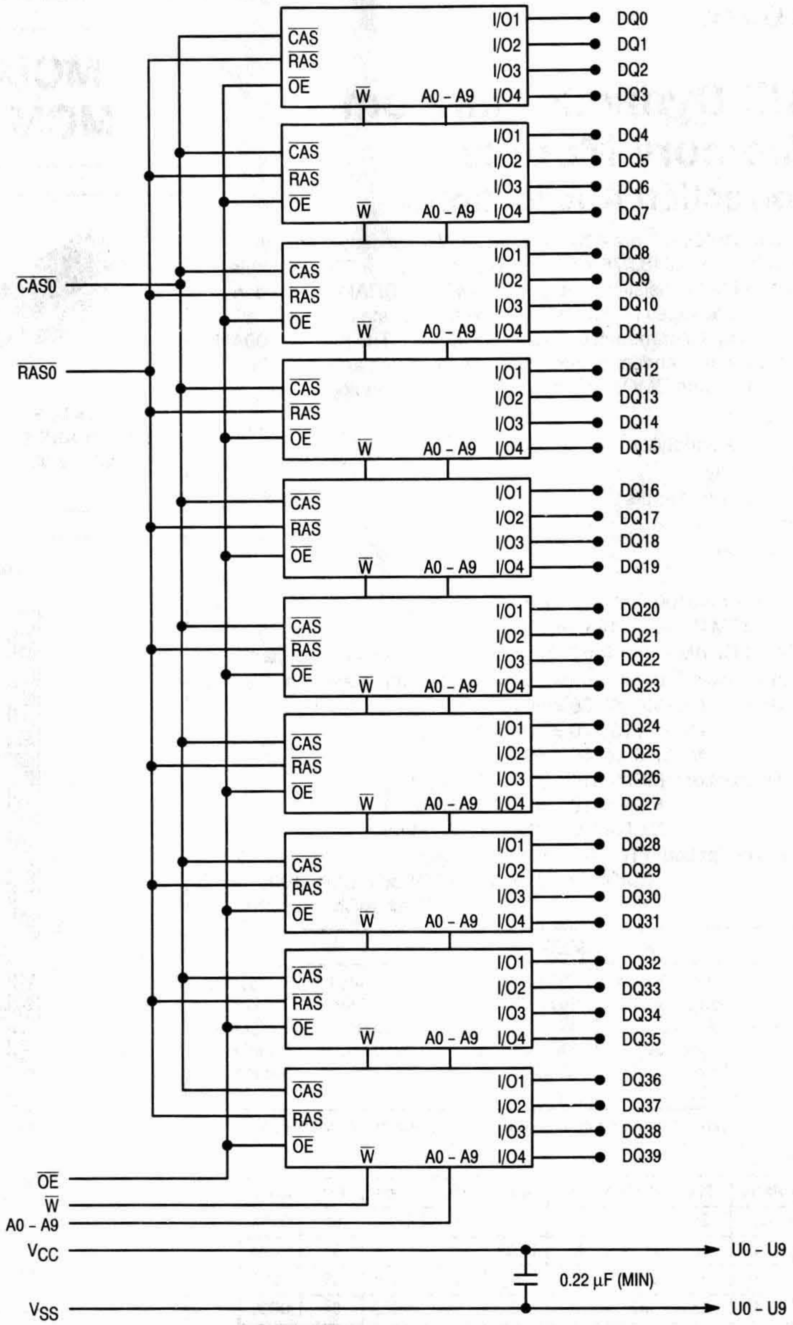
A0 – A9	Address Inputs	DQ0 – DQ39	Data Input/Output
$\overline{\text{CAS0}}$	Column Address Strobe	PD1 – PD5	Presence Detect
$\overline{\text{RAS0}}$	Row Address Strobe	$\overline{\text{W}}$	Read/Write Input
$\overline{\text{X40}}$	Configuration Detection	$\overline{\text{OE}}$	Output Enable
V_{CC}	Power (+ 5 V)	V_{SS}	Ground
NC	No Connection		

All power supply and ground pins must be connected for proper operation of the device.

PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	NC	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{\text{OE}}$	31	A8	43	NC	55	DQ28	67	PD1
8	DQ6	20	DQ8	32	A9	44	$\overline{\text{RAS0}}$	56	DQ29	68	PD2
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ30	69	PD3
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD4
11	PD5	23	DQ11	35	DQ17	47	$\overline{\text{W}}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	$\overline{\text{X40}}$	60	DQ32	72	V_{SS}

BLOCK DIAGRAM


$\overline{CAS}$
$\overline{RAS}$
$\overline{OE}$
$\overline{W}$
A0 - A9
I/O1
I/O2
I/O3
I/O4
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
DQ32
DQ33
DQ34
DQ35
DQ36
DQ37
DQ38
DQ39
$\overline{CAS0}$
$\overline{RAS0}$
$\overline{OE}$
$\overline{W}$
A0 - A9
V_{CC}
V_{SS}
U0 - U9
0.22 μF (MIN)
U0 - U9

PRESENCE DETECT PIN OUT			
Pin Name	**60 ns**	**70 ns**	**80 ns**
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}
PD5	NC	NC	NC
$\overline{X40}$	V_{SS}	V_{SS}	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	9.0	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	MCM40100-60, t_{RC} = 110 ns MCM40100-70, t_{RC} = 130 ns MCM40100-80, t_{RC} = 150 ns	I_{CC1}	— — —	1200 1000 850	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	20	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles	MCM40100-60, t_{RC} = 110 ns MCM40100-70, t_{RC} = 130 ns MCM40100-80, t_{RC} = 150 ns	I_{CC3}	— — —	1200 1000 850	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle	MCM40100-60, t_{PC} = 45 ns MCM40100-70, t_{PC} = 45 ns MCM40100-80, t_{PC} = 50 ns	I_{CC4}	— — —	700 700 600	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	MCM40100 MCM40L100	I_{CC5}	— —	10 2	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	MCM40100-60, t_{RC} = 110 ns MCM40100-70, t_{RC} = 130 ns MCM40100-80, t_{RC} = 150 ns	I_{CC6}	— —	1200 1000 850	mA	1
V_{CC} Power Supply Current Battery Backup Mode (t_{RC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$, DQ, A0 – A9 = V_{CC} – 0.2 V or 0.2 V)	MCM40L100 only	I_{CC7}	—	3.0	mA	1, 3
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)		$I_{lkg(I)}$	– 100	+ 100	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)		$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)		V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery backup. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit
Input Capacitance (A0 – A9)	C_{I1}	—	60	pF
Input Capacitance ($\overline{\text{W}}$, $\overline{\text{OE}}$, $\overline{\text{RAS0}}$, $\overline{\text{CAS0}}$)	C_{I2}	—	80	pF
I/O Capacitance (DQ0 – DQ39)	C_{DQ1}	—	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM40100-60 MCM40L100-60		MCM40100-70 MCM40L100-70		MCM40100-80 MCM40L100-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	165	—	185	—	205	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	50	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	100	—	100	—	105	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	40	—	40	—	45	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	200 k	70	200 k	80	200 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	20	10 k	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	11

NOTES: (continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) and/or t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}

READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM40100-60 MCM40L100-60		MCM40100-70 MCM40L100-70		MCM40100-80 MCM40L100-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	14
Refresh Period MCM40100 MCM40L100	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	50	—	ns	15
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	90	—	100	—	110	—	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	60	—	65	—	70	—	ns	15
$\overline{\text{CAS}}$ Precharge to Write Delay Time (Page Mode)	t_{CEHWL}	t_{CPWD}	70	—	70	—	75	—	ns	15
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Time	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{OE}}$	t_{GLREH}	t_{ROH}	10	—	10	—	10	—	ns	

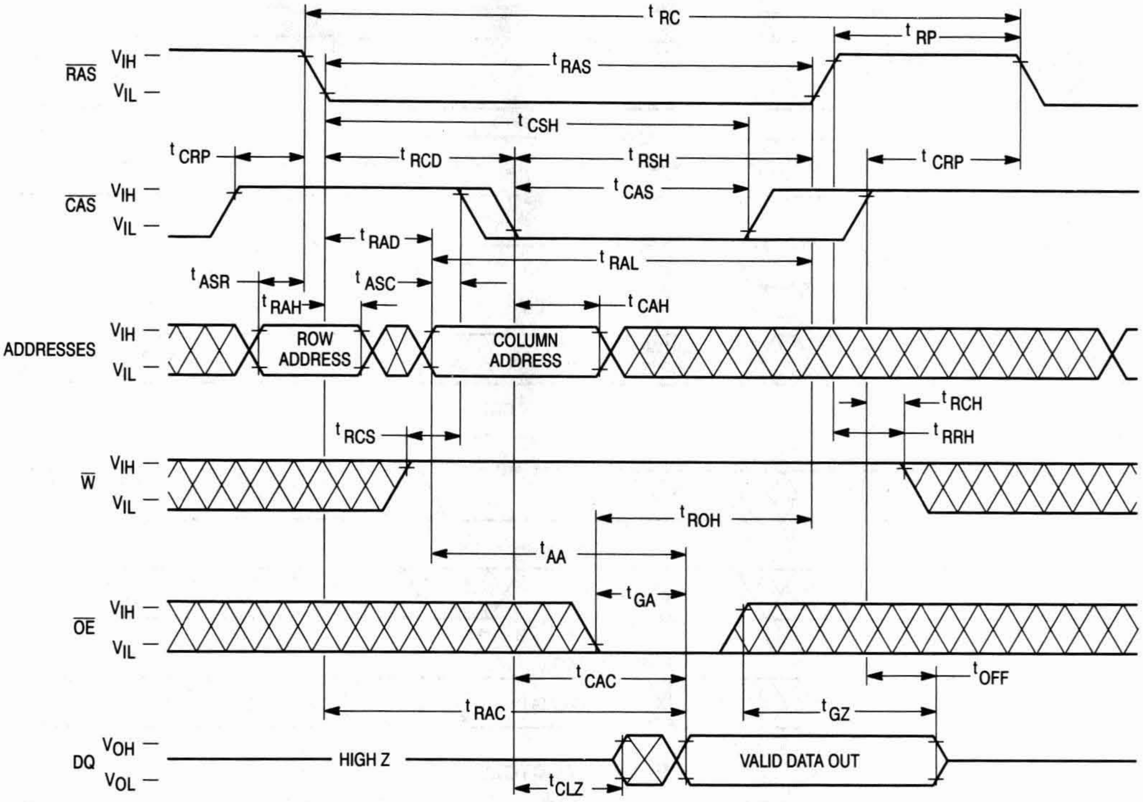
NOTES: (continued)

12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in late write or read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM40100-60 MCM40L100-60		MCM40100-70 MCM40L100-70		MCM40100-80 MCM40L100-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{OE}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	20	—	20	ns	
$\overline{OE}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	20	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{OE}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	20	ns	10
$\overline{OE}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	20	—	ns	

READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tRAD
tRAL
tASR
tASC
tRAH
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRCH
tRRH
tRCS
W
VIH
VIL
tROH
tAA
tGA
OE
VIH
VIL
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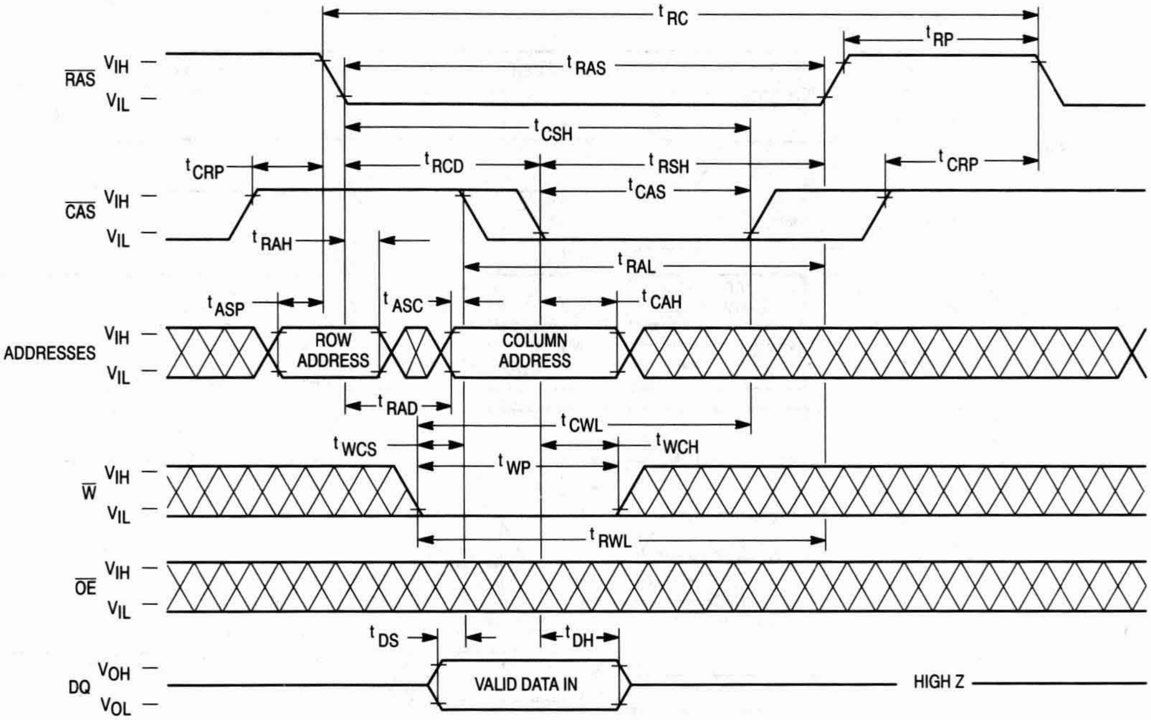
tOFF
tRAC
tGZ
DQ
VOH
VOL
HIGH Z
VALID DATA OUT
tCLZ

EARLY WRITE CYCLE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VIH
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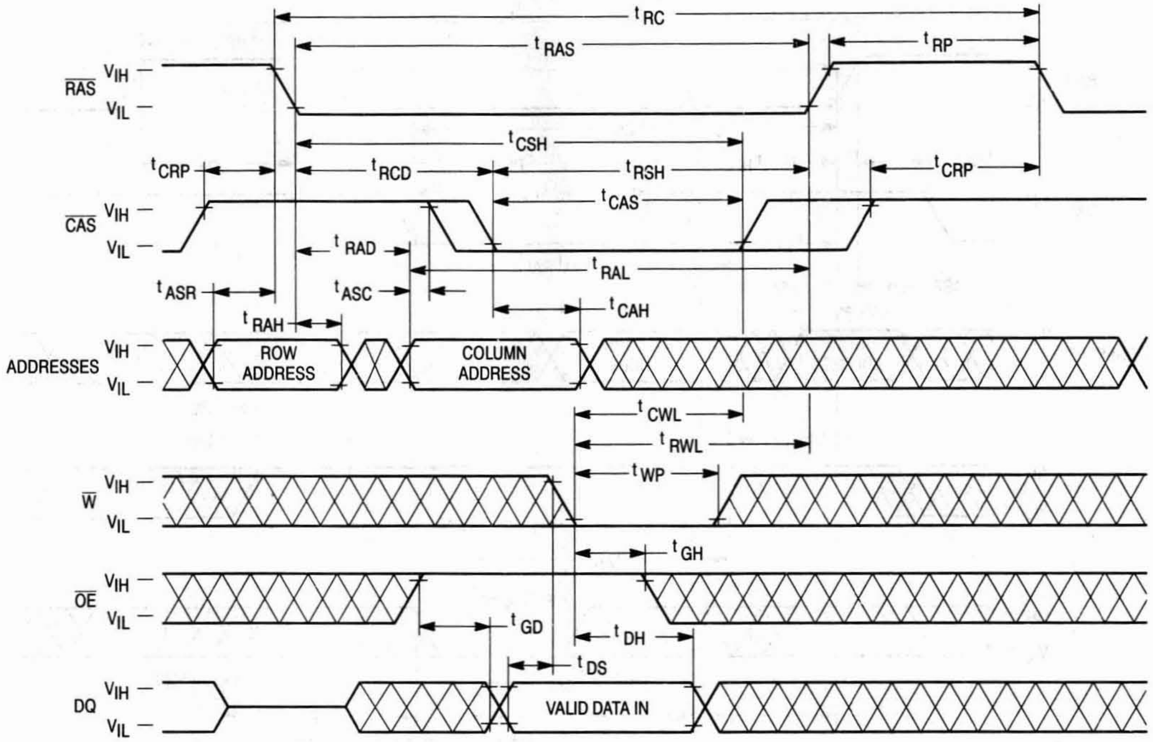
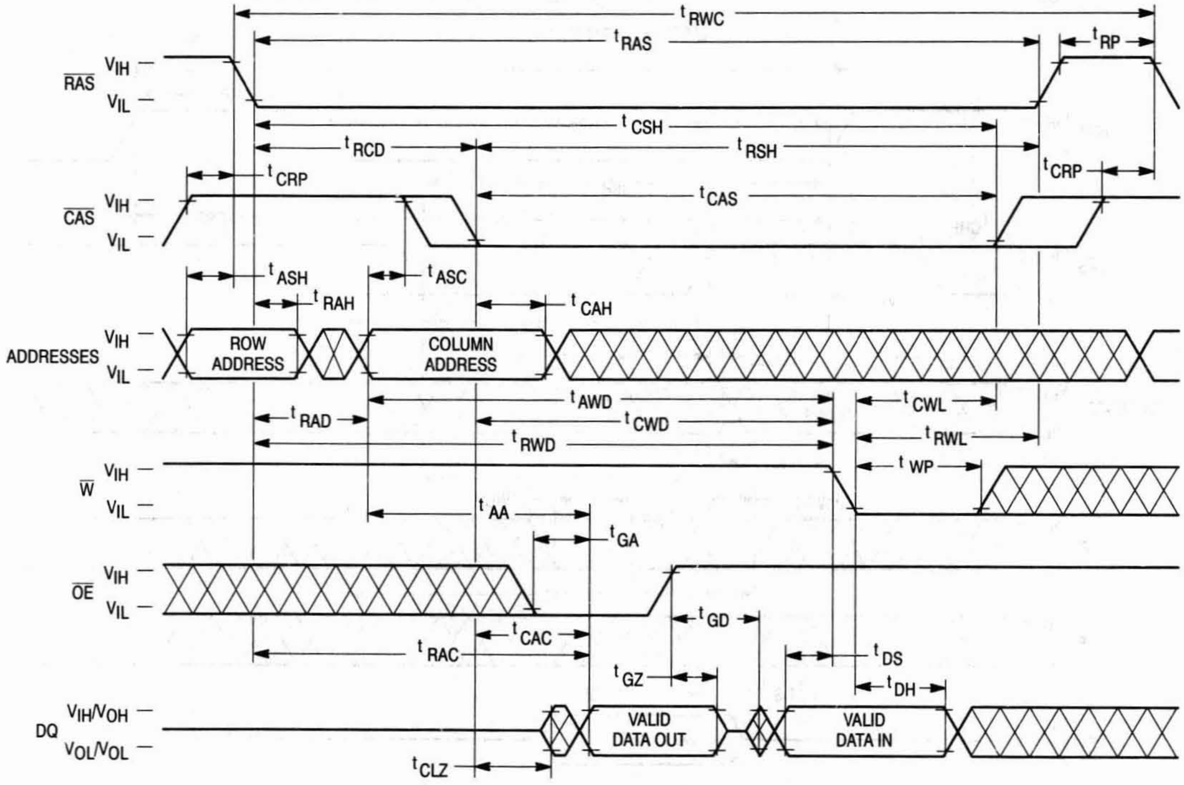
tRAH
tRAL
tASP
tASC
tCAH
ADDRESSES
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRAD
tCWL
tWCS
tWCH
tWP
W
VIH
VIL
tRWL
OE
VIH
VIL
tDS
tDH
DQ
VOH
VOL
VALID DATA IN
HIGH Z

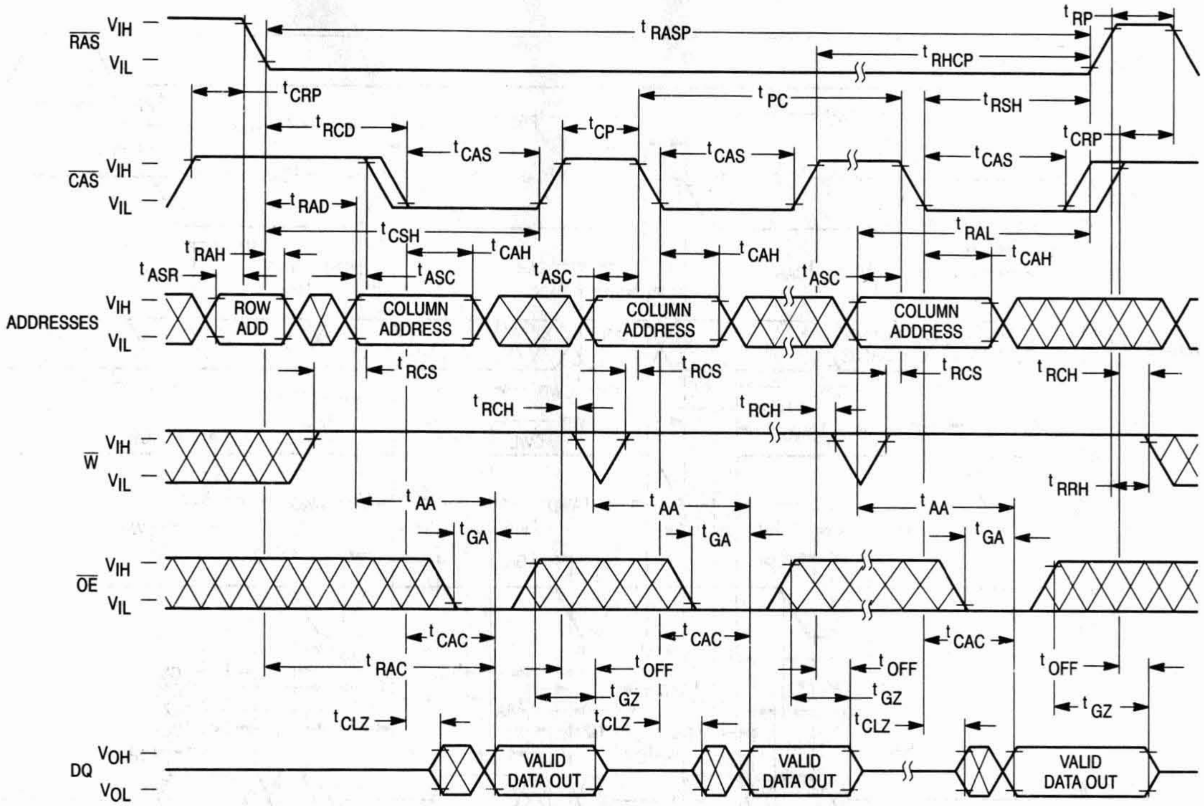
$\overline{\text{OE}}$ CONTROLLED WRITE CYCLE


t_{RC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{RAD}
t_{RAL}
t_{ASR}
t_{ASC}
t_{CAH}
t_{RAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{CWL}
t_{RWL}
t_{WP}
$\overline{W}$
V_{IH}
V_{IL}
t_{GH}
$\overline{OE}$
V_{IH}
V_{IL}
t_{GD}
t_{DH}
t_{DS}
DQ
V_{IH}
V_{IL}
VALID DATA IN

READ-WRITE CYCLE

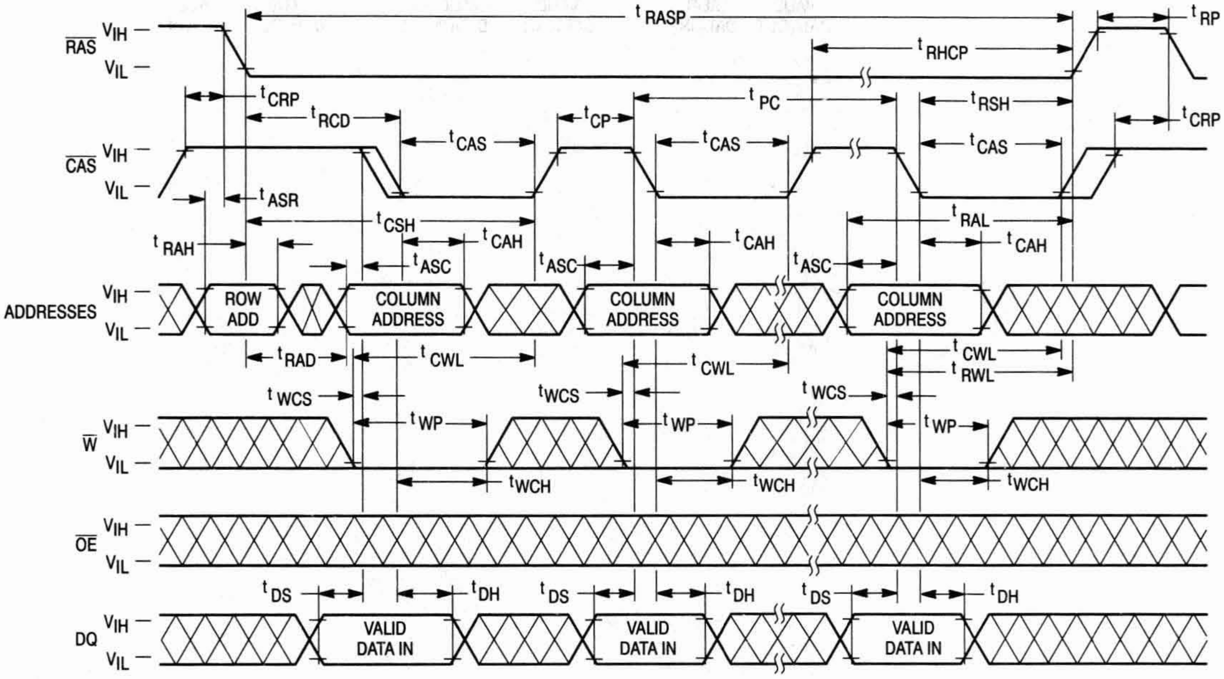

t_{RWC}
t_{RAS}
t_{RP}
$\overline{RAS}$
V_{IH}
V_{IL}
t_{CSH}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CRP}
t_{CAS}
$\overline{CAS}$
V_{IH}
V_{IL}
t_{ASH}
t_{ASC}
t_{RAH}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
ROW ADDRESS
COLUMN ADDRESS
t_{AWD}
t_{CWL}
t_{RAD}
t_{CWD}
t_{RWL}
t_{RWD}
t_{WP}
$\overline{W}$
V_{IH}
V_{IL}
t_{AA}
t_{GA}
$\overline{OE}$
V_{IH}
V_{IL}
t_{GD}
t_{CAC}
t_{RAC}
t_{DS}
t_{GZ}
t_{DH}
DQ
V_{IH}/V_{OH}
V_{OL}/V_{OL}
VALID DATA OUT
VALID DATA IN
t_{CLZ}

FAST PAGE MODE READ CYCLE



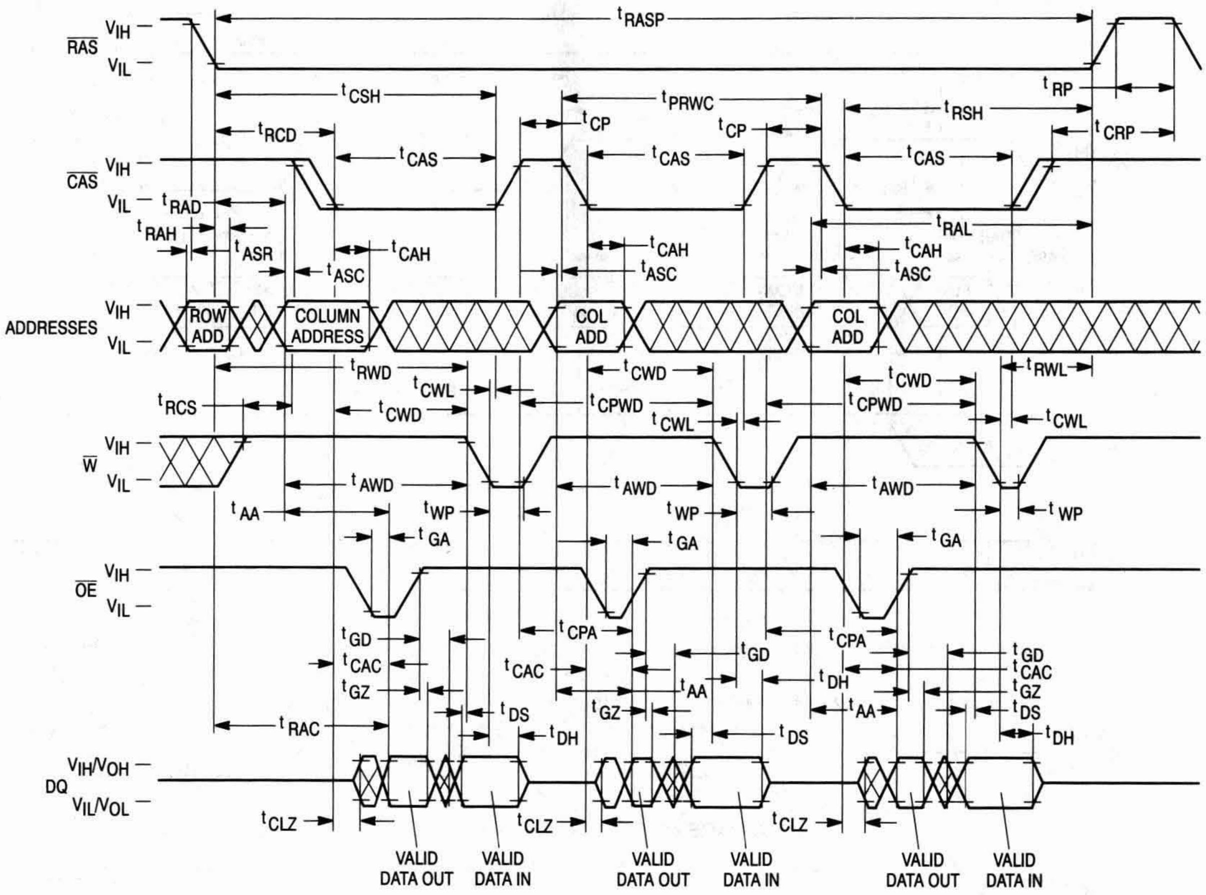
RAS
VIH
VIL
CAS
VIH
VIL
ADDRESSES
VIH
VIL
W
VIH
VIL
OE
VIH
VIL
DQ
VOH
VOL
tRASP
tRP
tRHCP
tCRP
tPC
tRSH
tRCD
tCP
tCAS
tCAS
tCAS
tCRP
tRAD
tCSH
tRAL
tRAH
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
ROW ADD
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRCS
tRCS
tRCS
tRCH
tRCH
tRCH
tRCH
tRRH
tAA
tAA
tAA
tGA
tGA
tGA
tCAC
tCAC
tCAC
tRAC
tOFF
tOFF
tOFF
tGZ
tGZ
tGZ
tCLZ
tCLZ
tCLZ
VALID DATA OUT
VALID DATA OUT
VALID DATA OUT

FAST PAGE MODE EARLY WRITE CYCLE



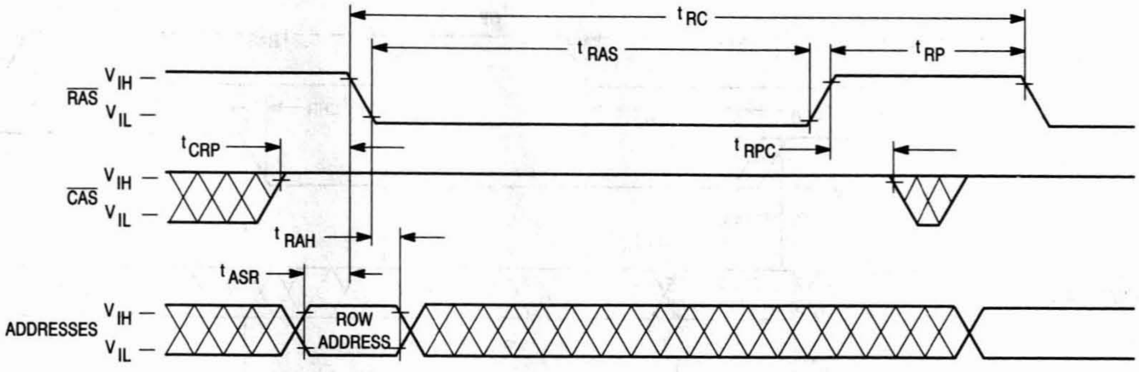
RAS
VIH
VIL
CAS
VIH
VIL
ADDRESSES
VIH
VIL
W
VIH
VIL
OE
VIH
VIL
DQ
VIH
VIL
tRASP
tRP
tRHCP
tCRP
tRCD
tCP
tPC
tRSH
tCRP
tCAS
tCAS
tCAS
tASR
tCSH
tRAL
tRAH
tCAH
tCAH
tCAH
tASC
tASC
tASC
ROW ADD
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
tRAD
tCWL
tCWL
tCWL
tRWL
tWCS
tWCS
tWCS
tWP
tWP
tWP
tWCH
tWCH
tWCH
tDS
tDH
tDS
tDH
tDS
tDH
VALID DATA IN
VALID DATA IN
VALID DATA IN

FAST PAGE MODE READ-WRITE CYCLE


RAS
VIH
VIL
tRASP
tRP
tCSH
tPRWC
tRSH
tCRP
tRCD
tCP
tCP
CAS
VIH
VIL
tCAS
tCAS
tCAS
tRAD
tRAH
tASR
tRAL
tCAH
tCAH
tCAH
tASC
tASC
tASC
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
COL ADD
COL ADD
tRWD
tCWD
tCWD
tRWL
tCWL
tCPWD
tCPWD
tRCS
tCWD
tCWL
tCWL
W
VIH
VIL
tAWD
tAWD
tAWD
tAA
tWP
tWP
tWP
tGA
tGA
tGA
OE
VIH
VIL
tGD
tCPA
tCPA
tCAC
tCAC
tGD
tGD
tGZ
tAA
tDH
tCAC
tGZ
tAA
tGZ
tDS
tDS
tRAC
tDH
tDS
tDH
DQ
VIH/VOH
VIL/VOL
tCLZ
tCLZ
tCLZ
VALID DATA OUT
VALID DATA IN
VALID DATA OUT
VALID DATA IN
VALID DATA OUT
VALID DATA IN

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

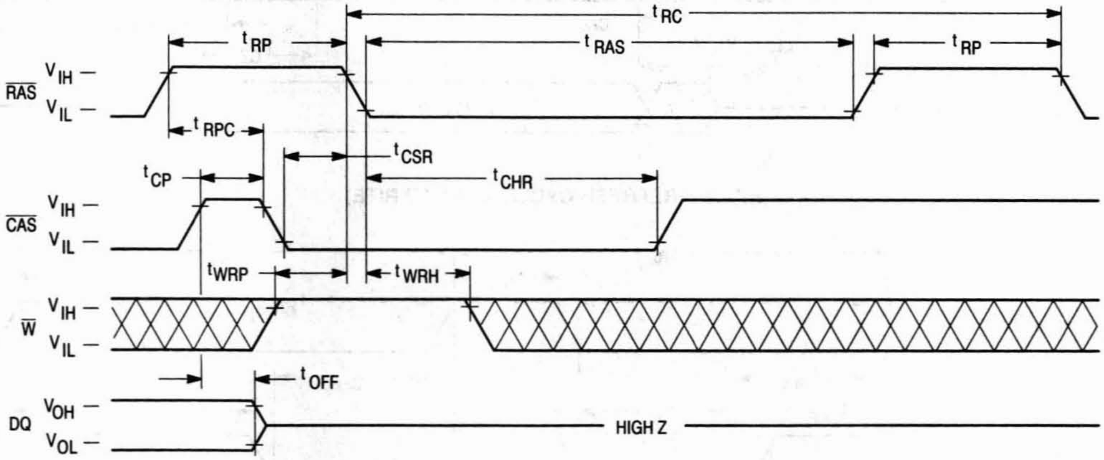
($\overline{\text{W}}$ and $\overline{\text{OE}}$ are Don't Care)



t RC
t RAS
t RP
RAS
V IH
V IL
t CRP
t RPC
CAS
V IH
V IL
t RAH
t ASR
ADDRESSES
V IH
V IL
ROW ADDRESS

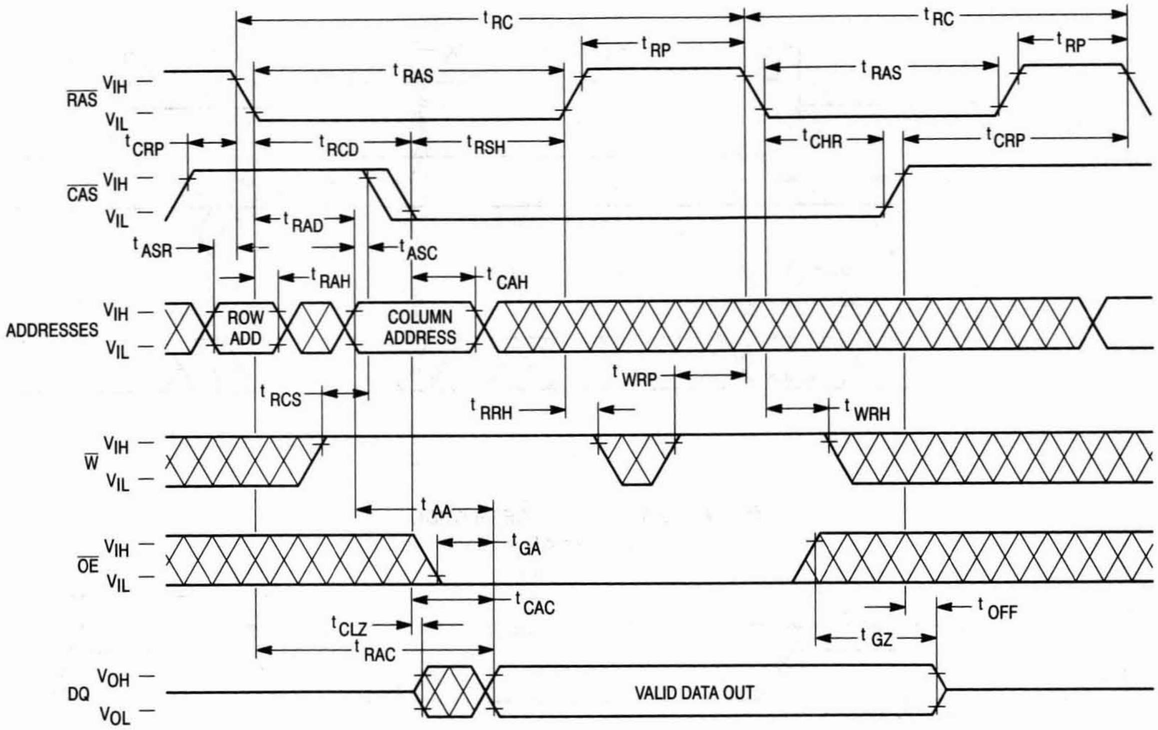
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{OE}}$ and A0 – A9 are Don't Care)

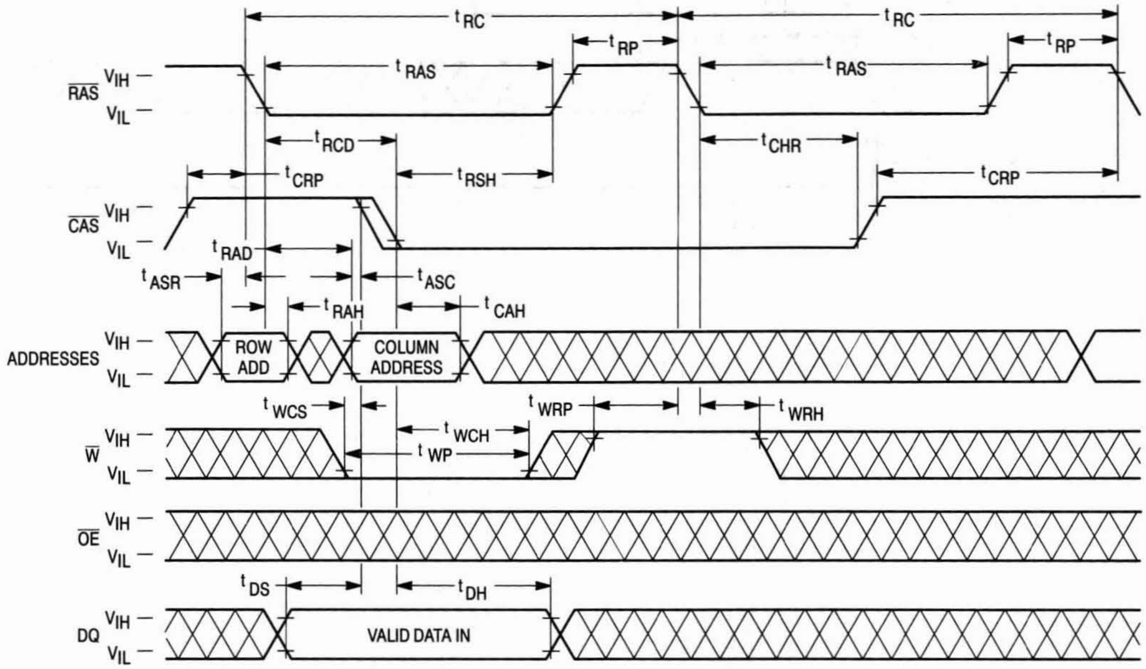


t RC
t RP
t RAS
t RP
RAS
V IH
V IL
t RPC
t CSR
t CP
t CHR
CAS
V IH
V IL
t WRP
t WRH
W
V IH
V IL
t OFF
DQ
V OH
V OL
HIGH Z

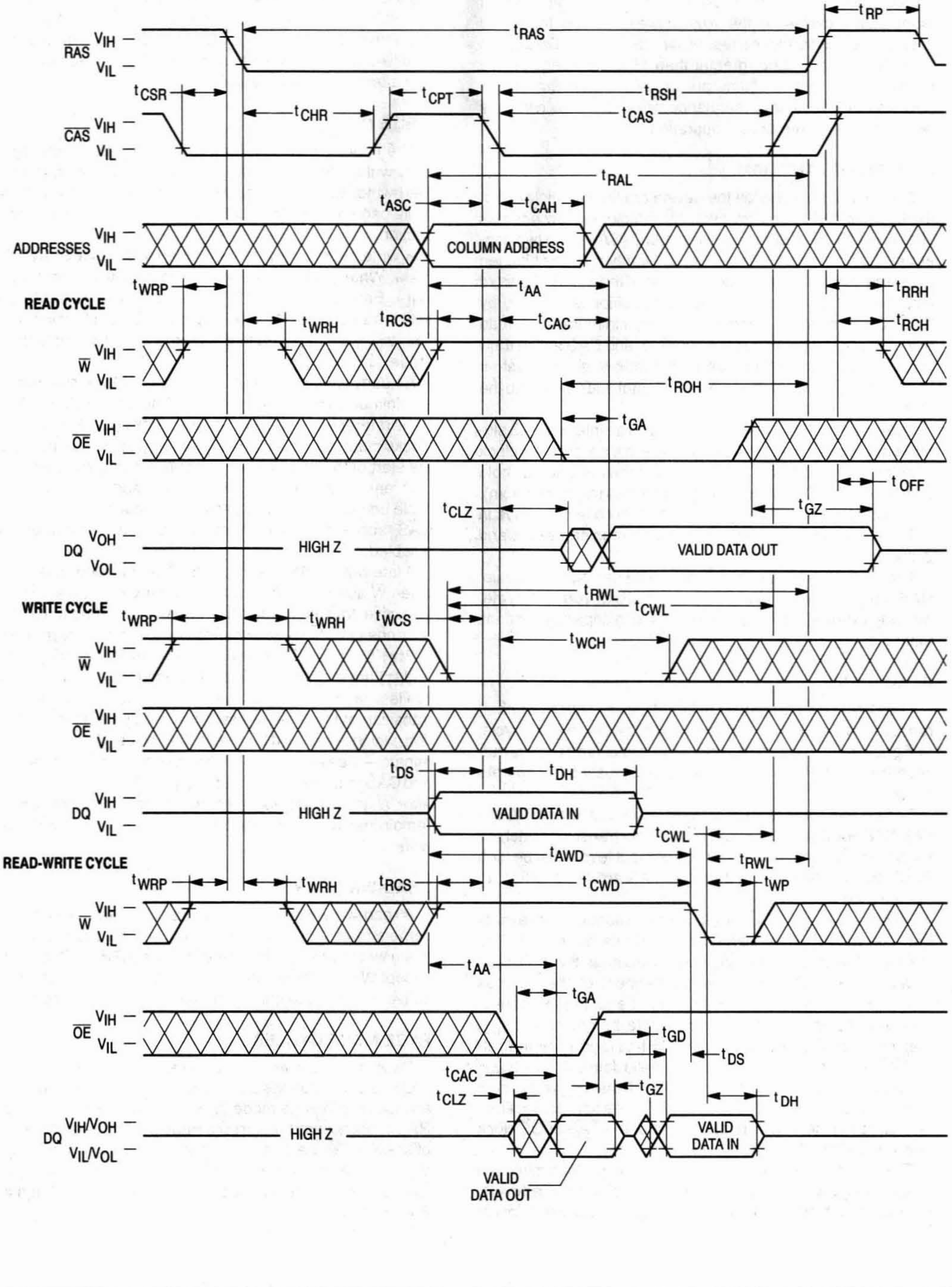
HIDDEN REFRESH CYCLE (READ)


t RC
t RC
t RP
t RP
t RAS
t RAS
RAS
VIH
VIL
t CRP
t RCD
t RSH
t CHR
t CRP
CAS
VIH
VIL
t RAD
t ASR
t ASC
t RAH
t CAH
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
t WRP
t RCS
t RRH
t WRH
W
VIH
VIL
t AA
OE
VIH
VIL
t GA
t CAC
t CLZ
t OFF
t RAC
t GZ
DQ
VOH
VOL
VALID DATA OUT

HIDDEN REFRESH CYCLE (EARLY WRITE)


t RC
t RC
t RP
t RP
t RAS
t RAS
RAS
VIH
VIL
t RCD
t CHR
t CRP
t RSH
t CRP
CAS
VIH
VIL
t RAD
t ASR
t ASC
t RAH
t CAH
ADDRESSES
VIH
VIL
ROW ADD
COLUMN ADDRESS
t WCS
t WRP
t WRH
t WCH
t WP
W
VIH
VIL
OE
VIH
VIL
t DS
t DH
DQ
VIH
VIL
VALID DATA IN

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE


$\overline{\text{RAS}}$ V_{IH} V_{IL}
t_{RAS}
t_{RP}
t_{CSR}
t_{CHR}
t_{CPT}
t_{RSH}
t_{CAS}
$\overline{\text{CAS}}$ V_{IH} V_{IL}
t_{RAL}
t_{ASC}
t_{CAH}
ADDRESSES V_{IH} V_{IL}
COLUMN ADDRESS
READ CYCLE
t_{WRP}
t_{AA}
t_{RRH}
t_{WRH}
t_{RCS}
t_{CAC}
t_{RCH}
$\overline{\text{W}}$ V_{IH} V_{IL}
t_{ROH}
t_{GA}
$\overline{\text{OE}}$ V_{IH} V_{IL}
t_{OFF}
t_{CLZ}
t_{GZ}
DQ V_{OH} V_{OL}
HIGH Z
VALID DATA OUT
WRITE CYCLE
t_{RWL}
t_{CWL}
t_{WRP}
t_{WRH}
t_{WCS}
t_{WCH}
$\overline{\text{W}}$ V_{IH} V_{IL}
$\overline{\text{OE}}$ V_{IH} V_{IL}
t_{DS}
t_{DH}
DQ V_{IH} V_{IL}
HIGH Z
VALID DATA IN
t_{CWL}
READ-WRITE CYCLE
t_{AWD}
t_{RWL}
t_{WRP}
t_{WRH}
t_{RCS}
t_{CWD}
t_{WP}
$\overline{\text{W}}$ V_{IH} V_{IL}
t_{AA}
t_{GA}
$\overline{\text{OE}}$ V_{IH} V_{IL}
t_{GD}
t_{DS}
t_{CAC}
t_{CLZ}
t_{GZ}
t_{DH}
DQ V_{IH}/V_{OH} V_{IL}/V_{OL}
HIGH Z
VALID DATA IN
VALID DATA OUT

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds or 128 milliseconds in case of low power device with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 word locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the module: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{\text{CAS}}$ and output enable ($\overline{\text{OE}}$) control read access time: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum and $\overline{\text{OE}}$ must be active t_{RAC}-t_{GA} (both minimum) after $\overline{\text{RAS}}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{\text{OE}}$ active transition does not occur in time, read access time is determined by either the $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ clocks are active. When either the $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers and $\overline{\text{OE}}$ disabled.

A late write cycle (referred to as $\overline{\text{OE}}$-controlled write) occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, $(t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but outputs are switched off by $\overline{\text{OE}}$ inactive transition, which is required to write to the device. Q may be indeterminate — see note 15 of AC Operating Conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle. $\overline{\text{OE}}$ must remain inactive for t_{GH} after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP}, while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM40100 require refresh every 16 milliseconds, while refresh time for the MCM40L100 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM40100, and 124.8 microseconds for the MCM40L100. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM40100 and 128 milliseconds on the MCM40L100.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decodes. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{\text{RAS}}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode entry) as in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

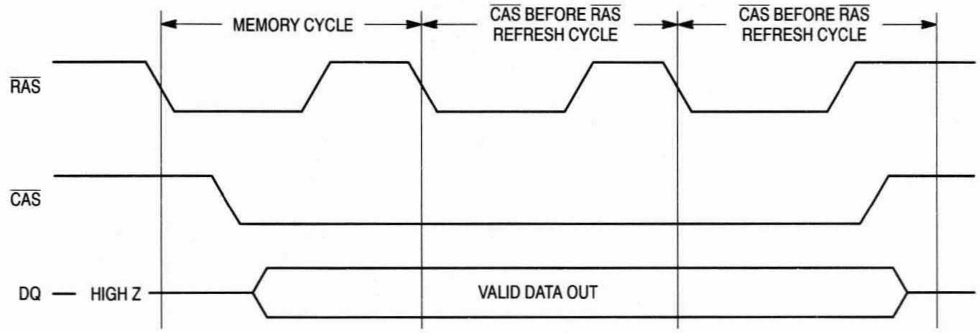


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 40100 or 40L100 X XX

Motorola Memory Prefix — MCM
Part Number — 40100 or 40L100
Package (AS = SIMM, ASG = Gold Pad SIMM) — X
Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers — MCM40100AS60 MCM40100ASG60
MCM40100AS70 MCM40100ASG70
MCM40100AS80 MCM40100ASG80
MCM40L100AS60 MCM40L100ASG60
MCM40L100AS70 MCM40L100ASG70
MCM40L100AS80 MCM40L100ASG80

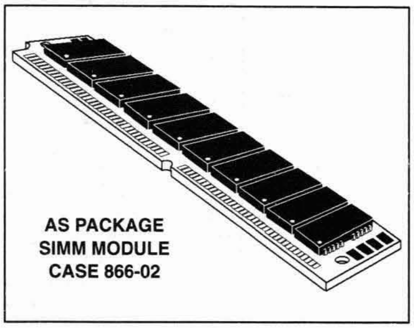
NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM40200
MCM40L200

2M x 40 Bit Dynamic Random Access Memory Module
for Error Correction Applications

The MCM40200 and MCM40L200 are 80M dynamic random access memory (DRAM) modules organized as 2,097,152 x 40 bits. The module is a double-sided 72-lead single-in-line memory module (SIMM) consisting of twenty MCM54400AN DRAMs housed in 20/26 J-lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM54400AN is a CMOS high-speed dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.


AS PACKAGE
SIMM MODULE
CASE 866-02

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM40200 = 16 ms (Max)
  MCM40L200 = 128 ms (Max)
- Consists of Twenty 1M x 4 DRAMs, and Twenty 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM40200-60 = 60 ns (Max)
  MCM40200-70 = 70 ns (Max)
  MCM40200-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM40200-60 = 6.71 W (Max)
  MCM40200-70 = 5.61 W (Max)
  MCM40200-80 = 4.79 W (Max)
- Low Standby Power Dissipation: TTL Levels = 220 mW (Max)
  CMOS Levels= 110 mW (Max, MCM40200)
  = 22 mW (Max, MCM40L200)

PIN NAMES

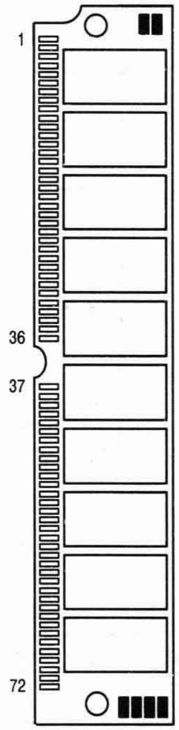
A0 – A9	Address Inputs	DQ0 – DQ39	Data Input/Output
$\overline{\text{CAS0}}$, $\overline{\text{CAS1}}$	Column Address Strobe	PD1 – PD5	Presence Detect
$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$	Row Address Strobe	$\overline{\text{W}}$	Read/Write Input
$\overline{\text{X40}}$	Configuration Detection	$\overline{\text{OE}}$	Output Enable
V_{CC}	Power (+ 5 V)	V_{SS}	Ground
NC	No Connection		

All power supply and ground pins must be connected for proper operation of the device.

PIN ASSIGNMENTS

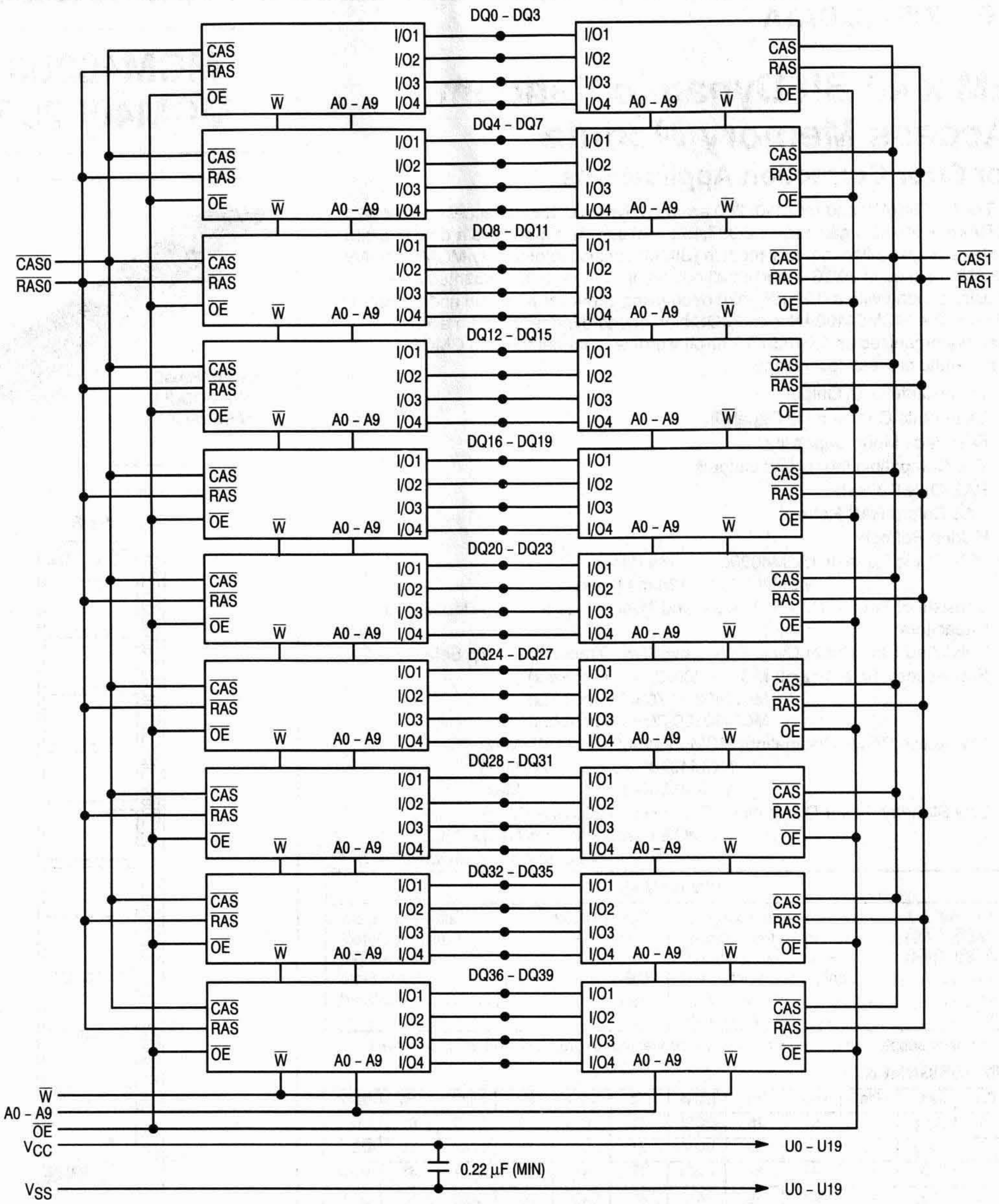
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	NC	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{\text{OE}}$	31	A8	43	$\overline{\text{CAS1}}$	55	DQ28	67	PD1
8	DQ6	20	DQ8	32	A9	44	$\overline{\text{RAS0}}$	56	DQ29	68	PD2
9	DQ7	21	DQ9	33	NC	45	$\overline{\text{RAS1}}$	57	DQ30	69	PD3
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD4
11	PD5	23	DQ11	35	DQ17	47	$\overline{\text{W}}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	$\overline{\text{X40}}$	60	DQ32	72	V_{SS}

TOP VIEW



5

2M x 40 BLOCK DIAGRAM


DQ0 – DQ3
DQ4 – DQ7
DQ8 – DQ11
DQ12 – DQ15
DQ16 – DQ19
DQ20 – DQ23
DQ24 – DQ27
DQ28 – DQ31
DQ32 – DQ35
DQ36 – DQ39
CAS
RAS
OE
W
A0 – A9
I/O1
I/O2
I/O3
I/O4
CAS0
RAS0
CAS1
RAS1
W
A0 – A9
OE
V_{CC}
V_{SS}
0.22 µF (MIN)
U0 – U19
U0 – U19

PRESENCE DETECT PIN OUT			
Pin Name	60 ns	70 ns	80 ns
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}
PD5	NC	NC	NC
$\overline{X40}$	V_{SS}	V_{SS}	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	9.15	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	MCM40200-60, t_{RC} = 110 ns MCM40200-70, t_{RC} = 130 ns MCM40200-80, t_{RC} = 150 ns	I_{CC1}	— — —	1220 1020 870	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	40	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles	MCM40200-60, t_{RC} = 110 ns MCM40200-70, t_{RC} = 130 ns MCM40200-80, t_{RC} = 150 ns	I_{CC3}	— — —	1220 1020 870	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle	MCM40200-60, t_{PC} = 45 ns MCM40200-70, t_{PC} = 45 ns MCM40200-80, t_{PC} = 50 ns	I_{CC4}	— — —	720 720 620	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	MCM40200 MCM40L200	I_{CC5}	— —	20 4	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	MCM40200-60, t_{RC} = 110 ns MCM40200-70, t_{RC} = 130 ns MCM40200-80, t_{RC} = 150 ns	I_{CC6}	— — —	1220 1020 870	mA	1
V_{CC} Power Supply Current Battery Backup Mode (t_{RC} = 125 μs; t_{RAS} = 1 μs; $\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$, DQ, A0 – A9 = V_{CC} – 0.2 V or 0.2 V)	MCM40L200 only	I_{CC7}	—	6.0	mA	1, 3
Input Leakage Current ($V_{SS} \leq V_{in} \leq V_{CC}$)		$I_{lkg(I)}$	– 200	200	μA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \leq V_{out} \leq V_{CC}$)		$I_{lkg(O)}$	– 20	20	μA	
Output High Voltage (I_{OH} = – 5 mA)		V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.
3. t_{RAS} (max) = 1 μs is only applied to refresh of battery backup. t_{RAS} (max) = 10 μs is applied to functional operating.

CAPACITANCE ($f = 1.0$ MHz, $T_A = 25°C$, $V_{CC} = 5$ V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit
Input Capacitance (A0 – A9)	C_{I1}	—	110	pF
Input Capacitance ($\overline{\text{W}}$, $\overline{\text{OE}}$)	C_{I2}	—	150	pF
Input Capacitance ($\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{CAS0}}$, $\overline{\text{CAS1}}$)	C_{I3}	—	80	pF
I/O Capacitance (DQ0 – DQ39)	C_{DQ1}	—	24	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\ \Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0\ V \pm 10\%$, $T_A = 0$ to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM40200-60 MCM40L200-60		MCM40200-70 MCM40L200-70		MCM40200-80 MCM40L200-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	165	—	185	—	205	—	ns	6
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	50	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	95	—	100	—	105	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	7, 8
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	7, 10
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	40	—	40	—	45	ns	7
$\overline{\text{CAS}}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	200 k	70	200 k	80	200 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	20	10 k	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements $t_T = 5.0$ ns.
5. To avoid bus contention and potential damage to the module, $\overline{\text{RAS0}}$ and $\overline{\text{RAS1}}$ may not be active low simultaneously.
6. The specification for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is ensured.
7. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
11. t_{OFF} (max) and/or t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM40200-60 MCM40L200-60		MCM40200-70 MCM40L200-70		MCM40200-80 MCM40L200-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	12
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	13
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	14
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	14
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	15
Refresh Period MCM40200 MCM40L200	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	16
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	50	—	ns	16
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	90	—	100	—	110	—	ns	16
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	60	—	65	—	70	—	ns	16
$\overline{\text{CAS}}$ Precharge to Write Delay Time (Page Mode)	t_{CEHWL}	t_{CPWD}	70	—	70	—	75	—	ns	16
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	

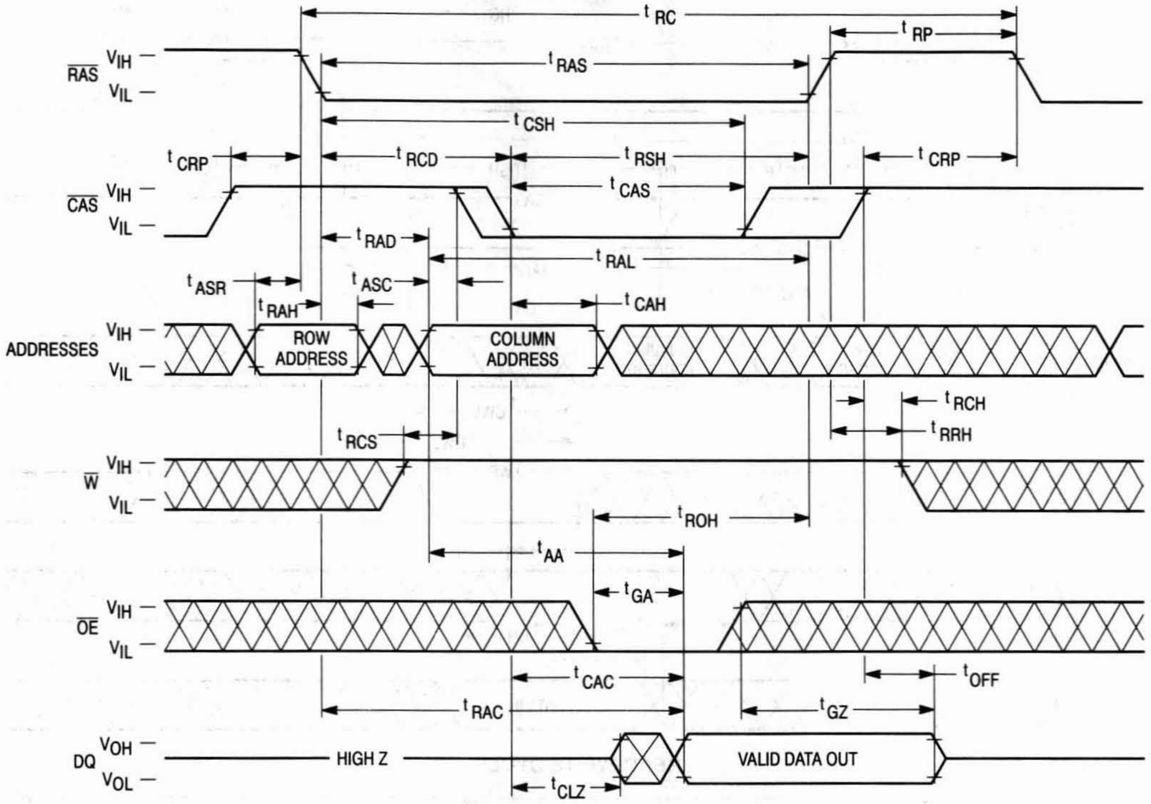
NOTES:

12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in late write or read-write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM40200A-60 MCM40L200A-60		MCM40200A-70 MCM40L200A-70		MCM40200A-80 MCM40L200A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Time	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{OE}}$	t_{GLREH}	t_{ROH}	10	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	20	—	20	ns	
$\overline{\text{OE}}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	20	—	ns	
Output Buffer Turn-Off Delay Time from $\overline{\text{OE}}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	20	ns	11
$\overline{\text{OE}}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	20	—	ns	

READ CYCLE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t ASR
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t RAH
t CAH
ADDRESSES
VIH —
VIL —
ROW ADDRESS
COLUMN ADDRESS
t RCH
t RRH
t RCS
W
VIH —
VIL —
t ROH
t AA
t GA
OE
VIH —
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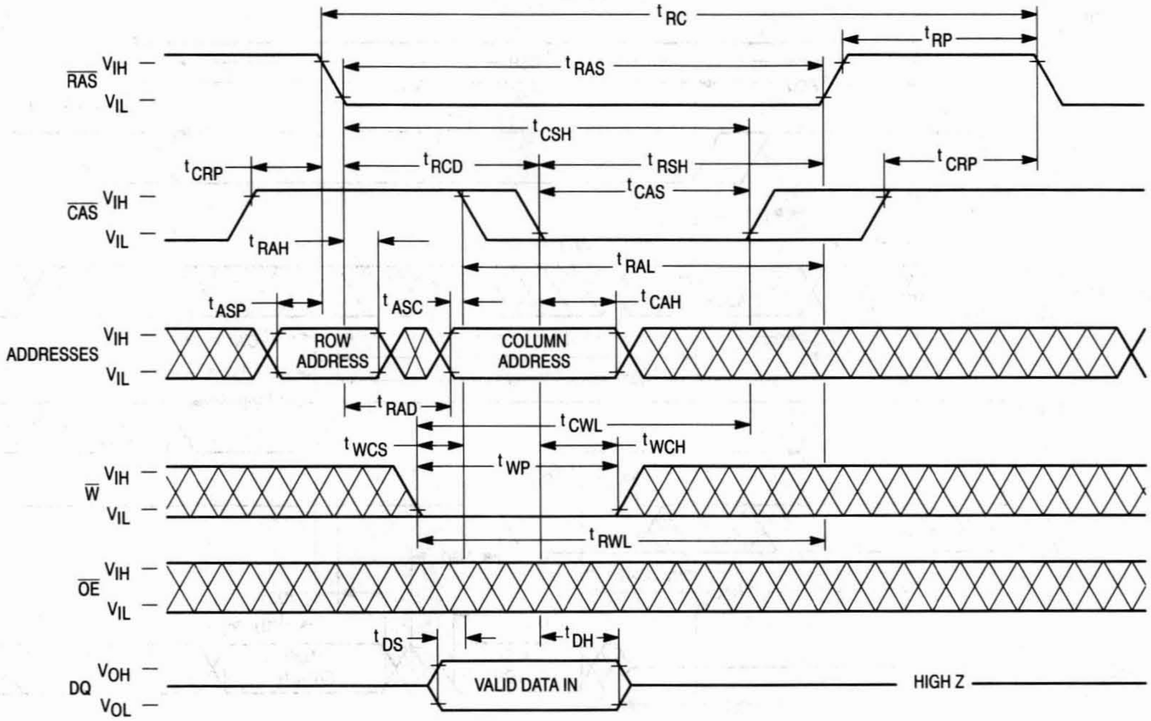
t GZ
DQ
VOH —
VOL —
HIGH Z
VALID DATA OUT
t CLZ

EARLY WRITE CYCLE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t WP
W
VIH —
VIL —
t RWL
OE
VIH —
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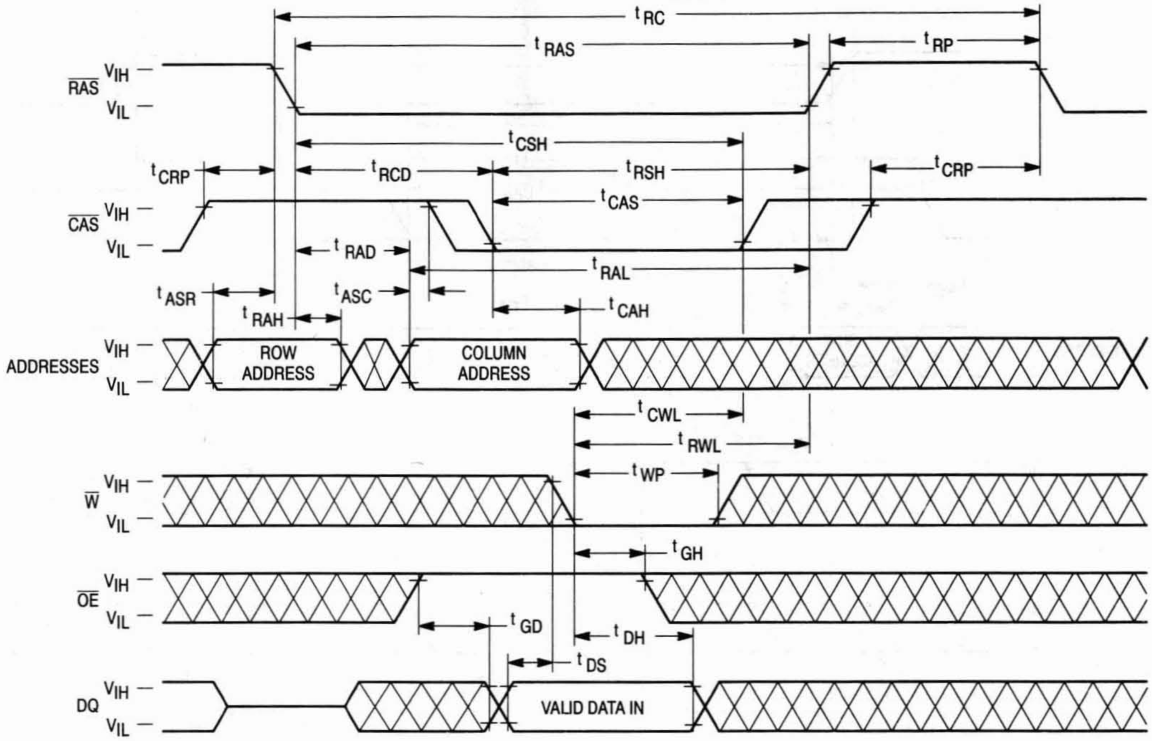
t DH
DQ
VOH —
VOL —
VALID DATA IN
HIGH Z

5

$\overline{\text{OE}}$ CONTROLLED WRITE CYCLE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ADDRESSES
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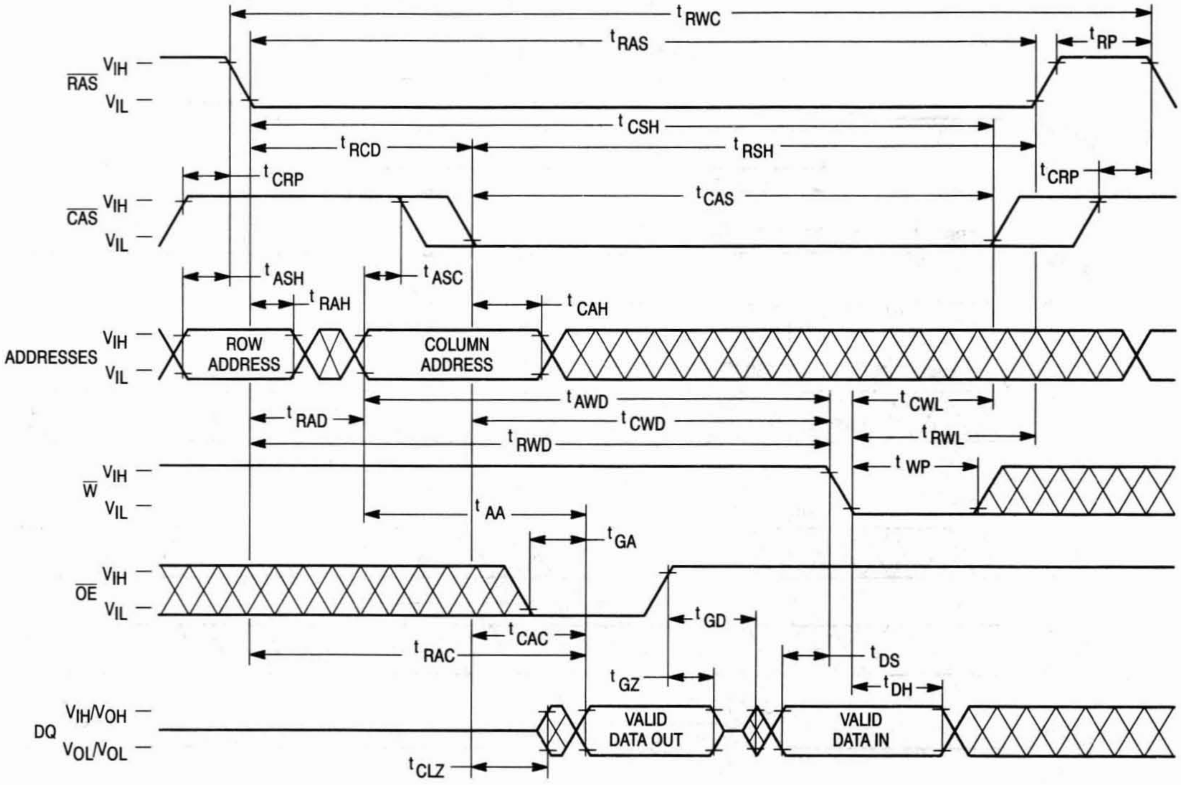
VIL
VALID DATA IN

READ-WRITE CYCLE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ADDRESSES
VIH
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W
VIH
VIL
t AA
t GA
OE
VIH
VIL
t GD
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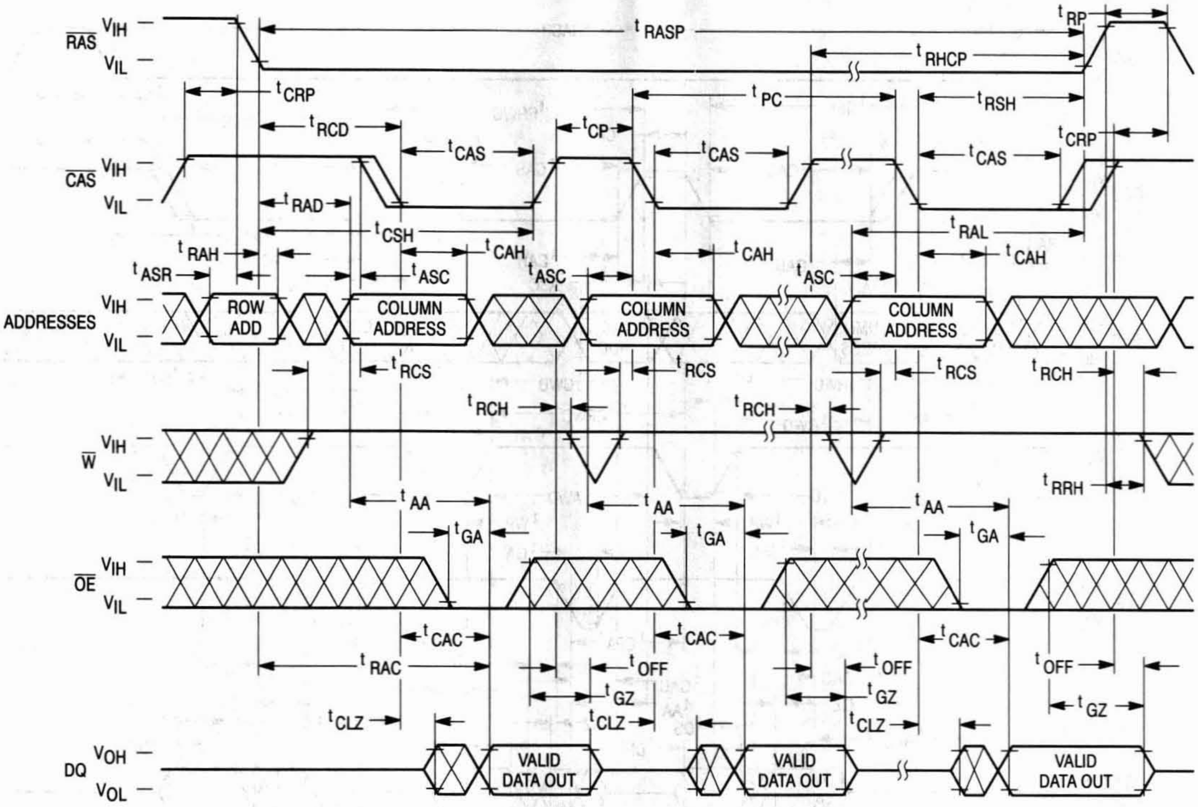
DQ
VIH/VOH
VOL/VOL
VALID DATA OUT
VALID DATA IN
t CLZ

FAST PAGE MODE READ CYCLE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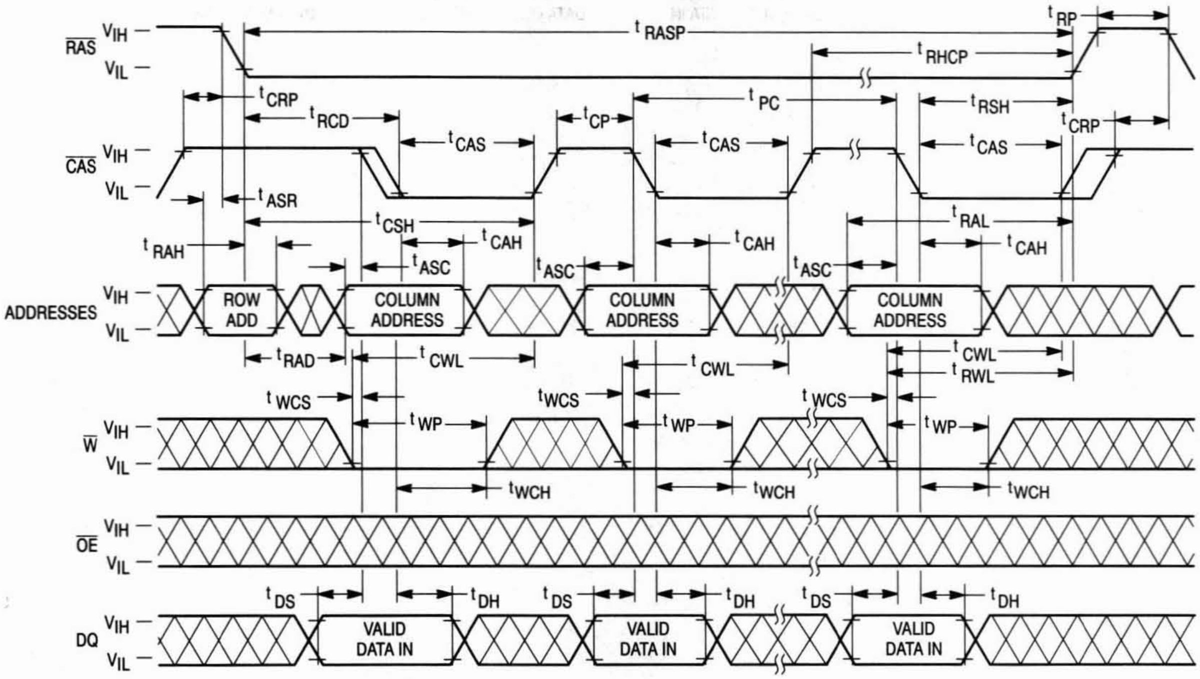
FAST PAGE MODE EARLY WRITE CYCLE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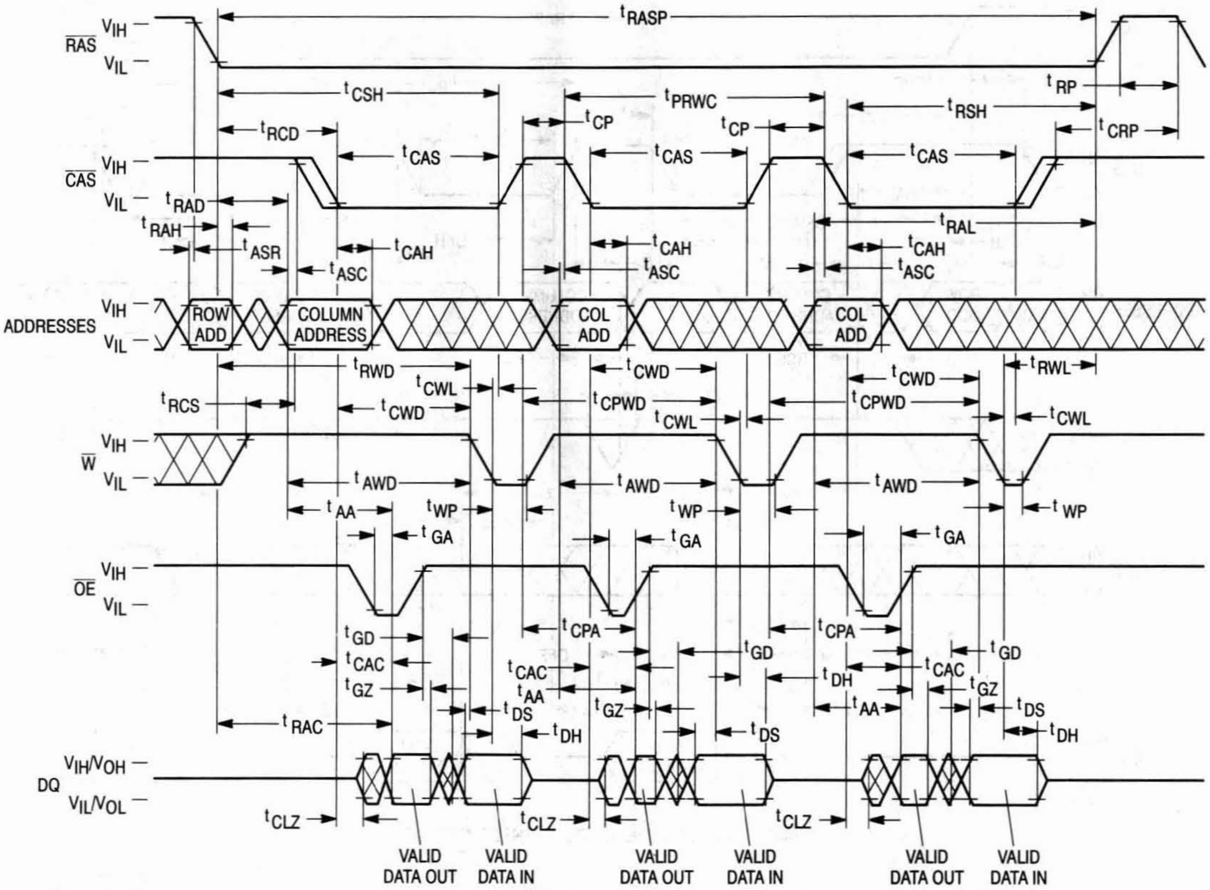
VALID DATA IN

FAST PAGE MODE READ-WRITE CYCLE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VIH
VIL
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VIH/VOH
VIL/VOL
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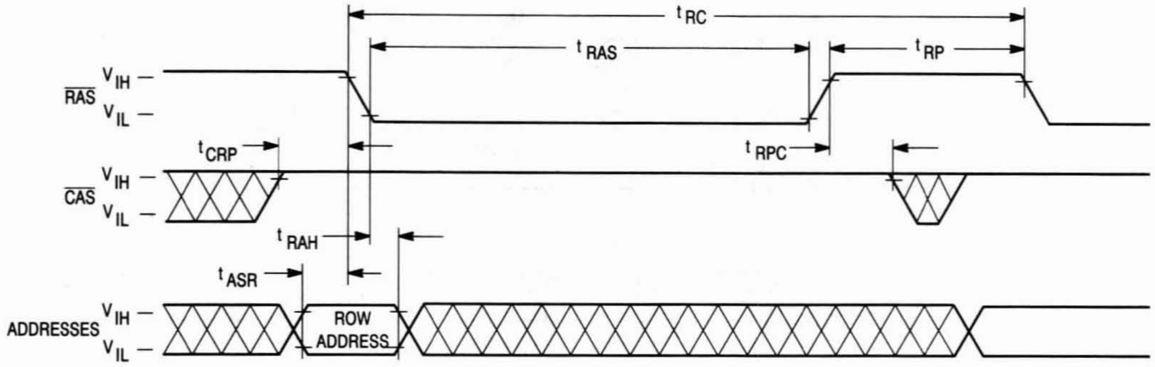
tRAD
tRAH
tASR
tCAH
tASC
tRAL
ROW ADD
COLUMN ADDRESS
COL ADD
tRWD
tCWD
tRWL
tCWL
tCPWD
tRCS
tAWD
tAA
tWP
tGA
tGD
tCAC
tGZ
tCPA
tDH
tDS
tRAC
tCLZ
VALID DATA OUT
VALID DATA IN

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

($\overline{\text{W}}$ and $\overline{\text{OE}}$ are Don't Care)



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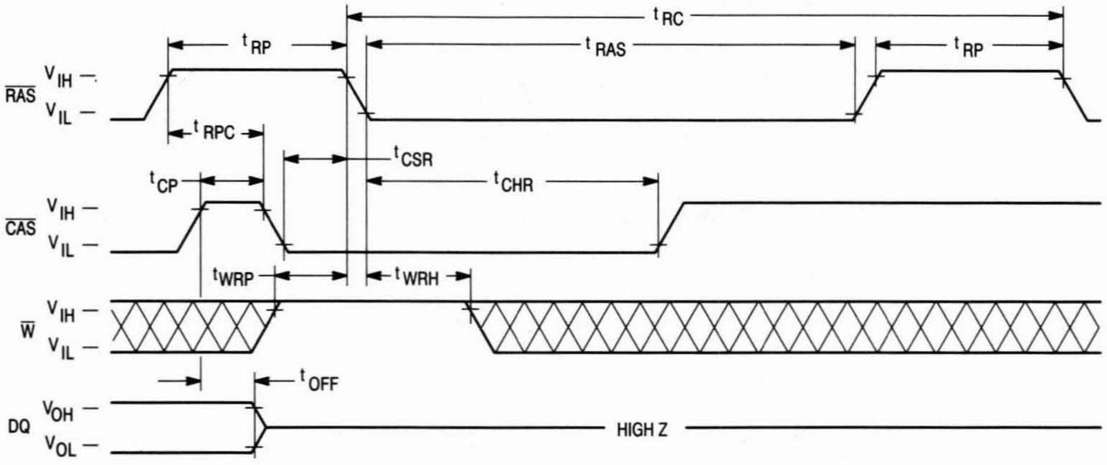
t RPC
CAS
V IH
V IL
t RAH
t ASR
ADDRESSES
V IH
V IL
ROW ADDRESS

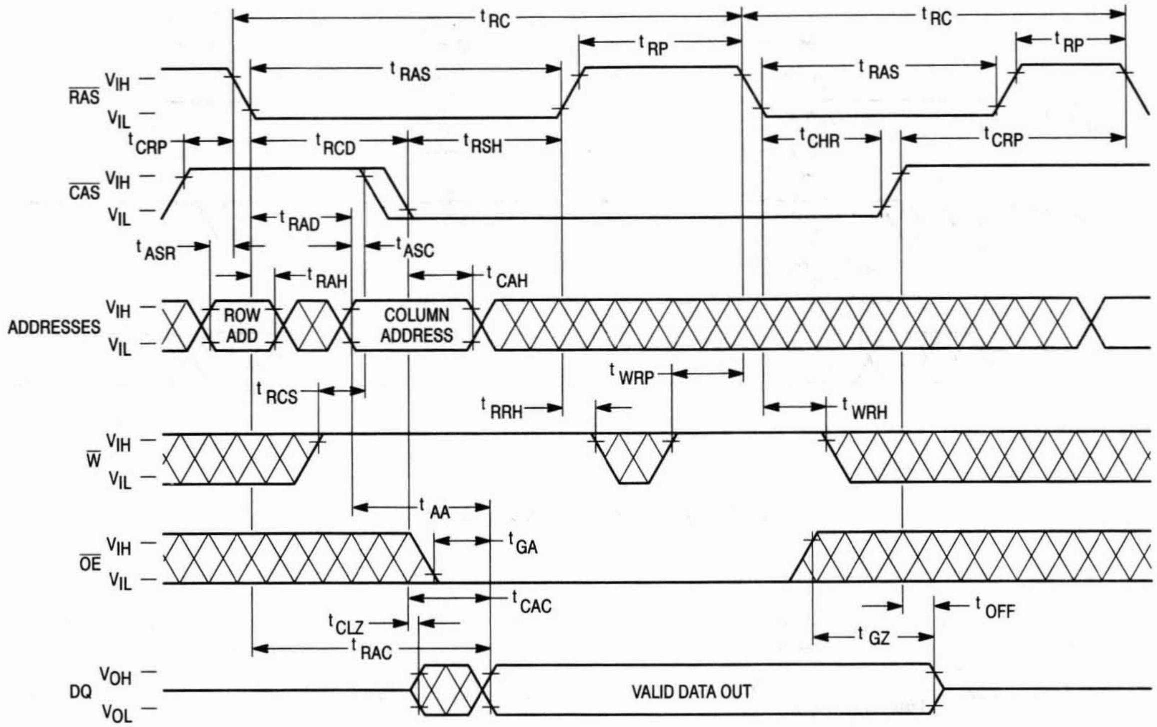
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

($\overline{\text{OE}}$ and A0 – A9 are Don't Care)



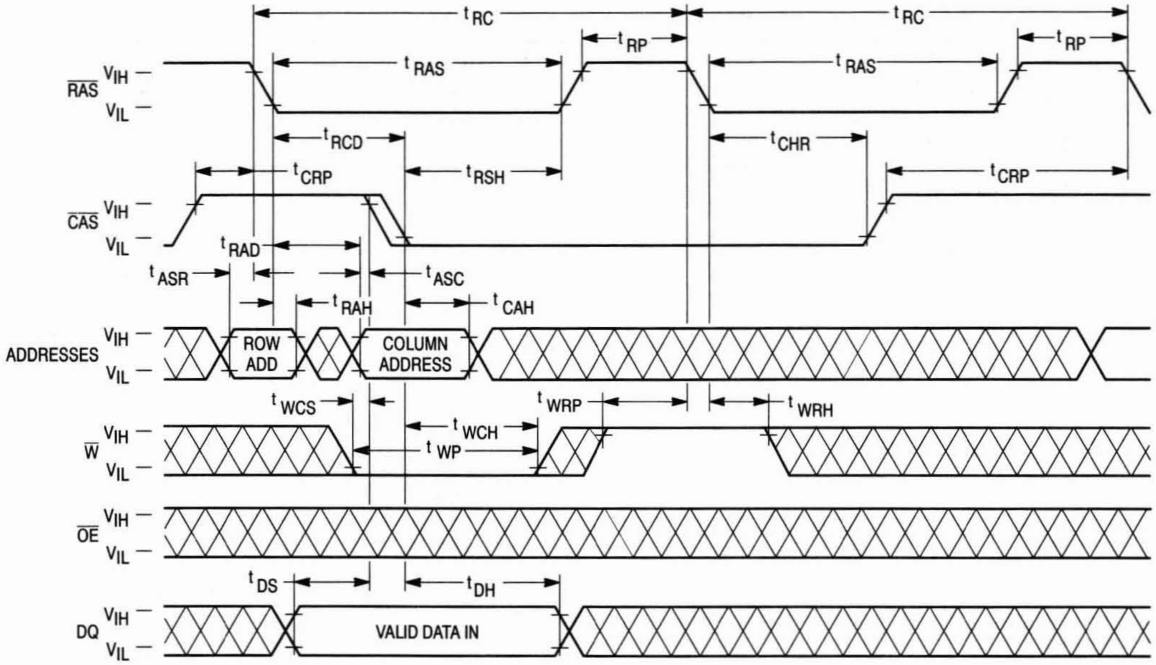
t RC
t RP
t RAS
t RP
RAS
V IH
V IL
t RPC
t CSR
t CP
t CHR
CAS
V IH
V IL
t WRP
t WRH
W
V IH
V IL
t OFF
DQ
V OH
V OL
HIGH Z

HIDDEN REFRESH CYCLE (READ)



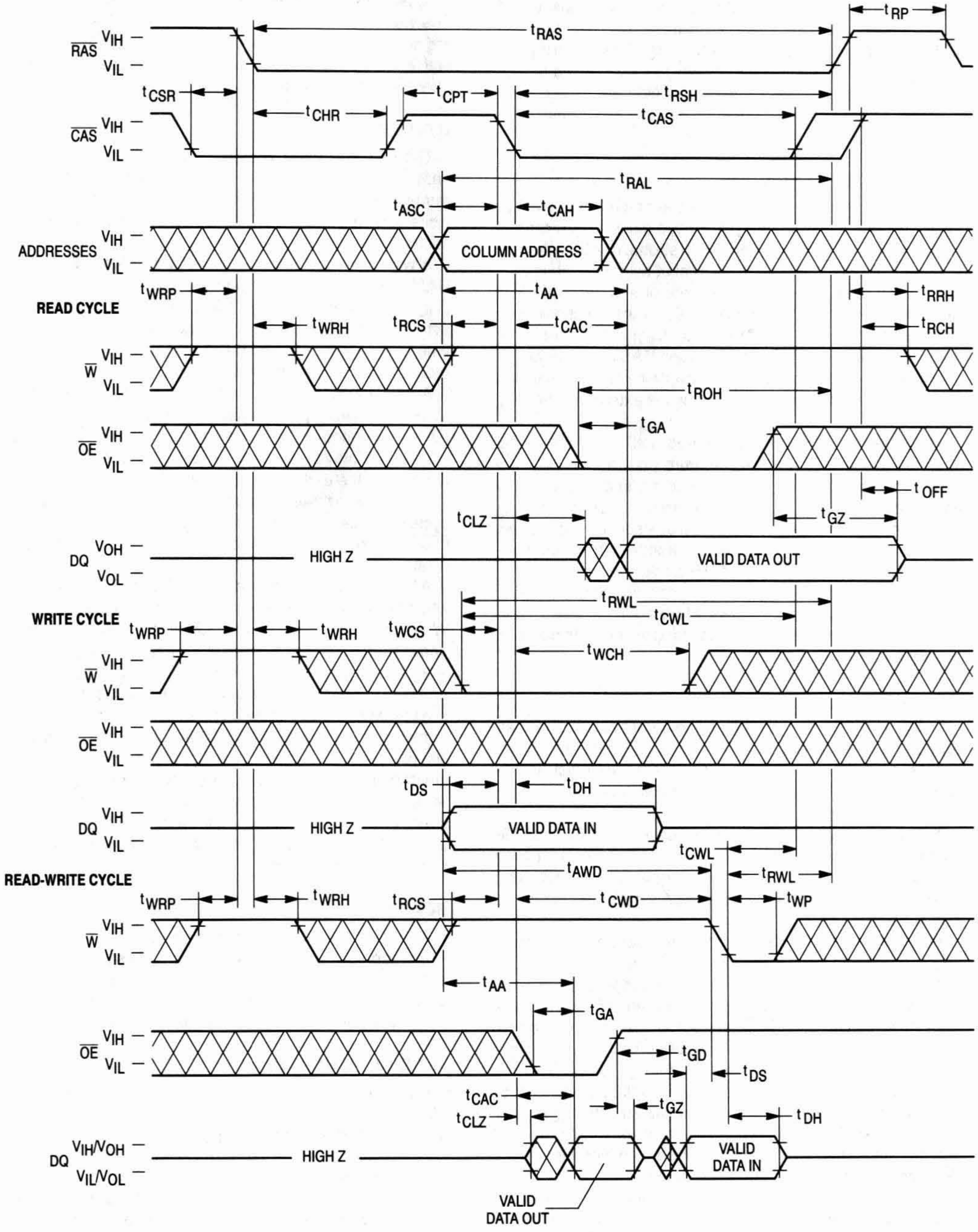
$\overline{RAS}$ V_{IH} V_{IL}
$\overline{CAS}$ V_{IH} V_{IL}
ADDRESSES V_{IH} V_{IL}
ROW ADD
COLUMN ADDRESS
$\overline{W}$ V_{IH} V_{IL}
$\overline{OE}$ V_{IH} V_{IL}
DQ V_{OH} V_{OL}
VALID DATA OUT
t_{RC}
t_{RC}
t_{RP}
t_{RP}
t_{RAS}
t_{RAS}
t_{CRP}
t_{RCD}
t_{RSH}
t_{CHR}
t_{CRP}
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
t_{WRP}
t_{RCS}
t_{RRH}
t_{WRH}
t_{AA}
t_{GA}
t_{CAC}
t_{CLZ}
t_{RAC}
t_{OFF}
t_{GZ}

HIDDEN REFRESH CYCLE (EARLY WRITE)



$\overline{RAS}$ V_{IH} V_{IL}
$\overline{CAS}$ V_{IH} V_{IL}
ADDRESSES V_{IH} V_{IL}
ROW ADD
COLUMN ADDRESS
$\overline{W}$ V_{IH} V_{IL}
$\overline{OE}$ V_{IH} V_{IL}
DQ V_{IH} V_{IL}
VALID DATA IN
t_{RC}
t_{RC}
t_{RP}
t_{RP}
t_{RAS}
t_{RAS}
t_{RCD}
t_{CHR}
t_{CRP}
t_{RSH}
t_{CRP}
t_{RAD}
t_{ASR}
t_{ASC}
t_{RAH}
t_{CAH}
t_{WCS}
t_{WRP}
t_{WRH}
t_{WCH}
t_{WP}
t_{DS}
t_{DH}

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



t_{RP}
t_{RAS}
$\overline{RAS}$ V_{IH} V_{IL}
t_{CSR}
t_{CPT}
t_{RSH}
t_{CHR}
t_{CAS}
$\overline{CAS}$ V_{IH} V_{IL}
t_{RAL}
t_{ASC}
t_{CAH}
ADDRESSES V_{IH} V_{IL}
COLUMN ADDRESS
t_{WRP}
t_{AA}
t_{RRH}
READ CYCLE
t_{WRH}
t_{RCS}
t_{CAC}
t_{RCH}
$\overline{W}$ V_{IH} V_{IL}
t_{ROH}
t_{GA}
$\overline{OE}$ V_{IH} V_{IL}
t_{OFF}
t_{CLZ}
t_{GZ}
DQ V_{OH} V_{OL}
HIGH Z
VALID DATA OUT
t_{RWL}
WRITE CYCLE
t_{CWL}
t_{WRP}
t_{WRH}
t_{WCS}
t_{WCH}
$\overline{W}$ V_{IH} V_{IL}
$\overline{OE}$ V_{IH} V_{IL}
t_{DS}
t_{DH}
DQ V_{IH} V_{IL}
HIGH Z
VALID DATA IN
t_{CWL}
READ-WRITE CYCLE
t_{AWD}
t_{RWL}
t_{WRP}
t_{WRH}
t_{RCS}
t_{CWD}
t_{WP}
$\overline{W}$ V_{IH} V_{IL}
t_{AA}
t_{GA}
$\overline{OE}$ V_{IH} V_{IL}
t_{GD}
t_{DS}
t_{CAC}
t_{GZ}
t_{CLZ}
t_{DH}
DQ V_{IH}/V_{OH} V_{IL}/V_{OL}
HIGH Z
VALID DATA IN
VALID DATA OUT

DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds or 128 milliseconds in case of low power device with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 word locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the module: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{\text{CAS}}$ and output enable ($\overline{\text{OE}}$) control read access time: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum and $\overline{\text{OE}}$ must be active $t_{RAC} - t_{GA}$ (both minimum) after $\overline{\text{RAS}}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{\text{OE}}$ active transition does not occur in time, read access time is determined by either the $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ clocks are active. When either the $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers and $\overline{\text{OE}}$ disabled.

A late write cycle (referred to as $\overline{\text{OE}}$-controlled write) occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, $(t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but outputs are switched off by $\overline{\text{OE}}$ inactive transition, which is required to write to the device. Q may be indeterminate — see note 15 of AC Operating Conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle. $\overline{\text{OE}}$ must remain inactive for t_{GH} after $\overline{\text{W}}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL}. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum t_{CP}, while RAS remains low (V_{IL}). The second CAS active transition while RAS is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM40200 require refresh every 16 milliseconds, while refresh time for the MCM40L200 is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM40200, and 124.8 microseconds for the MCM40L200. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM40200 and 128 milliseconds on the MCM40L200.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decodes. Three other methods of refresh, **RAS-only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode entry) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **CAS before RAS** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

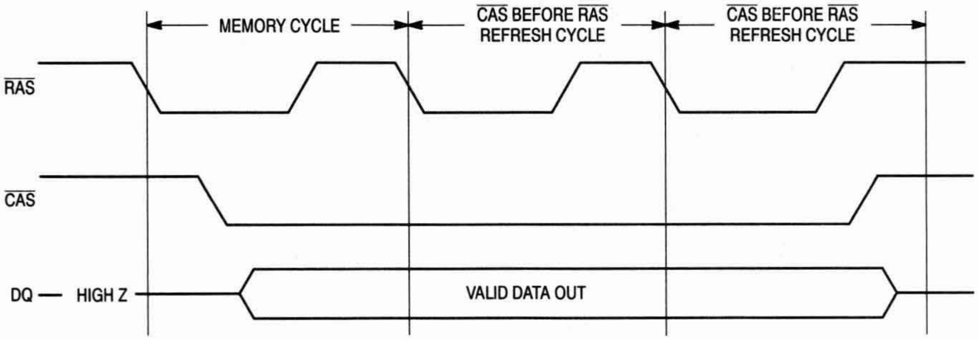


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION

(Order by Full Part Number)

MCM 40200 or 40L200 X XX

Motorola Memory Prefix — MCM

Part Number — 40200 or 40L200

Package (AS = SIMM, ASG = Gold Pad SIMM) — X

Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers —
MCM40200AS60 MCM40200ASG60
MCM40200AS70 MCM40200ASG70
MCM40200AS80 MCM40200ASG80

MCM40L200AS60 MCM40L200ASG60
MCM40L200AS70 MCM40L200ASG70
MCM40L200AS80 MCM40L200ASG80

NOTE: For mechanical data, please see Chapter 10.

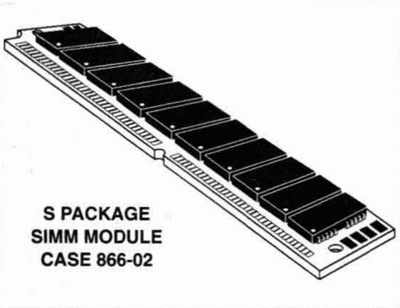
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM40400

Product Preview

4M x 40 Bit Dynamic Random Access Memory Module

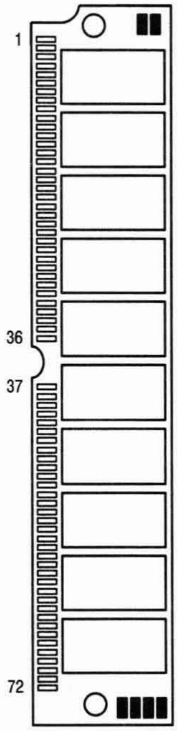
for Error Correction Applications



The MCM40400 is a dynamic random access memory (DRAM) module organized as 4,194,304 x 40 bits. The module is a double-sided 72-lead single-in-line memory module (SIMM) consisting of ten MCM517400 DRAMs housed in J-lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM517400 is a CMOS high-speed dynamic random access memory organized as 4,194,304 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh: MCM40400 = 32 ms (Max)
- Consists of Ten 4M x 4 DRAMs, and Ten 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM40400-60 = 60 ns (Max)
  MCM40400-70 = 70 ns (Max)
  MCM40400-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM40400-60 = 6.60 W (Max)
  MCM40400-70 = 5.50 W (Max)
  MCM40400-80 = 4.68 W (Max)
- Low Standby Power Dissipation: TTL Levels = 110 mW (Max)
  CMOS Levels= 55 mW (Max)

TOP VIEW

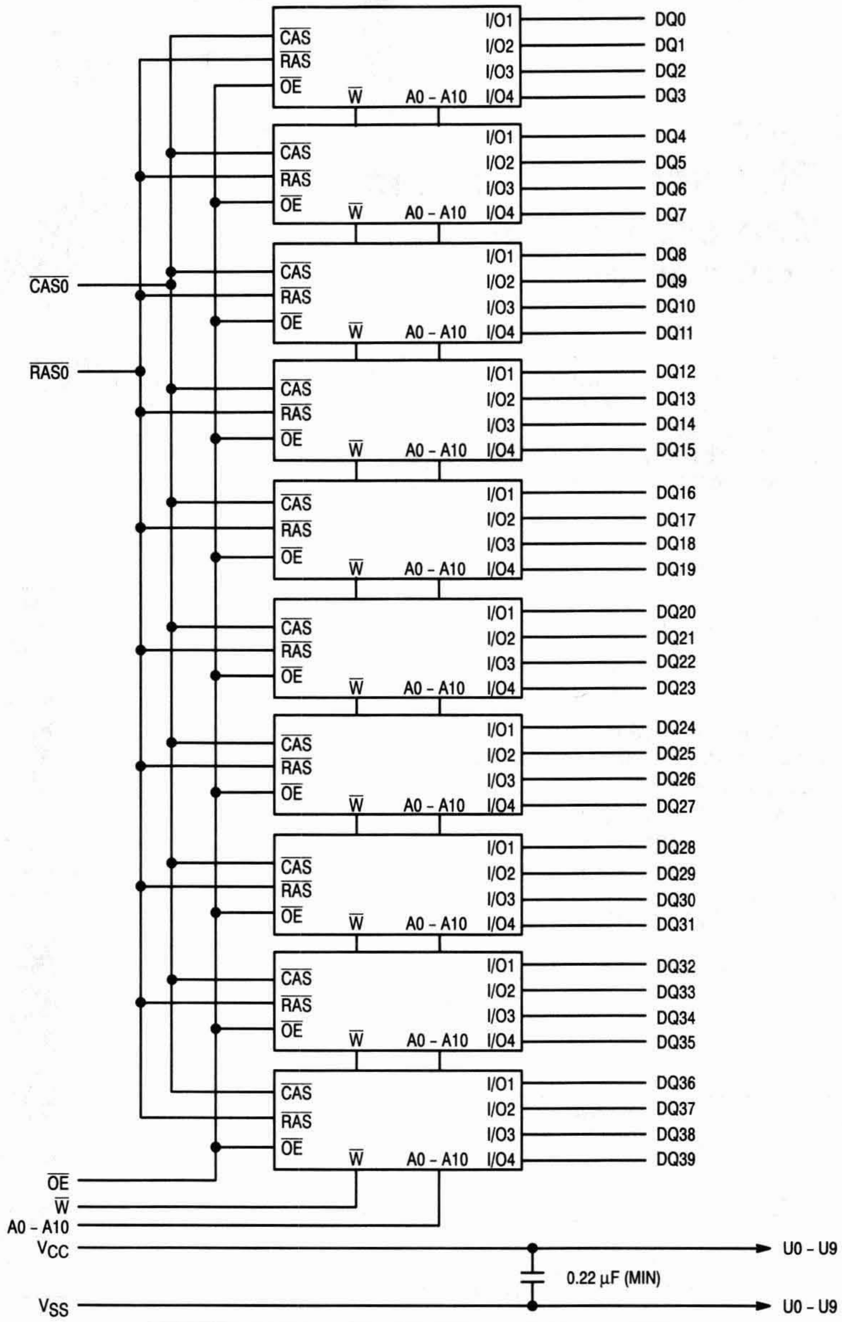


PIN NAMES			
A0 – A10	Address Inputs	DQ0 – DQ39	Data Input/Output
$\overline{CAS0}$	Column Address Strobe	PD1 – PD5	Presence Detect
$\overline{RAS0}$	Row Address Strobe	$\overline{W}$	Read/Write Input
$\overline{X40}$	Configuration Detection	$\overline{OE}$	Output Enable
V_{CC}	Power (+ 5 V)	V_{SS}	Ground
NC	No Connection		

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM


CAS0
RAS0
OE
W
A0 - A10
V_{CC}
V_{SS}
CAS
RAS
OE
W
A0 - A10
I/O1
I/O2
I/O3
I/O4
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
DQ32
DQ33
DQ34
DQ35
DQ36
DQ37
DQ38
DQ39
0.22 µF (MIN)
U0 - U9
U0 - U9

PRESENCE DETECT PIN OUT			
Pin Name	**60 ns**	**70 ns**	**80 ns**
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	NC	NC	NC
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}
PD5*	V_{SS}	V_{SS}	V_{SS}
$\overline{X40}$	V_{SS}	V_{SS}	V_{SS}

*PD5 tied to V_{SS} through a 2.6 kΩ resistor.

PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	A10	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{\text{OE}}$	31	A8	43	NC	55	DQ28	67	PD1
8	DQ6	20	DQ8	32	A9	44	$\overline{\text{RAS0}}$	56	DQ29	68	PD2
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ30	69	PD3
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD4
11	PD5	23	DQ11	35	DQ17	47	$\overline{\text{W}}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	$\overline{\text{X40}}$	60	DQ32	72	V_{SS}

ORDERING INFORMATION
(Order by Full Part Number)

MCM 40400 X XX

Motorola Memory Prefix — MCM
Part Number — 40400
Package (S = SIMM, SG = Gold Pad SIMM) — X
Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers —		
	MCM40400S60	MCM40400SG60
	MCM40400S70	MCM40400SG70
	MCM40400S80	MCM40400SG80

NOTE: For mechanical data, please see Chapter 10.

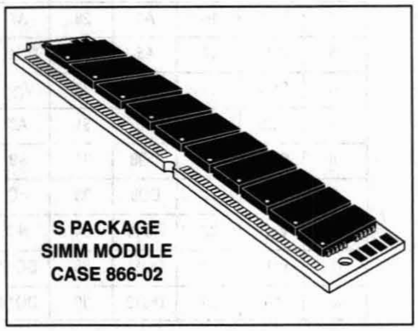
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM40800

Product Preview

8M x 40 Bit Dynamic Random Access Memory Module

for Error Correction Applications

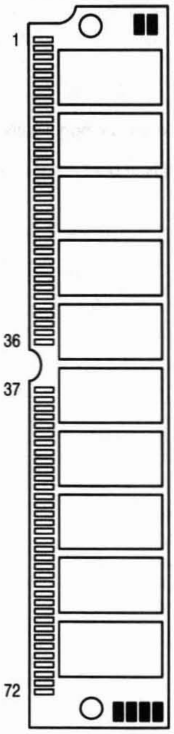


S PACKAGE
SIMM MODULE
CASE 866-02

The MCM40800 is a dynamic random access memory (DRAM) module organized as 2,097,152 x 40 bits. The module is a double-sided 72-lead single-in-line memory module (SIMM) consisting of twenty MCM517400 DRAMs housed in J-lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM517400 is a CMOS high-speed dynamic random access memory organized as 4,194,304 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh: MCM40800 = 32 ms (Max)
- Consists of Twenty 4M x 4 DRAMs, and Twenty 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM40800-60 = 60 ns (Max)
  MCM40800-70 = 70 ns (Max)
  MCM40800-80 = 80 ns (Max)
- Low Active Power Dissipation: MCM40800-60 = 6.71 W (Max)
  MCM40800-70 = 5.61 W (Max)
  MCM40800-80 = 4.79 W (Max)
- Low Standby Power Dissipation: TTL Levels = 220 mW (Max)
  CMOS Levels= 110 mW (Max)

TOP VIEW

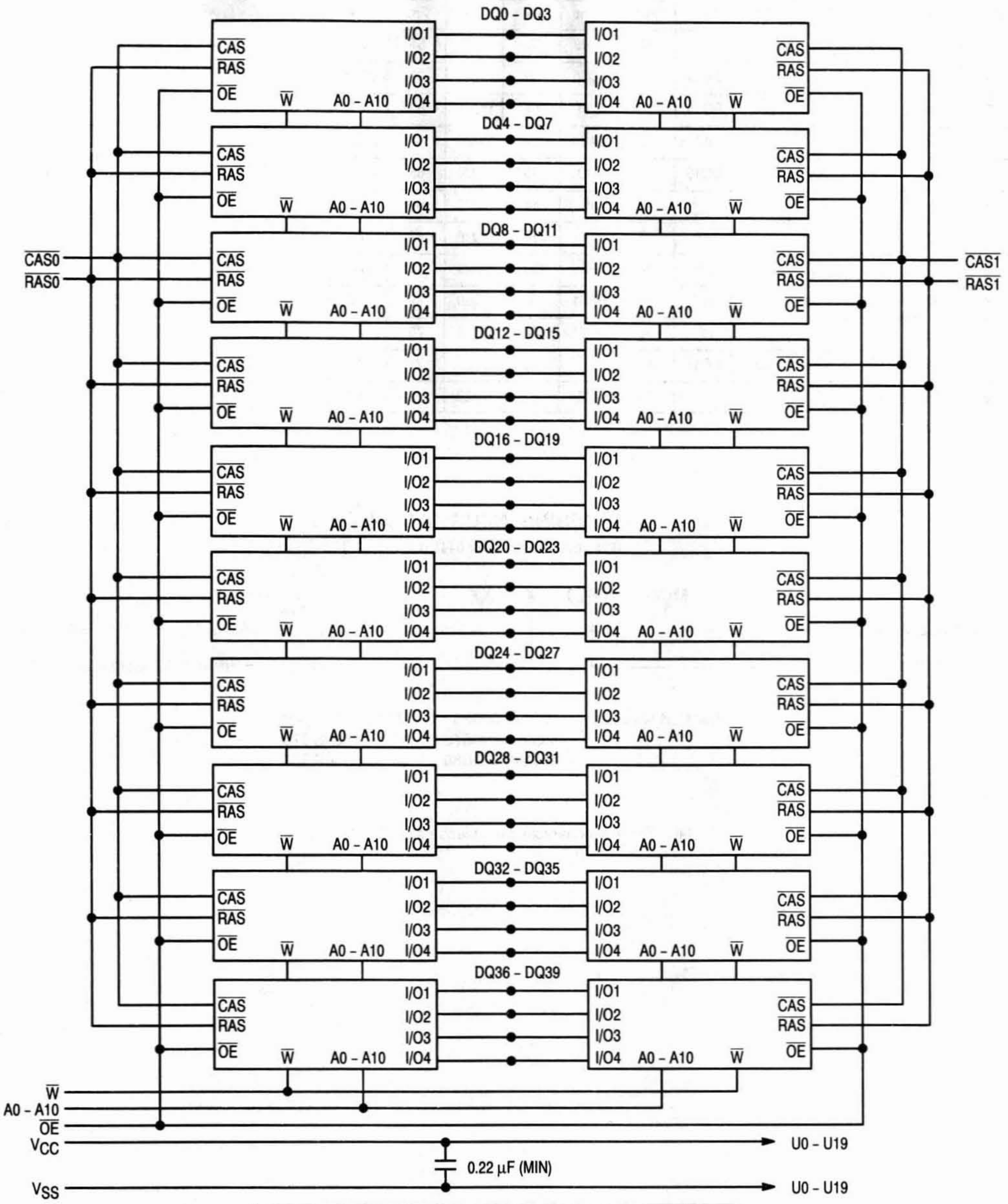


PIN NAMES			
A0 – A10	Address Inputs	DQ0 – DQ39	Data Input/Output
$\overline{\text{CAS0}}$, $\overline{\text{CAS1}}$	Column Address Strobe	PD1 – PD5	Presence Detect
$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$	Row Address Strobe	$\overline{\text{W}}$	Read/Write Input
$\overline{\text{X40}}$	Configuration Detection	$\overline{\text{OE}}$	Output Enable
V_{CC}	Power (+ 5 V)	V_{SS}	Ground
NC	No Connection		

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

8M x 40 BLOCK DIAGRAM


DQ0 - DQ3
DQ4 - DQ7
DQ8 - DQ11
DQ12 - DQ15
DQ16 - DQ19
DQ20 - DQ23
DQ24 - DQ27
DQ28 - DQ31
DQ32 - DQ35
DQ36 - DQ39
CAS
RAS
OE
W
A0 - A10
I/O1
I/O2
I/O3
I/O4
CAS0
RAS0
CAS1
RAS1
W
A0 - A10
OE
VCC
VSS
0.22 µF (MIN)
U0 - U19
U0 - U19

PRESENCE DETECT PIN OUT			
Pin Name	**60 ns**	**70 ns**	**80 ns**
PD1	NC	NC	NC
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}
PD5*	V_{SS}	V_{SS}	V_{SS}
$\overline{X40}$	V_{SS}	V_{SS}	V_{SS}

*PD5 tied to V_{SS} through a 2.6 kΩ resistor.

PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	A10	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{\text{OE}}$	31	A8	43	$\overline{\text{CAS1}}$	55	DQ28	67	PD1
8	DQ6	20	DQ8	32	A9	44	$\overline{\text{RAS0}}$	56	DQ29	68	PD2
9	DQ7	21	DQ9	33	NC	45	$\overline{\text{RAS1}}$	57	DQ30	69	PD3
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD4
11	PD5	23	DQ11	35	DQ17	47	$\overline{\text{W}}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	$\overline{\text{X40}}$	60	DQ32	72	V_{SS}

ORDERING INFORMATION
(Order by Full Part Number)

MCM 40800 X XX

Motorola Memory Prefix — MCM

Part Number — 40800

Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Package (S = SIMM, SG = Gold Pad SIMM) — X

Full Part Numbers — MCM40800S60 MCM40800SG60
MCM40800S70 MCM40800SG70
MCM40800S80 MCM40800SG80

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM72100

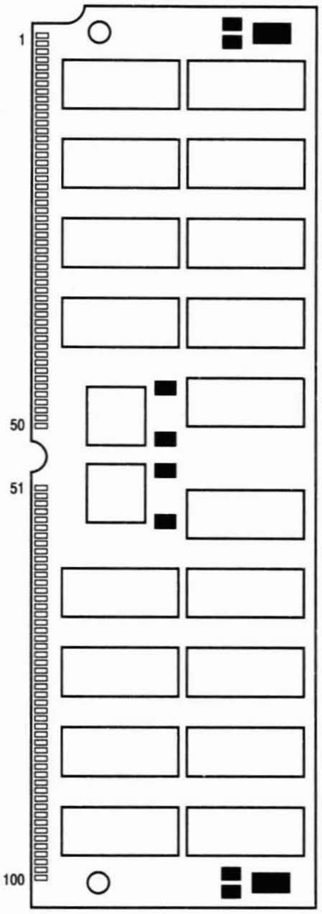
Product Preview

1M x 72 Bit Dynamic Random Access Memory Module

The MCM72100 is a dynamic random access memory (DRAM) module organized as 1,048,576 x 72 bits. The module is a 100-lead single-in-line memory module (SIMM) consisting of eighteen MCM54400AN DRAMs housed in 20/26 J-lead small outline packages (SOJ) and two SC63594FN buffers housed in 20-lead PLCC packages, mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM54400AN is a CMOS high-speed dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology. The SC63594FN is a 10-bit series terminated buffer/line driver with 20 ohm outputs.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  MCM72100 = 16 ms
- Consists of Eighteen 1M x 4 DRAMs, Two SC63594 FN Buffers, Two 10 µF (Min) Decoupling Capacitors, and Twenty-Two 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM72100-60 = 60 ns (Max)
  MCM72100-70 = 70 ns (Max)
  MCM72100-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM72100-60 = 12.98 W (Max)
  MCM72100-70 = 11.00 W (Max)
  MCM72100-80 = 9.52 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 130 W (Max)
  CMOS Levels = 120 W (Max)
- Gold-Plated 100-Pin Edge Connector

TOP VIEW

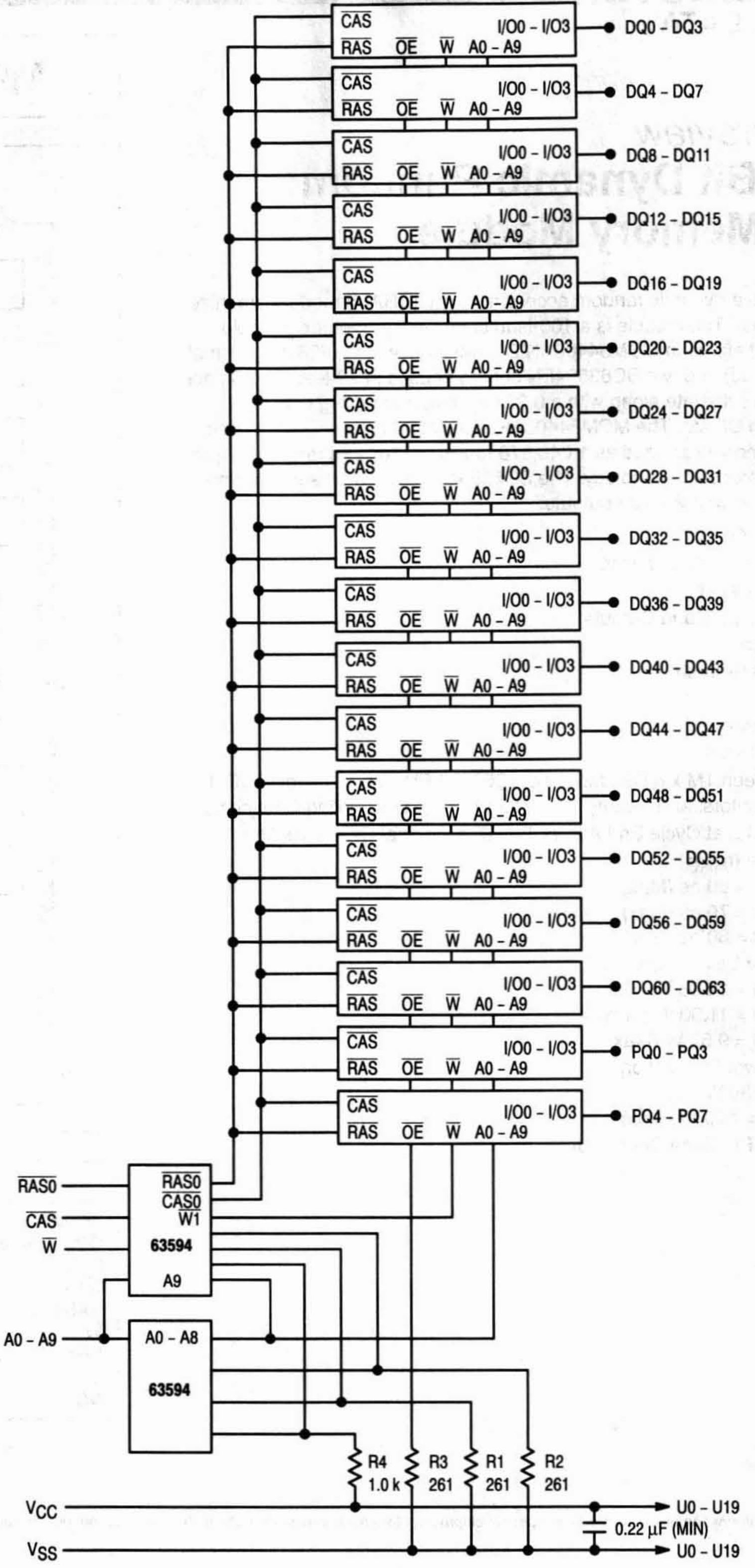


PIN NAMES

A0 – A9 .... Address Inputs
DQ0 – DQ63 .... Data Input/Output
PQ0 – PQ7 ..... Parity Data Input/Output
$\overline{\text{CAS}}$ .... Column Address Strobe
$\overline{\text{RAS0}}$ .... Row Address Strobe
$\overline{\text{W}}$ .... Read/Write Input
V_{CC} .... Power (+ 5 V)
V_{SS} .... Ground
NC .... No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

1M x 72 BLOCK DIAGRAM


CAS
RAS
OE
W
A0 – A9
I/O0 – I/O3
DQ0 – DQ3
DQ4 – DQ7
DQ8 – DQ11
DQ12 – DQ15
DQ16 – DQ19
DQ20 – DQ23
DQ24 – DQ27
DQ28 – DQ31
DQ32 – DQ35
DQ36 – DQ39
DQ40 – DQ43
DQ44 – DQ47
DQ48 – DQ51
DQ52 – DQ55
DQ56 – DQ59
DQ60 – DQ63
PQ0 – PQ3
PQ4 – PQ7
RAS0
CAS
W
RAS0
CAS0
W1
63594
A9
A0 – A9
A0 – A8
63594
R4
1.0 k
R3
261
R1
261
R2
261
VCC
VSS
0.22 µF (MIN)
U0 – U19
U0 – U19

PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DQ0	21	DQ10	41	A0	61	PQ4	81	DQ54
2	DQ1	22	DQ11	42	A1	62	PQ5	82	DQ55
3	DQ2	23	DQ12	43	V_{SS}	63	PQ6	83	V_{CC}
4	DQ3	24	DQ13	44	A2	64	PQ7	84	DQ24
5	DQ4	25	DQ14	45	A3	65	V_{CC}	85	DQ25
6	DQ5	26	DQ15	46	A4	66	DQ16	86	DQ26
7	DQ6	27	V_{SS}	47	A5	67	DQ17	87	DQ27
8	DQ7	28	DQ40	48	A6	68	DQ18	88	DQ28
9	V_{SS}	29	DQ41	49	A7	69	DQ19	89	DQ29
10	DQ32	30	DQ42	50	A8	70	DQ20	90	DQ30
11	DQ33	31	DQ43	51	V_{SS}	71	DQ21	91	DQ31
12	DQ34	32	DQ44	52	A9	72	DQ22	92	V_{SS}
13	DQ35	33	DQ45	53	NC	73	DQ23	93	DQ56
14	DQ36	34	DQ46	54	NC	74	V_{SS}	94	DQ57
15	DQ37	35	DQ47	55	NC	75	DQ48	95	DQ58
16	DQ38	36	V_{CC}	56	$\overline{W}$	76	DQ49	96	DQ59
17	DQ39	37	PQ0	57	$\overline{CAS}$	77	DQ50	97	DQ60
18	V_{CC}	38	PQ1	58	V_{SS}	78	DQ51	98	DQ61
19	DQ8	39	PQ2	59	$\overline{RAS0}$	79	DQ52	99	DQ62
20	DQ9	40	PQ3	60	NC	80	DQ53	100	DQ63

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

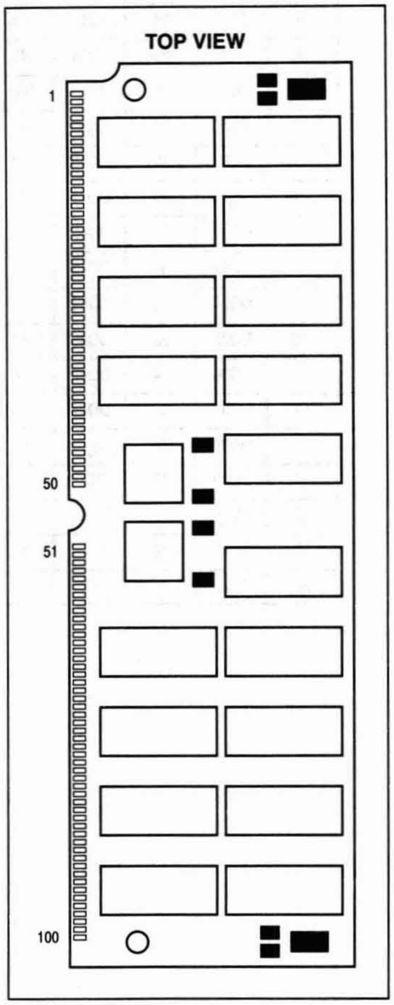
MCM72200

Product Preview

2M x 72 Bit Dynamic Random Access Memory Module

The MCM72200 is a dynamic random access memory (DRAM) module organized as 2,097,152 x 72 bits. The module is a 100-lead single-in-line memory module (SIMM) consisting of thirty-six MCM54400AN DRAMs housed in 20/26 J-lead small outline packages (SOJ) and four SC63594FN buffers housed in 20-lead PLCC packages, mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM54400AN is a CMOS high-speed dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology. The SC63594FN is a 10-bit series terminated buffer/line driver with 20 ohm outputs.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  MCM72200 = 16 ms
- Consists of Thirty-Six 1M x 4 DRAMs, Four SC63594FN Buffers, Two 10 µF (Min) Decoupling Capacitors, and Forty-Four 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM72200-60 = 60 ns (Max)
  MCM72200-70 = 70 ns (Max)
  MCM72200-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM72200-60 = 14.28 W (Max)
  MCM72200-70 = 12.30 W (Max)
  MCM72200-80 = 10.81 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 2.60 W (Max)
  CMOS Levels = 2.40 W (Max)
- Gold-Plated 100-Pin Edge Connector

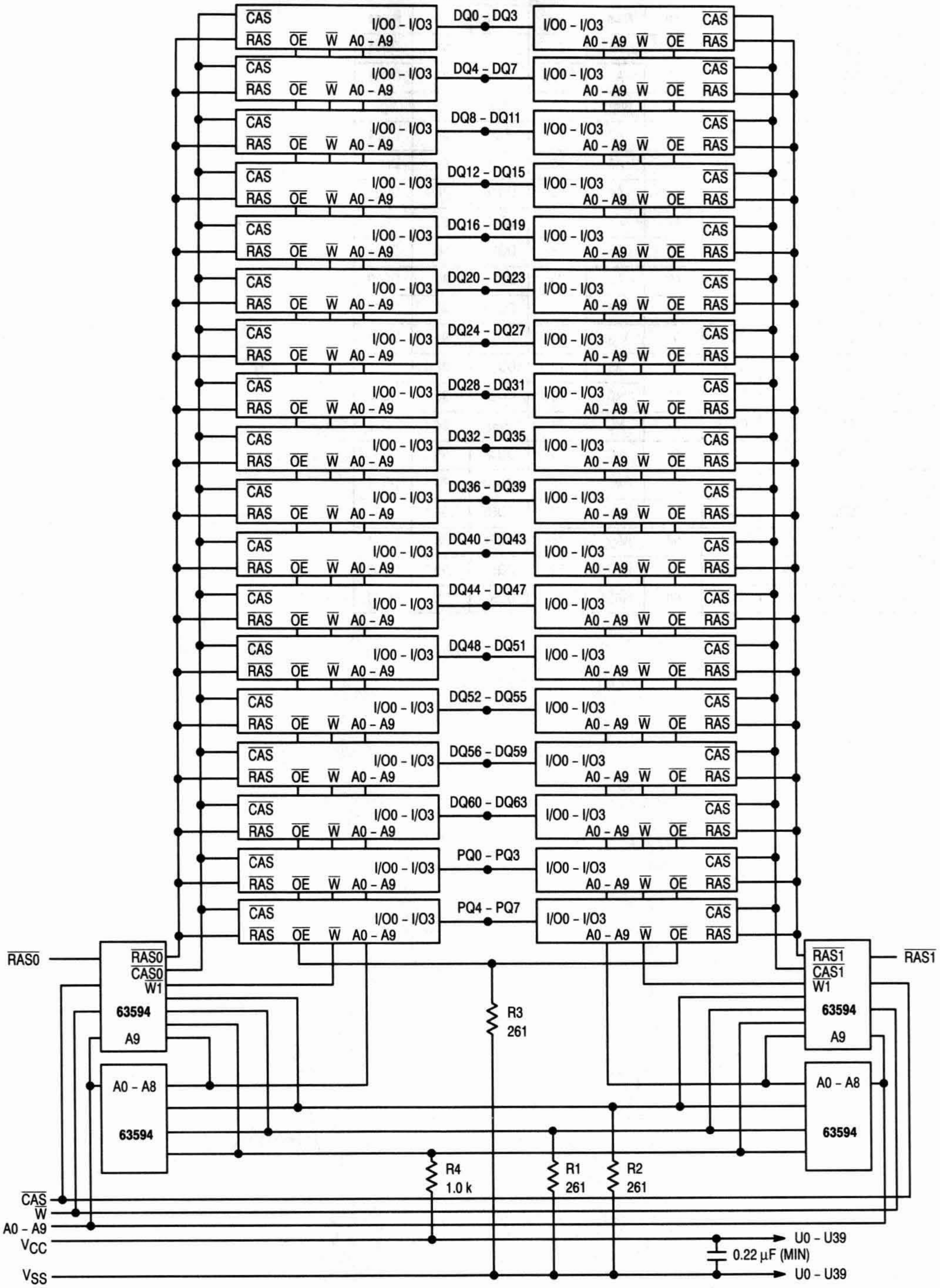


PIN NAMES

A0 – A9	Address Inputs
DQ0 – DQ63	Data Input/Output
PQ0 – PQ7	Parity Data Input/Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

2M x 72 BLOCK DIAGRAM


DQ0 – DQ3
DQ4 – DQ7
DQ8 – DQ11
DQ12 – DQ15
DQ16 – DQ19
DQ20 – DQ23
DQ24 – DQ27
DQ28 – DQ31
DQ32 – DQ35
DQ36 – DQ39
DQ40 – DQ43
DQ44 – DQ47
DQ48 – DQ51
DQ52 – DQ55
DQ56 – DQ59
DQ60 – DQ63
PQ0 – PQ3
PQ4 – PQ7
CAS
RAS
OE
W
A0 – A9
I/O0 – I/O3
RAS0
CAS0
W1
63594
A9
A0 – A8
RAS1
CAS1
R3
261
R4
1.0 k
R1
261
R2
261
CAS
W
A0 – A9
VCC
VSS
0.22 µF (MIN)
U0 – U39

PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DQ0	21	DQ10	41	A0	61	PQ4	81	DQ54
2	DQ1	22	DQ11	42	A1	62	PQ5	82	DQ55
3	DQ2	23	DQ12	43	V_{SS}	63	PQ6	83	V_{CC}
4	DQ3	24	DQ13	44	A2	64	PQ7	84	DQ24
5	DQ4	25	DQ14	45	A3	65	V_{CC}	85	DQ25
6	DQ5	26	DQ15	46	A4	66	DQ16	86	DQ26
7	DQ6	27	V_{SS}	47	A5	67	DQ17	87	DQ27
8	DQ7	28	DQ40	48	A6	68	DQ18	88	DQ28
9	V_{SS}	29	DQ41	49	A7	69	DQ19	89	DQ29
10	DQ32	30	DQ42	50	A8	70	DQ20	90	DQ30
11	DQ33	31	DQ43	51	V_{SS}	71	DQ21	91	DQ31
12	DQ34	32	DQ44	52	A9	72	DQ22	92	V_{SS}
13	DQ35	33	DQ45	53	NC	73	DQ23	93	DQ56
14	DQ36	34	DQ46	54	NC	74	V_{SS}	94	DQ57
15	DQ37	35	DQ47	55	NC	75	DQ48	95	DQ58
16	DQ38	36	V_{CC}	56	$\overline{W}$	76	DQ49	96	DQ59
17	DQ39	37	PQ0	57	$\overline{CAS}$	77	DQ50	97	DQ60
18	V_{CC}	38	PQ1	58	V_{SS}	78	DQ51	98	DQ61
19	DQ8	39	PQ2	59	$\overline{RAS0}$	79	DQ52	99	DQ62
20	DQ9	40	PQ3	60	$\overline{RAS1}$	80	DQ53	100	DQ63

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM72400

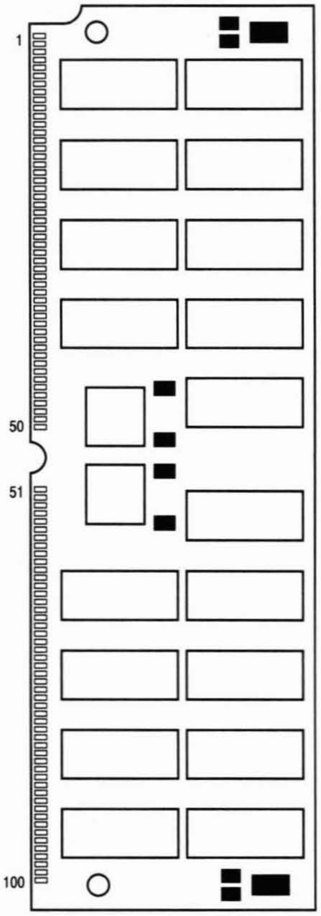
Product Preview

4M x 72 Bit Dynamic Random Access Memory Module

The MCM72400 is a dynamic random access memory (DRAM) module organized as 4,194,304 x 72 bits. The module is a 100-lead single-in-line memory module (SIMM) consisting of eighteen MCM517400 DRAMs housed in 24/28 J-lead small outline packages (SOJ) and two SC63594FN buffers housed in 20-lead PLCC packages, mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM517400 is a CMOS high-speed dynamic random access memory organized as 4,194,304 four-bit words and fabricated with CMOS silicon-gate process technology. The SC63594FN is a 10-bit series terminated buffer/line driver with 20 ohm outputs.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh: MCM72400 = 32 ms
- Consists of Eighteen 4M x 4 DRAMs, Two SC63594FN Buffers, Two 10 µF (Min) Decoupling Capacitors, and Twenty-Two 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM72400-60 = 60 ns (Max)
  - MCM72400-70 = 70 ns (Max)
  - MCM72400-80 = 80 ns (Max)
- Low Active Power Dissipation:
  - MCM72400-60 = 12.98 W (Max)
  - MCM72400-70 = 11.00 W (Max)
  - MCM72400-80 = 9.52 W (Max)
- Low Standby Power Dissipation:
  - TTL Levels = 1.30 W (Max)
  - CMOS Levels = 1.20 W (Max)
- Gold-Plated 100-Pin Edge Connector

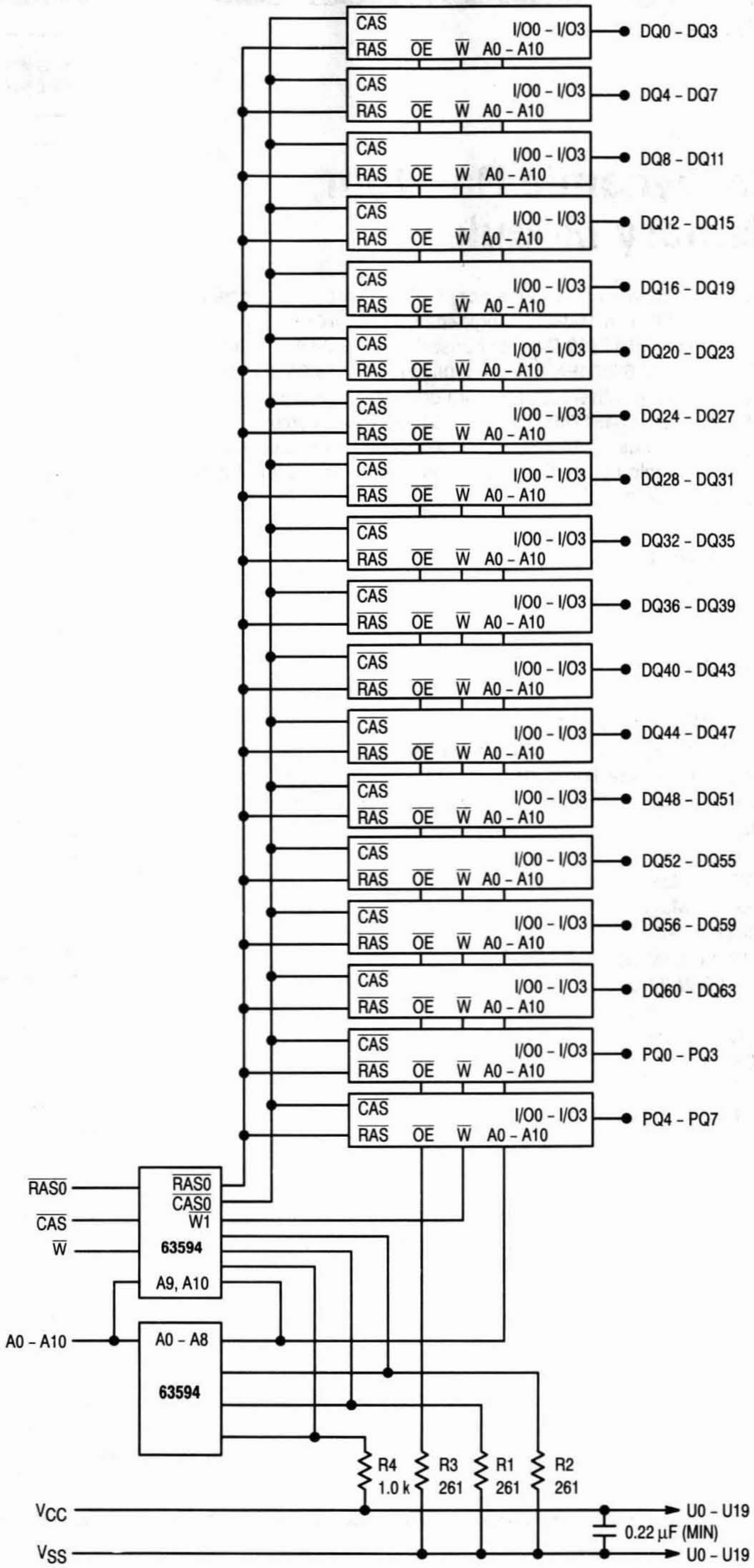
SG PACKAGE
SIMM MODULE
TOP VIEW



PIN NAMES	
A0 – A10	Address Inputs
DQ0 – DQ63	Data Input/Output
PQ0 – PQ7	Parity Data Input/Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{RAS0}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

4M x 72 BLOCK DIAGRAM


CAS
RAS
OE
W
A0 – A10
I/O0 – I/O3
DQ0 – DQ3
DQ4 – DQ7
DQ8 – DQ11
DQ12 – DQ15
DQ16 – DQ19
DQ20 – DQ23
DQ24 – DQ27
DQ28 – DQ31
DQ32 – DQ35
DQ36 – DQ39
DQ40 – DQ43
DQ44 – DQ47
DQ48 – DQ51
DQ52 – DQ55
DQ56 – DQ59
DQ60 – DQ63
PQ0 – PQ3
PQ4 – PQ7
RAS0
CAS
W
RAS0
CAS0
W1
63594
A9, A10
A0 – A10
A0 – A8
63594
R4 1.0 k
R3 261
R1 261
R2 261
VCC
VSS
0.22 µF (MIN)
U0 – U19
U0 – U19

PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DQ0	21	DQ10	41	A0	61	PQ4	81	DQ54
2	DQ1	22	DQ11	42	A1	62	PQ5	82	DQ55
3	DQ2	23	DQ12	43	V_{SS}	63	PQ6	83	V_{CC}
4	DQ3	24	DQ13	44	A2	64	PQ7	84	DQ24
5	DQ4	25	DQ14	45	A3	65	V_{CC}	85	DQ25
6	DQ5	26	DQ15	46	A4	66	DQ16	86	DQ26
7	DQ6	27	V_{SS}	47	A5	67	DQ17	87	DQ27
8	DQ7	28	DQ40	48	A6	68	DQ18	88	DQ28
9	V_{SS}	29	DQ41	49	A7	69	DQ19	89	DQ29
10	DQ32	30	DQ42	50	A8	70	DQ20	90	DQ30
11	DQ33	31	DQ43	51	V_{SS}	71	DQ21	91	DQ31
12	DQ34	32	DQ44	52	A9	72	DQ22	92	V_{SS}
13	DQ35	33	DQ45	53	A10	73	DQ23	93	DQ56
14	DQ36	34	DQ46	54	NC	74	V_{SS}	94	DQ57
15	DQ37	35	DQ47	55	NC	75	DQ48	95	DQ58
16	DQ38	36	V_{CC}	56	$\overline{W}$	76	DQ49	96	DQ59
17	DQ39	37	PQ0	57	$\overline{CAS}$	77	DQ50	97	DQ60
18	V_{CC}	38	PQ1	58	V_{SS}	78	DQ51	98	DQ61
19	DQ8	39	PQ2	59	$\overline{RAS0}$	79	DQ52	99	DQ62
20	DQ9	40	PQ3	60	NC	80	DQ53	100	DQ63

ORDERING INFORMATION
(Order by Full Part Number)

MCM 72400 X XX

Motorola Memory Prefix — MCM
Part Number — 72400
Package (SG = SIMM) — X
Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns) — XX

Full Part Numbers — MCM72400SG60
MCM72400SG70
MCM72400SG80

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM72800

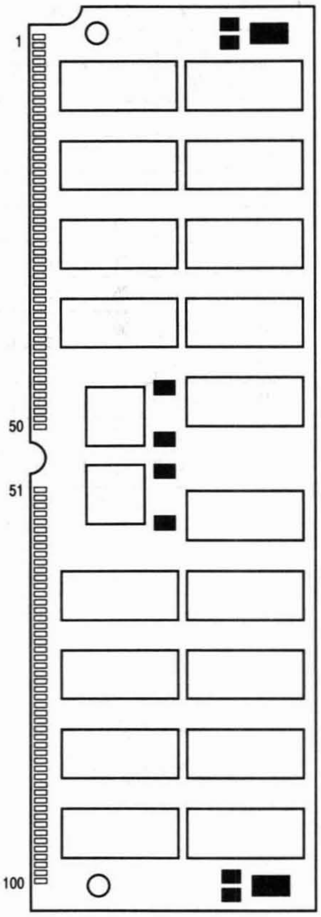
Product Preview

8M x 72 Bit Dynamic Random Access Memory Module

The MCM72800 is a dynamic random access memory (DRAM) module organized as 8,388,608 x 72 bits. The module is a double-sided 100-lead single-in-line memory module (SIMM) consisting of thirty-six MCM517400 DRAMs housed in 24/28 J-lead small outline packages (SOJ) and four SC63594FN buffers housed in 20-lead PLCC packages, mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM517400 is a CMOS high-speed dynamic random access memory organized as 4,194,304 four-bit words and fabricated with CMOS silicon-gate process technology. The SC63594FN is a 10-bit series terminated buffer/line driver with 20 ohm outputs.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh: MCM72800 = 32 ms
- Consists of Thirty-Six 4M x 4 DRAMs, Four SC63594FN Buffers, Two 10 µF (Min) Decoupling Capacitors, and Forty-Four 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM72800-60 = 60 ns (Max)
  - MCM72800-70 = 70 ns (Max)
  - MCM72800-80 = 80 ns (Max)
- Low Active Power Dissipation:
  - MCM72800-60 = 14.28 W (Max)
  - MCM72800-70 = 12.3 W (Max)
  - MCM72800-80 = 10.81 W (Max)
- Low Standby Power Dissipation:
  - TTL Levels = 2.60 W (Max)
  - CMOS Levels = 2.40 W (Max)
- Gold-Plated 100-Pin Edge Connector

SG PACKAGE
SIMM MODULE
TOP VIEW

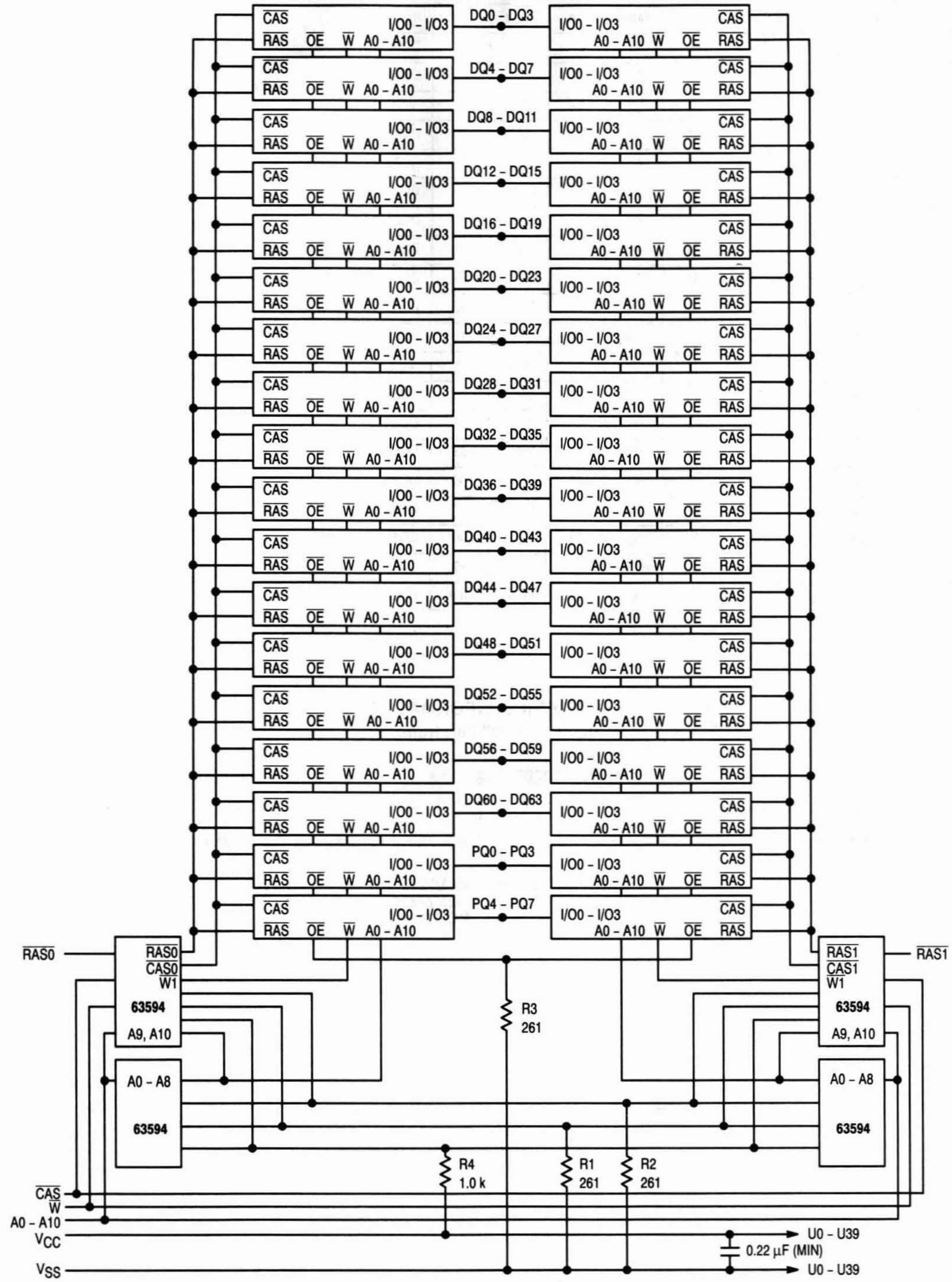


PIN NAMES

A0 – A10	Address Inputs
DQ0 – DQ63	Data Input/Output
PQ0 – PQ7	Parity Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS1}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

8M x 72 BLOCK DIAGRAM


CAS
RAS
OE
W
A0 – A10
I/O0 – I/O3
DQ0 – DQ3
DQ4 – DQ7
DQ8 – DQ11
DQ12 – DQ15
DQ16 – DQ19
DQ20 – DQ23
DQ24 – DQ27
DQ28 – DQ31
DQ32 – DQ35
DQ36 – DQ39
DQ40 – DQ43
DQ44 – DQ47
DQ48 – DQ51
DQ52 – DQ55
DQ56 – DQ59
DQ60 – DQ63
PQ0 – PQ3
PQ4 – PQ7
RAS0
RAS0
CAS0
W1
63594
A9, A10
A0 – A8
63594
RAS1
RAS1
CAS1
W1
63594
A9, A10
A0 – A8
63594
R3
261
R4
1.0 k
R1
261
R2
261
CAS
W
A0 – A10
VCC
VSS
U0 – U39
0.22 µF (MIN)
U0 – U39

PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DQ0	21	DQ10	41	A0	61	PQ4	81	DQ54
2	DQ1	22	DQ11	42	A1	62	PQ5	82	DQ55
3	DQ2	23	DQ12	43	V_{SS}	63	PQ6	83	V_{CC}
4	DQ3	24	DQ13	44	A2	64	PQ7	84	DQ24
5	DQ4	25	DQ14	45	A3	65	V_{CC}	85	DQ25
6	DQ5	26	DQ15	46	A4	66	DQ16	86	DQ26
7	DQ6	27	V_{SS}	47	A5	67	DQ17	87	DQ27
8	DQ7	28	DQ40	48	A6	68	DQ18	88	DQ28
9	V_{SS}	29	DQ41	49	A7	69	DQ19	89	DQ29
10	DQ32	30	DQ42	50	A8	70	DQ20	90	DQ30
11	DQ33	31	DQ43	51	V_{SS}	71	DQ21	91	DQ31
12	DQ34	32	DQ44	52	A9	72	DQ22	92	V_{SS}
13	DQ35	33	DQ45	53	A10	73	DQ23	93	DQ56
14	DQ36	34	DQ46	54	NC	74	V_{SS}	94	DQ57
15	DQ37	35	DQ47	55	NC	75	DQ48	95	DQ58
16	DQ38	36	V_{CC}	56	$\overline{W}$	76	DQ49	96	DQ59
17	DQ39	37	PQ0	57	$\overline{CAS}$	77	DQ50	97	DQ60
18	V_{CC}	38	PQ1	58	V_{SS}	78	DQ51	98	DQ61
19	DQ8	39	PQ2	59	$\overline{RAS0}$	79	DQ52	99	DQ62
20	DQ9	40	PQ3	60	$\overline{RAS1}$	80	DQ53	100	DQ63

ORDERING INFORMATION
(Order by Full Part Number)

MCM 72800 X XX

Motorola Memory Prefix
Part Number
Speed (60 = 60 ns, 70 = 70 ns, 80 = 80 ns)
Package (SG = SIMM)

Full Part Numbers — MCM72800SG60
MCM72800SG70
MCM72800SG80

General Memory Devices

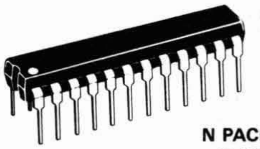
6

MCM2018A **6-3**
MCM2814 .... **6-8**
MCM60L256A-C **6-23**
MCM60L256A-V **6-31**

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM2018A

Fast 16K Bit Static RAM



N PACKAGE
PLASTIC
CASE 724

The MCM2018A is a 16,384 bit static random access memory organized as 2048 words by 8 bits, fabricated using Motorola's high-performance silicon-gate MOS (HMOS) technology. It uses an innovative design approach which combines the ease-of-use features of fully static operation (no external clocks or timing strobes required) with the reduced standby power dissipation associated with clocked memories. To the user this means low standby power dissipation without the need for address setup and hold times, nor reduced data rates due to cycle times that are longer than access times. Perfect for cache and sub-100 ns buffer memory systems, this high speed static RAM is intended for applications that demand superior performance and reliability.

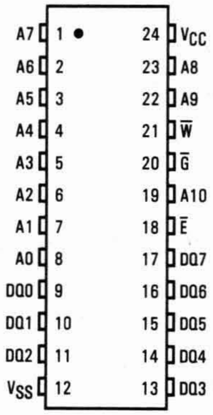
Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature provides significant system-level power savings.

The MCM2018A is in a 24-pin dual-in-line 300 mil wide package with the industry standard JEDEC approved pinout.

- Single +5 V Operation, ±10%
- Fully Static: No Clock or Timing Strobe Required
- Fast Access Time: MCM2018A-35 = 35 ns (Maximum)
  MCM2018A-45 = 45 ns (Maximum)
- Power Supply Current: 135 mA Maximum (Active)
  20 mA Maximum (Standby)
- Three-State Output

NOT RECOMMENDED
FOR NEW DESIGNS

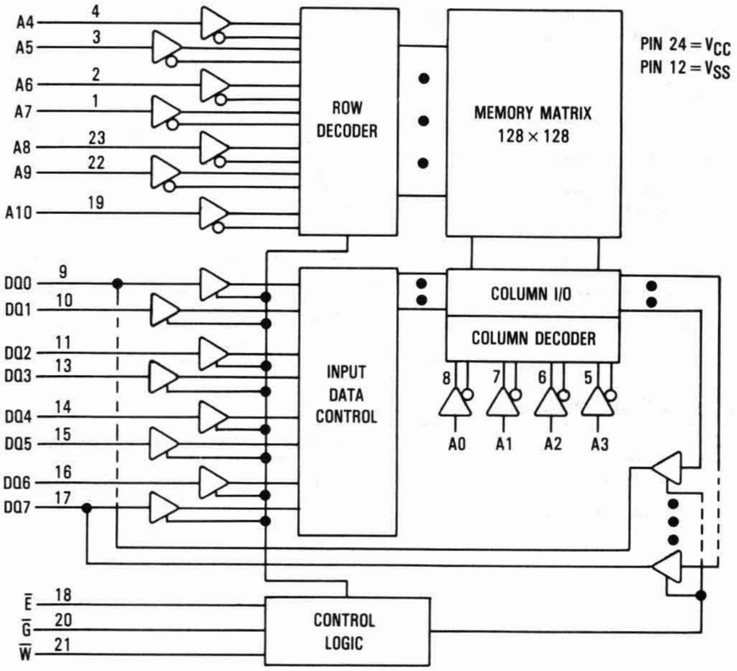
PIN ASSIGNMENT


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
DQ0 9
DQ1 10
DQ2 11
VSS 12
24 VCC
23 A8
22 A9
21 W̄
20 Ḡ
19 A10
18 Ē
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3

PIN NAMES

A0-A10	Address Input
DQ0-DQ7	Data Input/Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM


A4 4
A5 3
A6 2
A7 1
A8 23
A9 22
A10 19
ROW DECODER
MEMORY MATRIX 128 × 128
PIN 24 = VCC
PIN 12 = VSS
DQ0 9
DQ1 10
DQ2 11
DQ3 13
DQ4 14
DQ5 15
DQ6 16
DQ7 17
INPUT DATA CONTROL
COLUMN I/O
COLUMN DECODER
8 7 6 5
A0 A1 A2 A3
Ē 18
Ḡ 20
W̄ 21
CONTROL LOGIC

MODE SELECTION

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	V_{CC} Current	DQ
Standby	H	X	X	I_{SB}	High Z
Read	L	L	H	I_{CC}	Q
Write Cycle	L	X	L	I_{CC}	D

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage on Any Pin With Respect to V_{SS}	V_{in}, V_{out}	−0.5 to +7.0	V
DC Output Current	I_{out}	±20	mA
Power Dissipation	P_D	1.1	Watt
Temperature Under Bias	T_{bias}	−10 to +80	°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.0	3.0	6.0	V
	V_{IL}	−0.5*	0	0.8	V

*The device will withstand undershoots to the −2.5 volt level with a maximum pulse width of 50 ns. This is periodically sampled rather than 100% tested.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{CC} = 5.5 V, V_{in} = GND to V_{CC})	$I_{lkg(I)}$	−1.0	1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC})	$I_{lkg(O)}$	−1.0	1.0	μA
Operating Power Supply Current ($\overline{E}$ = V_{IL}, $I_{I/O}$ = 0 mA)	I_{CC}	—	135	mA
Standby Power Supply Current ($\overline{E}$ = V_{IH})	I_{SB}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$ and DQ	C_{in}	3	5	pF
	$\overline{E}$		5	7	
I/O Capacitance	DQ	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}=5$ V ±10%, $T_A=0$ to +70°C, Unless Otherwise Noted)

Input Pulse Levels	0 and 3.0 V	Input and Output Timing Measurement Reference Levels	1.5 V
Input Rise and Fall Times	5 ns	Output Load	See Figure 1

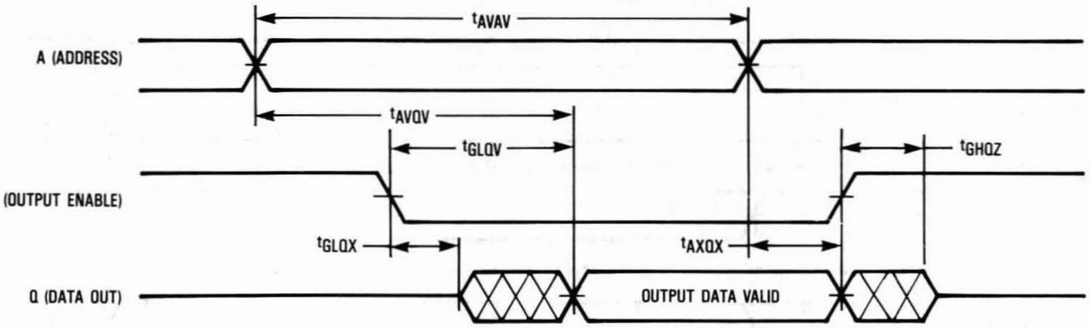
READ CYCLE (See Note 1)

Parameter	Symbol		MCM2018A-35		MCM2018A-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Address Valid to Address Valid (Read Cycle Time)	t_{AVAV}	t_{RC}	35	–	45	–	ns	
Address Valid to Output Valid (Address Access Time)	t_{AVQV}	t_{AC}	–	35	–	45	ns	
Chip Enable Low to Chip Enable High (Read Cycle Time)	t_{ELEH}	t_{RC}	35	–	45	–	ns	
Chip Enable Low to Output Valid (Chip Enable Access Time)	t_{ELQV}	t_{ACS}	–	35	–	45	ns	
Output Enable Low to Output Valid (Output Enable Access Time)	t_{GLQV}	t_{OE}	–	20	–	20	ns	
Chip Enable Low to Output Invalid (Chip Enable to Output Active)	t_{ELQX}	t_{CLZ}	5	–	5	–	ns	2
Chip Enable High to Output High Z (Chip Disable to Output Disable)	t_{EHQZ}	t_{CHZ}	0	20	0	20	ns	2
Output Enable Low to Output Invalid (Output Enable to Output Active)	t_{GLQX}	t_{OLZ}	0	–	0	–	ns	2
Output Enable High to Output High Z (Output Disable to Output Disable)	t_{GHQZ}	t_{OHZ}	0	20	0	20	ns	2
Address Invalid to Output Invalid (Output Hold Time)	t_{AXQX}	t_{OH}	5	–	5	–	ns	
Chip Enable Low to Power Up	t_{ELICCH}	t_{PU}	0	–	0	–	ns	
Chip Enable High to Power Down	t_{EHICCL}	t_{PD}	–	20	–	20	ns	

NOTES:

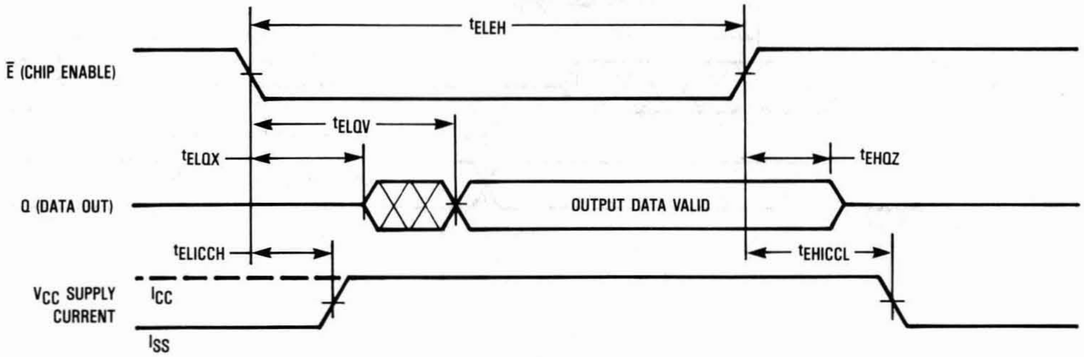
1. Transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IL} and V_{IH} (or between V_{IH} and V_{IL}) in a monotonic manner.
2. Transition is measured ±200 mV from the steady state output voltage with the output loading specified in Figure 1.
3. In read cycle 2, all addresses are valid prior to or coincident with chip enable ($\overline{E}$) transition low.

READ CYCLE 1 ($\overline{W}=V_{IH}$, $\overline{E}=V_{IL}$)



t_{AVAV}
A (ADDRESS)
t_{AVQV}
t_{GLQV}
t_{GHQZ}
$\overline{G}$ (OUTPUT ENABLE)
t_{GLQX}
t_{AXQX}
Q (DATA OUT)
OUTPUT DATA VALID

READ CYCLE 2 ($\overline{W}=V_{IH}$, $\overline{G}=V_{IL}$; See Note 3 Above)



t_{ELEH}
$\overline{E}$ (CHIP ENABLE)
t_{ELQV}
t_{ELQX}
t_{EHQZ}
Q (DATA OUT)
OUTPUT DATA VALID
t_{ELICCH}
t_{EHICCL}
V_{CC} SUPPLY CURRENT
I_{CC}
I_{SS}

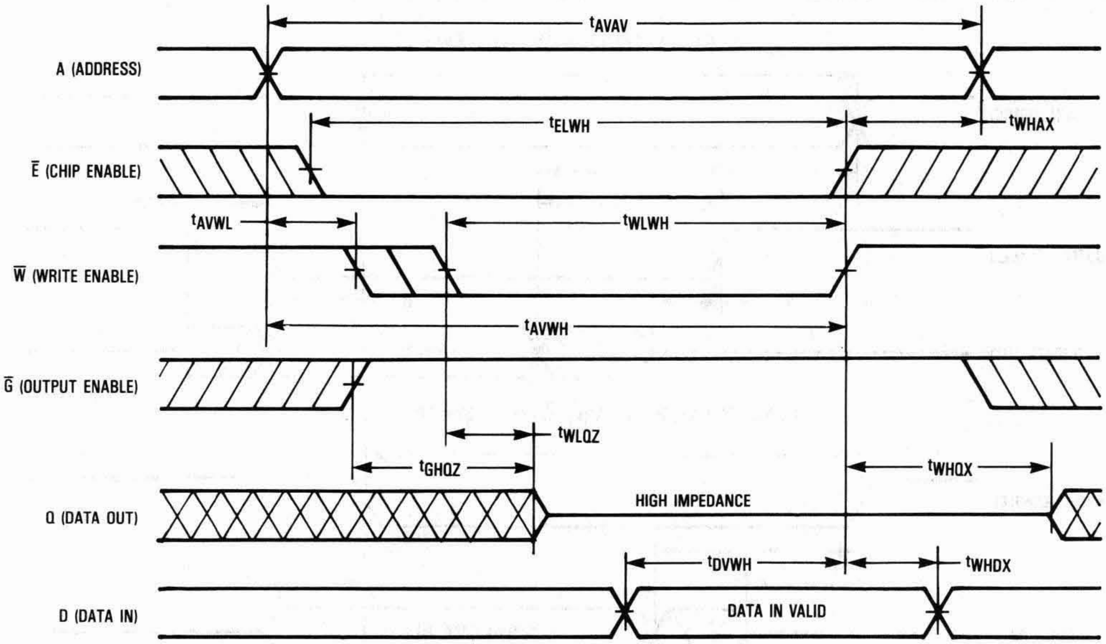
WRITE CYCLE (See Notes 1 and 2)

Parameter	Symbol		MCM2018A-35		MCM2018A-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Address Valid to Address Valid (Write Cycle Time)	t_{AVAV}	t_{WC}	35	—	45	—	ns	
Chip Enable Low to Write High (Chip Enable to End of Write)	t_{ELWH}	t_{EW}	30	—	40	—	ns	
Address Valid to Chip Enable Low (Address Setup to Chip Enable)	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to Write Low (Address Setup to Write)	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to Write High	t_{AVWH}	t_{AW}	30	—	40	—	ns	3
Write Low to Write High (Write Pulse Width)	t_{WLWH}	t_{WP}	30	—	35	—	ns	
Write High to Address Don't Care (Address Hold After End of Write)	t_{WHAX}	t_{WR}	0	—	0	—	ns	4
Write High to Output Don't Care (Output Active After End of Write)	t_{WHQX}	t_{WLZ}	0	—	0	—	ns	5
Write Low to Output High Z (Write Enable to Output Disable)	t_{WLQZ}	t_{WHZ}	0	20	0	20	ns	5
Data Valid to Write High (Data Setup to End of Write)	t_{DVWH}	t_{DS}	15	—	20	—	ns	3
Write High to Data Don't Care (Data Hold After End of Write)	t_{WHDX}	t_{DH}	0	—	0	—	ns	3, 5
Output Enable High to Output High Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	ns	

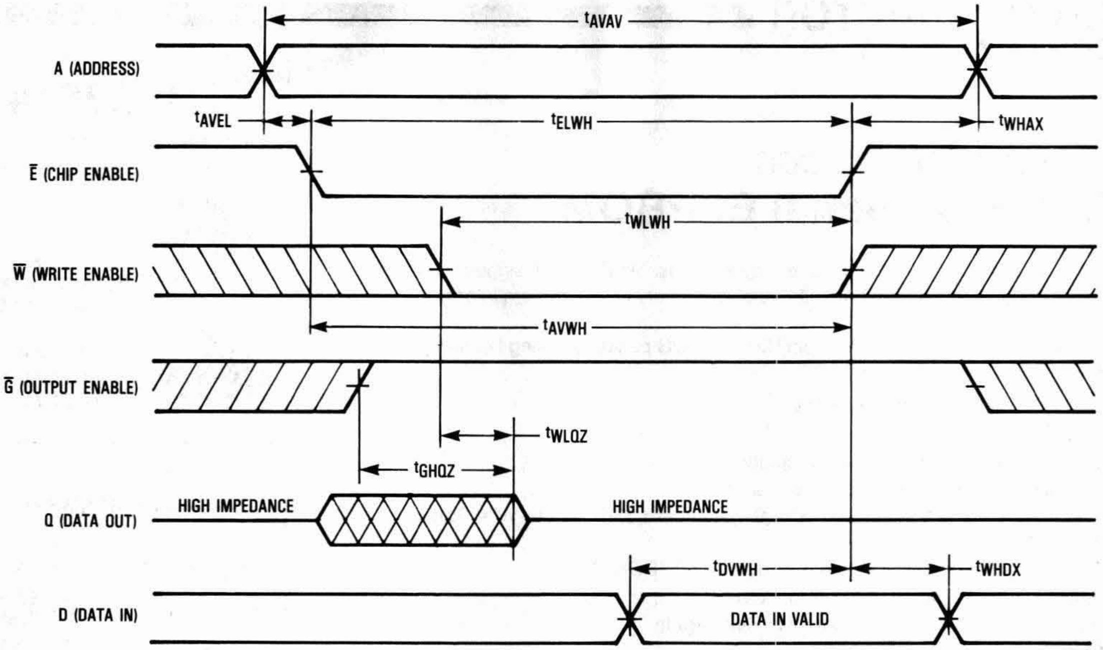
NOTES:

1. Write enable ($\overline{W}$) must be high during all address transitions.
2. If the chip enable ($\overline{E}$) low transition occurs simultaneously with the write enable ($\overline{W}$) transition, the output remains in a high impedance state.
3. Both chip enable ($\overline{E}$) and write enable ($\overline{W}$) must be active (low) to write data into the memory. Either signal can terminate the write cycle by going high. Data in setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
4. t_{WHAX} is measured from the earlier of, chip enable ($\overline{E}$) or write enable ($\overline{W}$) going high to the end of write cycle.
5. Output enable ($\overline{G}$) can be either low or high during a write cycle. If chip enable ($\overline{E}$) and $\overline{G}$ are both low during this period then the data input/output (DQ) pins are in the output state. Under these conditions input signals of opposite phase to the outputs must not be applied.

WRITE CYCLE 1 ($\overline{W}$ Controlled)



WRITE CYCLE 2 ($\overline{E}$ Controlled)


tAVAV
A (ADDRESS)
tAVEL
tELWH
tWHAX
Ē (CHIP ENABLE)
tWLWH
W̄ (WRITE ENABLE)
tAVWH
Ḡ (OUTPUT ENABLE)
tWLQZ
tGHQZ
HIGH IMPEDANCE
HIGH IMPEDANCE
Q (DATA OUT)
tDVWH
tWHDX
D (DATA IN)
DATA IN VALID

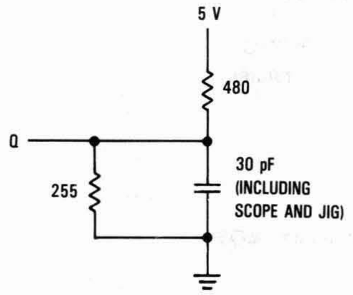

5 V
480
Q
255
30 pF
(INCLUDING
SCOPE AND JIG)

Figure 1. Output Load

ORDERING INFORMATION
(Order by Full Part Number)

MCM 2018A X XX

Motorola Memory Prefix — MCM
Part Number — 2018A
Package (N = 300-mil Plastic) — X
Speed (35 = 35 ns, 45 = 45 ns) — XX

Full Part Numbers—MCM2018AN35
MCM2018AN45

NOTE: For mechanical data, please see Chapter 10.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM2814

Advance Information

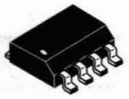
256 x 8 Bit Serial EEPROM

The MCM2814 is a 2048-bit serial electrically erasable PROM designed for handling data in applications requiring both non-volatile memory and in-system information updates.

The MCM2814 is fabricated in 8-pin DIP and SOG packages using floating-gate HCMOS EEPROM technology.

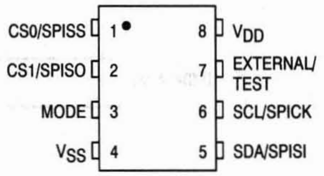
- 2048 Bits Organized as 256 Bytes
- Byte Programmable
- 3 V – 6 V Supply During Read Operations
- On-Chip Programming Voltage Generator
- Two Programming Modes: Two-Wire Serial Access, M-Bus/Four-Wire Serial Access SPI
- Data Protection of 1/4, 1/2, or 3/4 Array with EEPROM Bits
- Simultaneous Programming of 1 to 4 Bytes
- Automatic Byte Address Increment in Read Mode
- Chip Selection with Separate Pin
- Single 3 V to 6 V Supply During Programming
- Digital Filtering on Clock and Data Inputs
- Bit Program Operation: No Byte Erase Necessary
- Data Protection After Reset
- Write/Erase Endurance: 10,000 Cycles over 0 to 70°C
- Typically 100,000 W/E Cycles at Ambient Temperatures
- Data Retention: 10 Years

P SUFFIX
PLASTIC PACKAGE
CASE 626-04



G SUFFIX
PLASTIC PACKAGE
CASE 751-03

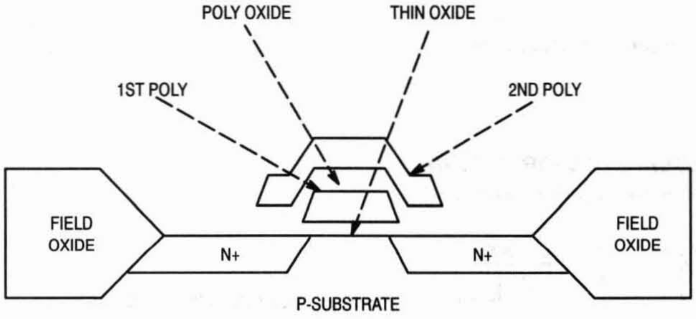
PIN ASSIGNMENT



PIN NAMES

V_{DD}	Power Supply
V_{SS}	Ground (Ref)
External/Test	Connected to On-Chip Voltage Multiplier Output
M-BUS MODE	
CS0	Chip Select (Hardwired)
CS1	Chip Select (Hardwired)
SDA	Serial Data I/O
SCL	Serial Clock Input
SPI MODE	
SPISS	Slave Select Input
SPISO	Serial Data Output
SPISI	Serial Data Input
SPICK	Serial Clock Input

FETMOS
(Floating-Gate Electron Tunnelling MOS)



IIC is a trademark of Philips.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

1. PIN DESCRIPTION

1.1 V_{SS}/V_{DD} (Pins 4/8)

V_{DD} and V_{SS} are used to power the circuit. In read mode this supply voltage must be comprised in the V_{DDR} range. (See **5.2 Electrical Characteristics**). In program mode this supply range is limited to V_{DDP}.

1.2 EXTERNAL/TEST (Pin 7)

This pin is used for testing the on-chip voltage multiplier that generates the programming voltage required for a program operation, and should be left open for 5 V only operation.

As this on-chip generator has a high impedance, an external supply can be connected to this pin. This also allows to block any inadvertent programming by maintaining this pin at V_{DD}.

1.3 MODE (Pin 3)

This pin is used to select one of two modes of operation: M-bus mode at the low logic level or SPI mode at high level.

This pin is usually hardwired to V_{SS} or V_{DD}. It should only be changed if the circuit is internally in a standby state. This pin is high impedance when V_{DD} is at V_{SS} level.

1.4 CS1/SPISO (Pin 2)

In M-bus mode, this pin is used for selecting multiple identical chips on the same serial bus. The chip address is formed by 5 bits predefined for this chip, followed by 2 additional chip select bits. These last two bits must correspond to the CS1/CS0 code for proper chip selection. Up to four MCM2814s can be connected on the same SCL and SDA lines. (See Figure 4.)

In SPI mode, this pin is a push-pull slave data output (SPISO). It will shift-out byte addresses and data as described in Section 4.

This pin is usually connected to the data input pin of a SPI master (MISO).

This pin can not be pulled higher than 0.5 V above V_{DD}, even if V_{DD} is at V_{SS} level.

1.5 CS0/SPISS (Pin 1)

In M-bus mode, this pin is used in conjunction with CS1 for chip selection. (See above.)

In SPI mode, this pin is a Slave Select input. In this mode the serial access is deselected when the SPISS input is high, and the SPISO data output pin is forced high impedance. Multiple chips using the same SPICK, SPISI, and SPISO lines, can be selected via this pin as described in Figure 10.

After powering up the device, a falling edge of the SPISS line is required to start the SPI serial access.

This pin is high impedance when V_{DD} is at V_{SS} level.

1.6 SCL/SPICK (Pin 6)

The serial clock is supplied on pin SCL/SPICK. This pin is an input only; therefore, the chip can only operate as a slave under the control of a serial bus master.

The clock input rising edge is used to shift in data present on the SDA/SPISI pin, and the falling edge is used to shift out data on the SDA or SPISO pin.

This pin is high impedance when V_{DD} is at V_{SS} level.

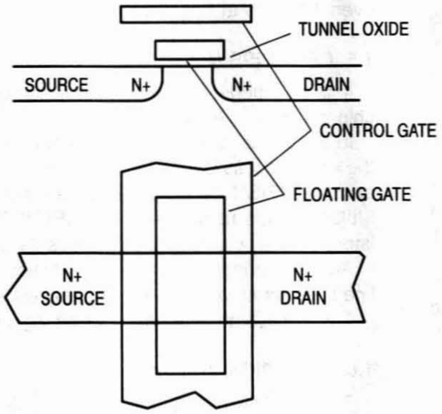
1.7 SDA/SPISI (Pin 5)

In M-bus mode, SDA pin is used to transmit data serially in the memory (Receiver) or from the memory (Transmitter). Data transmitted via this pin includes chip addresses, byte addresses, byte data, Read/Write, and acknowledge bits. When SDA is in output, it operates as a pull-down only device (Open-drain). The protocol of this transmission is described in Figures 5 and 6.

In SPI mode, this pin is a Slave data input (SPISI) only and is used to receive opcodes, byte addresses, and byte data. It is usually connected to the data output pin of a SPI master (MOSI).

This pin is high impedance when V_{DD} is at V_{SS} level.

2. EEPROM



	CG	D	S
READ	0 V	V_{DD}	0 V
PROG 1	0 V	V_{PP}	OPEN
PROG 0	V_{PP}	0 V	0 V

Figure 2. EEPROM Transistor

256 Bytes of EEPROM memory are implemented in a floating gate double poly-silicon process. A Byte Address register is used to select one of the bytes. Three basic states of operation can be distinguished:

- Standby state
- Read state
- Program state

2.1 EEPROM OPERATION

2.1.1 Standby State

In this state, neither a programming, nor a serial transmission occurs, and the power consumption is minimum. (See 3.4.1 and 4.5.)

2.1.2 Read State

In read state, the data of the selected byte is transferred from the memory array to the data shift register used for the serial transmission. This state is active during a serial transmission.

2.1.3 Program State

In this state, a programming voltage higher than V_{DD} is necessary. This voltage is generated by the on-chip voltage multiplier or can be supplied externally. During programming, V_{DD} must be within the V_{DDP} range. (See 5.2)

In M-bus mode, the programming starts at the end of a write command, when a STOP or a new START condition occurs. The programming is enabled at this time, as well as the on-chip voltage multiplier. If there is a capacitive load on the V_{PP} pin, the V_{PP} rise time should be added to the minimum program time t_{PROG}.

In SPI mode, programming could start when a write serial transmission is ended with an SPISS rising edge. Actual programming will happen only if enabled by a V_{PP} enable serial command. This command can be transmitted before or after the write sequence.

2.2 EEPROM DATA PROTECTION

Some circuitry has been included to prevent unwanted modification of EEPROM data, and is described below. However, a noisy serial link is very often the cause of bad data or data written to the wrong address. Besides measures to reduce this noise on the board, the serial clock and data inputs (SCL/SDA) have Schmitt triggers and digital filters to reject some of the noise.

2.2.1 Power Up Reset

Immediately after power is applied, programming is inhibited to prevent EEPROM data loss during the system power up.

In both modes, this condition is removed when a READ is performed.

In M-bus mode, this condition is removed by reading the data in any byte address using the normal read sequence.

In SPI mode, it is sufficient to send the READ opcode before a new V_{PP} enable command and the write sequence.

At Reset the following circuitry is initialized:

- The circuit is in standby state
- In M-bus mode, it is waiting for a start condition
- In SPI mode, it is waiting for a high to low SPISS transition
- The data outputs are high impedance (SDA, SPISO)
- The programming is disabled
- The on-chip V_{PP} generator is off

2.2.2 Programming Voltage Enable

In SPI mode only, an internal programming voltage enable flip-flop can be set or cleared with two separate opcodes, thus reducing the risk of unwanted EEPROM programming.

2.2.3 Array Write Protect

In both modes, byte address 255 ($FF) contains EEPROM bits with a special function. When one or two bits of this address are programmed at once, the programming of EEPROM sections is inhibited according to Table 1.

Table 1. EEPROM Write Protect

Data at ADDR $FF		Protected Addresses	No. of Bytes Protected
XXXX	00XX	No Write Prot.	—
XXXX	01XX	$C0 – $FB	60
XXXX	10XX	$80 – $FB	124
XXXX	11XX	$40 – $FB	188

This protection is reversible as address 255 ($FF) can be modified at any time.

2.3 EEPROM PROPERTIES

NO ERASE: Unlike most EEPROMs, it is not necessary to erase a byte before writing new data.

The program operation takes t_{PROG} and must be externally timed.

CUMULATIVE: As the programming operation is under external control, it can be done at once or at various time frames as long as the total programming time exceeds the specified minimum t_{PROG} value.

t_{PROG} is defined with V_{PP} at its programming level.

SELF LIMITING: Excess programming has no positive effect, as programmed EEPROM thresholds will asymptotically reach their nominal values. Programming durations above the recommended maximum t_{PROG} have negative impacts on the EEPROM programming endurance.

2.4 EEPROM RELIABILITY

Reliability figures are statistical in nature; therefore, no minimum or maximum specifications can be applied. The result of reliability tests will be published instead. These tests are conducted on a regular basis during the production life of a circuit and reports are available upon request.

2.4.1 Data Retention

Typical data retention should exceed 10 years for the specified operating temperature range. Data retention is usually tested with the device under bias, but without accessing the EEPROM array.

2.4.2 Read Stress

Unlike some non-volatile memories, there should be no disturbance of the stored data under continuous read of EEPROM bytes. The life limit under continuous read condition should therefore be similar to the normal operating life of the device.

2.4.3 Program Endurance

As for all EEPROMs, there is a wearout mechanism associated with the programming mechanism on the nonvolatile memory. More than 10,000 programming cycles should be possible per memory bit; additionally, 100,000 cycles is typical for the specified temperature range. A programming cycle is defined as a 0 to 1 to 0 programming. Unlike most EEPROMs where the whole byte is erased before being reprogrammed, if just one bit is modified in a byte, only this bit will see the programming stress.

Some endurance experiments have shown that the number of programming cycles can be increased if the V_{PP} rise time is increased. This can be achieved with an external capacitor on V_{PP} when the on-chip V_{PP} generator is used. In SPI mode, the V_{PP} should be enabled after the write command has been transmitted. If an external V_{PP} is provided, it should be ramped up only after the write command is transmitted. In this case, a V_{PP} above the maximum value also has a negative impact on the endurance.

2.5 V_{PP} VOLTAGE MULTIPLIER

In M-bus mode, the on-chip V_{PP} generator is turned on or off automatically during a program sequence.

In SPI mode, it is switched on only after a serial V_{PP} enable command has been issued, independently of write or read commands.

3. M-BUS OPERATING MODE

This MODE pin can be hardwired to V_{DD} or V_{SS} to select two different modes of operation. Differences are at the serial transmission level and in the EEPROM operation. They are called M-bus mode and SPI mode.

3.1 M-BUS MODE

Only two wires are needed to control the device operation. The serial transmission of this mode is similar to the IIC™ serial communication standard. It features:

- Up to 4 identical chips on the same 2 wire bus
- CS1/CS0 pins for chip selection
- SCL clock line, input only
- SDA line used as Input and Output
- Data acknowledge bit generated
- Auto programming after reception of new data
- Programming time under external control
- Write inhibit after reset

3.2 LEXICON

This lexicon will describe some terms used in this serial interface description.

MASTER: The device that initiates the serial transmission is designated as master. In general, it is the device generating the clock. This memory can never function as a master.

SLAVE: This memory always operates as a slave.

TRANSMITTER: The device with its SDA pin in output is a data transmitter. In the case of multiple devices in output, the device sending a low level will win due to the Open-Drain connection.

RECEIVER: A device that has been properly selected by a chip address followed by a write bit is a receiver, and will shift data present on the SDA pin in internal registers.

MSB: The Most Significant Bit is the first bit transmitted and received.

START CONDITION: The start condition is defined as a 1 to 0 transition of SDA when SCL is high. The first byte of data following a start condition includes the chip address followed by the Read/Write bit. All devices connected on the same bus receive this data to check if they are addressed.

STOP CONDITION: The stop condition is defined as a 0 to 1 transition of SDA when SCL is high. In this circuit, the stop condition is never mandatory. An EEPROM programming can be initiated by the STOP or also by any following START condition.

A STOP after a serial read sequence will put the device in standby state.

CHIP ADDRESS: The first byte transmitted after a START contains the chip address followed by the Read/Write bit. The 7 bit chip address is formed of 5 fixed bits followed by 2 chip select bits.

Fixed bits are 1010X for this device (X is a don't care bit). The 2 chip select bits must correspond to the 2 chip select inputs for proper chip selection. By this means, up to 4 identical chips can be connected on the same SDA/SCL lines, in order to form a memory bank of up to 8 KBits.

READ/WRITE BIT: The 8th bit transmitted by the master after the 7 bit chip address will indicate the direction of transfer for the next bytes (until a new start or stop). If low, the following bytes are transmitted by the master. If high, the following bytes are transmitted by the MCM2814.

BYTE ADDRESS: The first byte of data received by the memory after the chip address, will be latched in the byte address register and is used to select one of the 256 EEPROM bytes.

ACKNOWLEDGE BIT: This bit is sent by the selected receiver on the data line after a byte reception. Due to the open drain structure, a valid acknowledge bit corresponds to a low level. While operating as a transmitter, sending a sequence of data bits, this device will check the acknowledge bit generated by the master. The absence of this bit will stop the transmission of data.

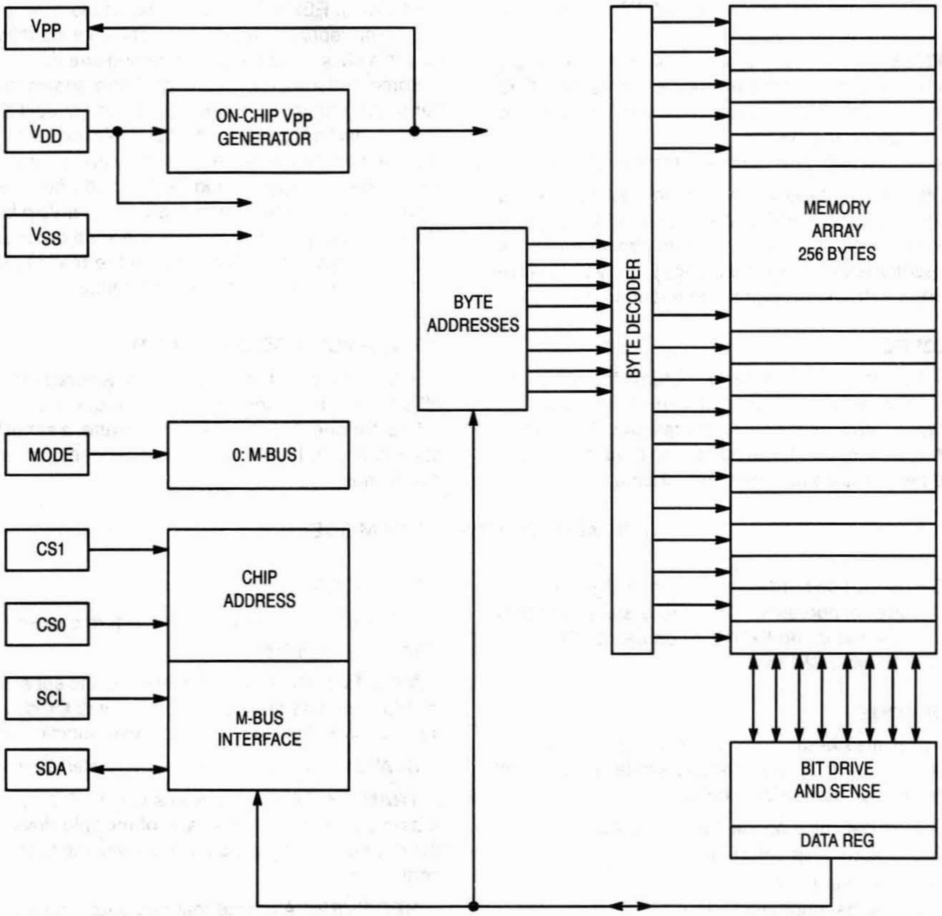
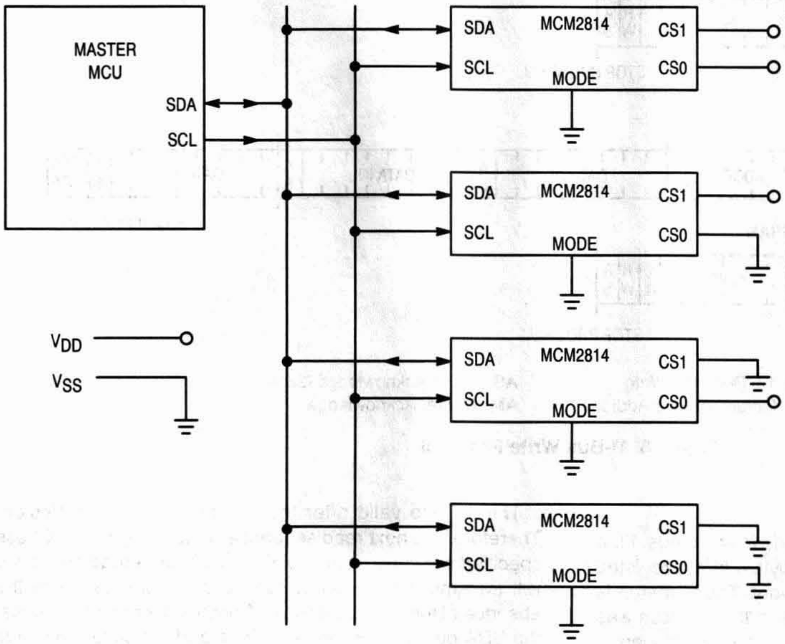


Figure 3. M-Bus Block Diagram

3.3 CHIP SELECTION

The two chip select bits transmitted in the chip address must match the status of CS1 and CS0 inputs.



PIN STATUS			CHIP ADDRESS
MODE	CS1	CS0	TRANSMITTED
0	1	1	1010 X11
0	1	0	1010 X10
0	0	1	1010 X01
0	0	0	1010 X00

Figure 4. M-Bus Chip Selection

3.4 PROTOCOL

At the protocol level, the transmission of data is defined in the form of sequences of Start (STA), Stop (STO) conditions, and bytes followed by acknowledge bits.

3.4.1 Standby State

When no serial transmission and no programming are made, the circuit is in standby. A STOP condition following a read sequence or a write byte address sequence (without data write), will put the circuit in standby. A new START condition will wake up the device, to get the chip address. If the chip address is not valid, the device will return to standby.

The power consumption is minimum in standby.

3.4.2 Write Sequence

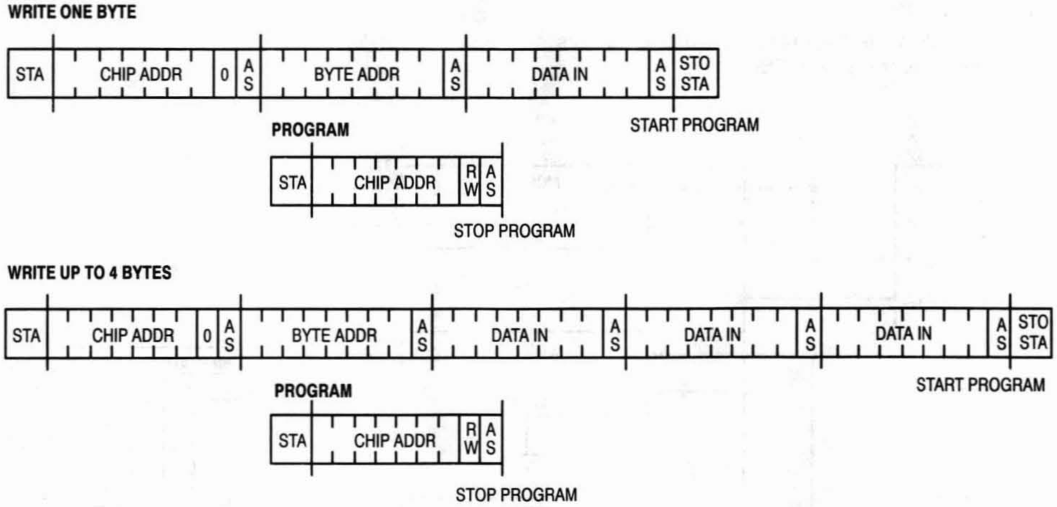
The serial write to the memory includes a serial transmission of the byte address and the data to be written. When this is completed by a stop or a new start condition, the programming sequence is initiated.

Programming is under control of the master. It is initiated by the write sequence just described, and stopped by any new valid selection of the chip. Therefore, the t_{PROG} time is defined as the time between these two operations, and is defined by the master.

Bad chip addresses or chip addresses for other chips on the same bus do not suspend the programming.

The on-chip V_{PP} generator is automatically turned on or off when needed. If an external V_{PP} is applied, the programming voltage is only allowed into the array during the above defined t_{PROG} time.

It is possible to program simultaneously up to 4 bytes, provided the 6 most significant bits of their addresses are identical. The byte address is incremented after each new data byte shifted in.


WRITE ONE BYTE
STA
CHIP ADDR
0
A S
BYTE ADDR
A S
DATA IN
A S
STO STA
PROGRAM
START PROGRAM
STA
CHIP ADDR
R W
A S
STOP PROGRAM
WRITE UP TO 4 BYTES
STA
CHIP ADDR
0
A S
BYTE ADDR
A S
DATA IN
A S
DATA IN
A S
DATA IN
A S
STO STA
PROGRAM
START PROGRAM
STA
CHIP ADDR
R W
A S
STOP PROGRAM

STA: Start Condition
STO: Stop Condition

R/W Bit: 1 = Read/0 = Write
INC: Increment Byte Address

AS: Slave Acknowledge (2814)
AM: Master Acknowledge

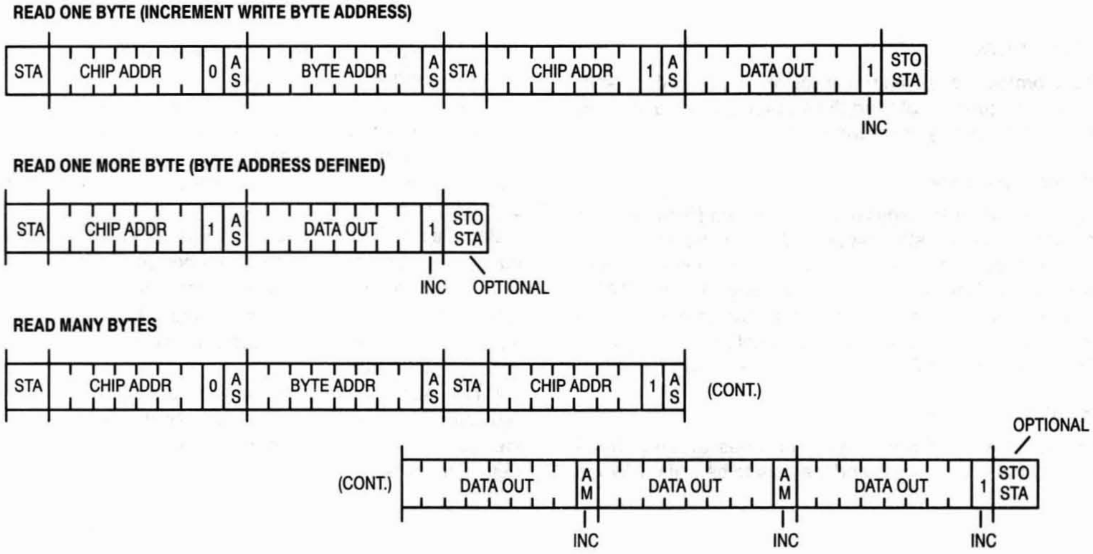
Figure 5. M-Bus Write Protocol

3.4.3 Read Sequence

Reading data from the memory is made in two steps. First the byte address must be loaded in the byte address register. Then data can be read out of the memory. The first step is only required to define the byte address. If this address was predefined from a previous read, this step can be skipped.

The byte address is automatically incremented after each-data byte transmitted.

This is also valid after the last byte of a transmission. Therefore, the next read sequence without any byte address specified will transmit data of the next byte. A read sequence will transmit data bytes of successive addresses until the absence of the acknowledge bit from the master. In this case, the SDA output driver will switch off and the circuit will go to standby.


READ ONE BYTE (INCREMENT WRITE BYTE ADDRESS)
STA
CHIP ADDR
0
A S
BYTE ADDR
A S
STA
CHIP ADDR
1
A S
DATA OUT
1
STO STA
INC
READ ONE MORE BYTE (BYTE ADDRESS DEFINED)
STA
CHIP ADDR
1
A S
DATA OUT
1
STO STA
INC
OPTIONAL
READ MANY BYTES
STA
CHIP ADDR
0
A S
BYTE ADDR
A S
STA
CHIP ADDR
1
A S
(CONT.)
OPTIONAL
(CONT.)
DATA OUT
A M
DATA OUT
A M
DATA OUT
1
STO STA
INC
INC
INC

STA: Start Condition
STO: Stop Condition

R/W Bit: 1 = Read/0 = Write
INC: Increment Byte Address

AS: Slave Acknowledge (2814)
AM: Master Acknowledge

Figure 6. M-Bus Read Protocol

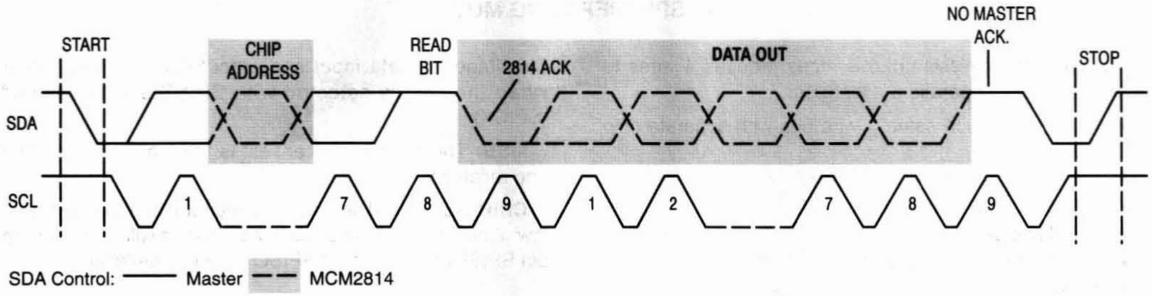

NO MASTER ACK.
START
CHIP ADDRESS
READ BIT
2814 ACK
DATA OUT
STOP
SDA
SCL
1
7
8
9
1
2
7
8
9
SDA Control:
Master
MCM2814

Figure 7. M-Bus Read Detail

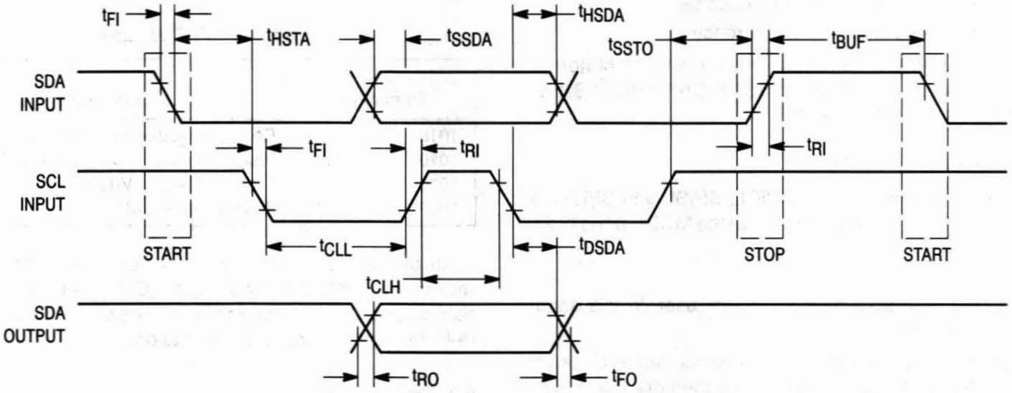

t_{FI}
t_{HSTA}
t_{SSDA}
t_{HSDA}
t_{SSTO}
t_{BUF}
SDA INPUT
t_{FI}
t_{RI}
t_{RI}
SCL INPUT
START
t_{CLL}
t_{DSDA}
STOP
START
t_{CLH}
SDA OUTPUT
t_{RO}
t_{FO}

Figure 8. M-Bus Timings

3.4.4 Signal Levels

Electrical and switching characteristics are described in Section 5.

During a trasmission, SDA line transitions must occur when SCL is low. A negative transition of SDA with SCL high is recognized as a START condition, the positive transition as a STOP condition.

The acknowledge bit is provided by the device receiving data. Therefore, during this time the data transmitter must leave the SDA line at high impedance.

As this memory has an open drain SDA output, an external pull-up resistor to V_{DD} should be included on SDA line.

4. SPI OPERATING MODE

The serial transmission of this mode requires 4 wires to control the device operation. It features:

- Multiple chips on same 3 wire bus with separate chip select lines
- SPISS chip selection
- SPICK clock line, input only
- SPISI line used as input only
- SPISO line used as output only
- No acknowledge bit
- Programming under control of the master via serial opcodes
- Programming time under external control
- Write inhibit after reset
- Write enable/disable via serial opcodes
- Byte address output for transparency

This SPI mode can be used with the SPI of Motorola Microprocessor MC6805S2/S3, MC6805K2/L3/L8, MC68HC05C4, and MC68HC11.

4.1 SPI SERIAL INTERFACE

The serial interface via pins SPICL, SPISI, and SPISO is compatible with the SPI standard when the MODE pin is high.

4.2 LEXICON

This lexicon will describe some terms used in this serial interface description.

MASTER: The device that generates the serial clock on SPICK is designated as master. This memory can never function as a master.

SLAVE: This memory always operates as a slave as the SPICK pin is always an input.

TRANSMITTER/RECEIVER: This device has separate pins for data transmission (SPISO) and reception (SPISI).

Simultaneous data input and output can therefore occur when the chip is selected with SPISS and is clocked (SPICK).

MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin SPISS is low. When the chip is not selected, no data will be input from pin SPISI, and output pin SPISO is high impedance.

4.3 SERIAL OP-CODE

The first byte transmitted after the chip is selected with SPISS going low, contains the opcode that defines the operation to be performed.

Table 2. SPI Opcodes

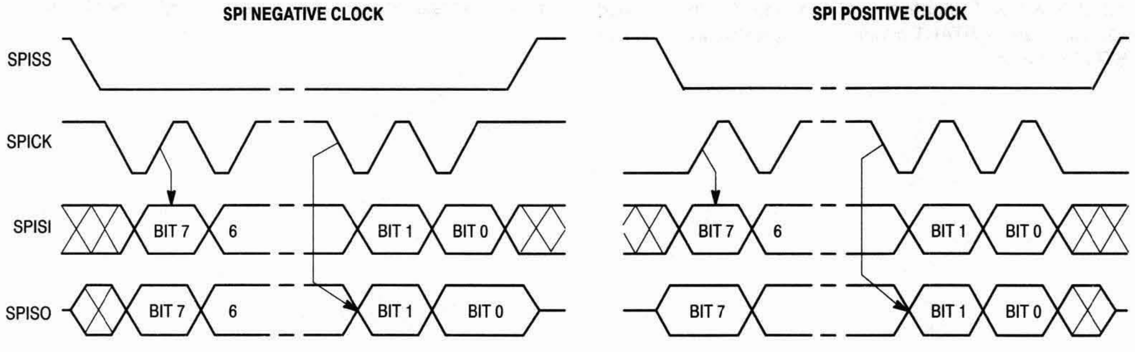
Data Transmitted		Operation
1010	0111	Read byte address followed by data
1010	0110	Program enable, V_{PP} generator ON.
1010	0100	Program disable, V_{PP} generator OFF.
1010	0010	Write (Program) data.

All other codes are invalid. After an invalid code is received, no data is shifted in the MCM2814 and the SPISO data output is high impedance until a new SPISS falling edge re-initializes the serial communication.

4.4 PROTOCOL

The MCM2814 SPI interface accepts both a negative or positive clock.

The SPI protocol for this device defines the bytes transmitted on the SPISI and SPISO data lines for proper chip operation.



Positive Clock Edge: Shift IN
Negative Clock Edge: Data OUT

Figure 9. SPI Clock Phase and Polarity

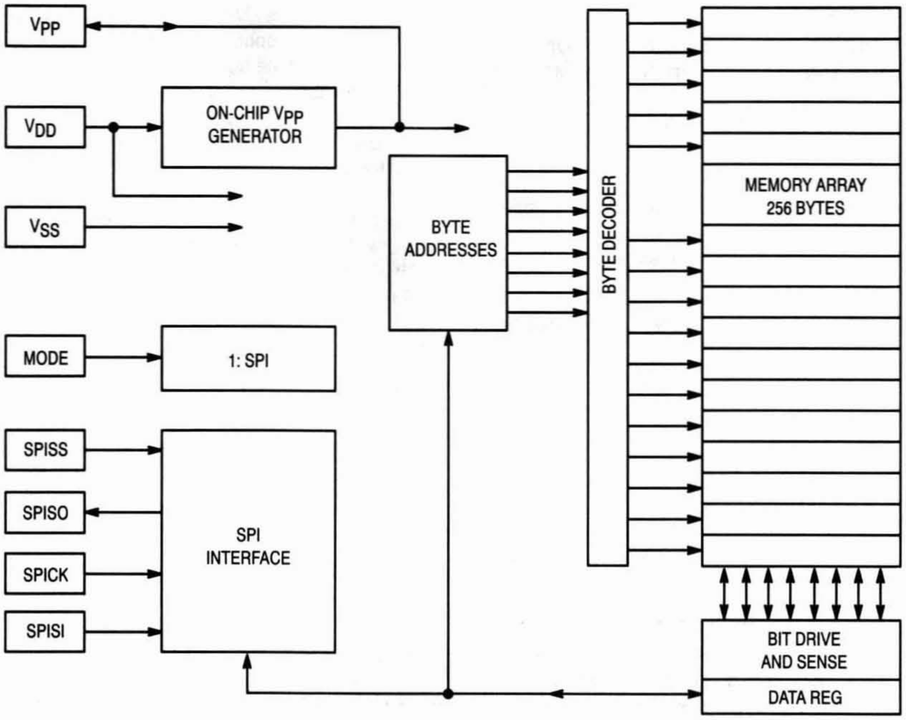

VPP
VDD
VSS
ON-CHIP VPP GENERATOR
BYTE ADDRESSES
BYTE DECODER
MEMORY ARRAY 256 BYTES
MODE
1: SPI
SPISS
SPISO
SPICK
SPISI
SPI INTERFACE
BIT DRIVE AND SENSE
DATA REG

Figure 10. SPI Block Diagram

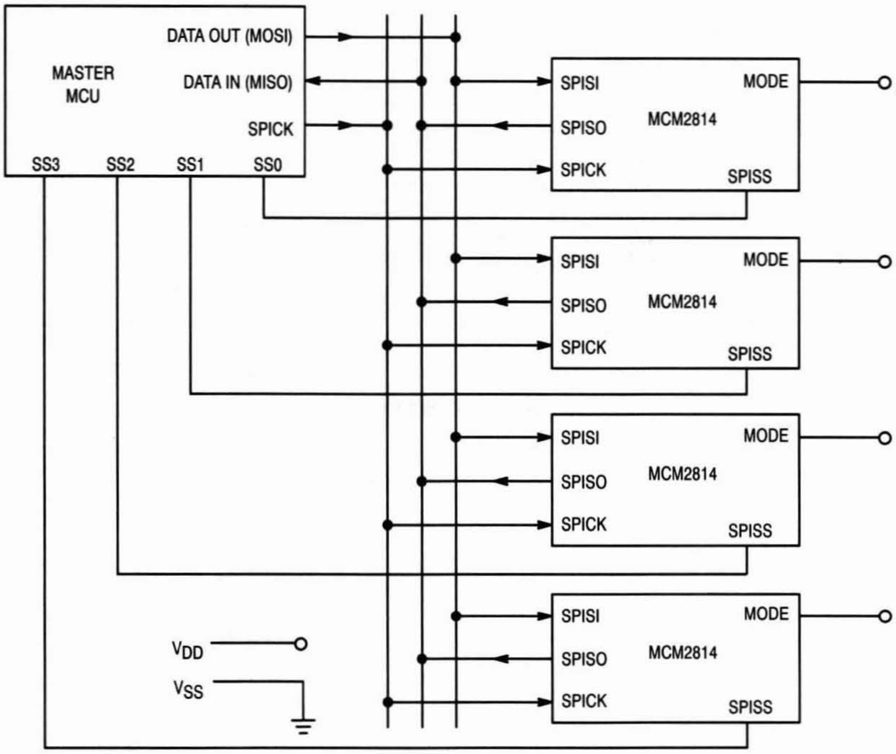

MASTER MCU
DATA OUT (MOSI)
DATA IN (MISO)
SPICK
SS3
SS2
SS1
SS0
SPISI
SPISO
SPICK
MODE
MCM2814
SPISS
VDD
VSS

Figure 11. SPI Chip Selection

4.5 STANDBY STATE

The circuit is in standby when no serial transmission takes place, when no write is waiting for the V_{PP} enable command and when the V_{PP} generator is off.

When SPISS is high, standby state will follow:

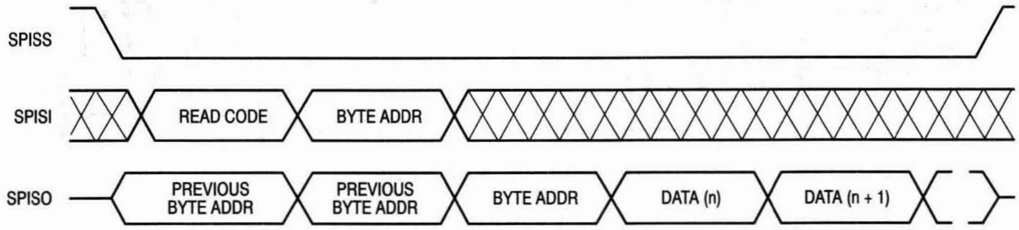
- A power up reset
- A V_{PP} disable command
- A Read, providing no V_{PP} enable command has been issued previously

The power consumption is minimum in standby.

4.6 READ SEQUENCE

Reading the memory via the serial SPI link requires the following sequence. The SPISS line is pulled low to select the device. The read opcode is transmitted on the the SPISI line followed by the byte address. When this is done, data on the SPISI line has no more influence on the memory. At the beginning of an SPI transaction, the SPISO buffer is turned on and will shift out the current byte address. This can be used for a relative addressing of the byte address. The new byte address is then transmitted followed by corresponding data. If just one byte is read, SPISS can be pulled back to the high level. It is possible to continue the read sequence, as the byte address is automatically incremented. The byte address is shifted out only once, in the beginning of a transmission.

READ ONE OR MORE BYTES


SPISS
SPISI
READ CODE
BYTE ADDR
SPISO
PREVIOUS BYTE ADDR
PREVIOUS BYTE ADDR
BYTE ADDR
DATA (n)
DATA (n + 1)

INVALID OPCODES

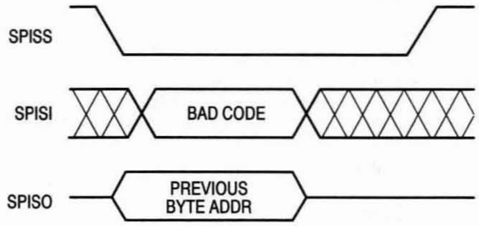

SPISS
SPISI
BAD CODE
SPISO
PREVIOUS BYTE ADDR

Figure 12. SPI Read

4.7 PROGRAM SEQUENCE

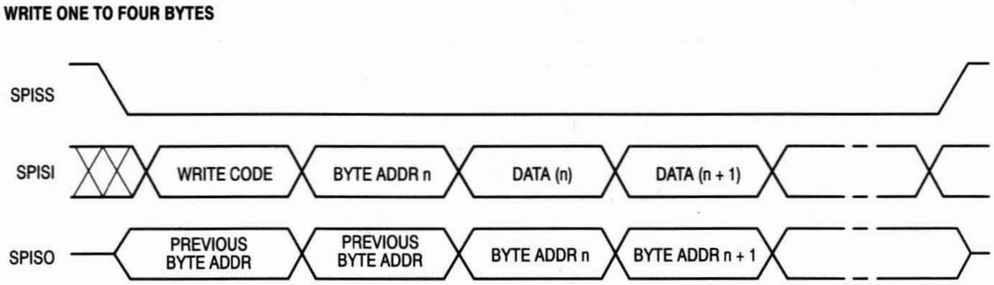
To program a byte, two separate conditions must be simultaneously present. The program must be enabled via the Vpp enable command, and a serial write must be done. The Vpp enable will also turn on the on-chip Vpp generator. At this time, the chip is obviously not in standby, even if SPISS is high. The program disable command will stop the on-chip Vpp supply and protect the EEPROM data against unwanted modifications. An external Vpp supply will also be internally enabled or disabled by this mechanism.

A write serial sequence includes an SPISS high to low transition, followed by the write code on the SPISI line. The byte address followed by the corresponding data to be written are then shifted through the SPISI pin. At the beginning of an SPI transaction, the SPISO buffer is turned on and will shift out the current byte address. This can be used for a relative addressing of the byte to be programmed. The new byte address is also echoed for possible checking by the master. If Vpp is enabled, the programming will start after the SPISS line goes back to a high level. It is also possible to issue the Vpp enable command after the write sequence.

If the Vpp enable command is issued after the serial write, no read or invalid code should be transmitted in between, as this would clear the programming latch containing the data to be programmed.

The programming is suspended when a new chip selection with SPISS low occurs. It is then possible to send a new write command to program new data. A Vpp enable or a read command will stop the programming.

It is possible to program simultaneously up to 4 bytes, provided the 6 most significant bits of their addresses are identical. The byte address is incremented after each new data byte shifted in.


WRITE ONE TO FOUR BYTES
SPISS
SPISI
WRITE CODE
BYTE ADDR n
DATA (n)
DATA (n + 1)
SPISO
PREVIOUS BYTE ADDR
PREVIOUS BYTE ADDR
BYTE ADDR n
BYTE ADDR n + 1

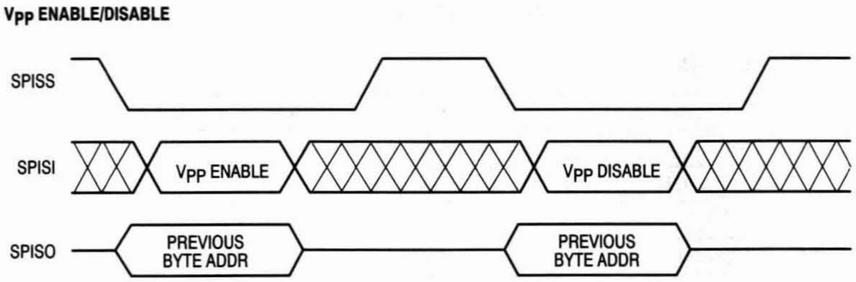

Vpp ENABLE/DISABLE
SPISS
SPISI
Vpp ENABLE
Vpp DISABLE
SPISO
PREVIOUS BYTE ADDR
PREVIOUS BYTE ADDR

Figure 13. SPI Program

4.8 SIGNAL LEVELS

Electrical and switching characteristics are described in Section 5.

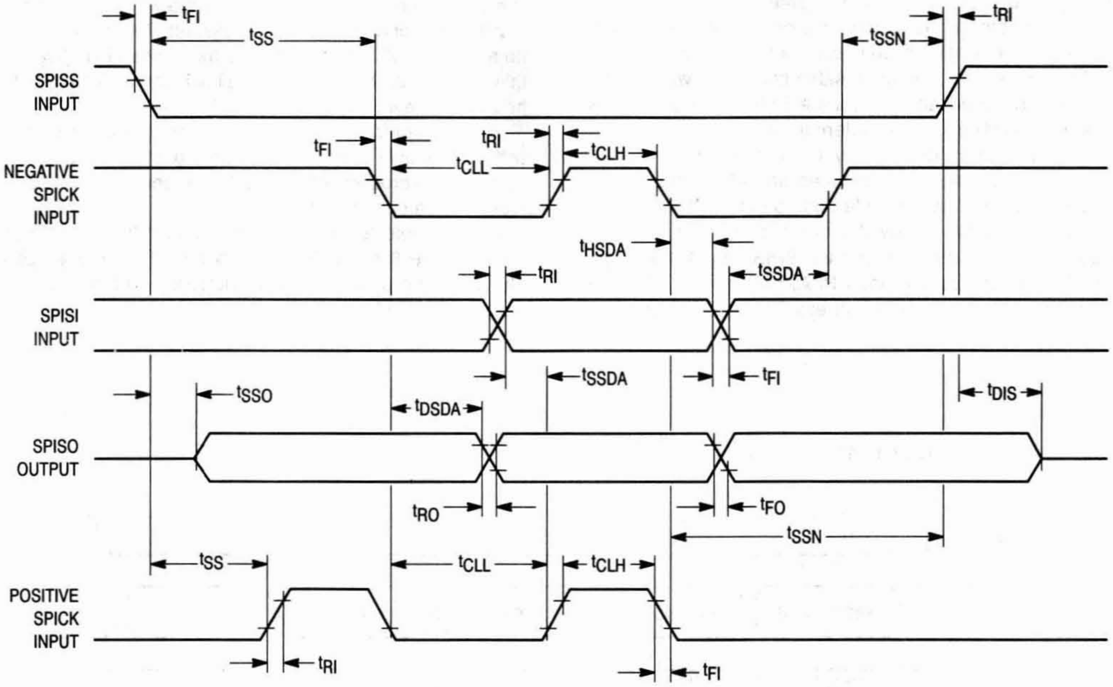

t_{FI}
t_{SS}
t_{SSN}
t_{RI}
SPISS INPUT
t_{FI}
t_{RI}
t_{CLL}
t_{CLH}
NEGATIVE SPICK INPUT
t_{HSDA}
t_{RI}
t_{SSDA}
SPISI INPUT
t_{SSDA}
t_{FI}
t_{SSO}
t_{DSDA}
t_{DIS}
SPISO OUTPUT
t_{RO}
t_{FO}
t_{SSN}
t_{SS}
t_{CLL}
t_{CLH}
POSITIVE SPICK INPUT
t_{RI}
t_{FI}

Figure 14. SPI Timing

5. CHARACTERISTICS

5.1 MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	– 0.3 to + 7.0	V
Input Voltage Pins 1, 3, 5, 6	V_{in}	– 0.3 to + 7.0	V
Input Voltage Pin 2	V_{in}	– 0.3 to V_{DD} + 0.3	V
Current on any Input	I_{in}	0.1	mA
Sink Current SDA	I_{SDAL}	10	mA
Sink Current SPISO	I_{SOL}	10	mA
Source Current SPISO	I_{SOH}	10	mA
Operating Temperature	T_A	0 to 70*	°C
Storage Temperature	T_S	– 55 to 125**	°C
Junction Temperature	T_j	150**	°C
Thermal Resistance	Th_{ja}	200	°C/W

* Specification over the temperature range, – 40 to + 125°C to be determined.

** In particular, continuous high temperature application may cause leakage of store charge in EEPROM, resulting in data loss.

NOTE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum operating conditions for extended periods may affect reliability.

5.2 ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage STANDBY	V_{DDS}	—	—	6.0	V
Supply Current STANDBY*	I_{DDS}	—	0.5	1.0	μA
Supply Voltage READ	V_{DDR}	3.0	—	6.0	V
Supply Current READ*	I_{DDR}	—	0.3	1.5	mA
Supply Voltage PROG	V_{DDP}	3.0**	—	6.0	V
Supply Current PROG*	I_{DDP}	—	0.5	3.0	mA

*Inputs at V_{SS} or V_{DD}.

**3 V device only. Standard is 4.5 V.

5.3 ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
SCL, SDA, SPISS, SPISI Inputs	Input Low Voltage	V_{IL}	− 0.3	—	0.3 x V_{DD}	V
	Input High Voltage	V_{IH}	0.7 x V_{DD}	—	V_{DD} + 0.3	V
	Input Leakage	I_{in}	—	—	± 10	μA
SDA/SPISO Pull Down Outputs	Output Low $I_{OL} < 10\ \mu A$	V_{OL}	—	—	0.1	V
	Output High Leakage	I_{OH}	—	—	± 10	μA
	Output Low I_{OL} = 3 mA, V_{DD} = 5 V	V_{OL}	—	—	0.4	V
	Output Low I_{OL} = 1 mA, V_{DD} = 3 V	V_{OL}	—	—	0.4	V
SPISO Pull Up Output	Output High I_{OH} = 1.6 mA, V_{DD} = 5 V	V_{OH}	V_{DD} − 0.8	—	—	V
	Output High I_{OH} = 0.4 mA, V_{DD} = 3 V		V_{DD} − 0.3	—	—	
MODE, CS1, CS0 Inputs	Input Low Voltage	V_{IL}	− 0.3	—	0.3 x V_{DD}	V
	Input High Voltage	V_{IH}	0.7 x V_{DD}	—	V_{DD} + 0.3	V
	Input Leakage	I_{in}	—	—	± 10	μA
Input Capacitance		C_{in}	—	10	—	pF

5.4 SWITCHING PARAMETERS

5.4.1 General Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Programming Time	1 Byte	t_{PROG}	10	—	—	ms
	4 Bytes		20	—	—	
Write/Erase	0 to 70°C	$cy_{W/E}$	—	—	10,000	cycles
	Ambient Temperature		—	100,000	—	

5.4.2 Serial Bus Input

Characteristic		Symbol	Min	Typ	Max	Unit
SDA/SPISI, SCL/SPICK, SPISS Inputs	Clock Frequency	F_{SCL}	0.0	—	125	kHz
	Clock High Time	t_{CLH}	4.0	—	—	μs
	Clock Low Time	t_{CLL}	4.0	—	—	μs
	Stop to Start Delay	t_{BUF}	4.0	—	—	μs
	Start Hold Time	t_{HSTA}	4.0	—	—	μs
	Data Hold Time	t_{HSDA}	0.0	—	—	μs
	Data Set-Up Time	t_{SSDA}	250	—	—	ns
	Input Rise Time	t_{RI}	—	—	1.0	μs
	Input Fall Time	t_{FI}	—	—	300	ns
	Stop Set-Up Time	t_{SSTO}	4.0	—	—	μs
	SPISS Lead Time	t_{SS}	4.0	—	—	μs
	SPISS Lag Time	t_{SSN}	4.0	—	—	μs

NOTE: All values refer to V_{IH} and V_{IL} levels.

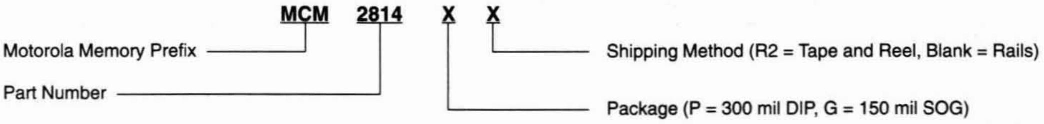
5.4.3 Serial Bus Output

Characteristic	Symbol	Min	Typ	Max	Unit
SDA/SPISO Outputs (V_{DD} = 5 V ± 10%, T_A = 0 to 70°C, C_L = 200 pF)					
Data Delay	t_{DSDA}	—	1.5	3.5	μs
Rise Time SDA	t_{RO}	—	—	*	ns
Rise Time SPISO	t_{RO}	—	—	100	ns
Fall Time	t_{FO}	—	—	100	ns
SPI Select Time	t_{SSO}	—	—	1.2	μs
Disable Time	t_{DIS}	—	1.5	3.5	μs
SDA/SPISO Outputs (V_{DD} = 3.3 V ± 10%, T_A = 0 to 70°C, C_L = 200 pF)					
Data Delay	t_{DSDA}	—	2.0	3.5	μs
Rise Time SDA	t_{RO}	—	—	*	ns
Rise Time SPISO	t_{RO}	—	—	200	ns
Fall Time	t_{FO}	—	—	200	ns
SPI Select Time	t_{SSO}	—	—	1.5	μs
Disable Time	t_{DIS}	—	2.0	3.5	μs

NOTE: All values refer to V_{IH} and V_{IL} levels.

*Depends on external pull-up resistor value where $t_{RI} = C_{bus}/R_{pull\text{-}up}$.

ORDERING INFORMATION
(Order by Full Part Number)


MCM
2814
X
X
Motorola Memory Prefix
Part Number
Shipping Method (R2 = Tape and Reel, Blank = Rails)
Package (P = 300 mil DIP, G = 150 mil SOG)

Full Part Numbers — MCM2814P
MCM2814G
MCM2814GR2

NOTE: For mechanical data, please see Chapter 10.

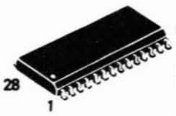
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM60L256A-C

Advance Information

32K × 8 Bit CMOS Static Random Access Memory

Extended Temperature Range: −40 to 85°C



F PACKAGE
SOG
CASE 751H

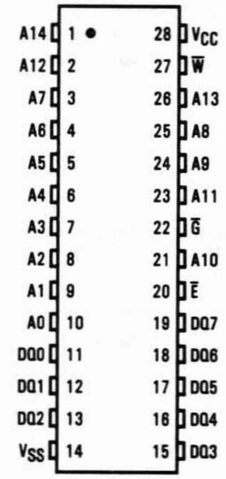
The MCM60L256A-C is a 262,144 bit low-power static random access memory organized as 32,768 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The operating current is 5 mA/MHz (typ) and the cycle time is 100 ns. For long cycle times (>100 ns), the automatic power down (APD) circuitry will temporarily shut down various power consuming circuits, thereby reducing the active power consumption.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. When $\overline{E}$ is a logic high, the part is placed in low power standby mode. The maximum standby current is 2 μA ($T_A = 25°C$). Chip enable also controls the data retention mode. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 50 ns. Thus the MCM60L256A-C is suitable for use in various microprocessor application systems where high speed, low power, and battery backup are required.

The MCM60L256A-C is offered in a 28 pin 330 mil gull-wing SO package.

- Single 5 V Supply, ±10%
- 32K × 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—27.5 mW/MHz (Typical Active)
- Output Enable and Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (Maximum Standby Current = 2 μA @ 25°C)
- Data Retention Supply Voltage = 2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Time: MCM60L256A-C10 = 100 ns (Max)

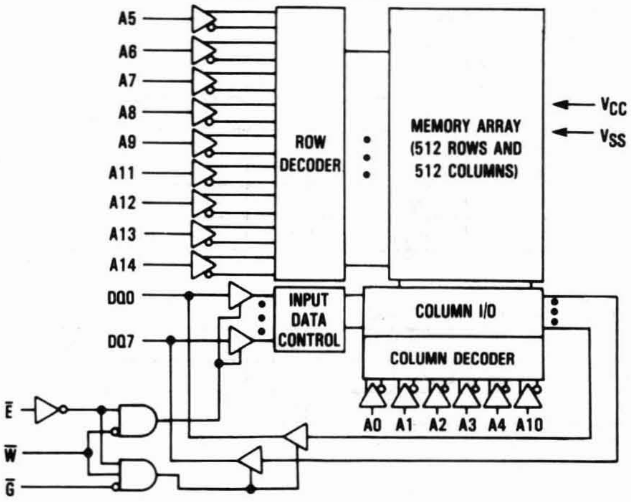
PIN ASSIGNMENT



A14 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ0 11
DQ1 12
DQ2 13
V_{SS} 14
28 V_{CC}
27 $\overline{W}$
26 A13
25 A8
24 A9
23 A11
22 $\overline{G}$
21 A10
20 $\overline{E}$
19 DQ7
18 DQ6
17 DQ5
16 DQ4
15 DQ3

PIN NAMES	
A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



A5
A6
A7
A8
A9
A11
A12
A13
A14
ROW DECODER
MEMORY ARRAY (512 ROWS AND 512 COLUMNS)
V_{CC}
V_{SS}
DQ0
DQ7
INPUT DATA CONTROL
COLUMN I/O
COLUMN DECODER
A0 A1 A2 A3 A4 A10
$\overline{E}$
$\overline{W}$
$\overline{G}$

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.3 to +7.0	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Power Dissipation (T_A = 25°C) SOG	P_D	0.6	W
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −40 to 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤50 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	<0.01	±1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	<0.01	±1.0	µA
Operating Current (Read Cycle) ($\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IH}, Other Input = V_{IH}/V_{IL}, I_{out} = 0 mA) t_{AVQV} = 1 µs	I_{CCA1}	—	10	15	mA
t_{AVQV} = 100 ns		—	—	70	
($\overline{E}$ = 0.2 V, $\overline{W}$ = V_{CC} − 0.2 V, Other Input = V_{CC} − 0.2 V/0.2 V, I_{out} = 0 mA) t_{AVQV} = 1 µs	I_{CCA2}	—	5	8	
t_{AVQV} = 100 ns		—	—	60	
Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	—	—	3.0	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{CC} = 2.0 to 5.5 V)	I_{SB2}	—	2	100	µA
(T_A = 25°C)		—	—	2	
Output Low Voltage (I_{OL} = 4.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	—	—	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance (V_{in} = 0 V)	All Inputs Except DQ	C_{in}	—	10	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	DQ	$C_{I/O}$	—	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = −40 to 85°C, Unless Otherwise Noted)

Input Pulse Levels . . . . 0.6 V, 2.4 V
Input Rise/Fall Time . . . . 5 ns
Input Timing Measurement Reference Levels . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . . .0.8 and 2.2 V
Output Load . . . . See Figure 1

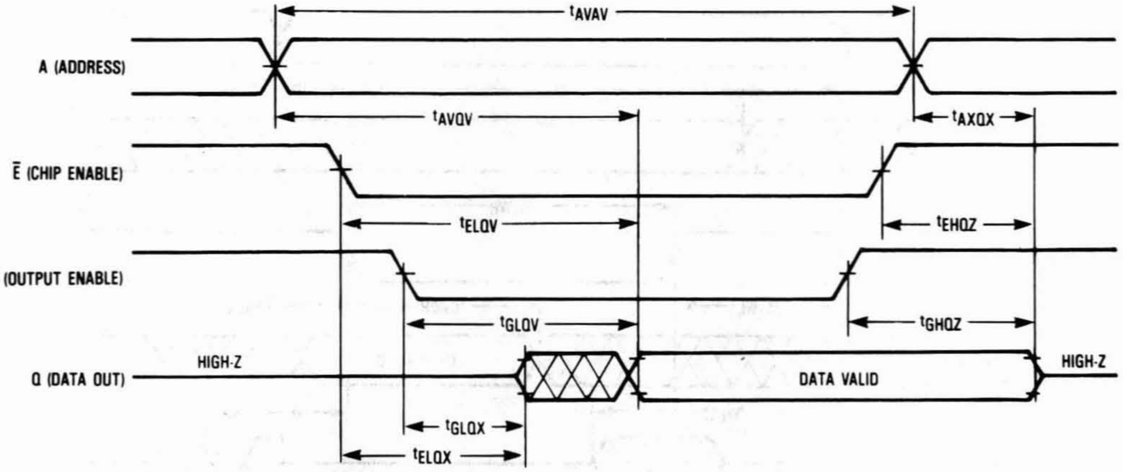
READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	Min	Max	Unit	Notes
Read Cycle Time	t_{AVAV}	t_{RC}	100	—	ns	—
Address Access Time	t_{AVQV}	t_{AA}	—	100	ns	—
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	—	100	ns	—
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	50	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	10	—	ns	—
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	10	—	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	—	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	35	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	35	ns	2, 3

NOTES:

1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 100 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.

READ CYCLE


t_{AVAV}
A (ADDRESS)
t_{AVQV}
t_{AXQX}
$\overline{E}$ (CHIP ENABLE)
t_{ELQV}
t_{EHQZ}
$\overline{G}$ (OUTPUT ENABLE)
t_{GLQV}
t_{GHQZ}
HIGH-Z
Q (DATA OUT)
DATA VALID
HIGH-Z
t_{GLQX}
t_{ELQX}

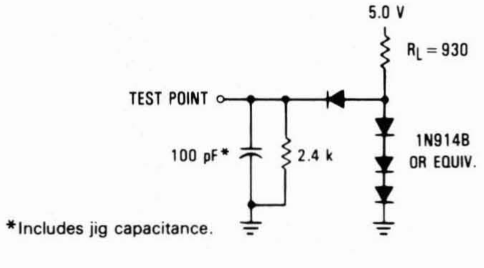

5.0 V
R_L = 930
TEST POINT
1N914B
OR EQUIV.
100 pF*
2.4 k
*Includes jig capacitance.

Figure 1. AC Test Load

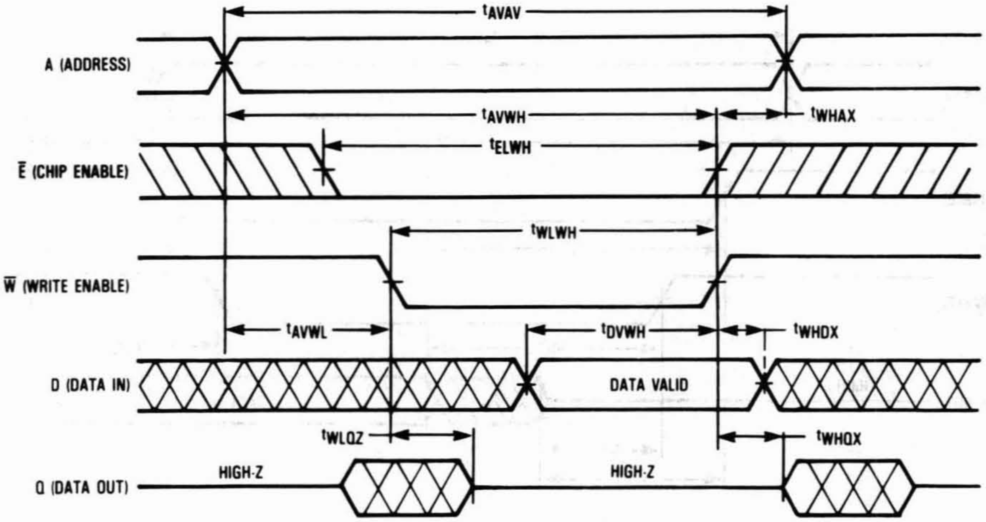
WRITE CYCLE 1 AND 2 (See Note 1)

Parameter	Symbol	Alt Symbol	Min	Max	Unit	Notes
Write Cycle Time	t_{AVAV}	t_{WC}	100	–	ns	–
Address Setup Time	t_{AVWL}/t_{AVEL}	t_{AS}	0	–	ns	–
Address Valid to End of Write	t_{AVWH}/t_{AVEH}	t_{AW}	80	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	60	–	ns	2
Data Valid to End of Write	t_{DVWH}/t_{DVEH}	t_{DW}	35	–	ns	–
Data Hold Time	t_{WHDX}/t_{EHDX}	t_{DH}	0	–	ns	–
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	25	ns	3, 4
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	10	–	ns	3, 4
Write Recovery Time	t_{WHAX}/t_{EHAX}	t_{WR}	0	–	ns	5
Chip Enable to End of Write	t_{ELWH}/t_{ELEH}	t_{CW}	80	–	ns	–

NOTES:

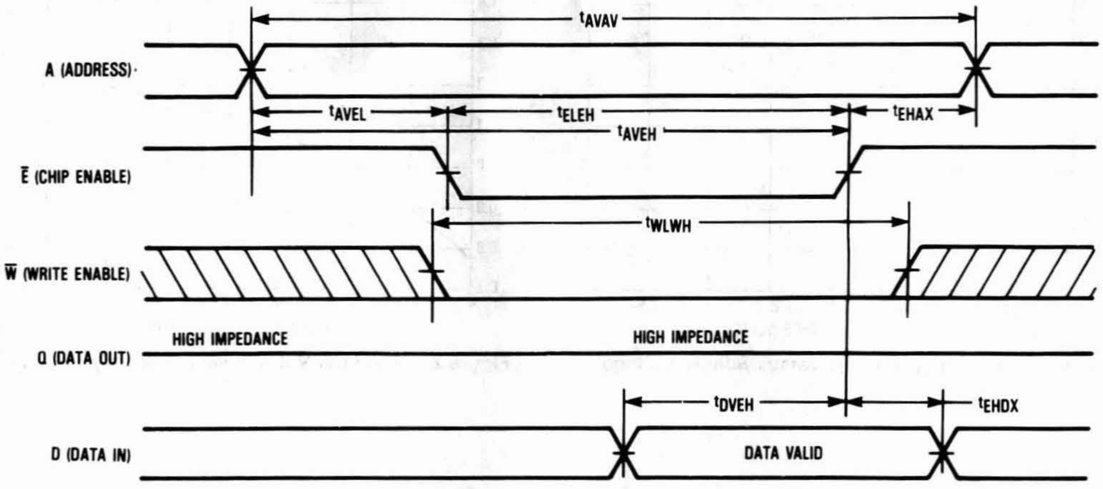
1. Outputs are in high impedance state if $\overline{G}$ is high during Write Cycle.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{E}$ and a low $\overline{W}$. If $\overline{W}$ goes low prior to $\overline{E}$ low then outputs will remain in a high impedance state.
3. All high-Z and low-Z parameters are considered in a high or low impedance state when the outputs have made a 100 mV transition from the previous steady state voltage.
4. These parameters are periodically sampled and not 100% tested.
5. t_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high to the end of write cycle.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



tAVAV
A (ADDRESS)
tAVWH
tWHAX
tELWH
Ē (CHIP ENABLE)
tWLWH
W̄ (WRITE ENABLE)
tAVWL
tDVWH
tWHDX
D (DATA IN)
DATA VALID
tWLQZ
tWHQX
Q (DATA OUT)
HIGH-Z
HIGH-Z

WRITE CYCLE 2 ($\overline{\text{E}}$ Controlled)

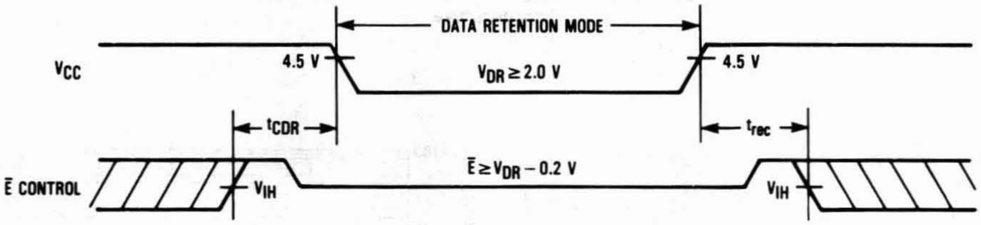

t_{AVAV}
A (ADDRESS)
t_{AVEL}
t_{ELEH}
t_{EHAX}
t_{AVEH}
$\overline{\text{E}}$ (CHIP ENABLE)
t_{WLWH}
$\overline{\text{W}}$ (WRITE ENABLE)
HIGH IMPEDANCE
Q (DATA OUT)
HIGH IMPEDANCE
t_{DVEH}
t_{EHDX}
D (DATA IN)
DATA VALID

DATA RETENTION CHARACTERISTICS ($T_A = -40$ to 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{\text{E}} \geq V_{CC} - 0.2$ V)		V_{DR}	2.0	–	5.5	V
Data Retention Current ($\overline{\text{E}} \geq V_{CC} - 0.2$ V)	$V_{CC} = 3.0$ V $V_{CC} = 5.5$ V	I_{CCDR}	– –	– –	50 100	μA
Chip Disable to Data Retention Time		t_{CDR}	0	–	–	ns
Operation Recovery Time		t_{rec}	t_{AVAV}*	–	–	ns

*t_{AVAV} = Read Cycle Time

DATA RETENTION MODE


DATA RETENTION MODE
V_{CC}
4.5 V
$V_{DR} \geq 2.0$ V
4.5 V
t_{CDR}
t_{rec}
$\overline{\text{E}} \geq V_{DR} - 0.2$ V
$\overline{\text{E}}$ CONTROL
V_{IH}
V_{IH}

NOTE: If the V_{IH} of $\overline{\text{E}}$ is 2.4 V in operation, I_{SB1} current flows during the period that the V_{CC} voltage is decreasing from 4.5 V to 2.4 V.

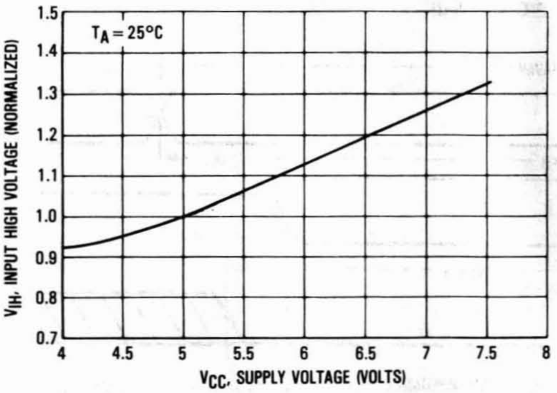


Figure 1. Input High Voltage versus Supply Voltage

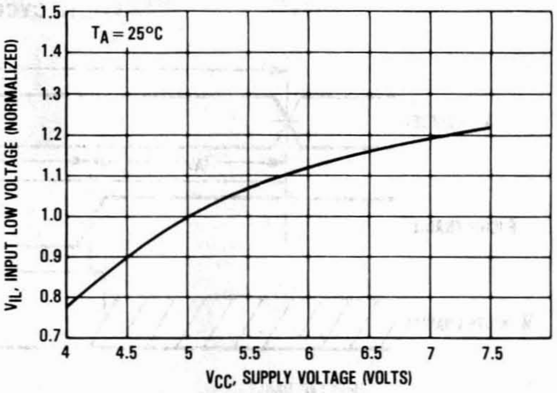


Figure 2. Input Low Voltage versus Supply Voltage

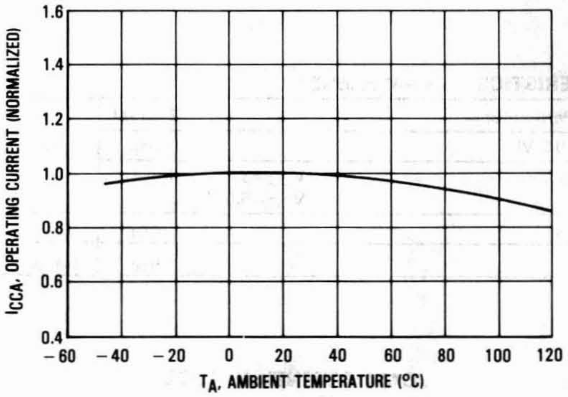


Figure 3. Operating Current versus Ambient Temperature

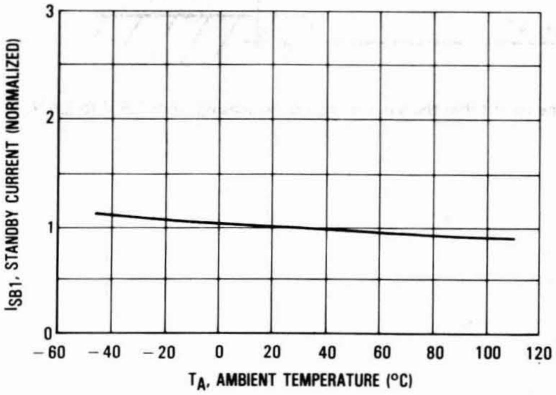


Figure 4. I_{SB1} Standby Current versus Ambient Temperature

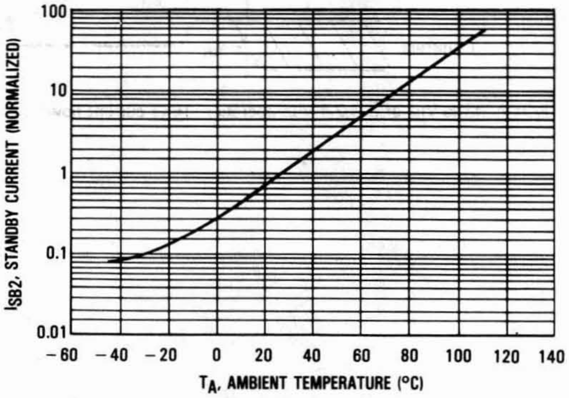


Figure 5. I_{SB2} Standby Current versus Ambient Temperature

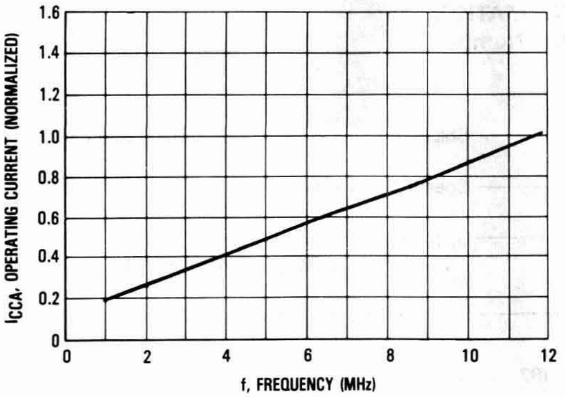


Figure 6. Low Power Operating Current versus Frequency (Read)

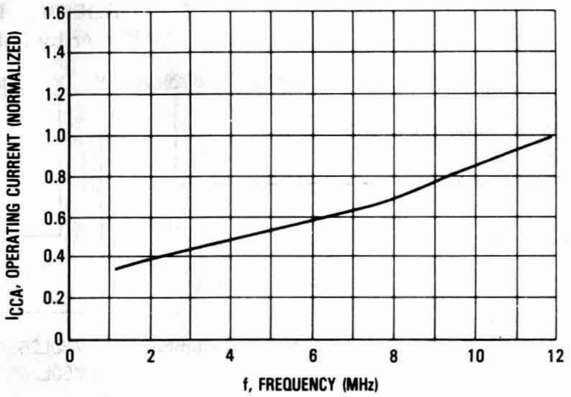


Figure 7. Operating Current versus Frequency (Write)

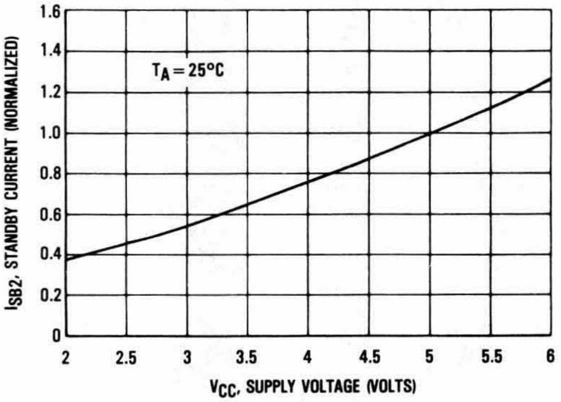


Figure 8. Low Power I_{SB2} Standby Current versus Supply Voltage

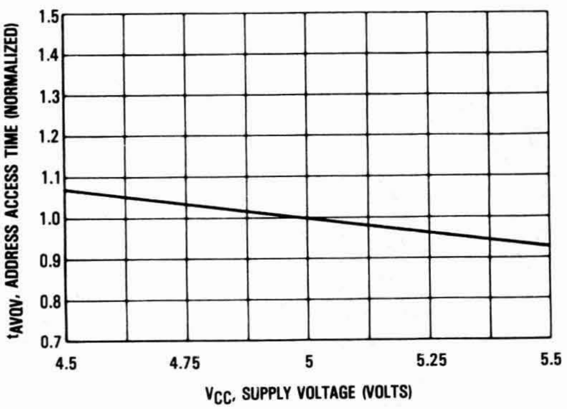


Figure 9. Access Time versus Supply Voltage

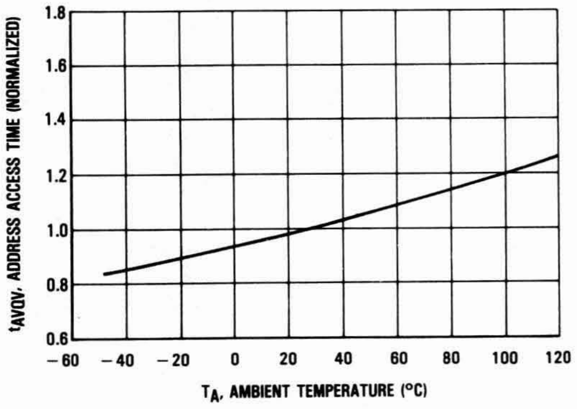


Figure 10. Access Time versus Ambient Temperature

ORDERING INFORMATION
(Order by Full Part Number)

MCM 60256A X X XX XX

Motorola Memory Prefix — MCM
Part Number — 60256A
F = Gull-Wing SO)
Operating Temperature Range (C = Industrial Range, −40 to 85°C)
Speed (10 = 100 ns)
Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Number — MCM60L256AFC10
MCM60L256AFC10R2

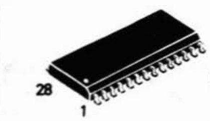
NOTE: For mechanical data, please see Chapter 10.

MCM60L256A-V

Advance Information

32K × 8 Bit CMOS Static Random Access Memory

Extended Temperature Range: −40 to 105°C



F PACKAGE
SOG
CASE 751H

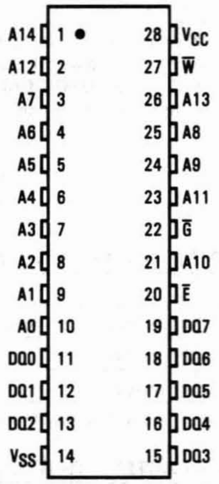
The MCM60L256A-V is a 262,144 bit low-power static random access memory organized as 32,768 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The operating current is 5 mA/MHz (typ) and the cycle time is 100 ns. For long cycle times (>100 ns), the automatic power down (APD) circuitry will temporarily shut down various power consuming circuits, thereby reducing the active power consumption.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. When $\overline{E}$ is a logic high, the part is placed in low power standby mode. The maximum standby current is 2 μA (T_A=25°C). Chip enable also controls the data retention mode. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 50 ns. Thus the MCM60L256A-V is suitable for use in various microprocessor application systems where high speed, low power, and battery backup are required.

The MCM60L256A-V is offered in a 28 pin 330 mil gull-wing SO package.

- Single 5 V Supply, ±10%
- 32K × 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—27.5 mW/MHz (Typical Active)
- Output Enable and Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (Maximum Standby Current=2 μA @ 25°C)
- Data Retention Supply Voltage=2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Time: MCM60L256A-V10=100 ns (Max)

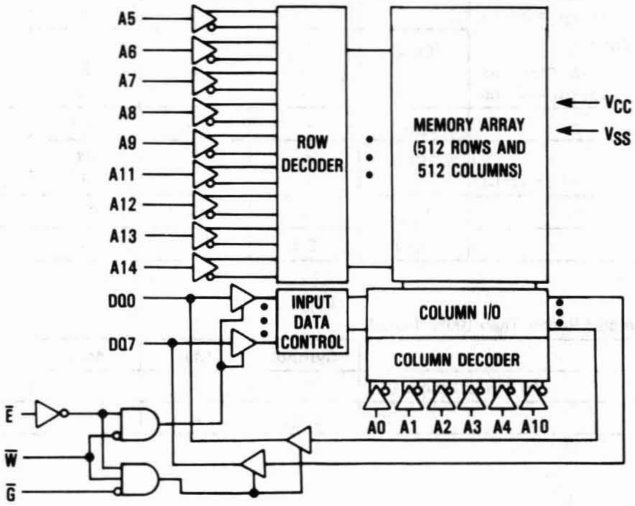
PIN ASSIGNMENT


A14 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ0 11
DQ1 12
DQ2 13
V_{SS} 14
28 V_{CC}
27 $\overline{W}$
26 A13
25 A8
24 A9
23 A11
22 $\overline{G}$
21 A10
20 $\overline{E}$
19 DQ7
18 DQ6
17 DQ5
16 DQ4
15 DQ3

PIN NAMES

A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM


A5
A6
A7
A8
A9
A11
A12
A13
A14
ROW DECODER
MEMORY ARRAY (512 ROWS AND 512 COLUMNS)
V_{CC}
V_{SS}
DQ0
DQ7
INPUT DATA CONTROL
COLUMN I/O
COLUMN DECODER
A0 A1 A2 A3 A4 A10
$\overline{E}$
$\overline{W}$
$\overline{G}$

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.3 to +7.0	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Power Dissipation (T_A = 25°C) SOG	P_D	0.6	W
Operating Temperature	T_A	−40 to +105	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −40 to 105°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤50 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	<0.01	±1.0	μA
Output Leakage Current ($\overline{E}=V_{IH}$ or $\overline{G}=V_{IH}$ or $\overline{W}=V_{IL}$, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	<0.01	±1.0	μA
Operating Current (Read Cycle) ($\overline{E}=V_{IL}$, $\overline{W}=V_{IH}$, Other Input = V_{IH}/V_{IL}, I_{out} = 0 mA) t_{AVQV} = 1 μs	I_{CCA1}	—	10	15	mA
t_{AVQV} = 100 ns		—	—	70	
($\overline{E}$ = 0.2 V, $\overline{W}=V_{CC}-0.2$ V, Other Input = $V_{CC}-0.2$ V/0.2 V, I_{out} = 0 mA) t_{AVQV} = 1 μs	I_{CCA2}	—	5	8	
t_{AVQV} = 100 ns		—	—	60	
Standby Current ($\overline{E}=V_{IH}$)	I_{SB1}	—	—	3.0	mA
Standby Current ($\overline{E}\geq V_{CC}-0.2$ V, V_{CC} = 2.0 to 5.5 V)	I_{SB2}	—	2	100	μA
(T_A = 25°C)		—	—	2	
Output Low Voltage (I_{OL} = 4.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	—	—	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance (V_{in} = 0 V)	All Inputs Except DQ	C_{in}	—	10	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	DQ	$C_{I/O}$	—	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = −40 to 105°C, Unless Otherwise Noted)

Input Pulse Levels . . . . 0.6 V, 2.4 V
Input Rise/Fall Time . . . . 5 ns
Input Timing Measurement Reference Levels . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . . .0.8 and 2.2 V
Output Load . . . . See Figure 1

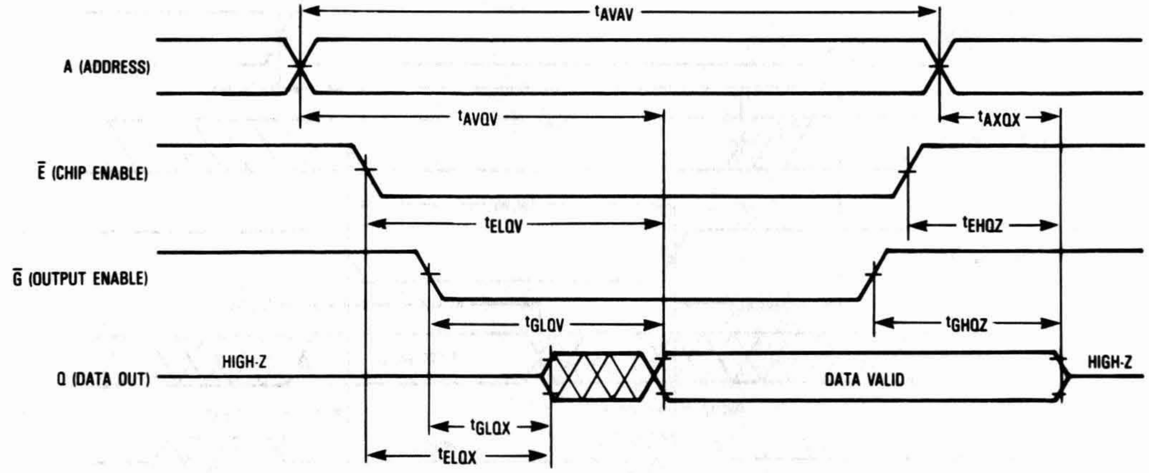
READ CYCLE (See Note 1)

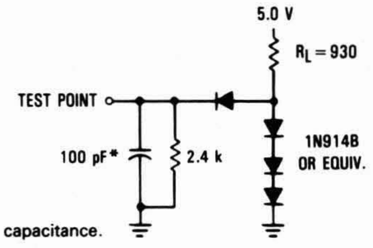
Parameter	Symbol	Alt Symbol	Min	Max	Unit	Notes
Read Cycle Time	t_{AVAV}	t_{RC}	100	—	ns	—
Address Access Time	t_{AVQV}	t_{AA}	—	100	ns	—
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	—	100	ns	—
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	50	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	10	—	ns	—
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	10	—	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	—	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	35	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	35	ns	2, 3

NOTES:

1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 100 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.

READ CYCLE


t_{AVAV}
A (ADDRESS)
t_{AVQV}
t_{AXQX}
$\overline{E}$ (CHIP ENABLE)
t_{ELQV}
t_{EHQZ}
$\overline{G}$ (OUTPUT ENABLE)
t_{GLQV}
t_{GHQZ}
Q (DATA OUT)
HIGH-Z
DATA VALID
HIGH-Z
t_{GLQX}
t_{ELQX}


5.0 V
R_L = 930
TEST POINT
100 pF*
2.4 k
1N914B
OR EQUIV.

*Includes jig capacitance.

Figure 1. AC Test Load

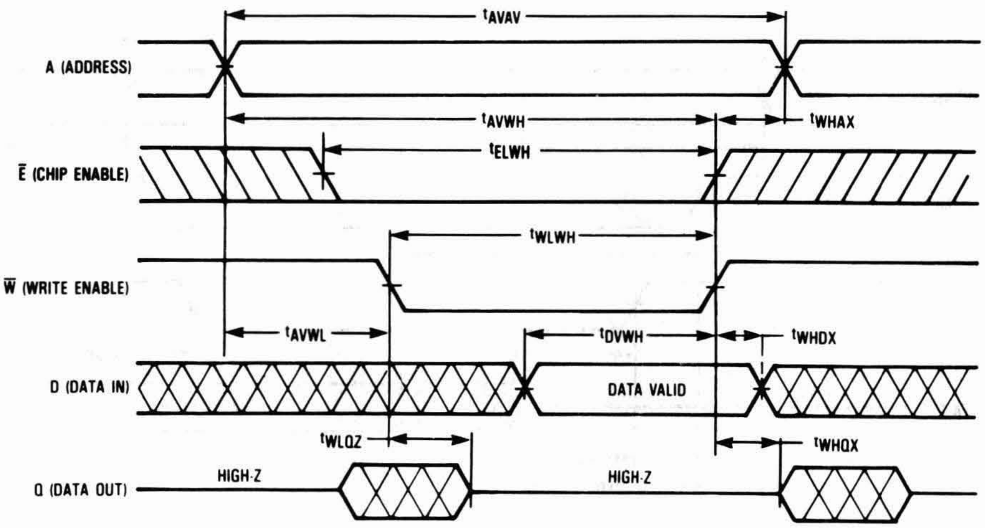
WRITE CYCLE 1 AND 2 (See Note 1)

Parameter	Symbol	Alt Symbol	Min	Max	Unit	Notes
Write Cycle Time	t_{AVAV}	t_{WC}	100	–	ns	–
Address Setup Time	t_{AVWL}/t_{AVEL}	t_{AS}	0	–	ns	–
Address Valid to End of Write	t_{AVWH}/t_{AVEH}	t_{AW}	80	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	60	–	ns	2
Data Valid to End of Write	t_{DVWH}/t_{DVEH}	t_{DW}	35	–	ns	–
Data Hold Time	t_{WHDX}/t_{EHDX}	t_{DH}	0	–	ns	–
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	30	ns	3, 4
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	10	–	ns	3, 4
Write Recovery Time	t_{WHAX}/t_{EHAX}	t_{WR}	0	–	ns	5
Chip Enable to End of Write	t_{ELWH}/t_{ELEH}	t_{CW}	80	–	ns	–

NOTES:

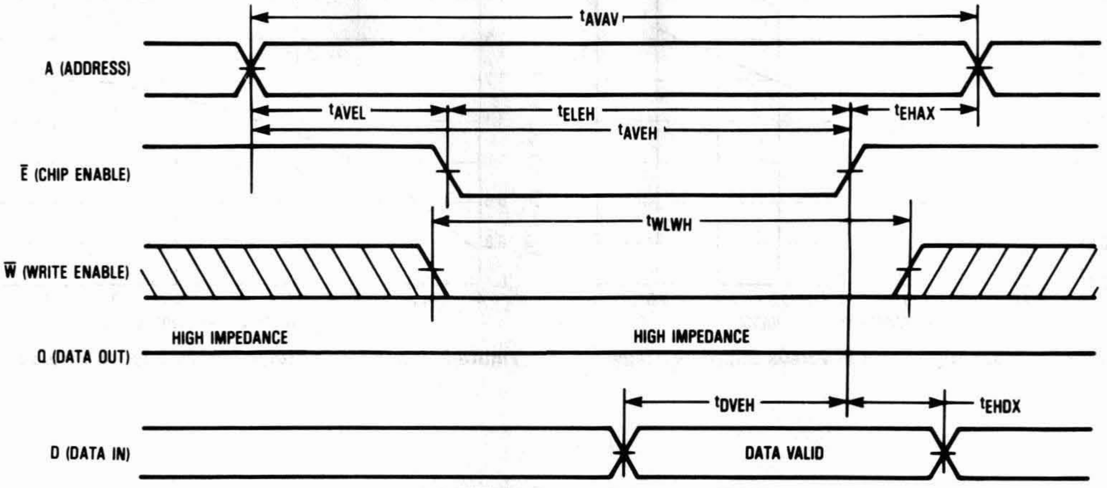
1. Outputs are in high impedance state if $\overline{G}$ is high during Write Cycle.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{E}$ and a low $\overline{W}$. If $\overline{W}$ goes low prior to $\overline{E}$ low then outputs will remain in a high impedance state.
3. All high-Z and low-Z parameters are considered in a high or low impedance state when the outputs have made a 100 mV transition from the previous steady state voltage.
4. These parameters are periodically sampled and not 100% tested.
5. t_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high to the end of write cycle.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



tAVAV
A (ADDRESS)
tAVWH
tWHAX
tELWH
E̅ (CHIP ENABLE)
tWLWH
W̅ (WRITE ENABLE)
tAVWL
tDVWH
tWHDX
D (DATA IN)
DATA VALID
tWLQZ
tWHQX
Q (DATA OUT)
HIGH-Z
HIGH-Z

WRITE CYCLE 2 ($\overline{E}$ Controlled)



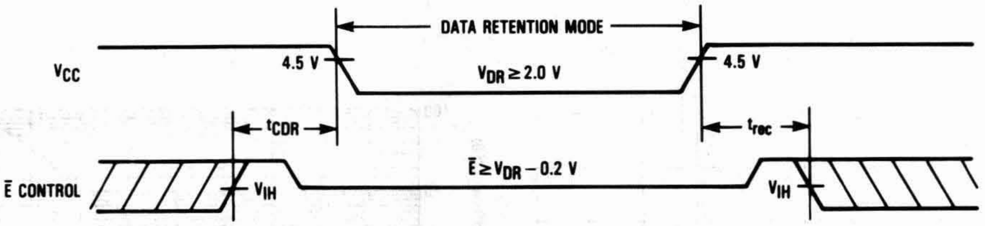
tAVAV
A (ADDRESS)
tAVEL
tELEH
tEHAX
tAVEH
Ē (CHIP ENABLE)
tWLWH
W̄ (WRITE ENABLE)
HIGH IMPEDANCE
HIGH IMPEDANCE
Q (DATA OUT)
tDVEH
tEHDX
D (DATA IN)
DATA VALID

DATA RETENTION CHARACTERISTICS ($T_A = -40$ to 105°C)

Parameter		Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E} \geq V_{CC} - 0.2$ V)		V_{DR}	2.0	–	5.5	V
Data Retention Current ($\overline{E} \geq V_{CC} - 0.2$ V)	$V_{CC} = 3.0$ V $V_{CC} = 5.5$ V	I_{CCDR}	– –	– –	50 100	μA
Chip Disable to Data Retention Time		t_{CDR}	0	–	–	ns
Operation Recovery Time		t_{rec}	t_{AVAV}*	–	–	ns

*t_{AVAV} = Read Cycle Time

DATA RETENTION MODE



DATA RETENTION MODE
VCC
4.5 V
VDR ≥ 2.0 V
4.5 V
tCDR
trec
Ē ≥ VDR − 0.2 V
Ē CONTROL
VIH
VIH

NOTE: If the V_{IH} of $\overline{E}$ is 2.4 V in operation, I_{SB1} current flows during the period that the V_{CC} voltage is decreasing from 4.5 V to 2.4 V.

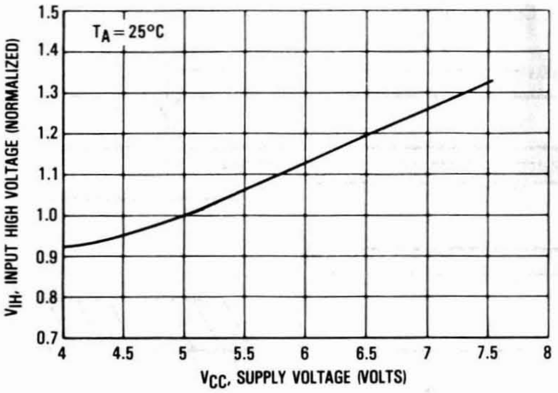


Figure 1. Input High Voltage versus Supply Voltage

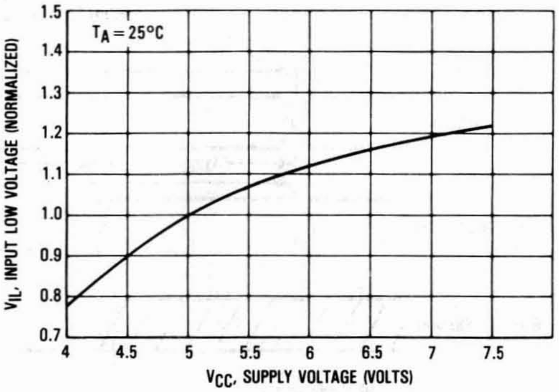


Figure 2. Input Low Voltage versus Supply Voltage

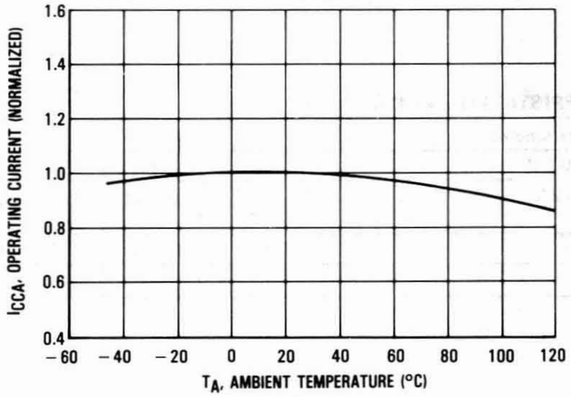


Figure 3. Operating Current versus Ambient Temperature

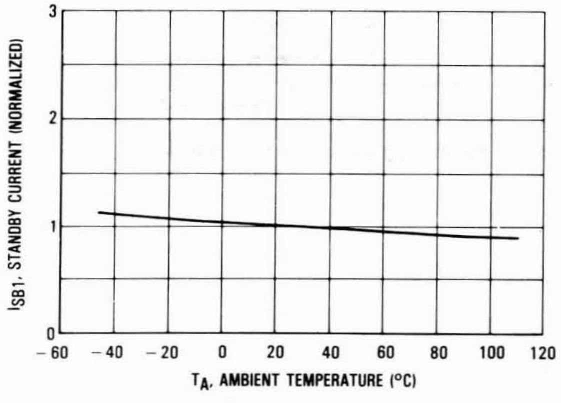


Figure 4. I_{SB1} Standby Current versus Ambient Temperature

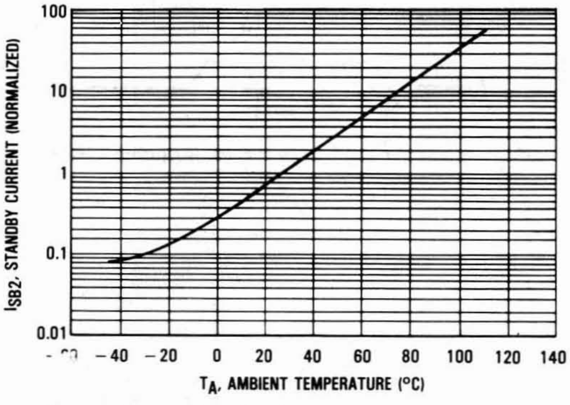


Figure 5. I_{SB2} Standby Current versus Ambient Temperature

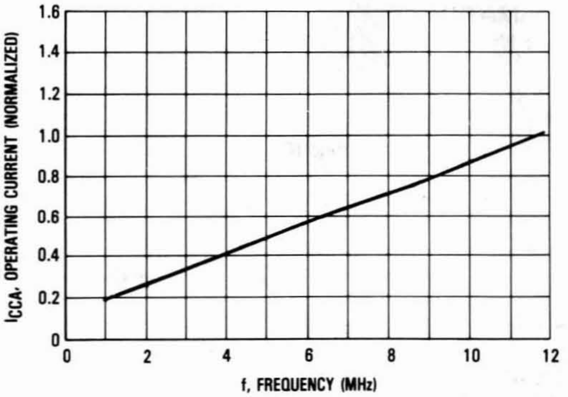


Figure 6. Low Power Operating Current versus Frequency (Read)

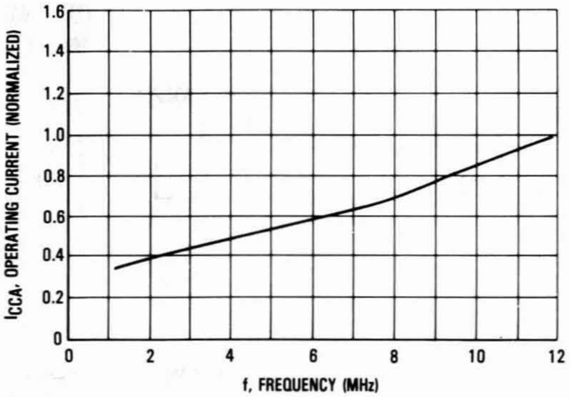


Figure 7. Operating Current versus Frequency (Write)

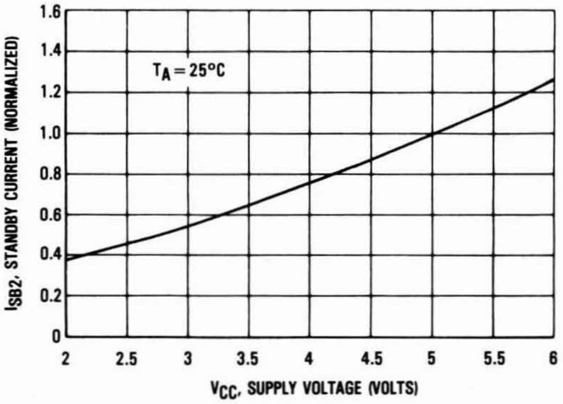


Figure 8. Low Power I_{SB2} Standby Current versus Supply Voltage

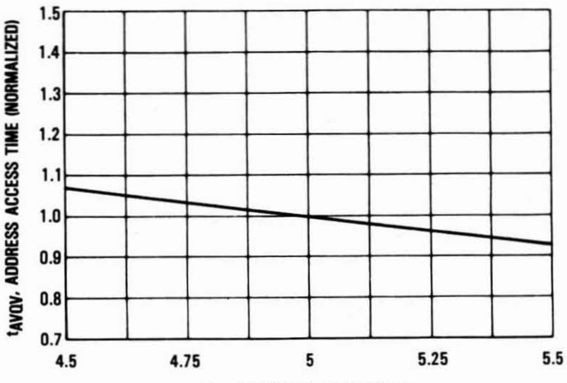


Figure 9. Access Time versus Supply Voltage

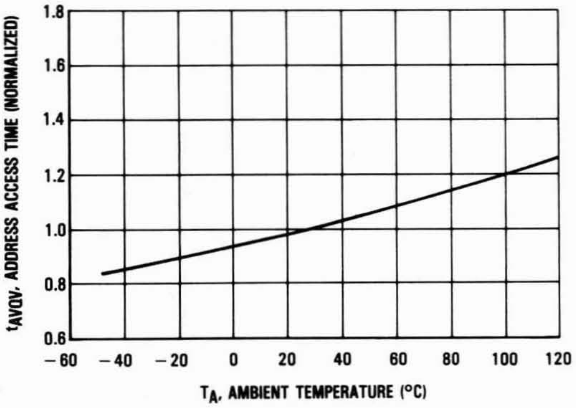


Figure 10. Access Time versus Ambient Temperature

ORDERING INFORMATION
(Order by Full Part Number)

MCM 60L256A X X XX XX

Motorola Memory Prefix — MCM

Part Number — 60L256A

F = Gull-Wing SO)

Operating Temperature Range (V = Extended Range, −40 to 105°C)

Speed (10 = 100 ns)

Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Number — MCM60L256AFV10
MCM60L256AFV10R2

NOTE: For mechanical data, please see Chapter 10.

Military Products

7

In addition to the parts covered in this data book, Motorola also offers a wide range of military memory parts. For more information, including a complete military memory product listing, please contact your Motorola representative.

Reliability Information

8

MOTOROLA CORPORATE QUALITY GOAL

IMPROVE PRODUCT AND SERVICES QUALITY TEN TIMES BY 1989 AND AT LEAST ONE HUNDRED FOLD BY 1991.

ACHIEVE SIX SIGMA CAPABILITY BY 1992.

With a deep sense of urgency, spread dedication to quality to every facet of the corporation and achieve a culture of continual improvement to ASSURE TOTAL CUSTOMER SATISFACTION. There is only one ultimate goal: zero defects in everything we do.

signed:

BOB GALVIN
Chairman

BILL WEISZ
Vice Chairman

JOHN MITCHELL
President

GEORGE FISHER
Deputy to Chief
Executive Office

GARY TOOKER
Chief to Corporate
Staff Officer

JACK GERMAIN
Motorola Director
of Quality

JIM LINCICOME
Government Electronics
Group

CARL LINDHOLM
International
Operations

LEVY KATZIR
New Enterprises

JIM NORLING
Semiconductor Products
Sector

STEVE LEVY
Japanese Operations

DON JONES
Chief Financial
Officer

JIM DONNELLY
Personnel

RAY FARMER
Communications Sector

ED STAIANO
General Systems
Group

GERHARD SCHULMEYER
Automotive & Industrial
Electronics Group

DIVISION QUALITY STATEMENT

MOTOROLA MOS MEMORY PRODUCTS DIVISION

COMMITMENT TO SIX SIGMA WORLD CLASS

The Memory Products Division staff is pleased to announce our commitment to be a World Class MOS Memory supplier. This means more bullet proof designs which can tolerate handling, processes at the limit and beyond, outstanding control of the manufacturing processes such that the integration of the design process will result in six sigma products.

We will accomplish this through our dedication to a continuous quality improvement culture. This will ensure our success in reaching the Motorola Corporate goal of total customer satisfaction.

Through our quality improvement process using SIX SIGMA methodology we can and will be the best memory supplier through WORLD CLASS product margins and services.

ENDORSEMENTS:

Jim George	**Bud Broeker**	**Lee Compton**	**Roger Kung**

Mike Parks	**Joy Jones**	**Michael Phillips**

SIX SIGMA
6σ
MOTOROLA

OUR SIX SIGMA CHALLENGE

WHAT IS SIX SIGMA?

Six Sigma is the required capability level to approach the Standard. The Standard is Zero Defects. Our goal is to be best-in-class in Product, Sales, and Service.

WHY SIX SIGMA?

The performance of a product is determined by how much margin exists between the process characteristics required by the design, and the actual value of those characteristics. These characteristics are produced by processes in the factory, and at the suppliers.

Each process attempts to reproduce its characteristics identically from unit to unit, but within each process some variation does occur. For some processes, such as those which use real-time feedback to control the outcome, the variation is quite small, and for others it may be quite large.

Variation of the process is measured in Standard Deviations (Sigma) from the Mean. The normal variation, defined as process width, is ±3 Sigma about the mean.

Approximately 2,700 parts per million parts/steps will fall outside the normal variation of ±3 Sigma, see Figure 1. This, by itself, does not appear disconcerting. However, when we build a product containing 1,200 parts/steps, we can expect 3.24 defects per unit (1200 × 0.0027), on an average. This would result in a rolled yield of less than 4%, which means fewer than 4 units out of every hundred would go through the entire manufacturing process without a defect, see Table 1.

Thus, we can see that for a product to be built virtually defect-free, it must be designed to accept characteristics that are significantly more than ±3 Sigma away from the Mean.

It can be shown that a design that can accept **twice the normal variation** of the process, or ±6 Sigma, can be expected to have no more than 3.4 parts per million defective for each characteristic, even if the process mean were to shift by as much as ±1.5 Sigma, see Figure 1. To quantify this, Capability Index (Cp) is used, where:

$$Cp = \frac{\text{design specification width}}{\text{process width}}$$

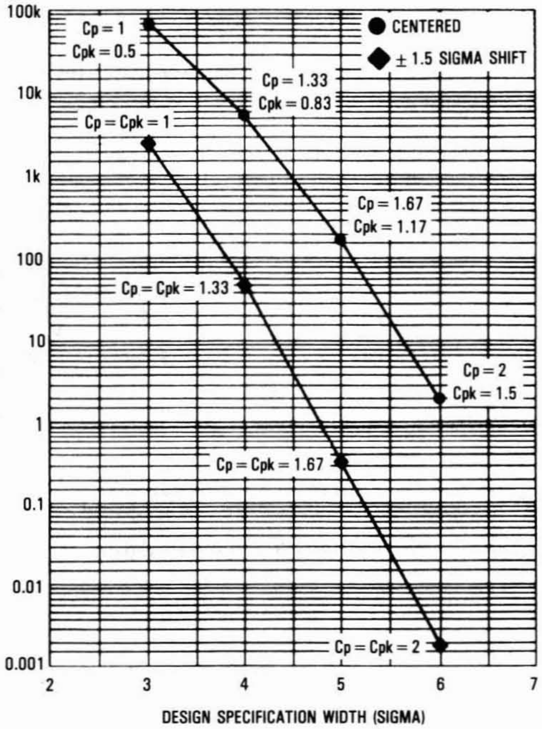


Figure 1. Standard Deviations from Mean

Table 1. Rolled Yield

TOTAL DEFECTS PER UNIT		ROLLED THROUGHPUT YIELD (%)
5.3	---------	0.5
4.6	---------	1.0
3.9	---------	2.0
3.5	---------	3.0
3.2	---------	4.0
3.0	---------	5.0
2.3	---------	10
1.9	---------	15
1.6	---------	20
1.4	---------	25
1.2	---------	30
1.0	---------	37
0.9	---------	40
0.8	---------	45
0.7	---------	50
0.6	---------	55
0.51	---------	60
0.43	---------	65
0.36	---------	70
0.29	---------	75
0.22	---------	80
0.16	---------	85
0.10	---------	90
0.05	---------	95
0.00	---------	100

ROLLED THROUGHPUT YIELD (%) = $100\ e^{-d/u}$

A design specification width of ±6 Sigma and a process width of ±3 Sigma yields a Cp of 12/6 = 2. However, as shown in Figure 2, the process mean can shift. When the process mean is shifted with respect to the design target mean, the Capability Index is adjusted with a factor k, and becomes Cpk. Cpk = Cp(1 − k), where:

$$k = \frac{\text{process shift}}{\text{design specification width}/2}$$

The k factor for ±6 Sigma design with a 1.5 Sigma process shift = 1.5/(12/2) = 0.25, and the Cpk = 2(1 − 0.25) = 1.5.

In the same case of a product containing 1,200 parts/steps, we would now expect only 0.0041 defects per unit (1200 × 0.0000034). This would mean that 996 units out of 1,000 would go through the entire manufacturing process without a defect (see Table 2).

It is our five year goal to achieve ±6 Sigma capability in Product, Sales, and Service.

Table 2. Overall Yield vs Sigma (Distribution Shifted ±1.5 σ)

NUMBER OF PARTS (STEPS)	±3 σ (%)	±4 σ (%)	±5 σ (%)	±6 σ (%)
1	93.32	99.379	99.9767	99.99966
7	61.63	95.733	99.839	99.9976
10	50.08	93.96	99.768	99.9966
20	25.08	88.29	99.536	99.9932
40	6.29	77.94	99.074	99.9864
60	1.58	68.81	98.614	99.9796
80	0.40	60.75	98.156	99.9728
100	0.10	53.64	97.70	99.966
150	–	39.38	96.61	99.949
200	–	28.77	95.45	99.932
300	–	15.43	93.26	99.898
400	–	8.28	91.11	99.864
500	–	4.44	89.02	99.830
600	–	2.38	86.97	99.796
700	–	1.28	84.97	99.762
800	–	0.69	83.02	99.729
900	–	0.37	81.11	99.695
1000	–	0.20	79.24	99.661
1200	–	0.06	75.88	99.593
3000	–	–	50.15	98.985
17000	–	–	0.02	94.384
38000	–	–	–	87.880
70000	–	–	–	78.820
150000	–	–	–	60.000

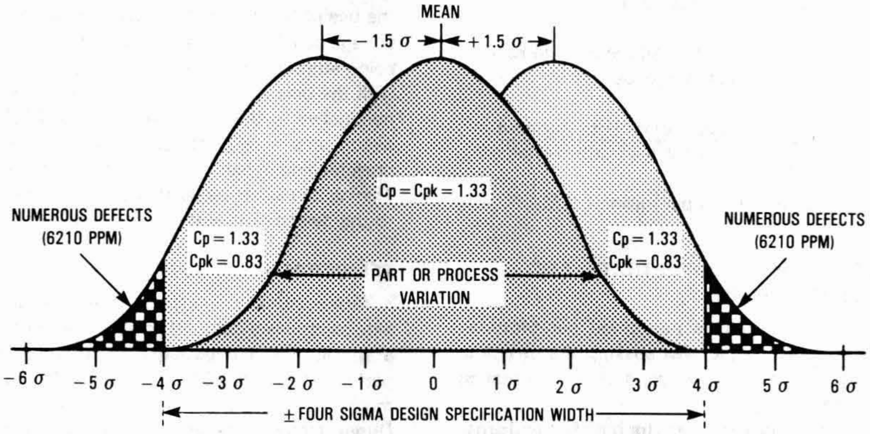

MEAN
− 1.5 σ
+ 1.5 σ
Cp = Cpk = 1.33
NUMEROUS DEFECTS (6210 PPM)
Cp = 1.33
Cpk = 0.83
PART OR PROCESS VARIATION
Cp = 1.33
Cpk = 0.83
NUMEROUS DEFECTS (6210 PPM)
− 6 σ
− 5 σ
− 4 σ
− 3 σ
− 2 σ
− 1 σ
0
1 σ
2 σ
3 σ
4 σ
5 σ
6 σ
± FOUR SIGMA DESIGN SPECIFICATION WIDTH

Figure 2a. Four Sigma Capability

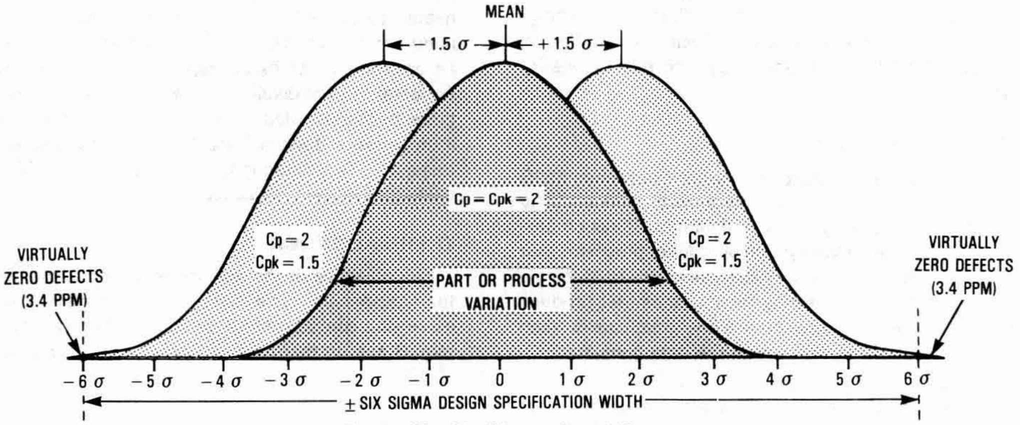

MEAN
− 1.5 σ
+ 1.5 σ
Cp = Cpk = 2
VIRTUALLY ZERO DEFECTS (3.4 PPM)
Cp = 2
Cpk = 1.5
PART OR PROCESS VARIATION
Cp = 2
Cpk = 1.5
VIRTUALLY ZERO DEFECTS (3.4 PPM)
− 6 σ
− 5 σ
− 4 σ
− 3 σ
− 2 σ
− 1 σ
0
1 σ
2 σ
3 σ
4 σ
5 σ
6 σ
± SIX SIGMA DESIGN SPECIFICATION WIDTH

Figure 2b. Six Sigma Capability

QUALITY MONITORING

Average Outgoing Quality (AOQ) refers to the number of devices per million that are outside specification limits at the time of shipment. Motorola has continually improved its outgoing quality, and has established a goal of zero defects. This level of quality will lead to vendor certification programs with many of our customers. The program ensures a certain level of quality, thus allowing a customer to either reduce or eliminate the need for incoming inspections.

By paying strict attention to quality at an early stage, the possibility of failures occurring further down the line is greatly minimized. Motorola's electrical parametric testing eliminates devices that do not conform to electrical specification. Additional parametric testing on a sample basis provides data for continued improvement.

AVERAGE OUTGOING QUALITY (AOQ) CALCULATION

$$\text{AOQ in PPM} = (\text{Process Average}) \cdot (\text{Lot Acceptance Rate}) \cdot (10^6)$$

$$\text{Process Average} = \frac{\text{Total Projected Reject Devices*}}{\text{Total Number of Devices}}$$

$$\text{Projected Reject Devices} = \frac{\text{Defects in Sample}}{\text{Sample Size}} \cdot \text{Lot Size}$$

Total Number of Devices = Sum of all the units in each submitted lot

$$\text{Lot Acceptance Rate} = 1 - \frac{\text{Number of Lots Rejected}}{\text{Number of Lots Tested}}$$

10^6 = Conversion to parts per million (PPM)

MARKING PERMANENCY, HERMETICITY, AND SOLDERABILITY MONITORS

Marking permanency testing is performed per Motorola specification. The procedure involves soaking the device in various solvents, brushing the markings, and then inspecting the markings for legibility.

Hermeticity monitoring includes tests for both fine and gross leaks in the hermetic package seal.

Solderability testing is used to ensure that device leads can be soldered without voids, discoloration, flaking, dewetting, or bridging. Typically, the test specifies steam preconditioning followed by a 235° to 260°C solder dip and microscope inspection of the leads.

RELIABILITY MONITORING

Motorola recognizes the need to monitor established MOS Memory products to maintain the level of quality and reliability demonstrated through the internal and joint qualification processes. Motorola maintains a system of monitor programs that provide monthly feedback on the extensive matrix of Motorola fabrication, assembly, and testing technologies that produce our products. As with qualification activity, great care is taken to assure the accuracy and quality of the data generated.

RELIABILITY STRESS TESTS

The following summary gives brief descriptions of the various reliability tests included in both reliability qualification and monitor programs. Not all of the tests listed are performed by each program and other tests can be performed when appropriate. Refer to Table 3.

Table 3. Stresses and Typical Stress Conditions

Stress	Typical Stress Condition
High Temperature Operating Life, Dynamic or Static	125°C, 6.0 V
Temperature Cycle	− 65°C to + 150°C Air to Air
Thermal Shock	− 65°C to + 150°C Liquid to Liquid
Temperature Humidity Bias	85°C, 85% RH, 5.0 V
Autoclave	121°C, 100% RH, 15 psig
Pressure Temperature Humidity Bias	148°C, 90% RH, 44 psig, 5.0 V
Low Temperature Operating Life	0°C/25°C, 6.0 V

HIGH TEMPERATURE OPERATING LIFE

High temperature operating life (HTOL or HTRB) testing is performed to accelerate failure mechanisms that are thermally activated through the application of extreme temperatures and the use of biased operating conditions. The temperature and voltage conditions used in the stress will vary with the product being stressed. However, the typical stress ambient is 125°C with the bias applied equal to or greater than the data sheet nominal value. All devices used in the HTOL test are sampled directly after final electrical test with no prior burn-in or other prescreening unless called out in the normal production flow. Testing can either be performed with dynamic signals applied to the device or in a static bias configuration.

TEMPERATURE CYCLE

Temperature cycle testing accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed per MIL-STD-883 or MIL-STD-750 with the minimum and maximum temperatures being − 65°C and + 150°C. During temperature cycle testing, devices are inserted into a cycling system and held at the cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minute minimum time period. The system employs a circulating air environment to assure rapid stabilization at the specified temperature. The dwell at each extreme, plus the two transition times of five minutes each (one up to the hot dwell temperature, another down to the cold dwell temperature), constitute one cycle. Test duration for this test will vary with device and packaging system employed.

THERMAL SHOCK

The objective of thermal shock testing is the same as that for temperature cycle testing—to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides additional stress in that the device is exposed to a sudden change in temperature due to the transfer time of ten seconds maximum as well as the increased thermal conductivity of a liquid ambient. This test is typically performed per MIL-STD-883 or MIL-STD-750 with the minimum and maximum temperatures being −65°C and +150°C. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes minimum, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five-minute dwells plus two ten-second transitions constitute one cycle.

---

*All rejects: visual, mechanical, and electrical (dc, ac, and high/low temperature).

TEMPERATURE HUMIDITY BIAS

Temperature humidity bias (THB or H^3TRB) is an environmental test performed at a temperature of 85°C and a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metallization.

AUTOCLAVE

Autoclave is an environmental test which measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Autoclave is a highly accelerated and destructive test.

PTHB (PRESSURE-TEMPERATURE-HUMIDITY-BIAS)

This test is performed to accelerate the effects of moisture penetration with the dominant effect being corrosion. The test detects similar failure mechanisms as THB but at a greatly accelerated rate. Conditions usually employed during the test are a temperature of 148°C, pressure of 44 psig or greater, a relative humidity of 90%, and a bias level which is the nominal rating of the device.

LOW TEMPERATURE OPERATING LIFE

This test is performed primarily to accelerate hot carrier injection effects in semiconductor devices by exposing them to room ambient or colder temperatures with the use of biased operating conditions. Threshold shifts or other parametric changes are typically the basis for failure. The length of this test will vary with temperature and bias conditions employed.

SYSTEM SOFT ERROR

System soft error is designed to detect errors caused by impact ionization of silicon by high energy particles. This stress is performed on a system level basis. The system is operated for millions of device hours to obtain an accurate measure of actual system soft error performance.

MECHANICAL SHOCK

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the ability of the device to withstand a sudden change in mechanical stress typically due to abrupt changes in motion as seen in handling, transportation, or actual use. The typical test condition would be as follows: acceleration = 1500 g, orientation = Y1 plane, t = 0.5 ms, and number of pulses = 5.

VARIABLE FREQUENCY VIBRATION

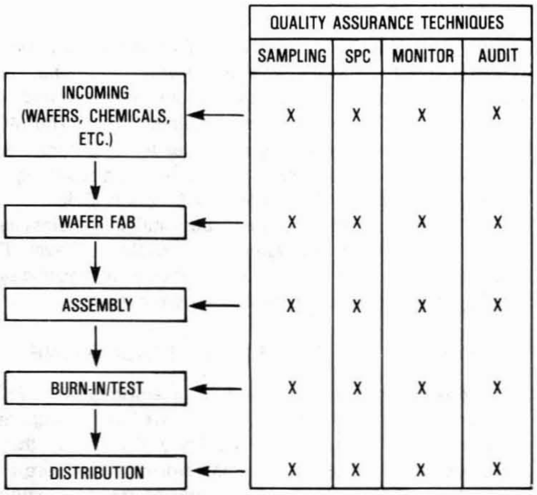
This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the ability of the device to withstand deterioration due to mechanical resonance. The typical test condition is: peak acceleration = 20 g, frequency range = 20 Hz to 20 kHz, and t = 48 minutes.

CONSTANT ACCELERATION

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to indicate structural or mechanical weaknesses in a device/packaging system by applying a severe mechanical stress. A typical test condition used is as follows: stress level = 30 kg, orientation = Y1 plane, and t = 1 minute.

QUALITY SYSTEMS

A Global Quality System is key to achieving our goal of "Best In Class". Quality systems are implemented in wafer fabrication, assembly, final test, and distribution world wide. Figure 3 depicts Quality Assurance involvement and the techniques applied in the general flow of product and Figure 4 shows Memory Manufacturing locations world wide.



	QUALITY ASSURANCE TECHNIQUES			
	SAMPLING	SPC	MONITOR	AUDIT
INCOMING (WAFERS, CHEMICALS, ETC.)	X	X	X	X
WAFER FAB	X	X	X	X
ASSEMBLY	X	X	X	X
BURN-IN/TEST	X	X	X	X
DISTRIBUTION	X	X	X	X

Figure 3. General Product Flow

Direct Customer interaction ensures the receipt of product that meets all of their requirements 100% of the time. In fact, the MOS Memories Reliability and Quality Assurance department has devised a customer advocate list that assigns key Reliability and Quality Assurance personnel to specific customers in order to facilitate any inquiry regarding quality, reliability, or any other issue they may want to discuss.

All processes and procedures that relate to the manufacturing of MOS Memories are fully documented, and regular audits are performed to ensure continuous adherence to proper procedures. We are always striving to produce and reproduce the highest quality product available throughout the world.

MOS Memory Products Division promotes the concept of statistical process controls throughout the entire manufacturing process. This is exemplified by our commitment to in-depth statistical process control training programs for everyone—from the line operator to upper management. Favorable results have already been realized from the initial phases of implementation, with much more to follow.

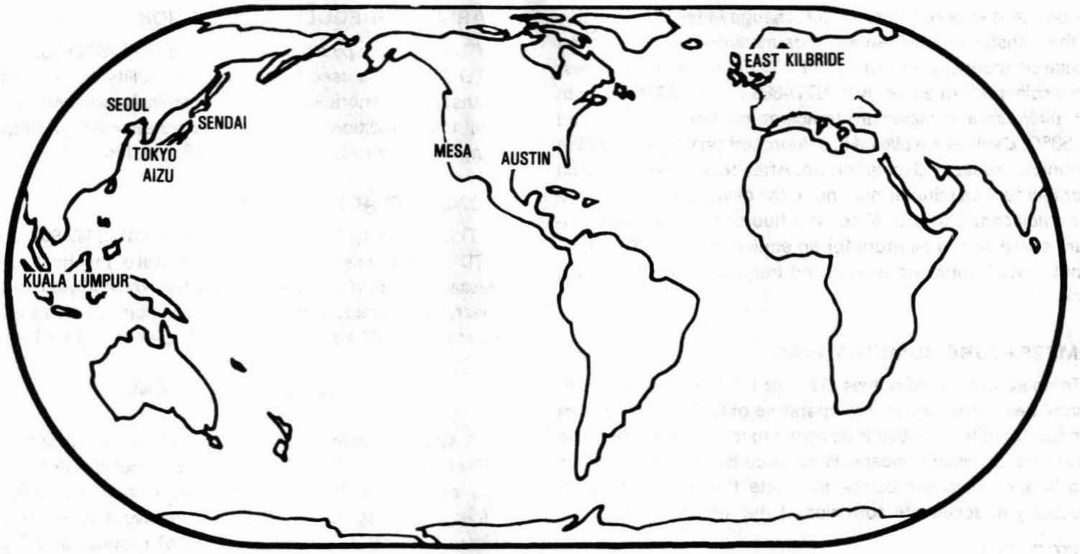


Figure 4. Wafer Fab/Assembly/Final Test Locations

The MOS Memory Products Division maintains a World Wide Quality Assurance system that is second to none. Daily status reports are received from remote locations, and any problems that arise are tackled on a timely basis. The MOS Memory Products Division is also a leader in accurate and efficient methods of quality data collection and reporting.

Every unit that the MOS Memory Products Division produces is coded so that complete traceability is maintained, including visibility to the wafer and assembly lot level. The Quality System ensures that we can provide any specific processing information to our customers on request.

INTERNAL QUALIFICATION DISCIPLINE

Motorola recognizes the need to establish that all MOS Memory devices, both new products as well as existing ones, reach and maintain a level of quality and reliability that is unsurpassed in the electronics marketplace. To ensure this, internal qualification requirements, procedures, and methods as well as vendor qualification specifications have been developed. These activities are intended to provide a consistent, comprehensive, and methodical approach to device qualification and to improve our customer's understanding of Motorola's qualification results and their subsequent application implications.

For qualification results to be valid and acceptable, the collected data must be proven accurate to the highest possible confidence level. Therefore, a complete device history and data log is kept with any lost or missing data potentially leading to test results that are unusable for qualification purposes. Testing conditions and pass/fail criteria are established before stressing begins. Strict adherence to these criteria and the use of control devices insure that the test results are valid and meaningful.

New MOS Memory devices which are under development or in the prototype stage are subject to requirements defined for the three levels of the development cycle. These levels are the alpha, beta, and introductory phases of device development. Each phase contains guidelines and controls concerning issues such as device labeling, number of customers, sample quantities, pricing and stocking levels, and open-order-entry timing. Decisions regarding these items are made jointly by marketing, design, product, and reliability personnel.

JOINT QUALIFICATION

As a result of the rigorous discipline used for internal qualification of Motorola MOS Memory products, our customers can benefit from joint qualification activities. Motorola's clearly defined qualification procedures improve the customer's ability to comprehend the qualification results in an effective manner which aides in their qualification decision making process. Through parallel qualification activities between Motorola and its customers, this procedure can cut qualification costs by reducing duplication of effort, improving resource utilization, and shortening introduction cycle time. This helps to ensure competitive edge advantages for our customers.

Joint Qualification activities result in a partnership type of interaction between Motorola and its customers on an engineering level. This assists our customers in two critical areas. First, it allows them to understand more clearly the strengths and weaknesses of Motorola's products. Secondly, our customers can make clear decisions concerning which stresses they need to concentrate on during their internal qualification activities.

HISTORICAL PERFORMANCE

Over the course of the last five years, significant achievements have been made on quality and delivery performance. The Six Sigma methodology will assist the MOS Memory Products Division in pursuit of our standard of zero defects and 100% on time delivery.

Figure 5 indicates the product Average Outgoing Quality performance as measured in parts per million.

As of October 1988 our average outgoing quality was below 50 parts per million. We are striving to reach Six Sigma.

1988 MALCOLM BALDRIGE NATIONAL QUALITY AWARD

Motorola won the first Malcolm Baldrige National Quality Award. The award recognizes the achievements of U.S. manufacturing and service companies. The award was established in 1987 to promote quality awareness, recognize the achievements of U.S. companies, and publicize successful quality strategies. Our quality process was examined for corporate quality leadership, information and analysis, planning, human resource utilization, quality assurance, quality improvement results, and Customer Satisfaction. Our fundamental objective—Everyone's overriding responsibility is Total Customer Satisfaction. Six Sigma Quality is a key initiative for the achievement of our fundamental objective.

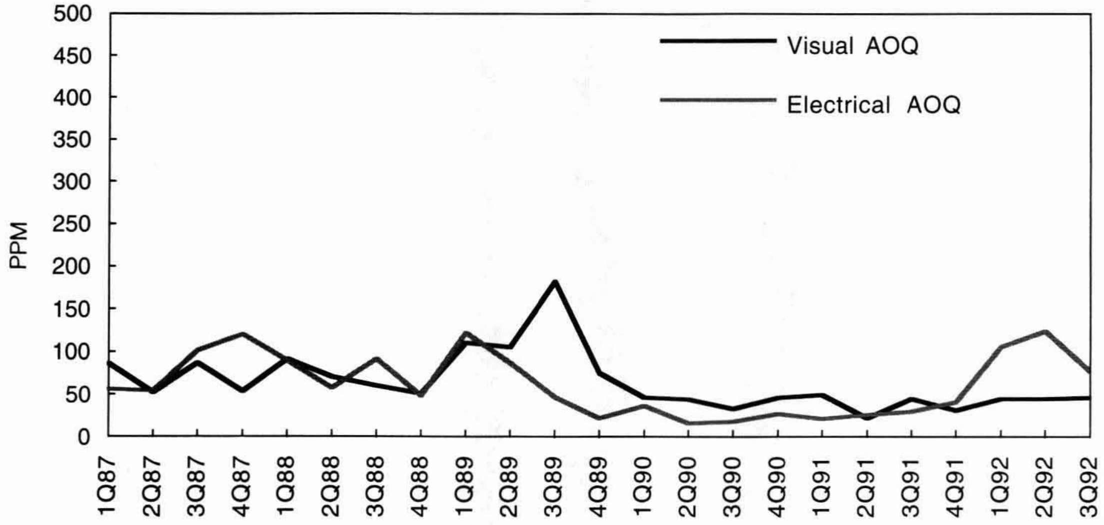


Figure 5. Motorola MOS Memory Products Division Average Outgoing Quality

AN986 Page, Nibble, and Static Column Modes: High-Speed, Serial-Access Options on 1M-Bit + DRAMs 9-3
AN987 DRAM Refresh Modes 9-7
AN1124 1M to 4M DRAM Upgrading 9-9
AN1125 DRAM Interface to the MC88200 M Bus .. 9-11
AN1127 High Speed DRAM Design for the 40 MHz MC68EC030 9-50
AN1202 Battery Backup of Self-Refreshing Dynamic Random Access Memory 9-67

Applications Information

9

9

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN986

Page, Nibble, and Static Column Modes: High-Speed, Serial-Access Options on 1M-Bit+DRAMs

The 1M-bit and higher density DRAMs offered by Motorola, in addition to operating in a standard mode at advertised access times, have special operating modes that will significantly decrease access time. These are page, nibble, and static column modes. All three modes are available in the 1M × 1 configuration; page and static column modes are also available on the 256K × 4 configuration. Read, write, and read-write operations can be mixed and performed in any order while these devices are operating in either random or special mode.

The comments that follow refer specifically to successive read operations for page, nibble, and static column modes on the 1M × 1 device. The read operation is chosen for sake of simplicity in illustrating these special operating modes. However, decreased access times will occur for all operations, performed in any order, when the device is operated in any of these modes. General operating comments apply to the 256K × 4 device as well.

All of these special operating modes are useful in applications that require high-speed serial access. Typical examples include video bit map graphics monitors or RAM disks. Page mode is the standard, available since the days of the 16K × 1 DRAM. Static column is the latest mode to be made available on DRAMs, and nibble mode first appeared somewhere in between. Page and static column offer the same column location access, but operate somewhat differently. Nibble is unlike either of the other modes, but faster than both in its niche. All modes are initiated after a standard read or write is performed.

Page and static column modes allow access to any of 1024 column locations on a specific row, while nibble allows access to a maximum of four bits. The location of the first bit in nibble mode determines the other bits to be accessed. Nibble mode allows the fastest access of the three devices (t_{NCAC}), all other parameters held equal, at about 1/4 the standard (t_{RAC}) rate. Page and static column access times (t_{CAC}, t_{AA}) are, respectively, about 1/3 and 1/2 the standard rate.

Cycle time is a better indicator of relative speed improvement, since it measures the minimum time between any two successive reads. Cycle time is approximately 1/4 for nibble and 1/3 for page and static column modes, with respect to a

Table 1. Operating Characteristic Comparison

Parameter		Page	Nibble	Static Column	Random
Access Time (ns)*	t_{CAC}	25	—	—	—
	t_{NCAC}	—	20	—	—
	t_{AA}	—	—	45	—
	t_{RAC}	—	—	—	85
Cycle Time (ns)*	t_{PC}	50	—	—	—
	t_{NC}	—	40	—	—
	t_{SC}	—	—	50	—
	t_{RC}	—	—	—	165
Accessible Bits		1024	4	1024	All
Order of Accessible Bits		Random	Fixed	Random	Random
Conditions	$\overline{RAS}$	Active	Active	Active	Cycle
	$\overline{CAS}$ or $\overline{CS}$**	Cycle	Cycle	Active	Cycle
	Addresses	Cycle	N/A	Cycle	Cycle
	Outputs	Cycle	Cycle	Active	Cycle
Time to Read 4 Bits (ns)*		235	205	235	660
Time to Read 1024 Unique Bits (ns)*		51,235	70,400	51,235	168,960

*Values for a 1M × 1 85-ns device.

**$\overline{CS}$ on Static Column.

Page: 4 bit read = $t_{RAC} + 3t_{PC}$
1024 bit read = $t_{RAC} + 1023t_{PC}$

Nibble: 4 bit read = $t_{RAC} + 3t_{NC}$
1024 bit read = $256 \cdot (t_{RAC} + 3t_{NC} + t_{RP})$

Static Column: 4 bit read = $t_{RAC} + 3t_{SC}$
1024 bit read = $t_{RAC} + 1023t_{SC}$

Random: 4 bit read = $4t_{RC}$
1024 bit read = $1024t_{RC}$

random cycle time of 165 nanoseconds. When operated in these high-speed modes, users will typically access most or all of the bits available to that mode, once the mode has been initiated. Thus the best measure of speed for nibble mode is the rate at which four bits are read, while the rate at which 1024 bits are read is the best measure of page or static column mode. When the actual operating conditions are considered, as described elsewhere, the difference between t_{CAC}, t_{NCAC}, and t_{AA} measurements hold relatively little significance.

Page mode is slightly more difficult to interface in a system than static column mode due to extra $\overline{\text{CAS}}$ pulses that are required in page mode. Static column generates less noise than page mode, because output buffers and $\overline{\text{CS}}$ are always active in this mode. Noise transients, generated every time $\overline{\text{CAS}}$ is cycled from inactive to active, are thus eliminated in the static column mode.

PAGE MODE

Page mode allows faster access to any of the 1024 column locations on a given row, typically at one third the standard (t_{RAC}) rate for randomly-performed operations. Page mode consists of cycling the $\overline{\text{CAS}}$ clock from active (low) to inactive (high) and back, and providing a column address, while holding the $\overline{\text{RAS}}$ clock active (low). A new column location can be accessed with each $\overline{\text{CAS}}$ cycle (t_{PC}).

Page mode is initiated with a standard read or write operation. Row address is latched by the $\overline{\text{RAS}}$ clock transition to active, followed by column address and $\overline{\text{CAS}}$ clock active. Performing a $\overline{\text{CAS}}$ cycle (t_{PC}) and supplying a column address while $\overline{\text{RAS}}$ clock remains active constitutes the first page mode cycle. Subsequent page mode cycles can be performed as long as $\overline{\text{RAS}}$ clock is active. The first access (data valid) occurs at the standard rate (t_{RAC}). All of the read operations in page mode following the initial operation are measured at the faster rate (t_{CAC}), provided all other timing minimums are maintained (see Figure 1a). Page mode cycle time determines how fast successive bits are read (see Figure 1b).

NIBBLE MODE

Nibble mode allows serial access to two, three, or four bits of data at a much higher rate than random operations (t_{RAC}). Nibble mode consists of cycling the $\overline{\text{CAS}}$ clock while holding the $\overline{\text{RAS}}$ clock active, like page mode. Internal row and column address counters increment at each $\overline{\text{CAS}}$ cycle, thus no external column addresses are required (unlike page or static column modes). After cycling $\overline{\text{CAS}}$ three times in nibble mode, the address sequence repeats and the same four bits are accessed again, in serial order, upon subsequent cycles of $\overline{\text{CAS}}$:

00, 01, 10, 11, 00, 01, 10, 11, . . .

Nibble mode operation is initiated with a standard read or write cycle. Row address is latched by $\overline{\text{RAS}}$ clock transition to active, followed by column addresses and $\overline{\text{CAS}}$ clock. Performing a $\overline{\text{CAS}}$ cycle (t_{NC}) while $\overline{\text{RAS}}$ clock remains active constitutes the first nibble mode cycle. Subsequent nibble mode cycles can be performed as long as the $\overline{\text{RAS}}$ clock is held active. The first access (data out) occurs at the standard rate (t_{RAC}). All of the read operations in nibble mode following the initial operation are measured at the faster rate (t_{NCAC}), provided all other timing minimums are maintained (see Figure 2a). Nibble mode cycle time determines how fast successive bits are read (see Figure 2b).

STATIC COLUMN MODE

This mode is useful in applications that require less noise than page mode. Output buffers are always on when the device is in this mode and $\overline{\text{CS}}$ clock is not cycled, resulting in fewer transients and simpler operation. It allows faster access to any of the 1024 column addresses on a given row, typically at half the standard (t_{RAC}) rate for randomly performed operations. Static column consists of changing column addresses while holding the $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ clocks active. A new column location can be accessed with each static column cycle (t_{SC}).

Static column mode operation is initiated with a standard read or write cycle. Row address is latched by $\overline{\text{RAS}}$ clock transition to active, followed by column addresses and $\overline{\text{CS}}$ clock. Performing an address cycle (t_{SC}) while $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ clocks remain active constitutes the first static column cycle. Subsequent static column cycles can be performed as long as the $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ clocks are held active. The first access (data out) occurs at the standard (t_{RAC}) rate. All of the read operations in static column following the initial operation are measured at the faster rate (t_{AA}), provided all other timing minimums are maintained (see Figure 3a). Static column cycle time determines how fast successive bits are read (see Figure 3b).

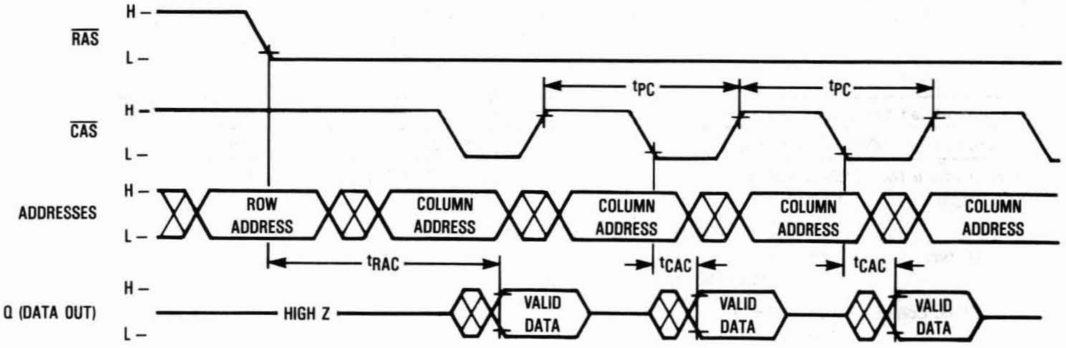


Figure 1a. Page Mode Read Cycle

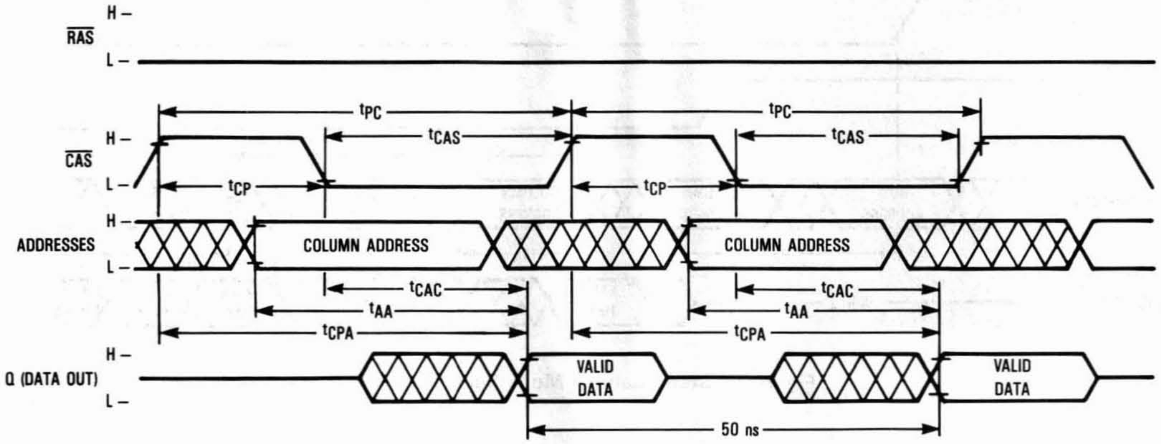

H –
RAS
L –
tPC
tPC
H –
CAS
L –
tCAS
tCAS
tCP
tCP
H –
ADDRESSES
L –
COLUMN ADDRESS
COLUMN ADDRESS
tCAC
tCAC
tAA
tAA
tCPA
tCPA
H –
Q (DATA OUT)
L –
VALID DATA
VALID DATA
50 ns

Figure 1b. Page Mode Cycle Minimum Timing

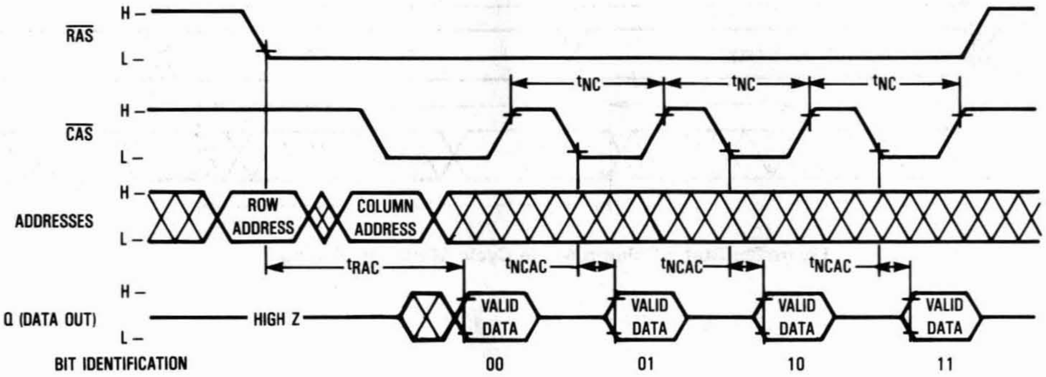

H –
RAS
L –
tNC
tNC
tNC
H –
CAS
L –
H –
ADDRESSES
L –
ROW ADDRESS
COLUMN ADDRESS
tRAC
tNCAC
tNCAC
tNCAC
H –
Q (DATA OUT)
L –
HIGH Z
VALID DATA
VALID DATA
VALID DATA
VALID DATA
BIT IDENTIFICATION
00
01
10
11

Figure 2a. Nibble Mode Read Cycle

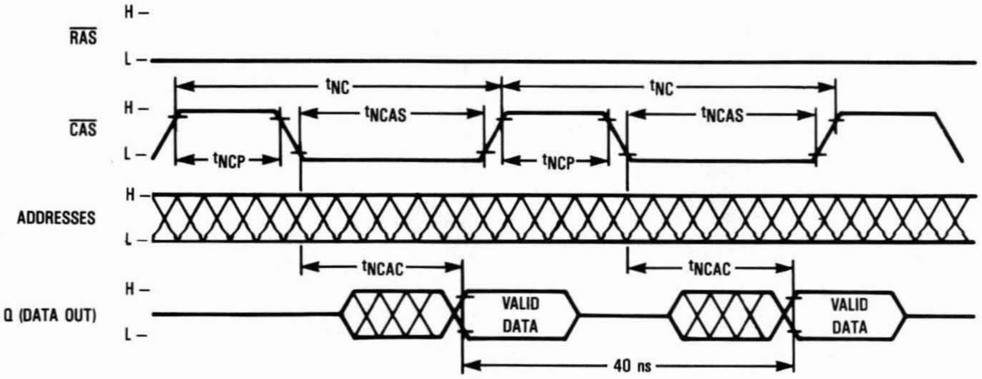

H –
RAS
L –
tNC
tNC
H –
CAS
L –
tNCAS
tNCAS
tNCP
tNCP
H –
ADDRESSES
L –
tNCAC
tNCAC
H –
Q (DATA OUT)
L –
VALID DATA
VALID DATA
40 ns

Figure 2b. Nibble Mode Cycle Minimum Timing

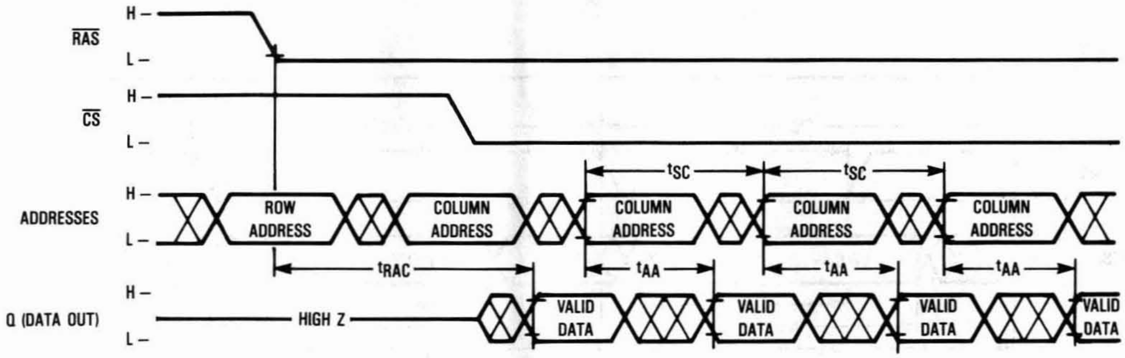

RAS
H –
L –
CS
H –
L –
ADDRESSES
H –
L –
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
t_{SC}
t_{SC}
t_{RAC}
t_{AA}
t_{AA}
t_{AA}
Q (DATA OUT)
H –
L –
HIGH Z
VALID DATA
VALID DATA
VALID DATA
VALID DATA

Figure 3a. Static Column Mode Read Cycle

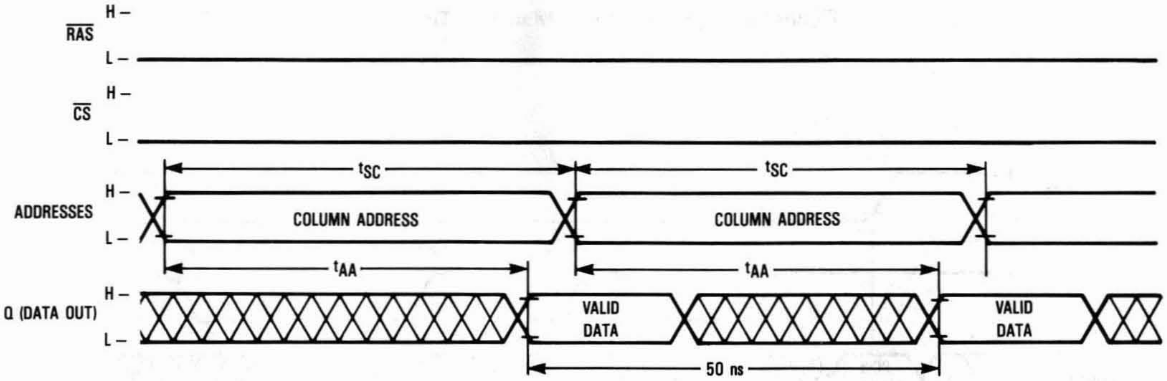

RAS
H –
L –
CS
H –
L –
ADDRESSES
H –
L –
t_{SC}
t_{SC}
COLUMN ADDRESS
COLUMN ADDRESS
t_{AA}
t_{AA}
Q (DATA OUT)
H –
L –
VALID DATA
VALID DATA
50 ns

Figure 3b. Static Column Mode Cycle Minimum Timing

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN987

DRAM Refresh Modes

DRAMs offer the lowest cost per bit of any memory, and for that reason are enormously popular in a wide range of applications. This low cost per bit is achieved with a very simple bit cell design, among other things, but rooted in this simplicity are some inherent drawbacks. One major limitation is the need to refresh each memory bit at regular intervals. This note discusses what refresh is, the reasons refresh is required for DRAM operation, and the various types of refresh available on the Motorola 1M × 1 and 256K × 4 DRAMs. Specific comments refer to the 1M × 1 85-ns DRAM. Refer to specific device data sheets for analogous information on other devices.

The heart of any memory device is the bit cell. A 1M DRAM has 1,048,576 of these cells in the memory array. Each cell holds a single bit of information in the form of a high or low voltage, where high voltage = a binary "1" and low voltage = a binary "0". The DRAM bit cell consists of one transistor and one capacitor. The transistor acts as a switch, regulating when the capacitor will charge and discharge, while the capacitor stores a high or low voltage charge.

All capacitors leak over time, slowly losing the charge stored in them, regardless of how carefully they are constructed. Junction and dielectric leakage are two capacitor discharge paths that are characteristic of the DRAM bit cell, and both are affected by temperature. The capacitor in the bit cell can hold a small charge, on the order of 35-125 fF ($fF = 1 \times 10^{-15}$ farads). As this charge dissipates through leakage paths, the small difference between a "1" and a "0" diminishes. If nothing is done to restore the charge on the capacitor to its initial value, the sensing circuitry on the DRAM will eventually be unable to detect a charge difference and will read the cell as a "0".

Thus, all the capacitors in the memory array must be periodically recharged, or refreshed. Refresh is accomplished by accessing each row in the array, one row at a time. When a row is accessed, it is turned on, and voltage is applied to the row, recharging each capacitor on the row to its initial value. Specified refresh time on the 1M × 1 DRAM is 8 milliseconds; every row must be recharged every 8 milliseconds. This is a vast improvement over refresh times required for earlier generations of DRAMs. The 16K × 1 DRAM required refresh every 2 milliseconds, the 256K × 1 DRAM requires a refresh every 4 milliseconds. Longer refresh times mean more time available for access to memory, and less time required to refresh the device.

Design and operation of the DRAM allow only one row to be refreshed at a time; 512 refresh cycles are required to refresh the entire 1M × 1 memory array. The array is actually 1024 rows by 1024 columns, but it operates electrically like two half arrays of 512 rows by 1024 columns. During refresh, every row is treated as if it runs through both halves of the array, refreshing 2048 column locations (bit cells) per row. This design results in fewer refresh cycles required to recharge the entire array, since only 512 rows need to be accessed, rather than 1024.

Refresh can be performed in either a single **burst** of 512 consecutive refresh cycles (one cycle per row) every 8 milliseconds, or **distributed** over time, one refresh cycle every 15 microseconds (8 milliseconds per 512 rows = 15.6 microseconds per row) on average, or some combination of these two extremes. As long as every row is refreshed within 8 milliseconds, the actual method used is best determined by system use of the DRAM. The burst takes 84 microseconds to complete (165 nanoseconds per row × 512 rows for 85 nanoseconds per device). During this burst refresh time, no memory operations can be performed on the device. Distributed refresh disables memory access for 165 nanoseconds every 15 microseconds.

The 1M × 1 DRAM can be refreshed in three ways: $\overline{\text{RAS}}$ only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, and hidden refresh. In addition, any normal read or write refreshes all 2048 bit cells on the row accessed. Regardless of the refresh method used, the time required to refresh one row is the random read or write ($\overline{\text{RAS}}$) cycle time (t_{RC}). When operating the device in page, nibble, or static column mode, only the row being accessed is refreshed. The device must be in normal random mode to utilize any of these specific refresh methods.

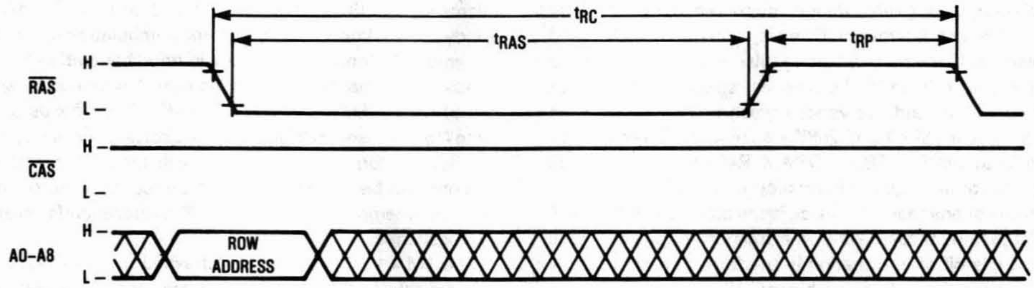
$\overline{\text{RAS}}$ only refresh requires external row counters, to ensure all rows are refreshed within the specified time, and externally-supplied row addresses. $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ relies on internal row counters and internally generates the address of the next row to be refreshed. Hidden refresh is a variation on $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh that holds valid data at the output while refresh is occurring. Whenever the device is in a refresh cycle, neither a read nor a write operation can be performed. Hidden refresh allows the device to be read ahead of refresh, then holds the valid data at the output while refresh cycles are in progress. It appears that the refresh is hidden among data cycles because valid data is maintained at the output.

$\overline{\text{RAS}}$ only refresh is performed by supplying row addresses A0–A8 and completing a $\overline{\text{RAS}}$ cycle (t_{RC}); switching $\overline{\text{RAS}}$ from inactive (high) to active (low), holding $\overline{\text{RAS}}$ low (t_{RAS}), then switching back to high, and holding $\overline{\text{RAS}}$ high (t_{RP}). A9 is ignored during $\overline{\text{RAS}}$ only refresh, since this address normally determines which half of the array is to be accessed. $\overline{\text{CAS}}$ must be held high through this $\overline{\text{RAS}}$ cycle, hence the name $\overline{\text{RAS}}$ only refresh. An external row counter is required for this refresh method. See Figure 1.

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is performed by switching $\overline{\text{CAS}}$ from high to low while $\overline{\text{RAS}}$ is high, then switching $\overline{\text{RAS}}$ low (t_{CSR}). This reversal of the usual clock order activates an internal row counter that generates addresses to be refreshed; external addresses are ignored in this cycle. $\overline{\text{CAS}}$ must be held low (t_{CHR}) after $\overline{\text{RAS}}$ transitions to low. After that time it can either be held low or switched to high. See Figure 2. The $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, specified on all DRAM data sheets that offer this type of refresh, is used to check for proper operation of the internal row counters and correct address generation.

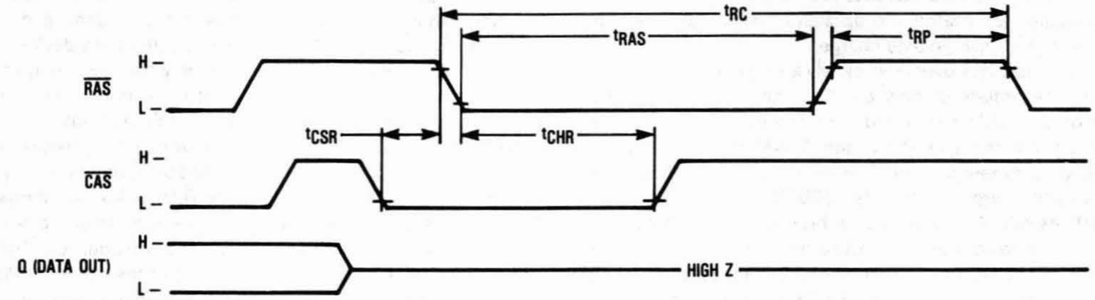
Hidden refresh is a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh that has been initiated during a read or write operation. At the end of a typical read cycle, $\overline{\text{CAS}}$ would be switched to high before $\overline{\text{RAS}}$, turning off the output. In a hidden refresh cycle, $\overline{\text{RAS}}$ is switched to high, concluding the $\overline{\text{RAS}}$ cycle (t_{RC}), while $\overline{\text{CAS}}$ is held low. $\overline{\text{RAS}}$ is held high (t_{RP}), then switched low, beginning another $\overline{\text{RAS}}$ cycle. As long as $\overline{\text{CAS}}$ is held low, data is valid at the output, resulting in a long read cycle. Since data can be read while the device is being refreshed, the refresh operation(s) appears to be hidden by the read cycle. The same refresh can be performed after a write cycle is initiated. This method of refresh allows refresh cycles to be mixed within read and write cycles. During the refresh cycle, a write operation cannot be performed. See Figure 3.

Refresh is an integral and necessary part of DRAM operation. Substantial improvement has been made in increasing the time between refresh cycles, but as long as the bit cell design utilizes a capacitor, periodic recharging will be required. Three methods of refresh are available on the 1M × 1 DRAM: $\overline{\text{RAS}}$ only, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, and hidden refresh. The Motorola 1M × 1 and 256K × 4 will work in virtually all systems as a result of flexibility provided by this assortment of refresh methods.



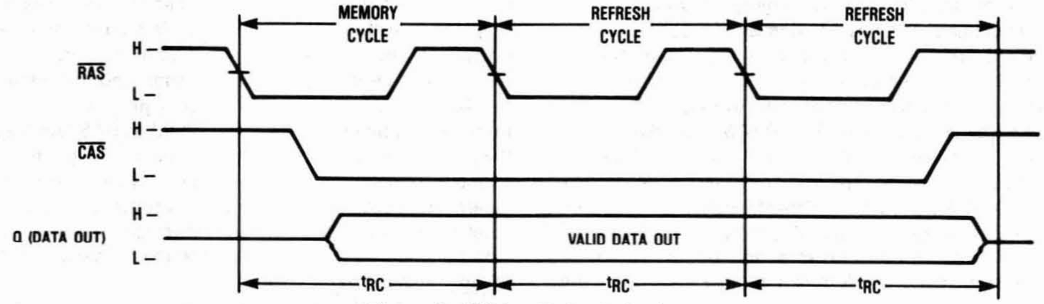
tRC
tRAS
tRP
H –
RAS
L –
H –
CAS
L –
H –
A0–A8
L –
ROW ADDRESS

Figure 1. $\overline{\text{RAS}}$ Only Refresh Cycle



tRC
tRAS
tRP
H –
RAS
L –
tCSR
tCHR
H –
CAS
L –
H –
Q (DATA OUT)
L –
HIGH Z

Figure 2. $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



MEMORY CYCLE
REFRESH CYCLE
REFRESH CYCLE
H –
RAS
L –
H –
CAS
L –
H –
Q (DATA OUT)
L –
VALID DATA OUT
tRC
tRC
tRC

Figure 3. Hidden Refresh Cycle

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN1124

1M to 4M DRAM Upgrading

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INTRODUCTION

Standards set through JEDEC and EIAJ allow upward compatibility from the 1M to 4M DRAM by using the same pinout for SOJ and ZIP packages. Such standards are set to ensure a stable DRAM supply when higher density memories are introduced. This eliminates the need for expensive redesigns of systems that can utilize the new memories.

Although the common pinout between the 1M and 4M DRAM requires little, if any, relayout of the PCB, caution must be exercised when upgrading because of potential incompatibilities with refresh and power up. Both of these involve differences in test mode entry between the 1M and 4M DRAM.

REFRESH

The dynamic memory cell is based on capacitor charge storage for each bit in the array. This charge will dissipate over time, so the entire array must periodically be refreshed to maintain the correct bit state. This is accomplished by cycling through all the rows of the array within a specified refresh time.

The 4M DRAM has 1024 rows instead of the 1M's 512 rows. Since the refresh period of the 4M is twice that of the 1M DRAM, the equivalent wait state of the 4M is the same as that of the 1M. This is summarized in Table 1.

Like the 1M DRAM, the 4M DRAM can be refreshed through a variety of ways: any read or write cycle, a RAS-only refresh, a CAS before RAS refresh, or a hidden refresh. A potential incompatibility between the 1M and 4M DRAM exists with the use of the CAS before RAS refresh.

On the 1M DRAM, the W pin is specified as a don't care during the CAS before RAS refresh. But on the 4M DRAM, the W pin must be high (disabled) for time t_{WRP} before RAS goes low and held high for time t_{WRH} after the transition. This will prevent the device from entering the JEDEC standard test mode. Figure 1 shows the CAS before RAS refresh timing for the 4M DRAM, and Figure 2 shows the test mode entry timing. The test mode is exited by performing either a RAS-only refresh cycle or a CAS before RAS refresh cycle. Test mode on the 1M DRAM is entered through use of a "supervoltage" on a separate test function pin, and is therefore completely unlike the 4M test mode entry.

POWER UP

Another potential incompatibility between the 1M and 4M DRAM occurs during the power up, and this must be addressed when upgrading. Both devices require a pause of 200 µs after power up, followed by 8 RAS cycles before proper device operation is guaranteed. The pause allows the internal substrate generator to establish the correct bias voltage. The 8 RAS cycles initialize all dynamic nodes within the RAM.

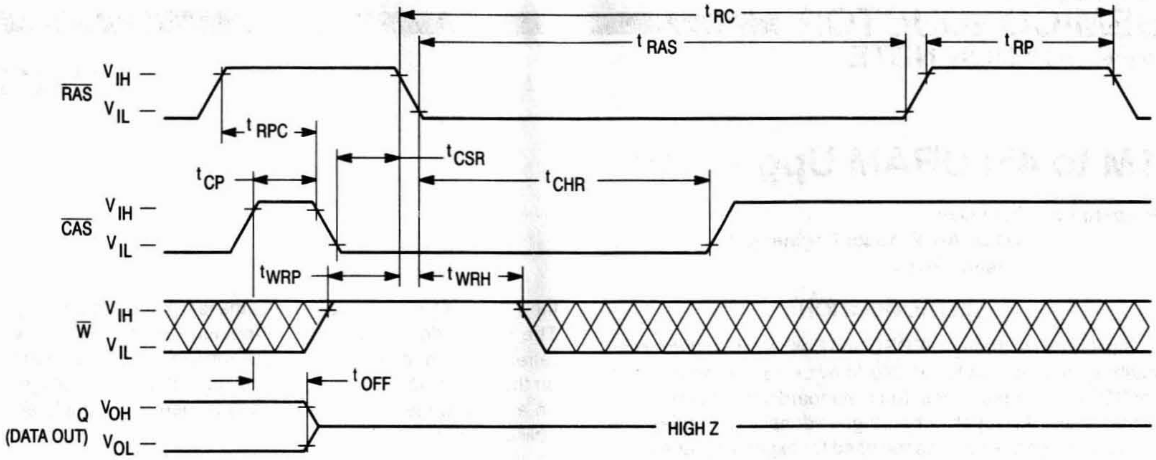
To prevent the 4M DRAM from entering the test mode, the 8 RAS cycles should be RAS-only refresh cycles or CAS before RAS refresh cycles. If these refresh modes are not used, the device could power up in the test mode, which can only be exited by performing a RAS-only refresh cycle or a CAS before RAS refresh cycle.

SUMMARY

Upgrading a system from a 1M DRAM to a 4M DRAM is easily accomplished if a few precautions are taken. The CAS before RAS refresh mode on the 4M DRAM requires that W be high during the RAS low transition. If W is a don't care, as on the 1M DRAM, the test mode could inadvertently be entered. Caution with the 4M DRAM must also be exercised during the power up. The 8 initialization cycles should be either RAS-only refresh cycles or CAS before RAS refresh cycles, so that the device comes up in its normal operating mode and not in the test mode.

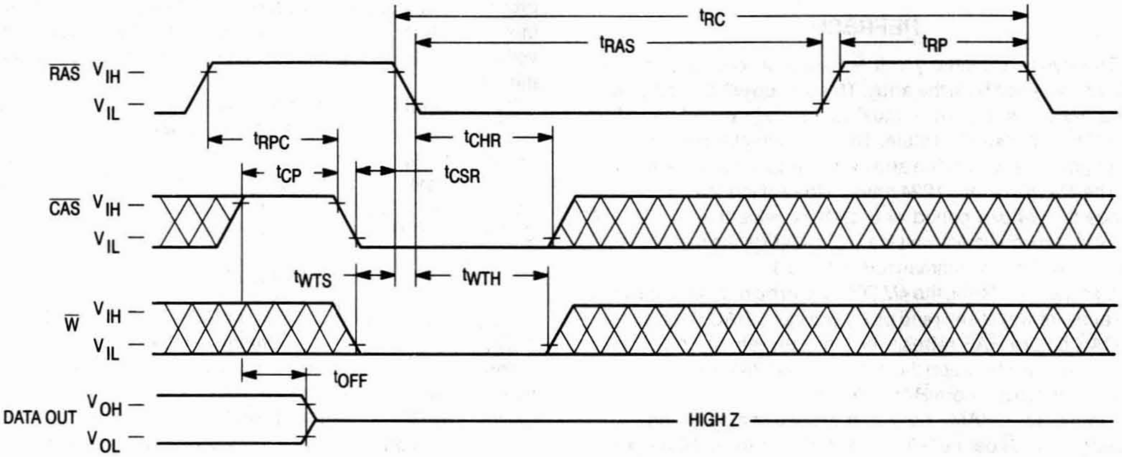
Table 1. Comparison of Refresh Requirements for the 4M and 1M DRAM
(Times Shown are for Devices with 70 ns Random Access Times)

	4M		1M	
	Normal Power	**Low Power**	**Normal Power**	**Low Power**
Number of Rows	1024	1024	512	512
Number of Bits per Row	4096	4096	2048	2048
Refresh Period (t_{RFSH})	16 ms	128 ms	8 ms	64 ms
Distributed Refresh Period	15.6 µs	124.8 µs	15.6 µs	124.8 µs
Burst Refresh Period	16 ms	128 ms	8 ms	64 ms
Time to Refresh 1 Row (t_{RC})	130 ns	130 ns	130 ns	130 ns
Cumulative Time to Refresh the Entire Array	133.1 µs	133.1 µs	66.6 µs	66.6 µs
Refresh Time/Operating Time	0.833%	0.104%	0.833%	0.104%



t RC
t RAS
t RP
RAS
V IH
V IL
t RPC
t CSR
t CP
t CHR
CAS
t WRP
t WRH
W
t OFF
Q
(DATA OUT)
V OH
V OL
HIGH Z

Figure 1. $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Timing for the 4M DRAM
(Addresses and $\overline{\text{G}}$ are Don't Care)



t RC
t RAS
t RP
RAS
V IH
V IL
t RPC
t CHR
t CP
t CSR
CAS
t WTS
t WTH
W
t OFF
DATA OUT
V OH
V OL
HIGH Z

Figure 2. Test Mode Entry Timing for the 4M DRAM

MOTOROLA
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APPLICATION NOTE

AN1125

Application Note

DRAM Interface to the MC88200 M Bus

This document describes the design and operation of a 25 to 33.3 MHz dynamic random-access memory (DRAM) interface to the M Bus of the Motorola MC88200 Cache/Memory Management (CMMU) Device. The memory interface is divided into two sub-systems: a CPU sub-system and a memory sub-system. The CPU sub-system includes one MC88100 CPU and two MC88200 CMMUs. The memory sub-system contains a DRAM array (which consists of two non-interleaved, 32-bit wide banks of single in-line memory module (SIMM) devices with byte parity) and a DRAM controller. The DRAM controller is implemented using programmable array logic (PAL), a Xilinx (a gate array), and discrete hardware. The memory sub-system is capable of parity generation and checking, automatic refresh, and burst mode accesses.

The memory interface system described in this document has been extracted from a larger application; therefore, some parts of the system are implemented in peripheral devices that are not discussed in this document. This design has been successfully implemented; however, it is not the only possible configuration of a memory interface to the MC88200.

The audience of this document is intended to be hardware systems designers with some knowledge of the M88000 family and some familiarity with DRAMs.

NOTE

> In this application note, assertion and negation are used to specify forcing a signal to a particular state. In particular, the terms assertion and assert refer to a signal that is active or true; negation and negate indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent. Throughout this document, active high signals are denoted by the signal name (i.e., SIGNAL), and active low signals are denoted by the signal name with an overbar (i.e., $\overline{\text{SIGNAL}}$.)

DESIGN OBJECTIVES

There were three objectives for this design. The first was to make a high performance system while limiting the cost of hardware and the board space used. The next was to protect data integrity using parity. The final objective was to make the design flexible.

The first objective was not quantifiable, but provided a general guideline for the design. Some performance enhancements such as interleaved memory and pipelined data paths could have been added to the design. However, each of these enhancements would have added a considerable amount to the total system cost and the board space used.

Parity checking was included in the design to protect data integrity on read accesses. Parity checking can be performed in series or in parallel. With series parity checking, the processor read is delayed until after parity evaluation has been performed on the data. In parallel parity checking, the processor reads the data first and is notified after the read whether the data is invalid; thus, parallel parity detection minimizes the read cycle latency relative to sequential parity checking. However, parallel parity checking is somewhat more complicated than sequential checking because with parallel checking the system must interrupt the processor after an error is detected. Also, with parallel parity checking, the memory location of the parity error must be stored since the CPU may already have begun executing another instruction when the interrupt is received. Parallel parity checking was used in this memory interface system. The higher performance of parallel checking relative to serial checking outweighed the cost of the few extra components needed for parallel checking.

The last objective of the design was to make this system flexible. By using programmable logic, some areas of the system have been designed to allow flexibility. For example, this design supports both page- and nibble-mode DRAMs to allow the end user the choice based on price and availability. Also, included in this system is the flexibility to add up to two more banks of DRAMs with little change to the control logic.

OVERVIEW

The DRAM interface system consists of a CPU sub-system and a memory sub-system (see Figure 1). An overview of these two sub-systems is given in the following paragraphs.

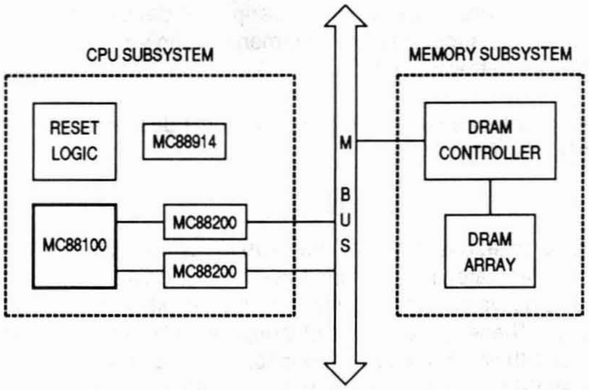


Figure 1. Functional Block Diagram of the DRAM Interface

CPU SUB-SYSTEM

The CPU sub-system contains one MC88100 CPU, two MC88200 CMMUs, system reset logic, and an MC88914 low skew CMOS clock driver. The MC88100 CPU is the engine for the system. The MC88200 devices provide high speed caching for both the instruction and data busses, facilitating no-wait-state memory operations for the MC88100. Each MC88200 device contains 16 KBytes of 4-way set associative cache as well as a two-level, demand-paged memory management unit and support for shared-memory multiprocessing.

The MC88914 low skew CMOS clock driver is used to synchronize the clock inputs for the CPU and two CMMUs and to generate the system clock. The MC88914 is supplied with a 50 or 66.6 MHz oscillator. The clock driver divides the frequency in half, and generates multiple, synchronized 25 or 33.3 MHz frequency clock signals. The outputs of the MC88914 are guaranteed to provide duty cycles and rise and fall times which meet the specifications of the CPU and CMMUs.

The M Bus signals interface the MC88200s to the memory system. The M Bus is a shared, multiplexed bus that accesses memory and memory-mapped peripheral devices. The M Bus includes a bus arbitration scheme that grants bus ownership to a single M Bus master. Table 1 lists the M Bus signals.

Table 1. M Bus Signals

Signal Name	Mnemonic	Type	Active
Bus Request	BR	Output	High
Bus Grant	BG	Input	High
Bus Acknowledge	BA	Output	High
Address/Data	AD31–AD0	I/O	High
Address/DataParity	ADP31–ADP0	I/O	High
Local Status	ST3–ST0	I/O	High
System Status	SS3–SS1	Input	Low

The four system status signals ($\overline{\text{SS3}}$–$\overline{\text{SS1}}$) provide the M bus master with a status reply which is generated by M bus slaves to reflect the status of the M bus. Table 2 lists the values of these signals. The local system status signals (ST3–ST0) of the two CMMUs and the OK and WAIT signals generated by the memory controller are wire-ORed together to produce the system status signals.

Table 2. M Bus System Status Signals

Status	SS3	$\overline{\text{SS2}}$	$\overline{\text{SS1}}$	$\overline{\text{SS0}}$
Error	0	x	x	x
Retry	1	0	x	x
Wait	1	1	0	x
End of Data (Data Phase)	1	1	1	0
OK (Phase Completed)	1	1	1	1

The M bus has control signals (C6-C0) which specify read and write operations, establish exclusive resource usage (locks), inhibit external caching, signal bus errors, and provide initialization. C0 indicates whether an MC88200 read or write cycle is in the address phase or data phase: when C0 is asserted, the MC88200 is in the address phase, and when C0 is negated, the MC88200 is in the data phase. Control signals C6-C1 have different meanings during the address and data phases of a cycle. A description of the control signals and their significance during address and data phases is provided in Table 3.

Table 3. MC88200 MBus Control Signals

Signal	Description
Address Phase (C0 Asserted)	
C1	Intent to Modify. Asserted if the transaction is a memory write or a read with intent to modify. This signal is used for data cache coherency control.
C2	Asserted for memory read. Negated for memory write.
C3	Lock. Asserted to lock out all other M bus devices.
C4	Cache Inhibit. Asserted if the MC88200 cannot cache the data transferred during the current memory access.
C5	Global. Asserted if the address's memory location may be shared by more than one MC88200.
C6	Reserved. Driven as zero.
Data Phase (C0 Negated)	
C1	Last data transfer. Asserted if the current data phase completes the transfer.
C2	Asserted for memory read. Negated for memory write.
C3	M Bus Byte Enable 3. Asserted if AD31–AD24 contain significant data.
C4	M Bus Byte Enable 3. Asserted if AD23–AD16 contain significant data.
C5	M Bus Byte Enable 3. Asserted if AD15–AD8 contain significant data.
C6	M Bus Byte Enable 3. Asserted if AD7–AD0 contain significant data.

MEMORY SUB-SYSTEM

The memory sub-system contains address latches, a DRAM array, data latches, parity generators and checkers, refresh logic, main memory control logic, and row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$) generation for the DRAM. The DRAM addresses are latched because addresses on the M bus are not held valid across clock edges. The outputs to the latches are always enabled in order to minimize access times.

When the MC88100 tries to access data or an instruction that is not in one of the CMMUs (i.e., the CPU misses in a CMMU), a burst read cycle to memory is performed to fill an entire cache line. The MC88200 makes an initial access to external memory to access the first word in the cache line and then fills the rest of the corresponding cache line (four 32-bit words total). Because the CMMU performs burst accesses, the DRAMs used in this system support fast access modes (page- or nibble-mode).

The DRAM array is divided into two banks of SIMMs, with four SIMM devices in each bank; thus, each bank has a 32-bit wide data bus with byte parity. Depending on whether one or both banks are filled, this arrangement allows for memory configurations of 4 and 8 Mbytes with 1 Mbit DRAMs or 16 and 32 Mbytes with 4 Mbit DRAMs. Table 4 presents the four different configuration options.

OVERVIEW

Figure 2 shows a block diagram of the memory sub-system. The memory sub-system consists of five major blocks: address multiplexing logic, DRAM array, data latching, parity generation and checking logic, and DRAM control logic. Each of these blocks is discussed in detail in the following paragraphs.

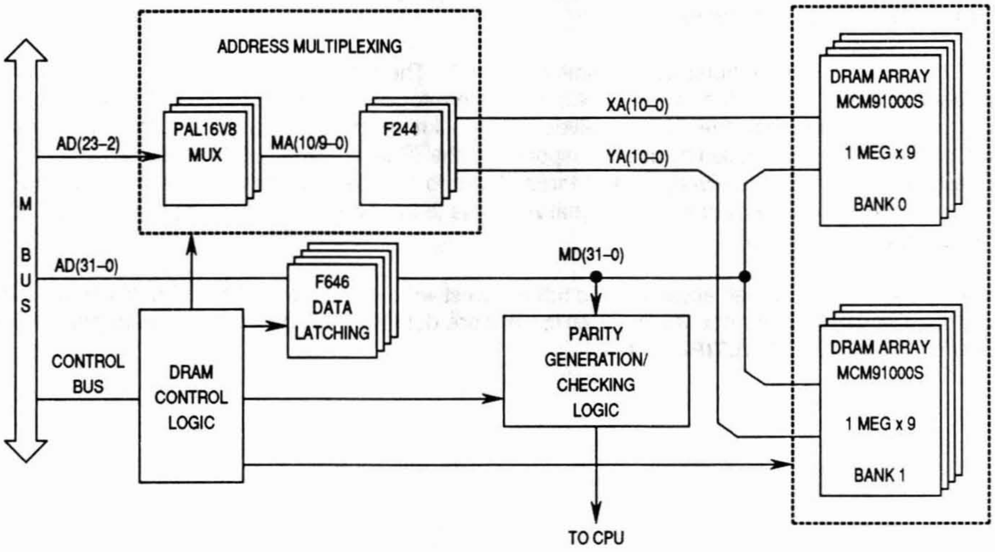

ADDRESS MULTIPLEXING
PAL16V8
MUX
MA(10/9–0)
F244
XA(10–0)
YA(10–0)
AD(23–2)
M
B
U
S
AD(31–0)
F646
DATA
LATCHING
MD(31–0)
PARITY
GENERATION/
CHECKING
LOGIC
CONTROL
BUS
DRAM
CONTROL
LOGIC
DRAM ARRAY
MCM91000S
1 MEG x 9
BANK 0
DRAM ARRAY
MCM91000S
1 MEG x 9
BANK 1
TO CPU

Figure 2. Address/Data Path to DRAM System

The Control Bus from the MBus to the DRAM control logic consists of the following M bus signals (see Table 1): BR, BG, BA, and $\overline{SS3}$–$\overline{SS0}$. The other signals in Figure 2 are listed in Table 5. Note that 4-Mbit DRAMs have eleven address lines while 1-Mbit DRAMs have ten address lines.

Table 4. Memory Sub-system Signal Descriptions

Signal	Description
MA10–MA0 (4 Mbit DRAMS) or MA9–MA0 (1 Mbit DRAMS)	Multiplexed address lines to the DRAM array.
XA10–XA0 (4 Mbit DRAMS) or XA9–XA0 (1 Mbit DRAMS)	Buffered multiplexed address lines for DRAM bank0.
YA10–YA0 (4 Mbit DRAMS) or YA9–YA0 (1 Mbit DRAMS)	Buffered multiplexed address lines for DRAM bank1.
MD31–MD0	Data lines to and from the DRAM array.

READ AND WRITE CYCLES

Figure 3 shows the basic read and write burst timings for the memory sub-system.

To initiate a read or write access, an MC88200 must become the bus master. For an MC88200 to become bus master, the following actions are performed: 1) the MC88200 requests M Bus mastership by asserting the BR signal, 2) the arbitration logic grants the bus by asserting the BG signal, and 3) the MC88200 then acknowledges the transfer with the BA signal.

The MC88200 has a minimum burst access time of 2:1:1:1. The memory interface system adds two wait states to each access, making the system a 4:3:3:3 system for burst read accesses. The first access is measured from the time when the CPU receives a bus acknowledge (BA) until a valid word of data is presented on the AD lines (signalled by an OK response on the $\overline{SS3}$–$\overline{SS0}$ lines). This takes four clocks. After the first valid word of data is received, it takes three clocks to access each subsequent word of data. For burst writes, the memory system adds an additional wait state to the initial access making the system a 5:3:3:3 system for burst write accesses.

To maintain the 4:3:3:3 burst read accesses and 5:3:3:3 burst write accesses, 100 ns DRAMs can be used at 25 MHz, but 80 ns DRAMs are needed at 33 MHz. A more detailed explanation of the data path timing is presented in **ADDRESS MULTIPLEXING**.

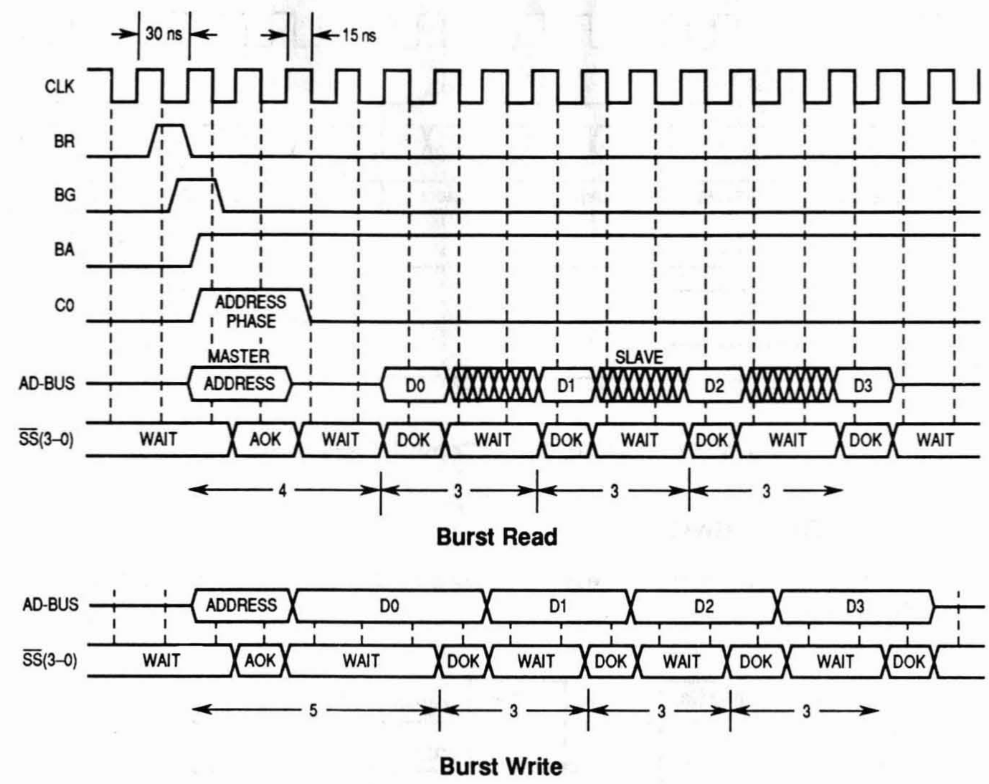

30 ns
15 ns
CLK
BR
BG
BA
CO
ADDRESS PHASE
MASTER
SLAVE
AD-BUS
ADDRESS
D0
D1
D2
D3
SS(3–0)
WAIT
AOK
DOK
4
3
3
3
Burst Read
AD-BUS
ADDRESS
D0
D1
D2
D3
SS(3–0)
WAIT
AOK
DOK
5
3
3
3
Burst Write

Figure 3. Burst Read and Write Cycle (33.33 MHz) Timings

BURST CYCLE CONTROL SIGNALS

Figure 4 shows the operation of the signals that control burst transactions.

The address on the M Bus is multiplexed to provide the row and column addresses for the DRAM array and is placed on the multiplexed address lines (MA10–MA0) (see **ADDRESS MULTIPLEXING**). The DRAM control logic starts the data phase of the cycle by asserting the row address strobe ($\overline{RAS}$) signal at the end of the address phase. The $\overline{RAS}$ signal remains asserted, and the column address strobe ($\overline{CAS}$) signal toggles low then high for each column address to indicate that a valid address is on the multiplexed address lines. The address is valid before the falling edge of $\overline{CAS}$ to comply with the specifications of the DRAMs. The memory output enable ($\overline{MEMOE}$) signal, generated by the DRAM control logic, is asserted on the same rising clock edge as the first $\overline{CAS}$ assertion and stays asserted for the entire period of the burst access. $\overline{MEMOE}$ is the output enable for the 74F646 latches. These latches drive data between the DRAMs and the M Bus .

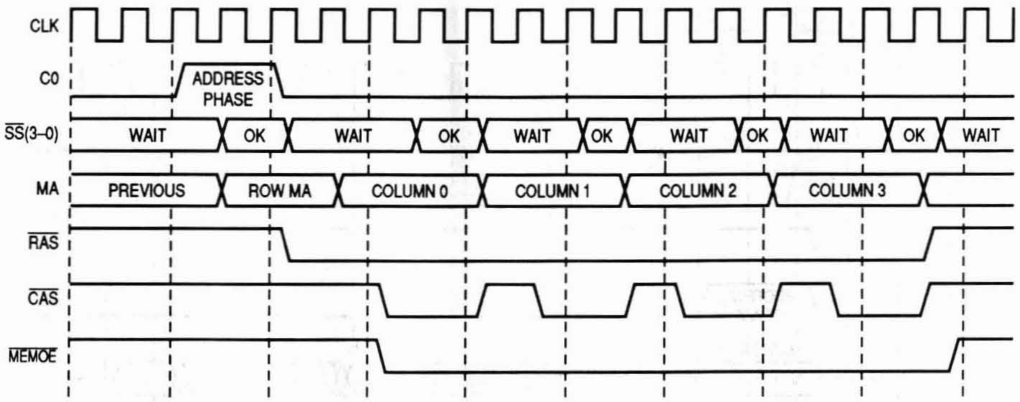


Figure 4. Burst Read Cycle Control Signals Timing

ADDRESS MULTIPLEXING

Figure 5 shows a block diagram of the address multiplexing hardware used to generate row and column addresses for the DRAM array.

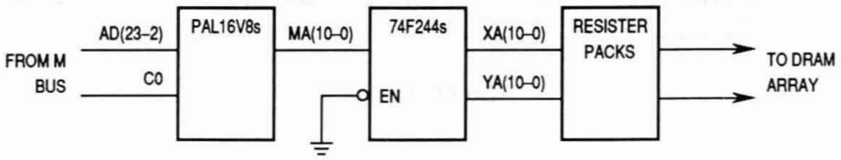


Figure 5. Address Multiplexing

Because the address and data from the MC88200 are time multiplexed on the M bus, the address must be latched during the address phase. Therefore, the multiplexing hardware must be able to latch addresses from the M bus as well as multiplex the addresses for the DRAMs.

In this system, to minimize the board space needed, PALs were used instead of latches and multiplexers. Three 15-ns PAL16V8s latch the address from the M Bus address/data lines (AD23 - AD2) during the address phase (C0 asserted) and then multiplex the address into row and column addresses. These row and column addresses are placed on the multiplexed address lines (MA10 - MA0). Address lines AD1–AD0 from the M bus are not used in the multiplexing. Instead, control signals C3-C6 from the MC88200 are used to indicate which byte or bytes are to be accessed. This implementation supports both 1-Mbit and 4-Mbit DRAMs. Because 1-Mbit DRAMs use only 10 address lines, MA10 is ignored when 1-Mbit DRAMs are used. Therefore, the multiplexed address lines for the DRAMs are referred to as MA10/9-MA0 for the rest of this document.

The addresses on MA10/9–MA0 are passed through 74F244 buffers (whose purpose is explained in the following paragraphs). The outputs of the buffers (address lines XA10/9–XA0 and YA10/9–YA0) are always enabled, and each set of address lines contain the same data as MA10/9–MA0. Lines XA10/9–XA0 connect to DRAM bank0 and lines YA10/9–YA0 connect to bank1. The buffer outputs are passed through series terminating resistors to reduce the amount of ringing on the address lines that connect to the DRAMs.

Each bank of DRAMs has an input capacitive load of 216 pF (54 pF per SIMM) on the address lines, but the PAL16V8s have a drive capability of only 50 pF on each line. Because the PALs do not supply enough capacitive drive to support the DRAMs without much derating, the output from the PALs is passed through

74F244 buffers. The capacitive drive capability of the 74F244s is also specified to 50 pF; however, the 74F244s provide larger sink and source currents than the PALs, thus reducing the derating caused by the capacitive loading of the DRAMs.

Even with the buffers, some derating is still required since each buffer output must drive a capacitive load of 216 pF (four SIMMS) which is 166 pF over the 74F244's specified capability. According to the Signetics FAST Logic Data Handbook, 1989, for the 'F00 family of TTL devices, 200 pF of load capacitance changes the propagation delay of the 74F244 to approximately 8 ns from the 3 ns specified for a 50 pF load; thus, the 74F244 buffers are derated 5 ns by the capacitive load.

Figure 6 shows the critical path for a DRAM access. The critical path is the signal route starting from the time the control signals are valid to when the DRAMs receive the $\overline{\text{CAS}}$ signals, and ending when the appropriate data reaches the CPU via the M bus. For the critical path, there is a maximum 9.5 ns derate delay allowed for capacitive loading and clock skew.

Equation 1 shows how the maximum derate delay is calculated (all times are in nanoseconds). This equation takes into account all of the critical delays through the data path, given a two wait state memory access. The terms used in equation 1 are defined as follows:

> Derate Delay—The amount of time allowed in this system for the delay caused by capacitive loading and clock skew.
>
> WAIT—Two clock cycles at 33.3 MHz. This is because of the two wait states added to each access by the system (see **READ AND WRITE CYCLES**).
>
> $\overline{\text{CAS}}$—The time required for the PAL16V8 to activate the $\overline{\text{CAS}}$ signal.
>
> F244—The maximum propagation delay through the $\overline{\text{CAS}}$ buffers.
>
> DRAM—The time required to access the DRAMs starting when $\overline{\text{CAS}}$ goes low.
>
> F646—The maximum propagation delay through the latching transceivers.
>
> 88K Data Setup—The amount of time required for the AD Bus data to be valid before the rising edge of the clock.
>
> (1) Derate Delay <= WAIT - (CAS + F244 + DRAM + F646 + 88k Data Setup)
>
> Derate Delay < = 60 - (8 + 6.5 + 20 + 10 + 6)
>
> Derate Delay < = 9.5 nS

The worst case output to output clock skew from the 88914 is 01.0 ns per clock; thus, the derate delay allowed for the 74F244 buffers is 8.5 ns (i.e., 9.5 ns - 1 ns). This is enough time since the 74F244 buffers are derated only 5 ns, as stated previously.

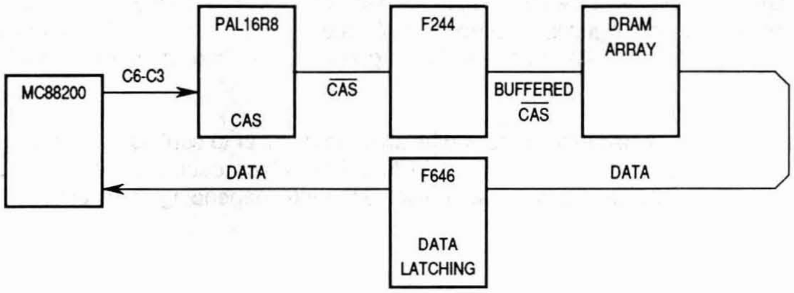


Figure 6. Data Path Flow

DRAM ARRAY

The DRAM array is composed of two banks of SIMMs with four SIMM devices in each bank (see Figure 7). Each SIMM device contains nine DRAMs; thus, each bank has a 32-bit wide data bus and one bit of parity per byte.

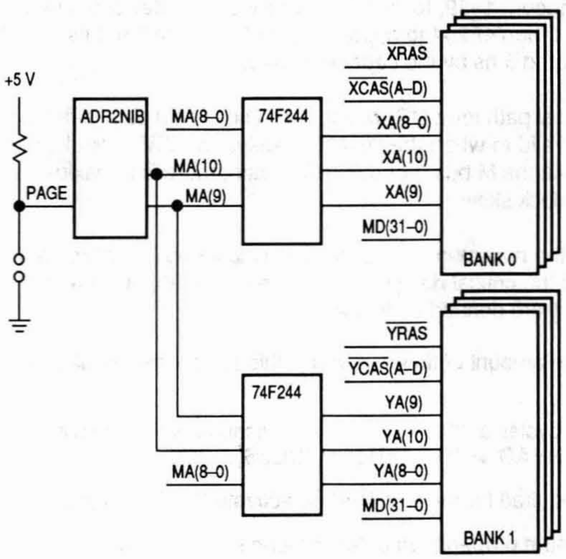


Figure 7. DRAM Array Block Diagram

The design of the memory system allows the user to configure the board for page- or nibble-mode DRAMs. Although this option increases the complexity of the hardware, it gives the user flexibility to choose DRAMs based on availability and price.

Page- or nibble-mode is selected by a jumper connected to the PAGE input of the PAGE/NIB PAL. When the PAGE input is asserted (no jumper attached), page mode is selected. The multiplexed nibble (MNIB) output is connected to MA9 in the DRAM array. The buffered MNIB signals, XNIB and YNIB, go to address bit XA9 of bank0 and address bit YA9 of bank 1, respectively, and automatically cycle through four words of data. If the PAGE input is negated (jumper attached), nibble-mode is selected and the MNIB output acts any other address output.

The data on the data in (DIN) pins of the DRAMs are latched by the DRAMs during write cycles as indicated by the assertion of the write enable signals, $\overline{XWE}$ (for bank 0) and $\overline{YWE}$ (for bank 1). The data out (DOUT) pins are driven by the DRAMs when $\overline{CAS}$ is asserted during read cycles (indicated when $\overline{XWE}$ and $\overline{YWE}$ are negated) .

Flexibility has also been introduced into the design by allowing the user to configure the board for either 1- or 4-Mbit DRAMs. The 1/4-Mbit jumper is connected to a PAL which decodes the lower four bits of the multiplexed address. This PAL decodes the addresses differently depending on whether the jumper is set to 1 Mbit or 4 Mbit.

DATA LATCHING

Because the M bus is not held valid by the CMMUs across clock edges, during a CPU write the data must be latched and held valid while C0 is negated (data phase) to meet the setup times for the DRAM array. On a CPU read, the data does not need to be latched because the DRAM holds the data valid across clock edges.

Four 74F646 registered transceivers (see Figure 8), latch the data going from the M bus to the DRAM array (i.e., in the B-to-A direction, from AD31–AD0 to MD31–MD0), but are transparent to data going in the other direction (from A-to-B). The clock for data going in the A-to-B direction is grounded since that data is not latched; however, the data flow from B-to-A is clocked by the system clock to ensure that the data is latched while it is valid.

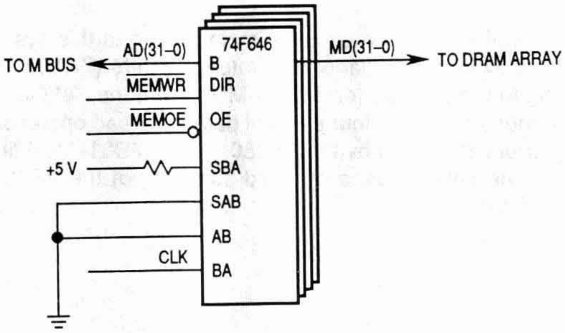


Figure 8. Data Latching

The 74F646 transceivers are enabled by the $\overline{\text{MEMOE}}$ signal. The direction of the device is selected by the memory write ($\overline{\text{MEMWR}}$) signal. When the $\overline{\text{MEMWR}}$ signal is asserted, indicating that the CPU is writing to memory, the flow is directed from the AD lines to the MD lines (B-to-A). When the CPU reads from memory, the $\overline{\text{MEMWR}}$ signal is negated, and data flows in the opposite direction (A-to-B). The $\overline{\text{MEMWR}}$ signal is asserted one state before $\overline{\text{MEMOE}}$ is asserted and held valid for one state after $\overline{\text{MEMOE}}$ is negated. This is to avoid possible contention in the 74F646s which could result from switching the direction and enabling the device on the same clock edge.

The select pins (SAB and SBA) for the 74F646s determine for each direction whether data is latched in that direction or transferred through the device in real-time (i.e., the device is transparent). When SAB and/or SBA is negated, the device is transparent in the corresponding direction. When SAB or SBA is asserted, data is latched in the corresponding direction. For this design, the flow from the M bus to the DRAM array is latched; therefore, SBA is tied high. In the other direction, the device is transparent, so SAB is tied low.

PARITY

The MC88200 CMMU devices have an automatic parity generation/checking feature which, on writes, generates parity for both addresses and data, and on reads, checks parity for both addresses and data. This feature can only be enabled or disabled for both addresses and data, not for only addresses or only data.

Since this DRAM interface system was originally part of a larger application, it was designed so that there could be another bus master in addition to the two MC88200s. To maintain parity detection, the other M bus master needed a method of generating a parity bit for each byte it wrote to memory, so parity generation/checking circuitry was added to the interface system for use by all of the possible bus masters. Therefore, in the design presented in this document, the automatic parity checking of the MC88200s has been disabled, and the MC88200s use the added parity circuitry. MC88200 automatic parity checking is disabled by clearing the parity enable bit (bit 15) in the MC88200 system control register (SCR).

Parity evaluation for an MC88200 system can be performed by hardware or software. Software parity detection requires no extra board space, but does not keep an accurate record of parity errors as hardware detection can. With software parity detection, when the processor receives the bus error signal, software diagnostic code is executed. This code may simply re-issue the instruction; however, no record of the error is kept. If the parity error does not occur on the next access, this method is successful, but if the instruction causes a parity error again, it may be necessary to read each byte of data separately to determine which byte generated the error.

Hardware parity evaluation requires more board space than software parity evaluation but keeps an accurate record of the occurrence of parity errors. When performing hardware detection, an error can be recorded as soon as it occurs. This ability provides an advantage over software parity detection since software detection may not be able to reproduce an intermittent error for diagnostic purposes. Because of this advantage, hardware parity detection was chosen for this interface system.

Figure 9 shows the parity generation/checking circuitry implemented in this system. Parity evaluation is performed on each byte of data by four 9-bit parity generator/checkers (74AS280s) using odd parity. On write operations, all data going to the DRAMs (on MD31–MD0) from the 74F646s is fed to the 74AS280s which perform parallel parity generation for the four bytes of data. On read operations, all data read from the DRAMs is checked for parity errors in parallel by the AS280s. The MD31–MD0 lines are connected to 4.7 KΩ pull-up resistors to reduce the noise caused by rapid switching of the AS280s. The AS280s switch rapidly anytime the MD31–MD0 lines tri-state.

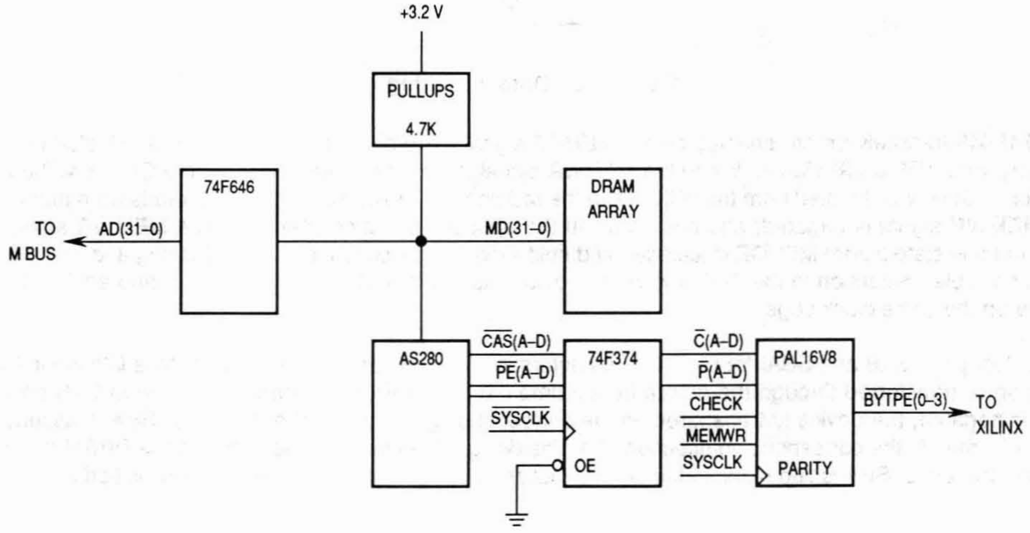


Figure 9. Parity Generation/Checking Circuitry

The 74AS280s check for parity during the data phase of a cycle and generate four parity error signals ($\overline{\text{PEA}}$–$\overline{\text{PED}}$) which indicate whether or not there was a parity error for each SIMM (A–D) in a bank. $\overline{\text{PEA}}$–$\overline{\text{PED}}$ are asynchronous signals and valid for only one clock period. Since it is possible, in the worst case, that these signals will not meet the setup time for a PAL, they are first latched by a 74F374. The 74F374 is used because it has a setup time of only 2 ns. The 74F374 output enable pin is connected to ground (i.e., outputs are enabled), and the clock is connected to the system clock. Therefore, the F374 latches the parity error data and holds it for one clock period.

The outputs of the 74F374s ($\overline{\text{PA}}$–$\overline{\text{PD}}$) are sent into the PARITY PAL where they are checked for valid parity. The PARITY PAL only checks $\overline{\text{PA}}$–$\overline{\text{PD}}$ while the CHECK signal is valid, as shown in Figure 10. The CHECK signal is asserted at the end of the CAS signal, after valid data has been checked by the AS280s for parity errors.

If a parity error is indicated during the time the CHECK signal is active, the PARITY PAL asserts the appropriate BYTPE0–BYTPE3 signal(s) to indicate which of the SIMMs produced the parity error. The BYTPE0–BYTPE3 signals are connected to a Xilinx gate array which controls parity errors in addition to other functions which are not related to this memory interface. The BYTPE0–BYTPE3 signals are held valid for three clock periods to allow the Xilinx to latch the information.

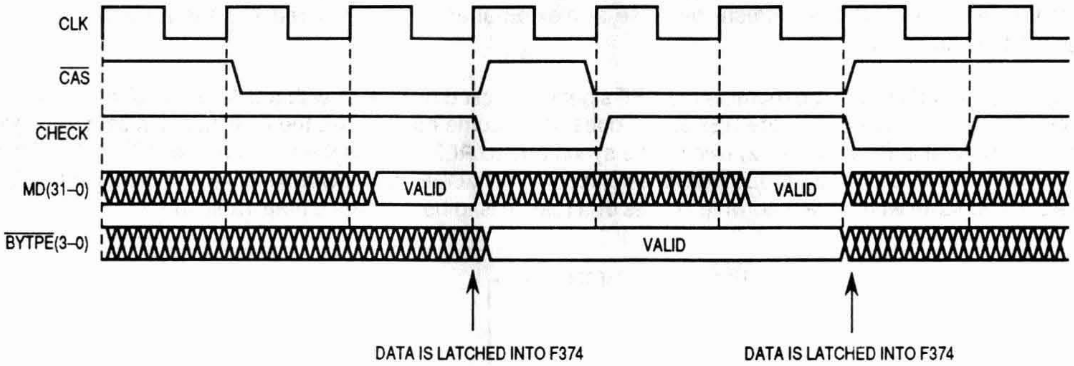


Figure 10. Parity Checking Timing

The memory parity status register (MPSR) in the Xilinx (see Figure 11), keeps track of all parity information. Four bits in the MPSR keep track of which bytes, if any, generated a parity error, and two bits keep track of which bank contained the SIMM with the error.

7	6	5	4	3	2	1	0
NA	NA	BANK1	BANK0	BYTE3	BYTE2	BYTE1	BYTE0

Figure 11. Memory Parity Status Register

When a memory parity error is detected, the appropriate bits in the MPSR are set, and the Xilinx sends a parity interrupt signal to a central interrupt controller. This interrupt controller is a peripheral chip which is external to the memory interface. When the interrupt controller receives a parity interrupt from the Xilinx, it sends an interrupt to the CPU which forces the CPU to execute an interrupt service routine. The interrupt controller has registers which contain information about the interrupt. The CPU reads the status of these registers to determine which device caused the interrupt: in this case, the Xilinx. Next, the CPU reads the MPSR in the Xilinx to determine which bank of memory and which byte(s) had the parity error thus indicating which SIMM device generated the error. Reading the MPSR clears the register and clears the interrupt in the Xilinx.

Once the CPU has determined that the interrupt was caused by a parity error, exception processing software should take over. This software can log the occurrence of parity errors for a system administrator or notify the user that a parity error occurred. This software can also re-issue the access which caused the error or run diagnostic tests on the memory system.

REFRESH CYCLE

The 1-Mbit and 4-Mbit DRAM refresh specification is 512 or more refresh cycles per 8 ms. To meet this specification, one refresh request must be sent at least every 15.625 µs. The time between refresh requests must allow for the longest amount of time any bus master can have the bus since refresh requests cannot interrupt a bus master's tenure. The refresh request ($\overline{\text{REF}}$) signal for this design is generated every 15 ms by a peripheral device which is not a part of the memory interface.

To reduce the amount of hardware required to support the refresh operation, the control logic generates a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh. Externally generated addresses are not necessary for a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh (as they are in a $\overline{\text{RAS}}$-only refresh) because any external address is ignored and the refresh address is generated internally.

The peripheral device that generates the $\overline{\text{REF}}$ signal is clocked by a clock with a different frequency than the system clock. To insure that the $\overline{\text{REF}}$ signal does not become metastable, the $\overline{\text{REF}}$ signal is sent through a 74F374 D flip-flop (see Figure 12) twice. The synchronized $\overline{\text{REF}}$ signal is then input to the MODE PAL which generates the $\overline{\text{MODE1}}$ and $\overline{\text{MODE0}}$ signals as outputs. The $\overline{\text{MODE1}}$ and $\overline{\text{MODE0}}$ signals are inputs to the CAS PAL and indicate whether a read/write access or a refresh is to be performed (see Table 4).

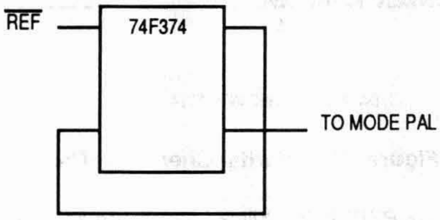


Figure 12. $\overline{\text{REF}}$ Synchronization by a D Flip-Flop

Table 5. $\overline{\text{MODE1}}$ and $\overline{\text{MODE0}}$ Function Description

MODE0	MODE1	Description
0	0	Refresh
0	1	NA
1	0	Read/Write
1	1	Idle

When both $\overline{\text{MODE}}$ signals are low, the CAS PAL asserts $\overline{\text{CAS}}$ to indicate that a refresh operation is to be performed. Next, the RAS PAL asserts the $\overline{\text{RAS0}}$ signal to refresh bank0, and then one clock later, the RAS PAL asserts $\overline{\text{RAS1}}$ to refresh bank1 (see Figure 13). In this manner, both banks of DRAMs go through a refresh cycle. The two $\overline{\text{RAS}}$ signals are staggered by one clock so that both banks of DRAMs are not activated at the same time. Activating both banks at the same time causes a large current draw; therefore, staggering the refresh operation minimizes current draw, which allows flexibility in choosing a power supply.

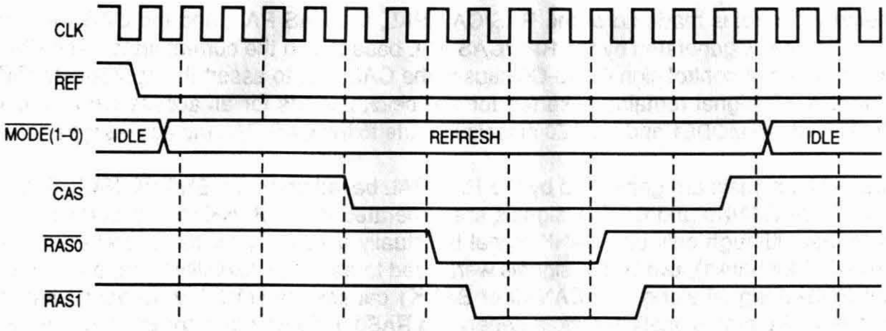


Figure 13. Refresh Cycle Timing Diagram

DRAM CONTROL LOGIC

The DRAM control logic consists of two parts (the state machine and the main memory control) which are implemented with 15-ns PAL devices. The overall functionality of each PAL is discussed in the following paragraphs. For more detailed information about the individual signals and states generated by the PALs, refer to **LIST OF LOGIC EQUATIONS** for the PAL logic equations.

The state machine is contained in the STATE PAL. The state machine generates 32 states which are output on pins Q0–Q4. The 32 states are generated based on C0, C1, $\overline{\text{WRITE}}$, and the previous state of the $\overline{\text{MODE1}}$ and $\overline{\text{MODE0}}$ signals (see Figure 14). The MODE PAL generates the $\overline{\text{MODE1}}$ and $\overline{\text{MODE0}}$ signals based on the current state.

The WRITE PAL asserts the clocked $\overline{\text{WRITE}}$ signal when it receives either a data bus acknowledge or an instruction bus acknowledge signal and control signal C2 is negated (indicating a write).

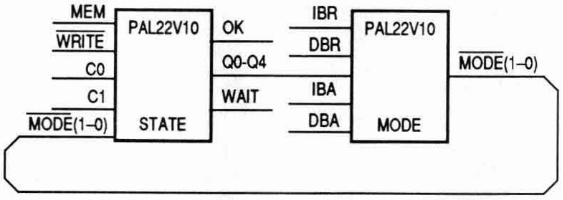


Figure 14. State Machine

The state machine changes state on the rising edge of every clock except when it is in state 0 (Idle) and $\overline{\text{WRITE}}$ and C0 are negated. Since the state machine changes states on every clock, the amount of external hardware needed is minimized. For example, during a burst cycle, no external counter is needed to keep track of the number of clocks that have passed. Instead the state machine replaces the counter since it steps through the states which indicate exactly which part of the transaction is being performed.

Nineteen of the 32 states are used during burst accesses, and seven other states are entered during refresh operations. The remaining six states are not used for the DRAM interface and are not presented here. The OK and WAIT signals are generated for the memory sub-system by the STATE PAL based on the status of the $\overline{\text{MODE1}}$ and $\overline{\text{MODE0}}$ signals and on control signals C0 and C1.

Because the state machine is so large, its state diagram cannot be shown in detail. However, Figure 15 shows the flow of the states for read and write operations, including bursting.

The main memory control is made up of the RAS/CAS PAL, the RAS PAL, and the CAS PAL (see Figure 16). The $\overline{\mathrm{ENCAS}}$ signal is generated by the RAS/CAS PAL based upon the current state. The $\overline{\mathrm{ENCAS}}$ signal along with one or more of control signals C3-C6 causes the CAS PAL to assert the appropriate $\overline{\mathrm{CASA}}$–$\overline{\mathrm{CASD}}$ signal(s). The $\overline{\mathrm{ENCAS}}$ signal remains asserted for two clock periods for all access types except refresh requests. Recall that the $\overline{\mathrm{MODE1}}$ and $\overline{\mathrm{MODE0}}$ signals indicate to the CAS PAL the access type.

The $\overline{\mathrm{RAS1}}$ and $\overline{\mathrm{RAS0}}$ signals are generated by the RAS PAL based upon the $\overline{\mathrm{ENRAS}}$, $\overline{\mathrm{RAEND}}$, BANK0, and BANK1 signals. The BANK0 and BANK1 signals are generated in the BANK PAL based upon the current address. Note that although only one BANK signal is actually necessary for this system (i.e. BANK=0 for bank0 and BANK=1 for bank1), two BANK signals were used to allow the flexibility to expand to four banks of DRAMs. The $\overline{\mathrm{ENRAS}}$ signal along with BANK0 or BANK1 causes the RAS PAL to assert either $\overline{\mathrm{RAS0}}$ or $\overline{\mathrm{RAS1}}$, respectively. Refresh signalling makes generating $\overline{\mathrm{RAS0}}$ or $\overline{\mathrm{RAS1}}$ more complex than generating the $\overline{\mathrm{CASA}}$–$\overline{\mathrm{CASD}}$ signals; therefore, the $\overline{\mathrm{RAEND}}$ signal is used to minimize the number of OR terms in the PAL equations. $\overline{\mathrm{RAEND}}$ negates $\overline{\mathrm{RAS0}}$ and $\overline{\mathrm{RAS1}}$.

When $\overline{\mathrm{RAS0}}$ or $\overline{\mathrm{RAS1}}$ is asserted, the $\overline{\mathrm{ANYRAS}}$ signal is also asserted. When any of the $\overline{\mathrm{CASA}}$–$\overline{\mathrm{CASD}}$ signals is asserted, the $\overline{\mathrm{ANYCAS}}$ signal is also asserted.

Figure 17 shows the timing of the $\overline{\mathrm{RAS}}$ and $\overline{\mathrm{CAS}}$ signals for a burst read operation. A summary of the control logic signals is given in Table 7.

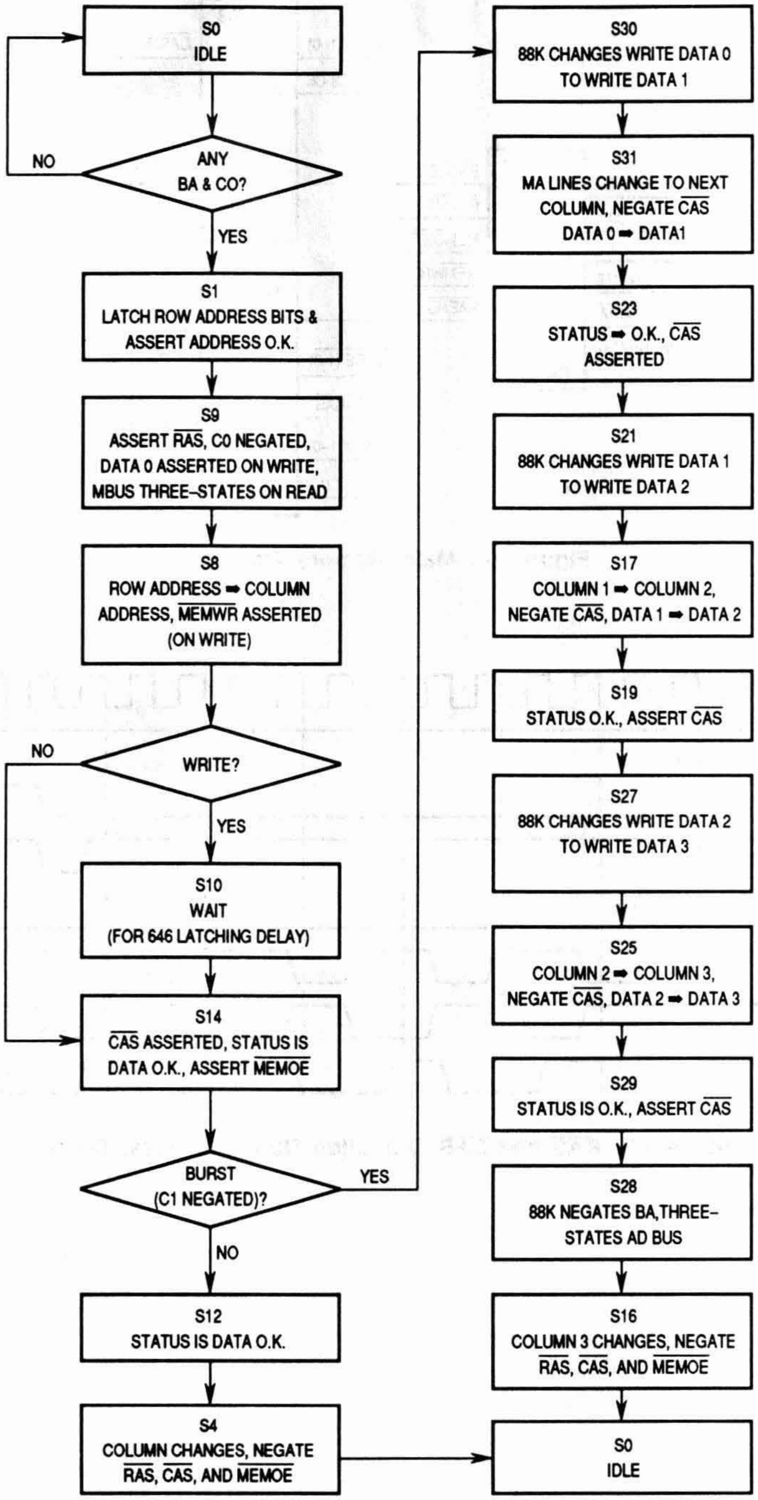

S0
IDLE
ANY
BA & CO?
NO
YES
S1
LATCH ROW ADDRESS BITS &
ASSERT ADDRESS O.K.
S9
ASSERT RAS, C0 NEGATED,
DATA 0 ASSERTED ON WRITE,
MBUS THREE–STATES ON READ
S8
ROW ADDRESS ➡ COLUMN
ADDRESS, MEMWR ASSERTED
(ON WRITE)
WRITE?
NO
YES
S10
WAIT
(FOR 646 LATCHING DELAY)
S14
CAS ASSERTED, STATUS IS
DATA O.K., ASSERT MEMOE
BURST
(C1 NEGATED)?
YES
NO
S12
STATUS IS DATA O.K.
S4
COLUMN CHANGES, NEGATE
RAS, CAS, AND MEMOE
S30
88K CHANGES WRITE DATA 0
TO WRITE DATA 1
S31
MA LINES CHANGE TO NEXT
COLUMN, NEGATE CAS
DATA 0 ➡ DATA1
S23
STATUS ➡ O.K., CAS
ASSERTED
S21
88K CHANGES WRITE DATA 1
TO WRITE DATA 2
S17
COLUMN 1 ➡ COLUMN 2,
NEGATE CAS, DATA 1 ➡ DATA 2
S19
STATUS O.K., ASSERT CAS
S27
88K CHANGES WRITE DATA 2
TO WRITE DATA 3
S25
COLUMN 2 ➡ COLUMN 3,
NEGATE CAS, DATA 2 ➡ DATA 3
S29
STATUS IS O.K., ASSERT CAS
S28
88K NEGATES BA,THREE–
STATES AD BUS
S16
COLUMN 3 CHANGES, NEGATE
RAS, CAS, AND MEMOE
S0
IDLE

Figure 15. State Machine Flow Diagram

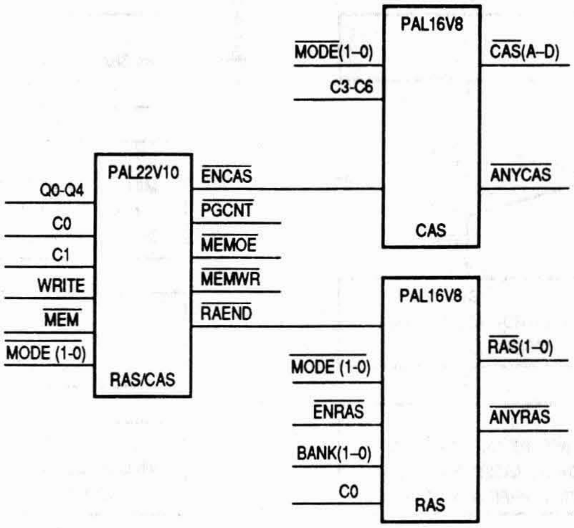

PAL16V8
MODE(1–0)
C3-C6
CAS(A–D)
ANYCAS
CAS
PAL22V10
Q0-Q4
C0
C1
WRITE
MEM
MODE (1-0)
RAS/CAS
ENCAS
PGCNT
MEMOE
MEMWR
RAEND
PAL16V8
MODE (1-0)
ENRAS
BANK(1–0)
C0
RAS
RAS(1–0)
ANYRAS

Figure 16. Main Memory Control

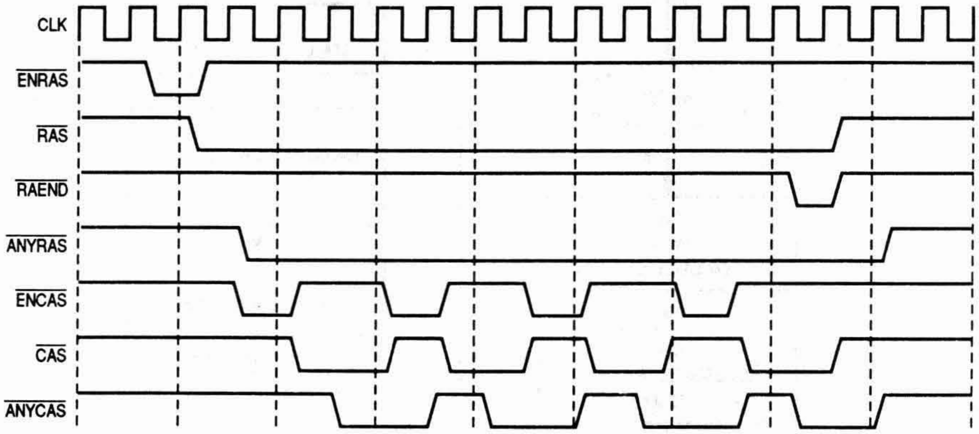

CLK
ENRAS
RAS
RAEND
ANYRAS
ENCAS
CAS
ANYCAS

Figure 17. RAS and CAS Operation During a Burst Read

Table 6. Control Signal Summary

Signal	Description	Generating PAL
Q4–Q0	The 32 states are output on these four signals. The state changes on every clock edge except when in state 0 with C0 and $\overline{\text{WRITE}}$ negated.	STATE
$\overline{\text{WRITE}}$	Indicates a read/write access. Asserted when either data bus acknowledge or instruction bus acknowledge is asserted and C2 is negated.	WRITE
OK	Asserted or negated depending on the MODE signals and C0 and C1. Indicates the status of the memory system during read/write accesses.	STATE
WAIT	Asserted or negated depending on the MODE signals and C0 and C1. Indicates the status of the memory system during read/write accesses.	STATE
$\overline{\text{MODE1}}$–$\overline{\text{MODE0}}$	Asserted or negated depending on the state. These signals indicate the type of access (see Table 4).	MODE
$\overline{\text{MEMOE}}$ (Memory Output Enable)	Output enable control for the 74F646s that interface the DRAMs and M Bus. Asserted one state before data is valid and negated on the state after the data bus is three-stated.	RAS/CAS
$\overline{\text{MEMWR}}$ (Memory Write)	Controls the direction of data between the DRAM array and the M bus. This signal is buffered in the 74F244s along with MA10MA0. The buffered outputs from the PAL which correspond to $\overline{\text{MEMWR}}$ are $\overline{\text{XWE}}$ and $\overline{\text{YWE}}$ for the bank0 and bank1 R/$\overline{\text{W}}$ inputs, respectively. The $\overline{\text{MEMWR}}$ signal is asserted one state before $\overline{\text{MEMOE}}$ and held for one clock after $\overline{\text{MEMOE}}$ is negated.	RAS/CAS
$\overline{\text{PGCNT}}$ (Page Count)	Asserted during burst cycles when using page-mode DRAMs. This signal increments the column address to access the next byte of data.	RAS/CAS
$\overline{\text{ENCAS}}$ (Enable $\overline{\text{CAS}}$)	Asserted or negated depending on the state. The $\overline{\text{ENCAS}}$ signal along with one or more of control signals C3-C6 causes the CAS PAL to assert the appropriate $\overline{\text{CASA}}$–$\overline{\text{CASD}}$ signal(s)	RAS/CAS
$\overline{\text{ENRAS}}$ (Enable $\overline{\text{RAS}}$)	Asserted or negated depending on the state. The $\overline{\text{ENRAS}}$ signal along with BANK0 or BANK1 causes the RAS PAL to assert either $\overline{\text{RAS0}}$ or $\overline{\text{RAS1}}$, respectively.	88RAS
$\overline{\text{RAEND}}$ (End $\overline{\text{RAS}}$)	Asserted or negated depending on the state. Causes the negation of $\overline{\text{RAS0}}$ and $\overline{\text{RAS1}}$.	RAS/CAS
$\overline{\text{ANYCAS}}$	Asserted when any of the $\overline{\text{CASA}}$–$\overline{\text{CASD}}$ signals is asserted.	CAS
$\overline{\text{ANYRAS}}$	Asserted when $\overline{\text{RAS0}}$ or $\overline{\text{RAS1}}$ is asserted	RAS

CONCLUSION

The memory system presented in this application note provides a high-performance, low cost design using either page- or nibble-mode DRAM technology. The system is a 4:3:3:3 for burst read accesses and a 5:3:3:3 for burst write accesses, adding latency to the minimum 2:1:1:1 access for an MC88100/88200 system. The system can use 1- or 4-Mbit DRAMs, allowing memory configurations from 4- to 32-Mbits. This system can run at 25 or 33.3 MHz, depending on the DRAM speed used. A higher frequency design could be implemented with interleaved banks of memory or a pipelined data path.

LIST OF LOGIC EQUATIONS

```
                NAME  BANK

                COMPANY      MOTOROLA

                PART         PAL16R6; 16V8

/*******************************************************************************/

/*      This device decodes the bank outputs.  BANK0 and BANK1 control      */

/*      which RAS signal is asserted.  1MBIT indicates whether the DRAM is.  */

/*      1 or 4 Mbit.  C0 determines when the address is valid.  This PAL also  */

/*      latches AD19, AD20, and AD21                                        */

/*******************************************************************************/

/**     Inputs          **/

CLK             /* System clock                                                  */

C0              ; M Bus control signal that determines when address is valid

1MBIT           ; Input from jumper.  Indicates 1 Mbit or 4 Mbit DRAMs. */

/AD19           ; Muxed address/data line 19                        */

/AD20           ; Muxed address/data line 20                        */

/AD21           ; Muxed address/data line 21                        */

AD22            ; Muxed address/data line 22                        */

AD23            ; Muxed address/data line 23                        */

AD24            ; Muxed address/data line 24                        */

AD25            ; Muxed address/data line 25                        */

/**     Outputs               **/

/BANK0                  /* Bank 0 selected                                       */

/BANK1                  /* Bank 1 selected                                       */

/LA19           /* Latched address 19                               */

/LA20           /* Latched address 20                               */

/LA21           /* Latched address 21                               */
```

```
/**     Logic Equations         **/

BANK0           =       1MBIT & C0 & /AD22

                        + /1MBIT & C0 &  /AD24

                        + BANK0 & /C0

BANK1           =       1MBIT & C0 & /AD23

                        + /1MBIT & C0 &  /AD25

                        + BANK1 & /C0

LA19            =       C0 & AD19

                        + /C0 & LA19

LA20            =       C0 & AD20

                        + /C0 & LA20

LA21            =       C0 & AD21


-----------------------------------------------------------------------------------------------

                NAME    PARITY

                COMPANY         MOTOROLA

                PART            PAL16V8

/*************************************************************************************/

/*      This device generates the parity error signals for each byte during a      */

/*      memory read operation.  Errors are asserted for 2 clock periods.                    */

/*      Error information is latched in the Xilinx.  ANYPE is generated to aid in   */

/*      troubleshooting.                                                 */

/*************************************************************************************/

/**     Inputs          **/

CLK                     /* System clock                         */

/CA                     /* Cas signal for byte A                */

/CB                     /* Cas signal for byte B                */

/CC                     /* Cas signal for byte C                */
```

```
/CD             /* Cas signal for byte D              */
PA              /* Parity error signal for byte A     */
PB              /* Parity error signal for byte B     */
PC              /* Parity error signal for byte C     */
PD              /* Parity error signal for byte D     */
/CHK            : Check signal indicating when to check for errors */
/MEMWR          /* Indicates a write to memory        */
/**     Outputs           **/
/BYTPE0         /* Indicates parity error on byte 0        */
/BYTPE1
/BYTPE2
/BTYPE3
/ANYPE          /* Indicates a parity error on any byte    */
/ANYPE1         /* Generated to hold signals an extra clock  */
/**     Logic Equations        **/
BYTPE0     =    CHK & /MEMWR & CA & PA
                + BYTPE0 & ANYPE
                + BYTPE0 & ANYPE1
BYTPE1     =    CHK & /MEMWR & CB & PB
                + BYTPE1 & ANYPE
                + BYTPE1 & ANYPE1
BYTPE2     =    CHK & /MEMWR & CC & PC
                + BYTPE2 & ANYPE
                + BYTPE2 & ANYPE1
BYTPE3     =    CHK & /MEMWR & CD & PD
                + BYTPE3 & ANYPE
                + BYTPE3 & ANYPE1
ANYPE      =    CHK & /MEMWR & CA & PA
```

```
                        + CHK & /MEMWR & CB & PB
                        + CHK & /MEMWR & CC & PC
                        + CHK & /MEMWR & CD & PD
                        + ANYPE &  /ANYPE1
ANYPE1          =       ANYPE                       + /C0 & LA21


-------------------------------------------------------------------------------------------------

                NAME  CAS
                COMPANY      MOTOROLA
                PART         PAL16R8
/*********************************************************************************/
/*      This device controls the registered CAS outputs.                        */
/*********************************************************************************/
/**     Inputs          **/
CLK                     /* System clock                                             */
/MODE0                  /* Together, MODE0 and MODE1 indicate what  */
/MODE1                  /*      type of access                      */
C3                      /* M Bus byte enable 3                      */
C4                      /* M Bus byte enable 4                      */
C5                      /* M Bus byte enable 5                      */
C6                      /* M Bus byte enable 6                      */
/ENCAS                  /* Enable CAS signal                        */
/**     Outputs                 **/
/CASA           /* Registered CAS signal for bits 31-24         */
/CASB           /* Registered CAS signal for bits 23-16         */
/CASC           /* Registered CAS signal for bits 15-8          */
/CASD           /* Registered CAS signal for bits 7-0           */
/ANYCAS                 /* Any CAS signal is asserted               */
```

```
/**     Logic Equations          **/

CASA  =      ENCAS & MODE1 & /MODE0 & C3

                  + ENCAS & MODE 1 & MODE0

CASB  =      ENCAS & MODE1 & /MODE0 & C4

                  + ENCAS & MODE 1 & MODE0

CASC  =      ENCAS & MODE1 & /MODE0 & C5

                  + ENCAS & MODE 1 & MODE0

CASD  =      ENCAS & MODE1 & /MODE0 & C6

                  + ENCAS & MODE 1 & MODE0

ANYCAS       =      ENCAS & /MODE1 & MODE0

                  + ENCAS & MODE1 & /MODE0

                  + ENCAS & MODE1 & MODE0


---------------------------------------------------------------------------------------------------

             NAME  RAS

             COMPANY     MOTOROLA

             PART        PAL16R8

/*************************************************************************************/

/*      This device controls the registered RAS outputs. BANK1 and BANK0     */

/*      control which RAS is to be asserted.  Each RAS is staggered during     */

/*      refresh by one clock.  This PAL also latches AD3-AD5.                 */

/*************************************************************************************/

/**     Inputs            **/

CLK                  /* System clock                                    */

/MODE0               /* Together, MODE0 and MODE1  indicate what  */

/MODE1               /*      type of access                  */

BANK0                /* Bank 0 selected                                 */

BANK1                /* Bank 1 selected                                 */
```

```
C0                   /* M Bus control signal for address/data phase   */

/ENRAS               /* Enable RAS signal                              */

/RAEND               /* RAS end signal                                         */

AD3                  /* Multiplexed address/data line 3                */

AD4                  /* Multiplexed address/data line 4                */

AD5                  /* Multiplexed address/data line 5                */

/**     Outputs              **/

/RAS0          /* Registered RAS signal for bank 0           */

/RAS1          /* Registered RAS signal for bank 1           */

/ANYRAS              /* Any RAS signal is asserted                     */

/LA3                 /* Latched address line 3                                 */

/LA4                 /* Latched address line 4                                 */

/LA5                 /* Latched address line 5                                 */

/**     Logic Equations      **/

RAS0  =        ENRAS & MODE1 & MODE0

                     + ENRAS & /MODE 1 & MODE0 & /BANK1 & /BANK0

                     + ENRAS & MODE1 & /MODE0 & /BANK1 & /BANK0

                     + RAS0 & /RAEND

RAS1  =        RAS0 & MODE1 & MODE0

                     + ENRAS & /MODE1 & MODE0 & /BANK1 & BANK0

                     + ENRAS & MODE1 & /MODE0 & /BANK1 & BANK0

                     + RAS1 & /MODE1 & MODE0 & /RAEND

                     + RAS1 & MODE1 & /MODE0 & /RAEND

ANYRAS        =      ENRAS

                     + RAS0 & MODE1 & MODE0

                     + RAS1 & MODE1 & MODE0

                     + ANYRAS & /MODE1 & MODE0 & /RAEND

                     + ANYRAS & MODE1 & /MODE0 & /RAEND
```

```
LA3          =      C0 & AD3

                    + /C0 & LA3

LA4          =      C0 & AD4

                    + /C0 & LA4

LA5          =      C0 & AD5

                    + /C0 & LA5



--------------------------------------------------------------------------------

             NAME  ARB

             COMPANY     MOTOROLA

             PART        PAL16L8 ; 16V8

/*******************************************************************************/

/*      This device arbitrates between the data CMMU and instruction CMMU. */

/*      Priorities are as follows :                                       */

/*      1. Refresh                  (RREQ)                                */

/*      2. Instruction CMMU     (IBG)                          */

/*      3. Data CMMU            (DBG)                */

/*******************************************************************************/

/**     Inputs          **/

CLK                 /* System clock                               */

/MODE0              /* Together, MODE0 and MODE1  indicate what */

/MODE1              /*      type of access                  */

IBR                 /* Instruction bus request from the instruction CMMU    */

DBR                 /* Data bus request from the data CMMU                  */

/RREQ               /* Refresh request                            */

/**     Outputs             **/

/DBG                /* Data bus grant                             */

/IBG                /* Instruction bus grant                */
```

```
/**     Logic Equations          **/

DBG          =     MODE0

                   + MODE1

                   + RREQ

                   + IBR

                   + /DBR

IBG          =     MODE0

                   + MODE1

                   + RREQ

                   +/IBR


----------------------------------------------------------------------------------------------------

             NAME  RAS/CAS

             COMPANY     MOTOROLA

             PART        PAL22V10

/*****************************************************************************/

/*      This device controls the main memory interface.                      */

/*****************************************************************************/

/**     Inputs           **/

CLK                 /* System clock                                          */

/MODE0              /* Together, MODE0 and MODE1  indicate what */

/MODE1              /*      type of access                      */

C0                  /* M Bus control signal indicating read or write cycle   */

C1            /* MBus control signal indicating the end of a burst transfer */

/WRITE              /* Indicates a read/write access                         */

/MEM                /* Address is in memory space                            */

Q0                  /* Q0 - Q4 indicate which state the state machine is in */

Q1
```

```
Q2

Q3

Q4

/**     Outputs          **/

/RAEND          /* End RAS signal                              */

/ENCAS          /* Enable CAS signal                     */

/MEMWR          /* Indicates a write to memory           */

/MEMOE      /* Output enable for 646 latches between MBus and DRAMs*/

/PGCNT          /* Used to toggle address lines for page-mode DRAMs */

/**     Logic Equations      **/

ENCAS       =   /Q1 & /Q2 & Q3 & /Q4 & MEM & /WRITE

                + /Q2 & Q3 & Q4 & MEM & Q0

                + /Q1 & /Q2 & Q3 & /Q4 & MODE1 & MODE0

                + /Q2 & Q3 & /Q4 & MEM & WRITE &  /Q0

                + /Q1 & /Q4 & Q0 & MODE1 & MODE0

                + Q1 & Q2 & Q3 & /Q4 & MODE1 & MODE0

                + /Q1 & /Q3 & Q4 & MEM & Q0

                + /Q2 & /Q4 & Q0 & MODE1 & MODE0

                + Q1 & Q2 & Q3 & Q4 & MEM

MEMOE       =   WRITE & Q0 & Q3 & MEM & /MODE0

                + Q1 & Q2 & MEM & /MODE0

                + /Q0 & /Q2 & Q3 & MEM & /MODE0

                + Q0 & Q4 & MEM & /MODE0

MEMWR       =   MEMWR & MEMOE

                + WRITE & Q0 & /Q4 & MEM & /MODE0

PGCNT       =   /Q0 & Q1 & Q2 & Q3 & /Q4 & MODE1 & /MODE0 & /C1

                + Q0  & Q1 & /Q3 & Q4

RAEND       =   /Q0 & Q1 & Q2 & Q3 & /Q4 & MODE1 & /MODE0 & C1
```

```
                        + /Q0 & Q1 & Q2 & Q3 & /Q4 & /MODE1 & MODE0

                        + Q0 & Q1 & Q2 & Q3 & /Q4 & MODE1 & MODE0

                        + Q0 & /Q1 & Q2 & Q3 & Q4


-----------------------------------------------------------------------------------

                NAME  MODE

                COMPANY      MOTOROLA

                PART         PAL22V10

/*********************************************************************************/

/*      This device determines which "master" is in control of the current cycle.  */

/*      It also generates the refresh request for the DRAM.                         */

/*********************************************************************************/

/**     Inputs              **/

CLK                 /* System clock                                         */

/MODE0              /* Together, MODE0 and MODE1  indicate what  */

/MODE1              /*        type of access                          */

Q0                  /* Q0 - Q4 indicate which state the state machine is in  */

Q1

Q2

Q3

Q4

/WRITE              /* Indicates a read/write access                  */

/MEM                /* Address is in memory space                     */

AD29                /* Multiplexed address/data line 29               */

AD31                /* Multiplexed address/data line 31               */

/**     Outputs               **/

/ENRAS              /* Enable RAS signal.                             */

CHECK               /* Used for parity checking                       */
```

```
/**     Logic Equations         **/

ENRAS           =       /Q0 & /Q1 & /Q2 & /Q3 & /Q4 & MODE1 & /MODE0 & /AD31
                        & AD20 & C0

                        + Q0 & Q1 &/Q2 &      & /Q4 & .MODE1 & MODE0 & MEM

                        + Q0 & Q1 & Q3 & /Q4 & MODE1 & MODE0

CHECK           =       /Q0 & /Q1 & Q2 & Q3 & /Q4 & MODE1 & /MODE0 & MEM
                        + /Q0 & /Q1 & /Q2 & /Q3 & Q4 & MODE1 & /MODE0 & MEM

                        + Q0 & /Q1 & /Q2 & /Q3 & Q4 & MODE1 & /MODE0 & MEM

                        + Q0 & /Q1 & /Q2 & Q3 & Q4 & MODE1 & /MODE0 & MEM

                        + Q0 & Q1 & Q2 & Q3 & Q4 & MODE1 & /MODE0 & MEM


--------------------------------------------------------------------------------------------------------

                NAME  AD2MA

                COMPANY       MOTOROLA

                PART          PAL16R6; 16V8

/*******************************************************************************/

/*      This device multiplexes the row and column bits to form the outputs       */

/*      MA5 through MA8.  During the address phase (C0 high),                    */

/*      the ADXX signals become the row address.  When ANYRAS                   */

/*      is asserted, the LAXX signals become the column address.  The column*/

/*      is held until the end of the memory cycle (ANYRAS is negated).   This   */

/*      device also latches AD13 and AD14.                                             */

/*******************************************************************************/

/**     Inputs          **/

CLK                     /* System clock                                         */

C0                      /* M Bus control signal for address/data phase    */

AD9                     /* Multiplexed address/data line 9                     */

AD10                    /* Multiplexed address/data line 10                    */

AD11                    /* Multiplexed address/data line 11                    */
```

```
AD12                /* Multiplexed address/data line 12            */
AD13                /* Multiplexed address/data line 13            */
AD14                /* Multiplexed address/data line 14            */
LA20                /* Latched address line 20                     */
LA21                /* Latched address line 21                     */
/**     Outputs              **/
LA13                /* Latched address line 13                     */
LA14                /* Latched address line 14                     */
MA5                 /* Multiplexed address line 5                  */
MA6                 /* Multiplexed address line 6                  */
MA7                 /* Multiplexed address line 7                  */
MA8                 /* Multiplexed address line 8                  */
/**     Logic Equations      **/
LA13        =       C0 & AD13
                    + /C0 & LA13
LA14        =       C0 & AD14
                    + /C0 & LA14
MA5         =       C0 &  /ANYRAS & AD9
                    + ANYRAS & LA13
MA6         =       C0 & /ANYRAS & AD10
                    + ANYRAS & LA14
MA7         =       C0 & /ANYRAS & AD11
                    + ANYRAS & LA20
MA8         =       C0 & /ANYRAS & AD12
                    + ANYRAS & LA21
```

```
---------------------------------------------------------------------------------------------

                  NAME  AD2MA/2

                  COMPANY       MOTOROLA

                  PART          PAL16R6; 16V8

/*************************************************************************************/

/*        This device multiplexes the row and column bits to form the outputs       */

/*        MA0, MA2, MA3, and MA10.  During the address phase (C0 high),            */

/*        the ADXX signals become the row address.  When ANYRAS                    */

/*        is asserted, the LAXX signals become the column address.  The column*/

/*        is held until the end of the memory cycle (ANYRAS is negated).           */

/*************************************************************************************/

/**       Inputs            **/

CLK                         /* System clock                                                 */

C0                          /* M Bus control signal for address/data phase     */

AD15                        /* Multiplexed address/data line 15                 */

AD16                        /* Multiplexed address/data line 16                 */

AD17                        /* Multiplexed address/data line 17                 */

AD18                        /* Multiplexed address/data line 18                 */

AD22                        /* Multiplexed address/data line 22                 */

AD23                        /* Multiplexed address/data line 23                 */

LA4                         /* Latched address line 4                                   */

LA5                         /* Latched address line 5                                   */

/**       Outputs                  **/

MA0                         /* Multiplexed address line 0                       */

MA2                         /* Multiplexed address line 2                       */

MA3                         /* Multiplexed address line 3                       */

MA10                 /* Multiplexed address line 10                      */

LA18                        /* Latched address line 18                          */
```

```
LA23                    /* Latched address line 23                    */

/**     Logic Equations         **/

LA23        =       C0 & AD23
                    + /C0 & LA23
LA18        =       C0 & AD18
                    + /C0 & LA18
MA0         =       C0 &  /ANYRAS & AD15
                    + ANYRAS & LA22
MA2         =       C0 & /ANYRAS & AD16
                    + ANYRAS & LA23
MA3         =       C0 & /ANYRAS & AD17
                    + ANYRAS & LA4
MA10  =     C0 & /ANYRAS & AD18
                    + ANYRAS & LA5


------------------------------------------------------------------------------------------------------------

            NAME  ADR2NIB
            COMPANY     MOTOROLA
            PART        PAL16R6; 16V8
/*************************************************************************************/
/*      This device latches LA2 and LA7 and controls page mode or nibble       */
/*      mode address operation.  It also controls the multiplexing of the row   */
/*      and column memory address as well as the changing of the memory        */
/*      address during page mode.                                               */
/*************************************************************************************/
/**     Inputs          **/
CLK                     /* System clock                                 */
C0                      /* M Bus control signal for address/data phase   */
```

```
PGCNT           /* Signal used to increment column address       */
ANYRAS          /* Indicates that a RAS signal is asserted       */
PAGE  /*Signal from jumper indicating page or nibble mode DRAMs */
AD2             /* Multiplexed address/data line 2      */
AD6             /* Multiplexed address/data line 6      */
AD7             /* Multiplexed address/data line 7      */
AD8             /* Multiplexed address/data line 8      */
LA3             /* Latched address line 5                         */
LA19            /* Latched address line 19              */
/**     Outputs                 **/
LA2             /* Latched address line 2                         */
LA7             /* Latched address line 7                         */
MA1             /* Multiplexed address line 1           */
MA4             /* Multiplexed address line 4           */
MNIB            /* Multiplexed address line 9           */
DRAS
/**     Logic Equations         **/
DRAS  =     ANYRAS
LA2         =   C0 & AD2
                + /C0 & LA2
LA7         =   C0 & AD7
                + /C0 & LA7
MA1         =   PAGE & C0 & /ANYRAS & AD7
                + PAGE     & ANYRAS & /LA2 & /PGCNT & /DRAS
                + PAGE & /C0 & ANYRAS & /MA1 & PGCNT & DRAS
                + PAGE & /C0 & ANYRAS & MA1 & /PGCNT & DRAS
                + /PAGE & C0 & /ANYRAS & AD6        /* nibble mode */
                + /PAGE & /C0 & ANYRAS & LA7
```

```
MA4         =     PAGE & C0 & /ANYRAS & AD6
                  + PAGE      & ANYRAS & LA3 & /PGCNT & /DRAS
                  + PAGE & /C0 & ANYRAS & MA4 & /PGCNT & DRAS
                  +PAGE & /C0 & ANYRAS & /MA4 & PGCNT & DRAS & MA1
                  + PAGE & /C0 & ANYRAS & MA4           & DRAS &/ MA1
                  + /PAGE & C0 & /ANYRAS & AD8        /* nibble mode   */
                  + /PAGE & /C0 & ANYRAS & LA19
MNIB        =     PAGE & C0 & /ANYRAS & AD8
                  + PAGE        & ANYRAS & LA19
                  + /PAGE  C0 & /ANYRAS & AD2         /* nibble mode   */
                  + /PAGE       & ANYRAS & LA3

--------------------------------------------------------------------------------------------

            NAME  WRITE
            COMPANY     MOTOROLA
            PART        PAL22V10
/***************************************************************************/
/*    This device decodes the physical memory address space and also      */
/*    generates the WRITE signal.                                                   */
/***************************************************************************/
/**   Inputs          **/
CLK                 /* System clock                                        */
/MODE0              /* Together, MODE0 and MODE1 indicate what  */
/MODE1              /*      type of access                      */
C0                  /* M Bus control signal for address/data phase   */
C2                  /* M Bus control signal indicating memory read/write  */
AD29                /* Multiplexed address/data line 29              */
AD30                /*     "              "         "  30              */
```

```
AD31                /*    "           "        "  31           */
/SRST         /* System reset signal                          */
/**     Outputs              **/
/MEM                /* Indicates address is a valid memory address   */
/WRITE              /* Indicates memory write                                  */
/**     Logic Equations      **/
MEM          =      /SRST & /AD31 & /AD30 & AD29 & C0
                    + /SRST &  MEM & /MODE1 & MODE0
                    + /SRST &  MEM & MODE1 & /MODE0
WRITE =             /SRST & C2 & C0
                    + /SRST & WRITE & /MODE1 & MODE0
                    + /SRST & WRITE & MODE1 & /MODE0


------------------------------------------------------------------------------------------------
              NAME  STATE
              COMPANY     MOTOROLA
              PART        PAL22V10
/*******************************************************************************/
/*      This device holds the system state machine.  It also controls the WAIT   */
/*      and OK signals to the 88K.                                              */
/*******************************************************************************/
/**     Inputs            **/
CLK                 /* System clock                                            */
C0                  /* M Bus control signal indicating read or write cycle   */
C1            /* M Bus control signal indicating the end of a burst transfer  */
/MEM                /* Indicates a write to memory                  */
/WRITE              /*  Indicates a read/write access               */
/MODE0              /* Together, MODE0 and MODE1  indicate what  */
```

```
/MODE1              /*      type of access                            */

/**     Outputs           **/

Q0                  /* Q0 - Q4 indicate which state the state machine is in */

Q1

Q2

Q3

Q4

OK                  /* Used to tell whether the memory transaction was     */
                    /*completed successfully                               */

/**     Logic Equations           **/

Q0          =       Q0 & /Q1 & Q2 & /Q4 & MODE1 & MODE0

                    + Q0 & /Q1 & /Q3

                    + Q0 & /Q1 & Q2 & /Q4 & MODE1 & WRITE

                    + Q0 & Q1 & Q4

                    + /Q0 & /Q1 & /Q2 & /Q3 & /Q4 & MODE1 & C0

                    + Q1 & Q2 & Q3 & MOED1 & MODE0

                    + /Q1 & /Q2 &  /Q3 & /Q4 & MODE1 & MODE0

                    + Q1 & Q2 & Q3 & Q4

                    + Q0 & Q1 & Q3

                    + Q0 & /Q2 & Q4

                    + Q0 & Q1 & /Q2

                    + Q0 & /Q1 & Q2 & /Q3

Q1          =       MODE1 & MODE0 & Q0 & /Q2 & /Q3

                    + MODE1 & MODE0 & /Q0 & Q1 & Q2 & Q3

                    + MODE1 & /MODE0 & /Q0 & Q1 & /Q2 & /Q4

                    + MODE0 & Q0 & /Q2 & /Q3 & MEM

                    + Q0 & /Q2 & /Q3

                    + Q0 & Q1 & /Q2 & /Q3
                    + /Q0 & /Q2 & Q3 & /Q4
                    + Q1 & Q2 & Q3 & Q4
                    + Q0 & /Q2 & /Q3 & Q4
                    + Q0 & Q2 & /Q3 & /Q4
Q2          =       /Q0 & Q3 & /Q4 & MODE0 & /MEM
                    + Q2 & Q3 & /Q4
                    + /Q0 & Q3 & /Q4 & MODE0 & MODE1
                    + /Q0 & Q3 & /Q4 & /MODE0 & /MODE1
                    + Q0 & Q1 & Q2
                    + Q0 & /Q1 & Q3 & Q4
                    + /Q0 & Q3 & /Q4 & /WRITE
                    + Q0 & Q2 & /Q4
                    + Q1 & Q2 & /Q4
                    + Q1 & Q2 & Q3
                    + /Q0 & Q1 & Q3 & /Q4
Q3          =       Q0 & /Q1 & Q3 & /MODE0 & /WRITE
                    + Q0 & /Q1 & Q3 & /MODE1
                    + /Q2 & Q3 & /Q4
                    + Q0 & /Q2 & /Q4 & /MODE1 & /MEM
                    + Q0 & /Q2 & /Q4 & /MODE0 & /MODE1
                    + /Q0 & Q1 & Q2 & Q3
                    + Q0 & Q1 & /Q2
                    + Q0 & /Q1 & Q3 & Q4
                    + Q1 & Q3 & /Q4
Q4          =       /Q0 & Q1 & Q2 & Q3 & /C1 & /MODE0
                    + Q0 & Q4
                    + Q2 & Q3 & Q4
OK          =       MODE1 & /MODE0 & MEM & /Q0 & Q1 & Q2 & Q3 & /Q4 &  C1
```

```
                    + MODE1 & /MODE0 & MEM & Q0 & /Q1 & /Q2 & Q3 &  Q4 & WRITE

                    + MODE1 & /MODE0 & MEM & Q0 & /Q1 & Q2 & Q3 & Q4 &  /WRITE

/WAIT       =       /MODE1 & MODE0 & Q0 & /Q1 & /Q2 & /Q3 & /Q4 & MEM

                    + MODE1 & /MODE0 & Q0 & Q1 & Q2 & Q3 & Q4 & MEM &  WRITE

                    + MODE1 & /MODE0 & /Q0 & Q1 & /Q2 & Q3 & /Q4 & MEM  & WRITE

                    + MODE1 & /MODE0 & /Q0 & /Q1 & /Q2 & /Q3 & /Q4 & C0

                    + MODE1 & /MODE0 & /Q0 & Q1 & Q2 & Q3 & /Q4 & MEM & /WRITE

                    + MODE1 & /MODE0 & Q0 & /Q1 & Q2 & Q3 & Q4 & MEM & /WRITE

                    + MODE1 & MODE0 & Q0 & Q1 & /Q3 & Q4 & MEM & /WRITE

                    + MODE1 & /MODE0 & Q0 & /Q1 & /Q2 & Q4 & MEM & WRITE

                    + MODE1 & /MODE0
```

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN1127

Application Note

High Speed DRAM Design for the 40 MHz MC68EC030

This design demonstrates a memory solution using inexpensive DRAM to provide the performance and density required for today's high performance embedded control systems.

DIFFERENCES IN DRAM AND SRAM

While SRAMs are generally easier to interface at higher speeds, they are limited in size and by higher cost. DRAMs provide larger capacities at a lower price, but have increased interfacing complexity and slower access time. The DRAM addresses must be multiplexed to divide them between the row and column addresses. Instead of the SRAM's simple chip select, DRAMs require two signals to latch in the row and column addresses. The DRAM output enable and write enable signals are similar to their SRAM equivalents.

Except for the newer bursting SRAM like the MCM62940, SRAMs generally require less access time, but the time is constant for each address. Because the DRAM separates the addresses between row and column, access times between different memory locations vary greatly. If both row and column addresses are needed, the access time is 2 to 3 times longer than changing only the column addresses. The MC68EC030 exploits the difference in DRAM access time by bursting, which stores the next three long words in the MC68EC030 on-chip caches. There are three main types of DRAM: page mode, static column and nibble mode. Each of these allows subsequent accesses to memory locations in different ways. Page mode requires both the column address and the column address strobe to be changed to access the next address with the same row address. Static column requires only the column address to be changed to access the next address with the same row address. Nibble mode requires only the column address strobe to be changed, but only four contiguous memory locations can be accessed.

A final difference between the two memory types gives them their names. SRAMs (Static Random Access Memory) are static memory devices i.e., the data will remain as long as the part is powered. The DRAMs (Dynamic Random Access Memory) are dynamic and require periodic refreshing to avoid losing data. Because the DRAM are unavailable during refresh, a DRAM design may have lower performance than an SRAM design of the same speed. The performance difference depends on the number of MPU accesses attempted during refresh.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ACCESS TIMING

The MC68EC030 has three types of accesses suitable for DRAM; read access with burst, read access without burst, and write access without burst. Figure 1 shows the timing for a read access with burst. Figure 2 shows a read access without burst. Figure 3 shows a write access. The DRAM interface logic further divides these three types of accesses based on whether the access immediately follows the previous access or there was one or more idle clock periods in between. Figures 1, 2 and 3 show accesses with one or more idle clocks before $\overline{\text{AS}}$ going low. Figure 4 shows a burst read being immediately followed by a byte write access. The MC68EC030 uses about 60% of the bus with 5 clock initial, 2 clock bursting. The remaining 40% is available to other bus masters. Thus, for a large portion of the time, the accesses are not back-to-back and will have one or more idle clock periods in between accesses.

The read access with burst is the most challenging for the DRAM interface, but allows read accesses to fill the on-chip caches efficiently. Studies show that typical programs spend most of their execution time in a few main routines or tight loops (known as locality of reference). Therefore, for any given instruction, the probability is high that you will need the next sequential instruction or will loop back to a nearby instruction. In a burst access, the MC68EC030 reads the first long word of the burst access, and then reads the next three sequential long words. The MC68EC030 provides only the first longword's address. The remaining three longwords are modulo four offsets from the starting longword's address. The MC68EC030 requests the burst access by the Cache Burst REQuest ($\overline{\text{CBREQ}}$) signal. The burst is acknowledged to the MC68EC030 by Synchronous TERMination ($\overline{\text{STERM}}$) signal and Cache Burst ACKnowledge ($\overline{\text{CBACK}}$).

The three types of accesses start the same. The multiplexer passes the row addresses through to the DRAM. The control logic asserts the row address strobe ($\overline{\text{RAS}}$) signal. $\overline{\text{RAS}}$ is based on the MC68EC030 address strobe ($\overline{\text{AS}}$) being asserted, a decode of the address pins, and the state machine indicating the $\overline{\text{RAS}}$ recovery time is over. Next, after a $\overline{\text{RAS}}$ assertion to row address hold time, the ROW address/COLumn address (ROW/$\overline{\text{COL}}$) change switches the addresses to the column address of the first long word being accessed. The control logic asserts the column strobe ($\overline{\text{CS}}$). Then the control logic asserts the $\overline{\text{STERM}}$ before the rising edge of the fifth clock. In a read without burst access, the DRAMs present all four bytes of data to the MC68EC030 and the MC68EC030 selects which bytes it needs. In a write access, the $\overline{\text{CS}}$ signals the DRAM which bytes to store. In a read burst access, the MC68EC030 always requires all 32 bits for each of the four accesses.

The $\overline{\text{CS}}$ are divided between the four byte lanes. These byte lanes are selected by a decode of the SIZe (SIZ1, SIZ0), lower two addresses (A1, A0) and the Read/Write (R/$\overline{\text{W}}$). Upper Upper byte ($\overline{\text{UU}}$) is the byte enable for D31 - D24. Upper Middle byte ($\overline{\text{UM}}$) is the byte enable for D23 - D16. Lower Middle byte ($\overline{\text{LM}}$) is the byte enable for D15 - D8. Lower Lower byte ($\overline{\text{LL}}$) is the byte enable for D7 - D0.

$\overline{\text{UU}}$ = $\overline{\text{AS}}$ & $\overline{\text{R/W}}$ & $\overline{\text{A1}}$ & $\overline{\text{A0}}$; write access
# $\overline{\text{AS}}$ & R/W ; read access

$\overline{\text{UM}}$ = $\overline{\text{AS}}$ & $\overline{\text{R/W}}$ & $\overline{\text{SIZ0}}$ & $\overline{\text{A1}}$; write access word or long word
# $\overline{\text{AS}}$ & $\overline{\text{R/W}}$ & SIZ1 & $\overline{\text{A1}}$; write access word or 3 byte
# $\overline{\text{AS}}$ & $\overline{\text{R/W}}$ & $\overline{\text{A1}}$ & A0 ; write access byte 2
# $\overline{\text{AS}}$ & R/W ; read access

$\overline{\text{LM}}$ = $\overline{\text{AS}}$ & $\overline{\text{R/W}}$ & $\overline{\text{SIZ1}}$ & $\overline{\text{SIZ0}}$ & $\overline{\text{A1}}$; write access long word
# $\overline{\text{AS}}$ & $\overline{\text{R/W}}$ & SIZ1 & SIZ0 & $\overline{\text{A1}}$; write access 3 byte
# $\overline{\text{AS}}$ & $\overline{\text{R/W}}$ & $\overline{\text{SIZ0}}$ & $\overline{\text{A1}}$ & A0 ; write access word or long word
# $\overline{\text{AS}}$ & $\overline{\text{R/W}}$ & A1 & $\overline{\text{A0}}$; write access byte 3
# $\overline{\text{AS}}$ & R/W ; read access

$\overline{\text{LL}}$ = $\overline{\text{AS}}$ & $\overline{\text{R/W}}$ & $\overline{\text{SIZ1}}$ & $\overline{\text{SIZ0}}$; write access long word
# $\overline{\text{AS}}$ & $\overline{\text{R/W}}$ & SIZ1 & SIZ0 & A0 ; write access 3 byte
# $\overline{\text{AS}}$ & $\overline{\text{R/W}}$ & SIZ1 & A1 ; write access word or 3 byte
# $\overline{\text{AS}}$ & $\overline{\text{R/W}}$ & A1 & A0 ; write access byte 4
# $\overline{\text{AS}}$ & R/W ; read access

Now, the access differs based on the status of the $\overline{\text{CBREQ}}$ of the MC68EC030. The $\overline{\text{CBREQ}}$ signals the state machine to add the extra burst clocks required. The MC68EC030 reads the data on the falling edge of the fifth clock of the access. The control logic changes the column address with that falling clock edge. The data hold time required by the MC68EC030 is guaranteed by the minimum switching time of the multiplexing PAL and the DRAM data hold time. The access continues with the $\overline{\text{STERM}}$ being asserted at every other rising clock edge and the data being presented to the MC68EC030 on the following falling edge.

The read bursts, read without burst and write accesses again become the same with the last long word access. For the read without burst and write access, the last long word access is also the first long word access. $\overline{\text{RAS}}$ goes high with the falling edge of the final clock of the access. The ROW/$\overline{\text{COL}}$ and $\overline{\text{CS}}$ go high with the rising edge of the clock after the last access. This completes the access. The logic delays the next access by one clock if the $\overline{\text{AS}}$ is asserted before the $\overline{\text{RAS}}$ is recharged.

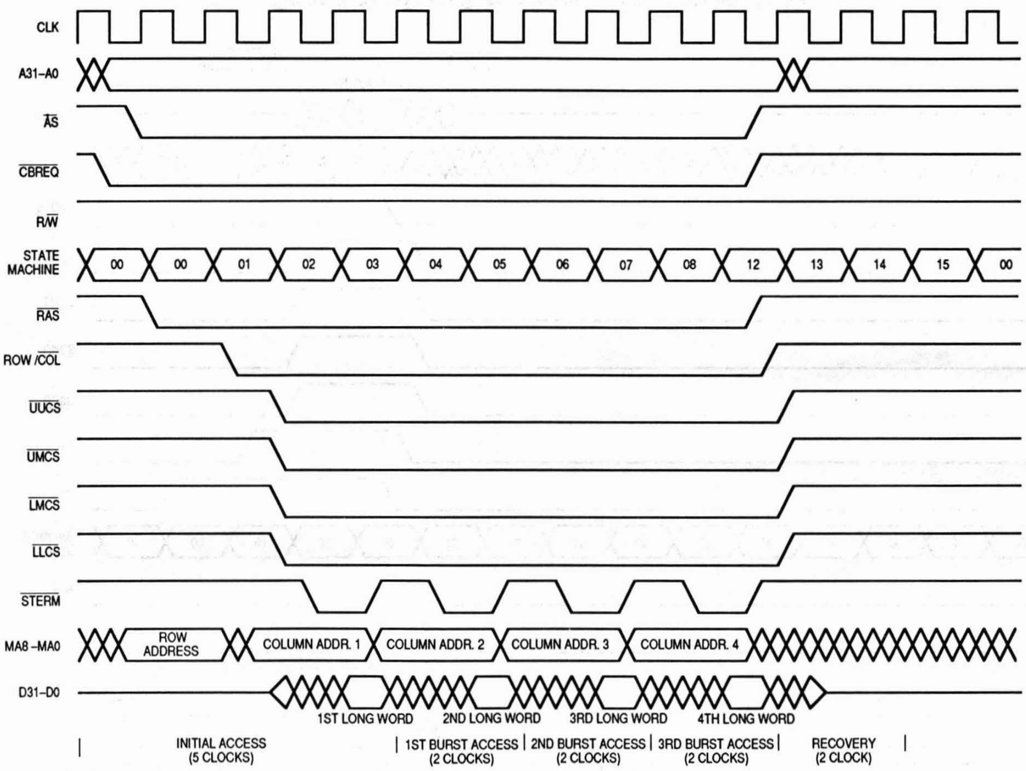

CLK
A31–A0
AS
CBREQ
R/W
STATE MACHINE
00
00
01
02
03
04
05
06
07
08
12
13
14
15
00
RAS
ROW /COL
UUCS
UMCS
LMCS
LLCS
STERM
MA8 –MA0
ROW ADDRESS
COLUMN ADDR. 1
COLUMN ADDR. 2
COLUMN ADDR. 3
COLUMN ADDR. 4
D31–D0
1ST LONG WORD
2ND LONG WORD
3RD LONG WORD
4TH LONG WORD
INITIAL ACCESS (5 CLOCKS)
1ST BURST ACCESS (2 CLOCKS)
2ND BURST ACCESS (2 CLOCKS)
3RD BURST ACCESS (2 CLOCKS)
RECOVERY (2 CLOCK)

Figure 1. Burst Read Access Followed by Idle Clocks

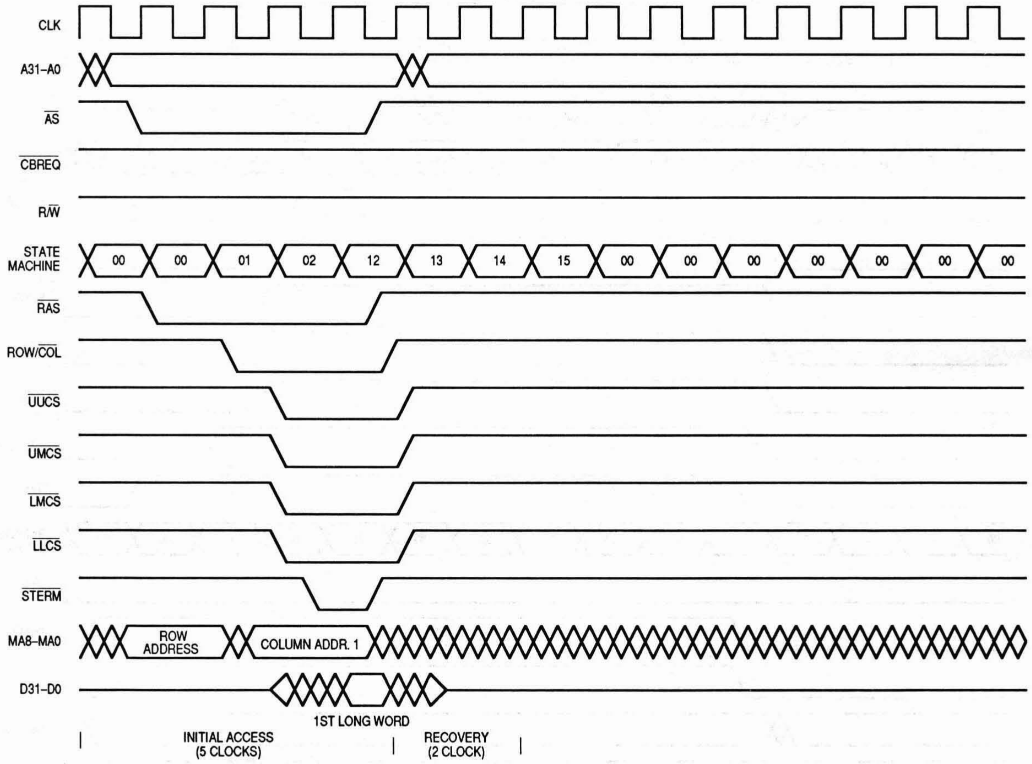

CLK
A31–A0
AS
CBREQ
R/W
STATE MACHINE
00
00
01
02
12
13
14
15
00
00
00
00
00
00
00
RAS
ROW/COL
UUCS
UMCS
LMCS
LLCS
STERM
MA8–MA0
ROW ADDRESS
COLUMN ADDR. 1
D31–D0
1ST LONG WORD
INITIAL ACCESS (5 CLOCKS)
RECOVERY (2 CLOCK)

Figure 2. Non-Burst Read Access Followed by Idle Clocks

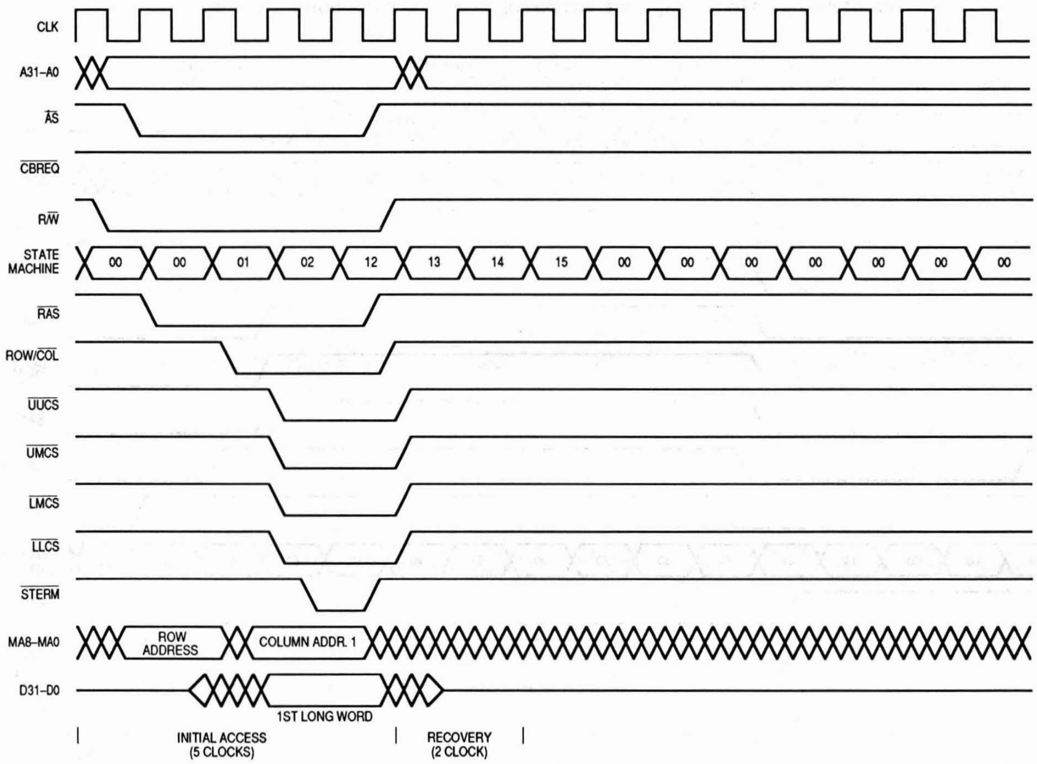

CLK
A31–A0
AS
CBREQ
R/W
STATE MACHINE
00
00
01
02
12
13
14
15
00
00
00
00
00
00
00
RAS
ROW/COL
UUCS
UMCS
LMCS
LLCS
STERM
MA8–MA0
ROW ADDRESS
COLUMN ADDR. 1
D31–D0
1ST LONG WORD
INITIAL ACCESS (5 CLOCKS)
RECOVERY (2 CLOCK)

Figure 3. Non-Burst Write Access Followed by Idle Clocks

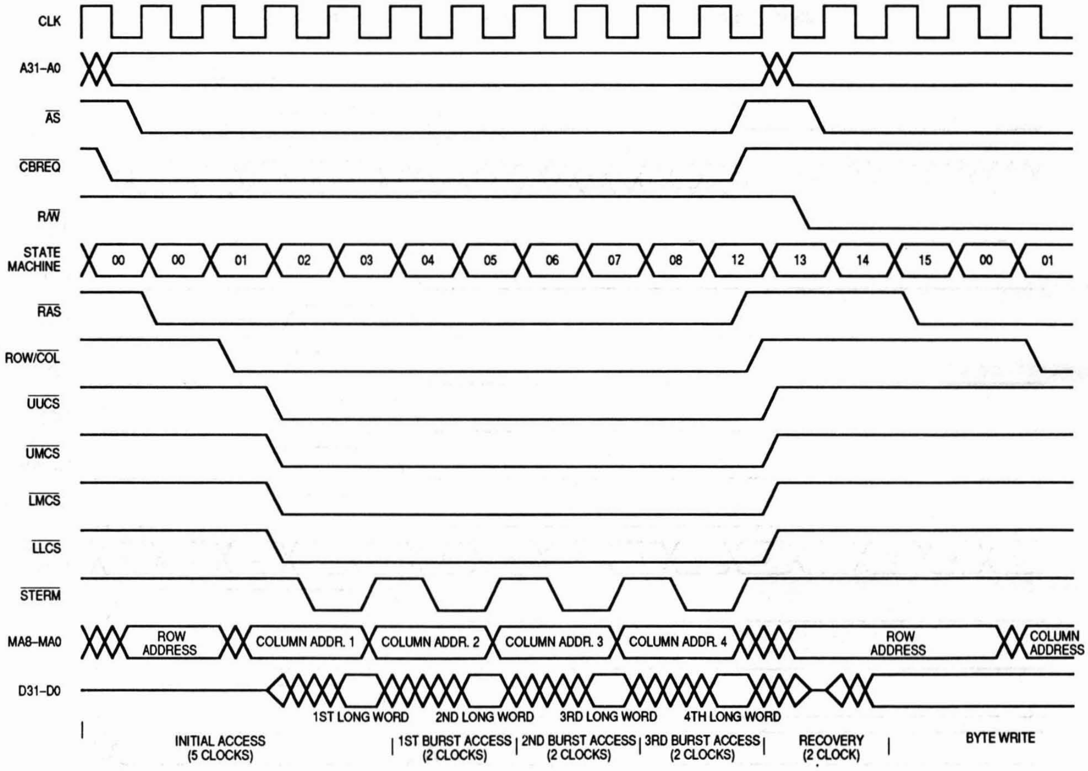
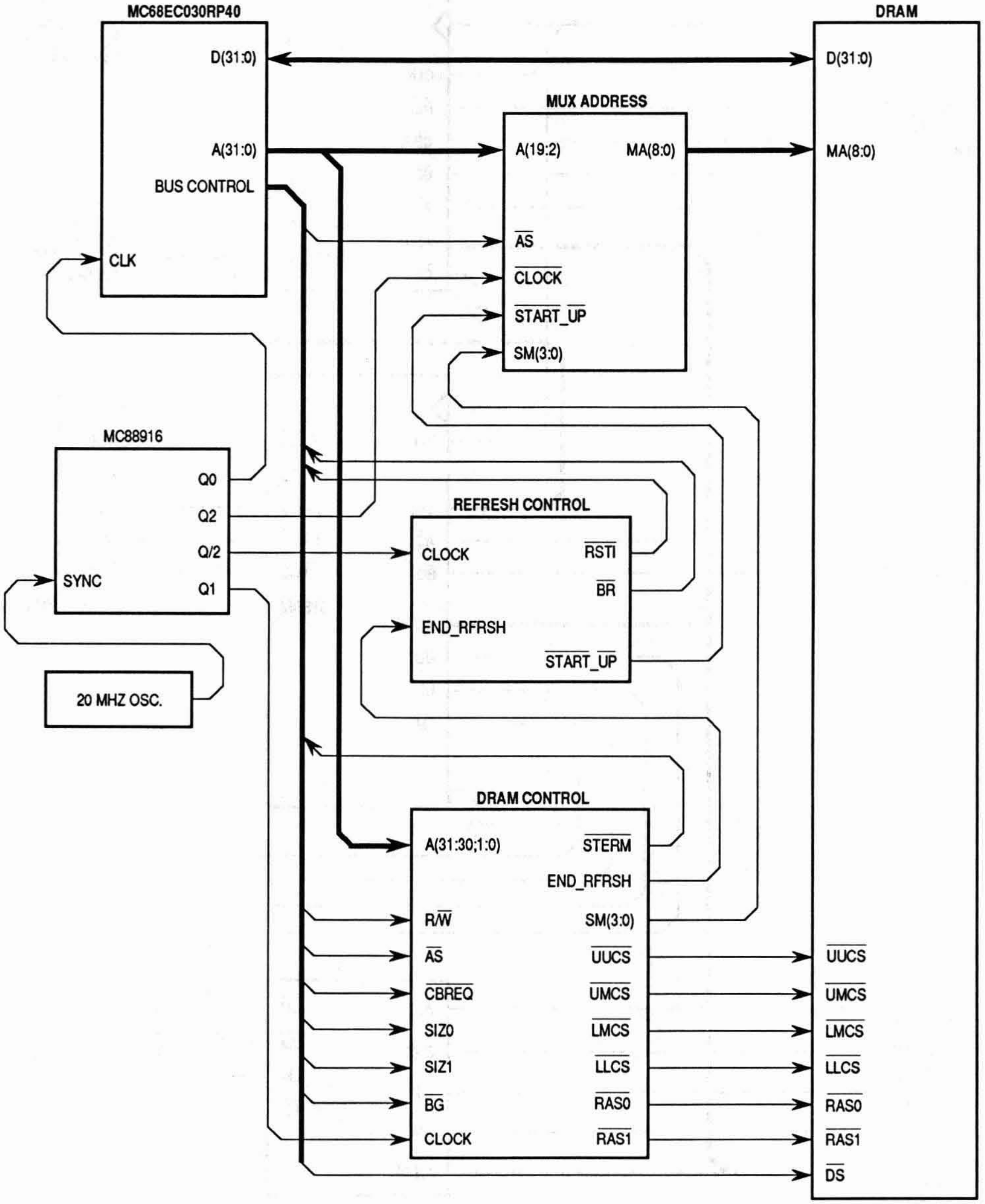

CLK
A31–A0
AS
CBREQ
R/W
STATE MACHINE
00
00
01
02
03
04
05
06
07
08
12
13
14
15
00
01
RAS
ROW/COL
UUCS
UMCS
LMCS
LLCS
STERM
MA8–MA0
ROW ADDRESS
COLUMN ADDR. 1
COLUMN ADDR. 2
COLUMN ADDR. 3
COLUMN ADDR. 4
ROW ADDRESS
COLUMN ADDRESS
D31–D0
1ST LONG WORD
2ND LONG WORD
3RD LONG WORD
4TH LONG WORD
INITIAL ACCESS (5 CLOCKS)
1ST BURST ACCESS (2 CLOCKS)
2ND BURST ACCESS (2 CLOCKS)
3RD BURST ACCESS (2 CLOCKS)
RECOVERY (2 CLOCK)
BYTE WRITE

Figure 4. Burst Read Access Followed Immediately by a Byte Write Access

DESIGN OVERVIEW

This design (Figure 5) has five main parts: MC68EC030RP40, memory control logic, address multiplexing, one megabyte memory, and refresh control logic. These five parts interact to provide 5 clocks read initial access, 2 clocks read burst access, and 5 clocks write access at 40 MHz. The memory control logic is the most difficult part because of the tight timing requirements.

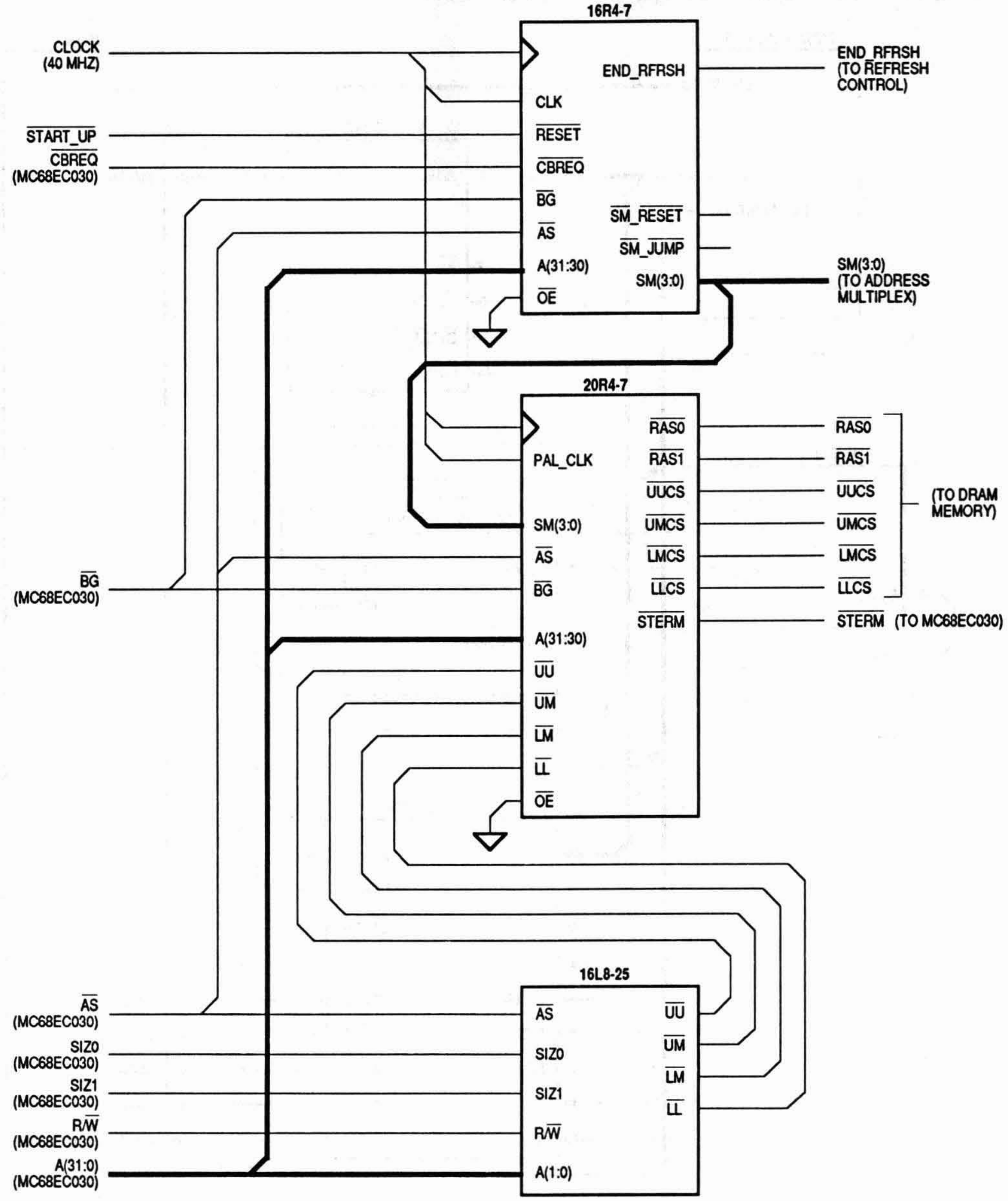


MC68EC030RP40
D(31:0)
A(31:0)
BUS CONTROL
CLK
DRAM
D(31:0)
MA(8:0)
MUX ADDRESS
A(19:2)
MA(8:0)
AS
CLOCK
START_UP
SM(3:0)
MC88916
Q0
Q2
Q/2
SYNC
Q1
20 MHZ OSC.
REFRESH CONTROL
CLOCK
RSTI
BR
END_RFRSH
START_UP
DRAM CONTROL
A(31:30;1:0)
STERM
END_RFRSH
R/W
SM(3:0)
AS
UUCS
CBREQ
UMCS
SIZ0
LMCS
SIZ1
LLCS
BG
RAS0
CLOCK
RAS1
UUCS
UMCS
LMCS
LLCS
RAS0
RAS1
DS

Figure 5. MC68EC030 System with DRAM Control

MEMORY CONTROL LOGIC

The memory control logic (Figure 6) has three subsections: DRAM address strobe generation, state machine generation, and access termination generation. The DRAM output enables connect to Data Strobe ($\overline{\text{DS}}$) of the MC68EC030. The DRAMs drive the bus when $\overline{\text{RAS}}$, $\overline{\text{CS}}$, $\overline{\text{DS}}$ are asserted low and R/$\overline{\text{W}}$ is asserted high.



16R4-7
CLOCK (40 MHZ)
START_UP
CBREQ (MC68EC030)
CLK
RESET
CBREQ
BG
AS
A(31:30)
OE
END_RFRSH
SM_RESET
SM_JUMP
SM(3:0)
END_RFRSH (TO REFRESH CONTROL)
SM(3:0) (TO ADDRESS MULTIPLEX)
20R4-7
PAL_CLK
SM(3:0)
AS
BG
A(31:30)
UU
UM
LM
LL
OE
RAS0
RAS1
UUCS
UMCS
LMCS
LLCS
STERM
RAS0
RAS1
UUCS
UMCS
LMCS
LLCS
(TO DRAM MEMORY)
STERM (TO MC68EC030)
BG (MC68EC030)
16L8-25
AS (MC68EC030)
SIZ0 (MC68EC030)
SIZ1 (MC68EC030)
R/W (MC68EC030)
A(31:0) (MC68EC030)
AS
SIZ0
SIZ1
R/W
A(1:0)
UU
UM
LM
LL

Figure 6. Memory Control Logic

The DRAMs address strobe generation provides the $\overline{\text{RAS}}$ and $\overline{\text{CS}}$. These two signals tell the DRAMs when the row and column addresses are valid, respectively. These addresses must be valid concurrent or before their respective $\overline{\text{RAS}}$ or $\overline{\text{CS}}$ are asserted. In addition, the logic must hold the addresses for a certain amount of time after the respective strobes. The $\overline{\text{RAS}}$ is split into two signals, with identical signal generation for the $\overline{\text{RAS}}$ pair. The split decreases the capacitive loading the PALs must drive. A 7 ns PAL was used for the worst case timing of $\overline{\text{CS}}$ asserted to data valid on the first access. This provides 4 ns margin for clock skew and wire delay between DRAMs and processor. The $\overline{\text{CS}}$ uses the byte enables to determine which byte the DRAMs store on a write. The byte enables are generated in a separate PAL because of the lack of terms to decode the address and size signals.

The equation for $\overline{\text{RAS}}$ assertion consists of the $\overline{\text{RAS}}$ assertion in normal access and the $\overline{\text{RAS}}$ assertion for refreshes. For the purposes of this design, the memory is assumed to be on the second gigabyte of address space (A31 = 0, A30 = 1).

$\overline{\text{RAS}}$x = $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$; $\overline{\text{RAS}}$ assert states 0 to 3
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & SM2 ; $\overline{\text{RAS}}$ assert states 4 to 7
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & SM3 & $\overline{\text{SM3}}$ & $\overline{\text{SM1}}$ & $\overline{\text{SM0}}$; $\overline{\text{RAS}}$ assert state 8
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & SM3 & $\overline{\text{SM2}}$ & SM1 & $\overline{\text{SM0}}$ & CLK ; $\overline{\text{RAS}}$ assert state 12
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & SM3 & $\overline{\text{SM2}}$ & $\overline{\text{SM1}}$ & $\overline{\text{SM0}}$; $\overline{\text{RAS}}$ assert state 15
# AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM1 ; refresh $\overline{\text{RAS}}$ state 2,3
# AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & SM2 ; refresh $\overline{\text{RAS}}$ state 4 to 7

The equation for $\overline{\text{CS}}$ assertion consists of the $\overline{\text{CS}}$ assertion in normal access and the $\overline{\text{CS}}$ assertion for refreshes. For the purposes of this design, the DRAM memory is assumed to be on the second gigabyte of address space (A31 = 0, A30 = 1).

$\overline{\text{UUCS}}$:= AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM0 ; refresh $\overline{\text{CS}}$ state 1, 3
# AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM1 ; refresh $\overline{\text{CS}}$ states 2, 3
# AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & SM2 & $\overline{\text{SM1}}$; refresh $\overline{\text{CS}}$ state 4, 5
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM0 & $\overline{\text{UU}}$; $\overline{\text{CS}}$ assert states 1, 3
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM1 & $\overline{\text{UU}}$; $\overline{\text{CS}}$ assert states 2, 3
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & SM2 & $\overline{\text{UU}}$; $\overline{\text{CS}}$ assert states 4 to 7
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & SM3 & SM2 & $\overline{\text{SM1}}$ & $\overline{\text{SM0}}$ & $\overline{\text{UU}}$; $\overline{\text{CS}}$ assert state 8
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & SM3 & $\overline{\text{SM2}}$ & SM1 & $\overline{\text{SM0}}$ & $\overline{\text{UU}}$; $\overline{\text{CS}}$ assert state 12

$\overline{\text{UMCS}}$:= AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM0 ; refresh $\overline{\text{CS}}$ state 1, 3
# AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM1 ; refresh $\overline{\text{CS}}$ states 2, 3
# AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & SM2 & $\overline{\text{SM1}}$; refresh $\overline{\text{CS}}$ state 4, 5
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM0 & $\overline{\text{UM}}$; $\overline{\text{CS}}$ assert states 1, 3
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM1 & $\overline{\text{UM}}$; $\overline{\text{CS}}$ assert states 2, 3
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & SM2 & $\overline{\text{UM}}$; $\overline{\text{CS}}$ assert states 4 to 7
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & SM3 & SM2 & $\overline{\text{SM1}}$ & $\overline{\text{SM0}}$ & $\overline{\text{UM}}$; $\overline{\text{CS}}$ assert state 8
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & SM3 & $\overline{\text{SM2}}$ & SM1 & $\overline{\text{SM0}}$ & $\overline{\text{UM}}$; $\overline{\text{CS}}$ assert state 12

$\overline{\text{LMCS}}$:= AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM0 ; refresh $\overline{\text{CS}}$ state 1, 3
# AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM1 ; refresh $\overline{\text{CS}}$ states 2, 3
# AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & SM2 & $\overline{\text{SM1}}$; refresh $\overline{\text{CS}}$ state 4, 5
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM0 & $\overline{\text{LM}}$; $\overline{\text{CS}}$ assert states 1, 3
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM1 & $\overline{\text{LM}}$; $\overline{\text{CS}}$ assert states 2, 3
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & SM2 & $\overline{\text{LM}}$; $\overline{\text{CS}}$ assert states 4 to 7
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & SM3 & SM2 & $\overline{\text{SM1}}$ & $\overline{\text{SM0}}$ & $\overline{\text{LM}}$; $\overline{\text{CS}}$ assert state 8
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & SM3 & $\overline{\text{SM2}}$ & SM1 & $\overline{\text{SM0}}$ & $\overline{\text{LM}}$; $\overline{\text{CS}}$ assert state 12

$\overline{\text{LLCS}}$:= AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM0 ; refresh $\overline{\text{CS}}$ state 1, 3
AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM1 ; refresh $\overline{\text{CS}}$ states 2, 3
AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & SM2 & $\overline{\text{SM1}}$; refresh $\overline{\text{CS}}$ state 4, 5
$\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM0 & $\overline{\text{LL}}$; $\overline{\text{CS}}$ assert states 1, 3
$\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM1 & $\overline{\text{LL}}$; $\overline{\text{CS}}$ assert states 2, 3
$\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & SM2 & $\overline{\text{LL}}$; $\overline{\text{CS}}$ assert states 4 to 7
$\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & SM3 & SM2 & $\overline{\text{SM1}}$ & $\overline{\text{SM0}}$ & $\overline{\text{LL}}$; $\overline{\text{CS}}$ assert state 8
$\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & SM3 & $\overline{\text{SM2}}$ & SM1 & $\overline{\text{SM0}}$ & $\overline{\text{LL}}$; $\overline{\text{CS}}$ assert state 12

The state machine generation provides information on the state of the bus cycle to the rest of the control logic. The four bits of the state machine provide 16 states. The control logic does not use all the possible states. The state machine PAL includes two state machine control signals. State Machine JuMP (SMJMP) jumps the state to the closing sequence of states for a DRAM access. State Machine ReSeT (SMRST) resets the state to the initial state of a DRAM access. A 7 ns PAL meets the timing requirements of the state machine within a clock period. The state machine PAL recognizes and responds to the new state. The state machine control signals must meet the proper setup time to the next clock edge. This total sequence is 17.5 ns, 7.5 ns less than the 40 MHz clock period. A 10 ns PAL would use 27 ns for the three stages, 2 ns more than the 40 MHz clock period.

The $\overline{\text{SMRST}}$ equation holds the state machine in state 0 during reset and while the MC68EC030 is not accessing the DRAM. If the state machine is to be used for other peripherals (e.g., ROM timing), then the $\overline{\text{SMRST}}$ equation would have to be altered to enable the counting for other peripherals. For the purposes of this design, the memory is assumed to be on the second gigabyte of address space (A31 = 0, A30 = 1).

$\overline{\text{SMRST}}$ = AS & BG & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & $\overline{\text{SM1}}$ & $\overline{\text{SM0}}$; idle clock
$\overline{\text{RESET}}$; reset
$\overline{\text{AS}}$ & A31 ; access to non-DRAM
$\overline{\text{AS}}$ & A31 & $\overline{\text{A30}}$; access to non-DRAM
$\overline{\text{SMRST}}$ & $\overline{\text{CLK}}$; hold for last half of clock

The $\overline{\text{SMJMP}}$ equation jumps the state at the end of a burst access, a non-burst access and a refresh. If the state machine is to be used for other peripherals (e.g., ROM timing), then the $\overline{\text{SMJMP}}$ equation would have to be altered to complete the counting for other peripherals. For the purposes of this design, the memory is assumed to be on the second gigabyte of address space (A31 = 0, A30 = 1).

$\overline{\text{SMJMP}}$ = $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & SM3 & SM2 & $\overline{\text{SM1}}$ & $\overline{\text{SM0}}$ & $\overline{\text{CBREQ}}$; end burst; state 8
$\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM1 & SM0 & CBREQ ; end non-burst; state 2
AS & $\overline{\text{BG}}$ & $\overline{\text{SM3}}$ & SM2 & SM1 & SM0 ; end refresh; state 5

The state machine equations are expressed both as their algorithm and their specific equations. If the state machine is to be used for other peripherals (e.g., ROM timing), then the $\overline{\text{SMJMP}}$ and $\overline{\text{SMRST}}$ equations would have to be altered to count for other peripherals. The state machine is a grey code counter, i.e., only one bit changes at a time This prevents the difference in the high to low and low to high transition times from causing spikes in other decode logic. SM3 is the high order bit, SM0 is the low order bit.

S00 = 0000 S01 = 0001 S02 = 0011 S03 = 0010
S04 = 0110 S05 = 0111 S06 = 0101 S07 = 0100
S08 = 1100 S09 = 1101 S10 = 1111 S11 = 1110
S12 = 1010 S13 = 1011 S14 = 1001 S15 = 1000

```
STATE  Sn:
       IF        SMJMP          THEN    S12     ; jump to ending sequence
       ELSE IF   SMRST          THEN    S0      ; hold in reset
       ELSE      Sn+1
```

$\overline{\text{SM3}}$:= $\overline{\text{SMRST}}$; state reset
# $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SMRST & SMJMP ; state 0 to 3
# $\overline{\text{SM3}}$ & SM2 & SM1 & SMRST & SMJMP ; state 4, 5
# $\overline{\text{SM3}}$ & SM2 & $\overline{\text{SM1}}$ & SM0 & SMRST & SMJMP ; state 7

$\overline{\text{SM2}}$:= $\overline{\text{SMRST}}$; state reset
# $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & $\overline{\text{SM1}}$ & $\overline{\text{SM0}}$ & SMRST & SMJMP ; state 0
# $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM0 & SMRST & SMJMP ; state 1,2
# SM3 & SM2 & SM1 & $\overline{\text{SM0}}$ & SMRST & SMJMP ; state 11
# SM3 & $\overline{\text{SM2}}$ & SMRST & SMJMP ; state 12 to 15
# $\overline{\text{SMJMP}}$; jump to state 12

$\overline{\text{SM1}}$:= $\overline{\text{SMRST}}$; state reset
# $\overline{\text{SM3}}$ & SM2 & SM1 & SM0 & SMRST & SMJMP ; state 5
# $\overline{\text{SM3}}$ & SM2 & $\overline{\text{SM1}}$ & SM0 & SMRST & SMJMP ; state 6
# $\overline{\text{SM1}}$ & $\overline{\text{SM0}}$ & SMRST & SMJMP ; state 0, 7, 8, 15
# $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM0 & SMRST & SMJMP ; state 13, 14

$\overline{\text{SM0}}$:= $\overline{\text{SMRST}}$; state reset
# $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM1 & SMRST & SMJMP ; state 2, 3
# $\overline{\text{SM3}}$ & SM2 & $\overline{\text{SM1}}$ & SMRST & SMJMP ; state 6, 7
# SM3 & SM2 & SM1 & SMRST & SMJMP ; state 10, 11
# SM3 & $\overline{\text{SM2}}$ & $\overline{\text{SM1}}$ & SMRST & SMJMP ; state 14, 15
# $\overline{\text{SMJMP}}$; jump to state 12

The $\overline{\text{STERM}}$ signals the termination of a transfer to or from the processor based on the state machine state. The $\overline{\text{STERM}}$ is also connected to $\overline{\text{CBACK}}$. This means that a burst request by the MC68EC030 is acknowledged by the DRAM. If other 32-bit peripherals are not cached, then $\overline{\text{CBACK}}$ can be connected to $\overline{\text{RAS}}$. The disadvantage to this is the increased capacitance load that $\overline{\text{RAS}}$ must drive. To convert this design to a non-bursting DRAM interface, pull the $\overline{\text{CBREQ}}$ inputs into the PALs high and do not connect $\overline{\text{STERM}}$ to $\overline{\text{CBACK}}$. If the access was not a burst request, the MC68EC030 ignores the $\overline{\text{CBACK}}$. The setup and hold times of the MC68EC030 on $\overline{\text{STERM}}$ requires a 7 ns PAL. The $\overline{\text{STERM}}$ has a 2 ns set up and 6 ns hold requirement for each rising edge. The control logic asserts $\overline{\text{STERM}}$ when the state machine count is correct and the 40 MHz clock is low. The control logic continues to assert $\overline{\text{STERM}}$ while the clock is high. This means the $\overline{\text{STERM}}$ is asserted and negated off the falling edge of the clock.

$\overline{\text{STERM}}$ = $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{CLK}}$ & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM1 & SM0 ;last half of state 2
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{CLK}}$ & $\overline{\text{SM3}}$ & SM2 & SM1 & $\overline{\text{SM0}}$; last half of state 4
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{CLK}}$ & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & $\overline{\text{SM1}}$ & SM0 ; last half of state 6
# $\overline{\text{AS}}$ & $\overline{\text{A31}}$ & A30 & $\overline{\text{CLK}}$ & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & $\overline{\text{SM1}}$ & SM0 ; last half of state 8
# $\overline{\text{STERM}}$ & CLK ; keep first half of clock

ADDRESS MULTIPLEXING

The control logic handles the address multiplexing in two parts, row and column address multiplexing and burst address multiplexing. The DRAMs use multiplex address bits MA0 and MA1 for the bursting address. These pass through a PAL and multiplex A4 and A5 for the row address with A2 and A3 for the column address. The control logic increments MA0 and MA1 from A2 and A3 modulo 4 (00,01,10,11,00,...) for the four long words of the burst. The DRAM holds the data valid for 5 ns after the column address change for the burst. This allows the MC68EC030 data hold time to be easily met. Figure 7 shows the address multiplexing logic.

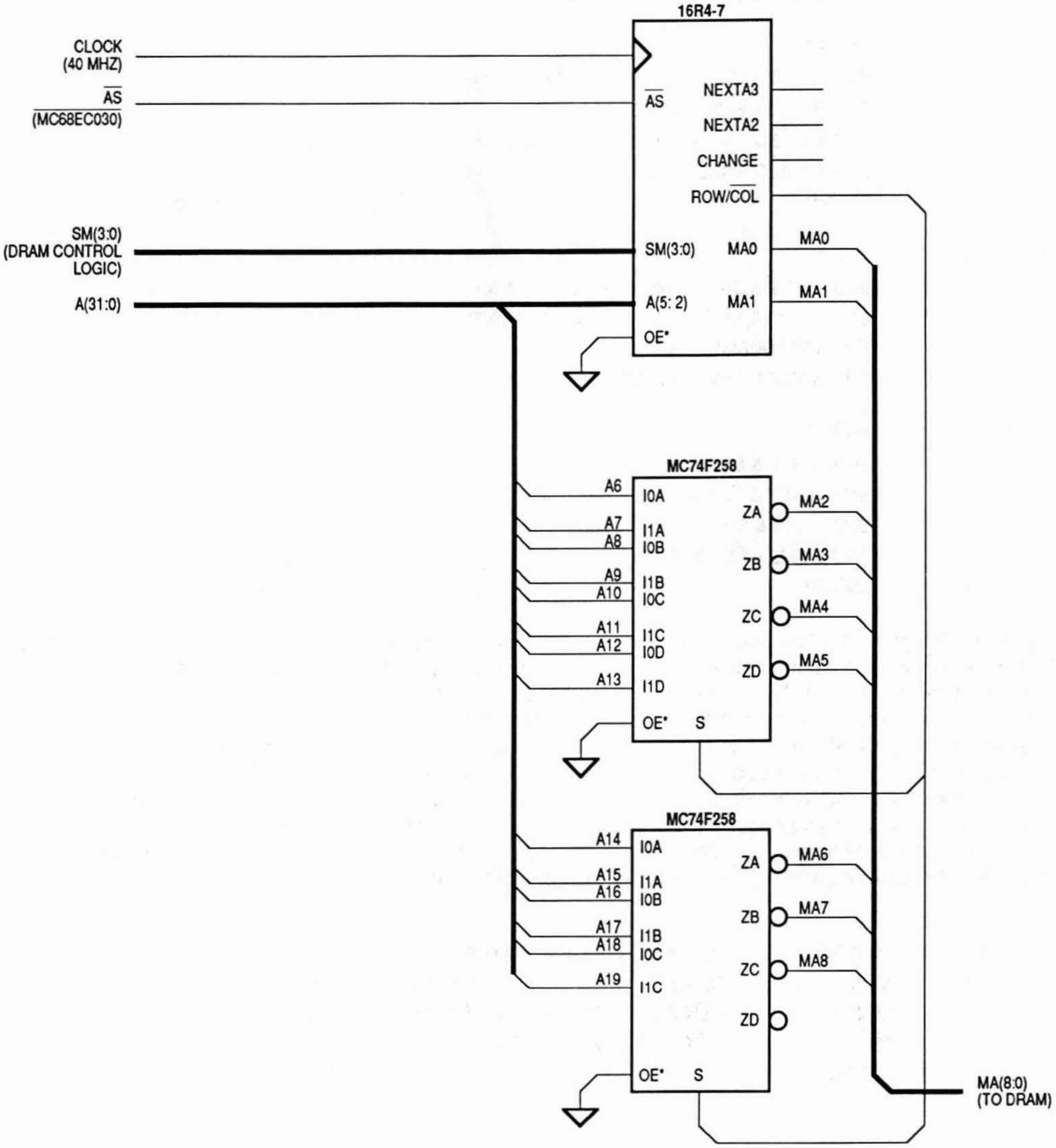

16R4-7
CLOCK (40 MHZ)
$\overline{AS}$ ($\overline{MC68EC030}$)
$\overline{AS}$
NEXTA3
NEXTA2
CHANGE
ROW/$\overline{COL}$
SM(3:0) (DRAM CONTROL LOGIC)
SM(3:0)
MA0
MA0
A(31:0)
A(5: 2)
MA1
MA1
OE*
MC74F258
A6
I0A
ZA
MA2
A7
I1A
A8
I0B
ZB
MA3
A9
I1B
A10
I0C
ZC
MA4
A11
I1C
A12
I0D
ZD
MA5
A13
I1D
OE*
S
MC74F258
A14
I0A
ZA
MA6
A15
I1A
A16
I0B
ZB
MA7
A17
I1B
A18
I0C
ZC
MA8
A19
I1C
ZD
OE*
S
MA(8:0) (TO DRAM)

Figure 7. Address Multiplexing Logic

The MA0 and MA1 equations have three parts. A combinatorial equation that drives the DRAM, a registered equation that selects the next address, and a registered equation that says when to change the address.

MA0 = ROW/COL & A4 ; row address
# A2 & $\overline{\text{CLK}}$ & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & $\overline{\text{SM1}}$ & SM0 ; state 1 col. addr.
# $\overline{\text{ROW/COL}}$ & MA0 & CLK ; column address hold
# $\overline{\text{ROW/COL}}$ & NXTA0 & $\overline{\text{CLK}}$; column address change

MA1 = ROW/COL & A5 ; row address
# A3 & $\overline{\text{CLK}}$ & $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & $\overline{\text{SM1}}$ & SM0 ; state 1 col. addr.
# $\overline{\text{ROW/COL}}$ & MA1 & CLK ; column address hold
# $\overline{\text{ROW/COL}}$ & NXTA1 & $\overline{\text{CLK}}$; column address hold

NXTA0 := CHANGE & $\overline{\text{MA0}}$; next lw col. addr.
# $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & $\overline{\text{SM1}}$ & A2 ; 1st col. addr.,state 0, 1
# $\overline{\text{CHANGE}}$ & NXTA0 ; hold column address

NXTA1 := CHANGE & MA0 & $\overline{\text{MA1}}$; next lw col. addr.
# CHANGE & $\overline{\text{MA0}}$ & MA1 ; next lw col. addr.
# $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & $\overline{\text{SM1}}$ & A3 ; 1st col. addr.,state 0, 1
# $\overline{\text{CHANGE}}$ & NXTA1 ; hold column address

CHANGE := $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & $\overline{\text{SM1}}$ & SM0 ; last half of state 1
# $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & SM1 & $\overline{\text{SM0}}$; last half of state 3
# $\overline{\text{SM3}}$ & SM2 & SM1 & SM0 ; last half of state 5
# $\overline{\text{SM3}}$ & SM2 & $\overline{\text{SM1}}$ & $\overline{\text{SM0}}$; last half of state 7

The rest of the DRAM address lines are passed through MC74F258 multiplexers to switch between the row and column addresses. The row address must be valid concurrently or before the $\overline{\text{RAS}}$ generation and held for 10 ns. The column address must be valid concurrently or before the $\overline{\text{CS}}$ generation. There is a 5 ns data hold from the changing of the column address. The $\overline{\text{ROW/COL}}$ signals the change from row to column address to the multiplexers.

$\overline{\text{ROW/COL}}$ = $\overline{\text{SM3}}$ & $\overline{\text{SM2}}$ & $\overline{\text{SM1}}$ & SM0 & $\overline{\text{AS}}$; assert for col. addr. state 1
# $\overline{\text{ROW/COL}}$ & $\overline{\text{AS}}$; hold col. addr.

ONE MEGABYTE OF MEMORY

This is by far the easiest part of the design. It is eight MCM514258A 80 ns static column 256K x 4 DRAMs. The $\overline{\text{RAS}}$, $\overline{\text{CS}}$, and write enable signals are driven by the memory control logic. The address multiplexing logic drives the addresses. The output enable ($\overline{\text{G}}$) is connected to the Data Strobe ($\overline{\text{DS}}$) of the MC68EC030 to prevent bus contention on a read access followed immediately by a write access. The data bus must three-state within 25 ns of $\overline{\text{DS}}$ negation on a read access. The data must remain valid on a read for at least 0 ns after $\overline{\text{DS}}$ negating. The MCM514258A-80 three-states its bus 0 to 20 ns after $\overline{\text{G}}$ going high. On a write, all byte lanes will be driven by the MC68EC030, but only certain byte lanes will have valid data. The valid bytes are selected by the $\overline{\text{CS}}$ that decode the address and size pins. Figure 8 shows the DRAM.

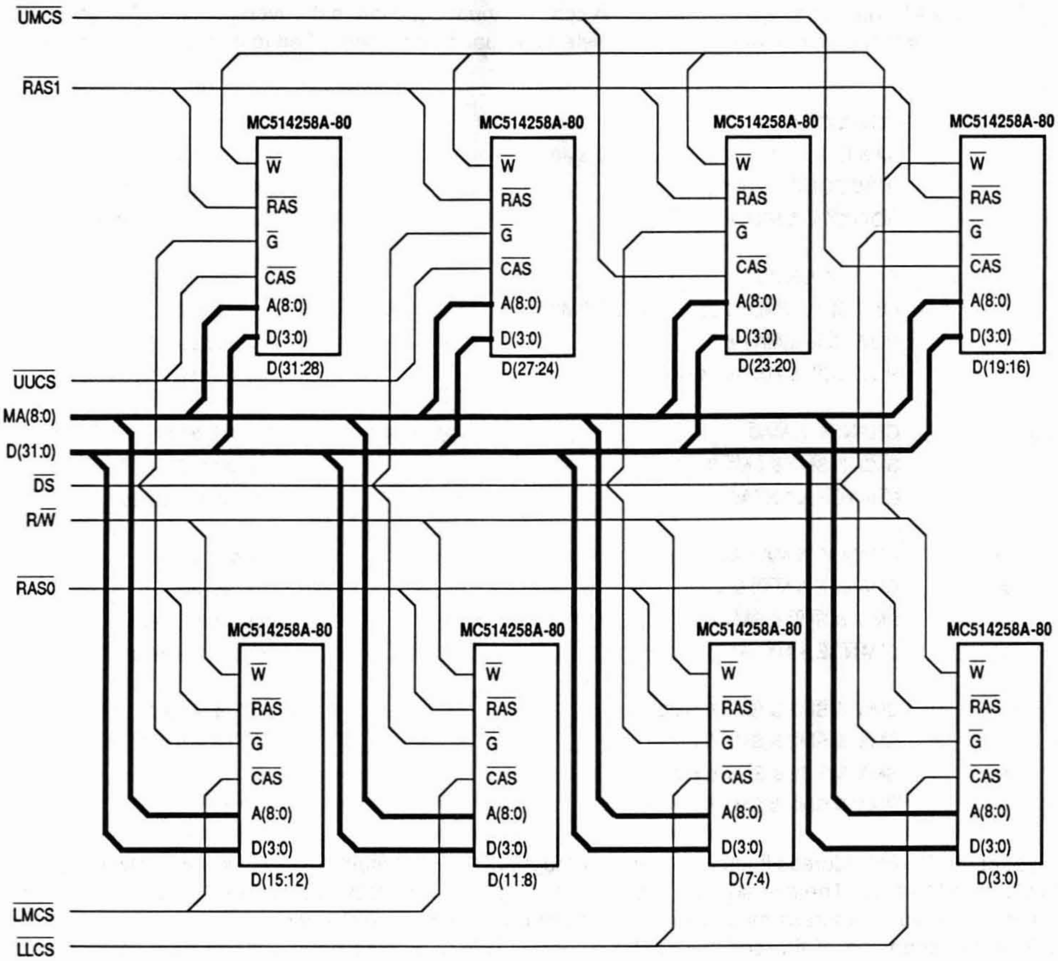

UMCS
RAS1
MC514258A-80
W
RAS
G
CAS
A(8:0)
D(3:0)
D(31:28)
MC514258A-80
D(27:24)
MC514258A-80
D(23:20)
MC514258A-80
D(19:16)
UUCS
MA(8:0)
D(31:0)
DS
R/W
RAS0
MC514258A-80
D(15:12)
MC514258A-80
D(11:8)
MC514258A-80
D(7:4)
MC514258A-80
D(3:0)
LMCS
LLCS

Figure 8. DRAM Control Logic

A larger memory is obtained by using eight 1M x 4 DRAMs (4 megabytes), thirty-two 1M x 1 DRAMs (4 megabytes) or thirty-two 4M x 1 DRAMs (16 megabytes). $\overline{\text{AS}}$ and $\overline{\text{DS}}$ signals are both used to minimize loading on either signal when using thirty-two DRAMs. Alternatively, the ROW/$\overline{\text{COL}}$ signal is attached to Bus Grant ACKnowledge ($\overline{\text{BGACK}}$) of the MC68EC030 to provide a guaranteed bus inactive cycle between each DRAM cycle. If ROW/$\overline{\text{COL}}$ is connected to $\overline{\text{BGACK}}$, then the output enables can be grounded and the DRAM will three-state when $\overline{\text{CS}}$ negates.

REFRESH CONTROL LOGIC

The MCM514258A requires all 512 rows to be refreshed every 8 ms. This corresponds to one row every 15.625 μs. The refresh control logic signals every 12.8 μs that a refresh cycle is needed. The slightly higher refresh rate of the control logic provides margin to ensure the data is not lost and minimizes the amount of refresh logic required. In order for the refresh to work correctly, there should not be any access longer than 55 clocks. Since the longest read-modify-write for DRAM access would be 13 clocks, the access limit is dependent on other devices. The reason for the limit is the bus request, when signaling a required refresh, is asserted for up to 64 clocks. With bus arbitration, the refresh operation requires 9 clocks. The refresh, with its associated bus mastership, must occur within the remaining 55 clocks. A refresh rate of 12.8 μs means the

DRAMs are not available to the MC68EC030 about 1.5% of the time. Since the MC68EC030 is not halted during this time and the internal caches are still available to the integer unit, this corresponds to less than 1.5% reduction in performance.

The refresh control logic consists of a MC74LS393 dual four bit counter. The first counter is clocked at 20 MHz, and in turn clocks the second counter. The four outputs of the second counter are NANDed through half of a MC74LS20 dual four input NAND gate to generate the Bus Request ($\overline{\text{BR}}$). The MC68EC030 responds with a Bus Grant ($\overline{\text{BG}}$). The state machine and DRAM control PALs use the $\overline{\text{BG}}$ signal to indicate that a refresh cycle should occur. At the end of the refresh cycle, the END_ReFReSH ($\overline{\text{END\_RFRSH}}$) clears the MC74LS393 counter to begin the count to the next refresh. Figure 9 shows the refresh control logic.

$\overline{\text{END\_RFRSH}}$ = $\overline{\text{BG}}$ & AS & $\overline{\text{SM3}}$ & SM2 & SM1 & $\overline{\text{SM0}}$; end refresh state 4
# $\overline{\text{BG}}$ & AS & $\overline{\text{SM3}}$ & SM2 & SM1 & SM0 ; end refresh state 5
# $\overline{\text{BG}}$ & AS & SM3 & $\overline{\text{SM2}}$ & SM1 & $\overline{\text{SM0}}$; end refresh state 12

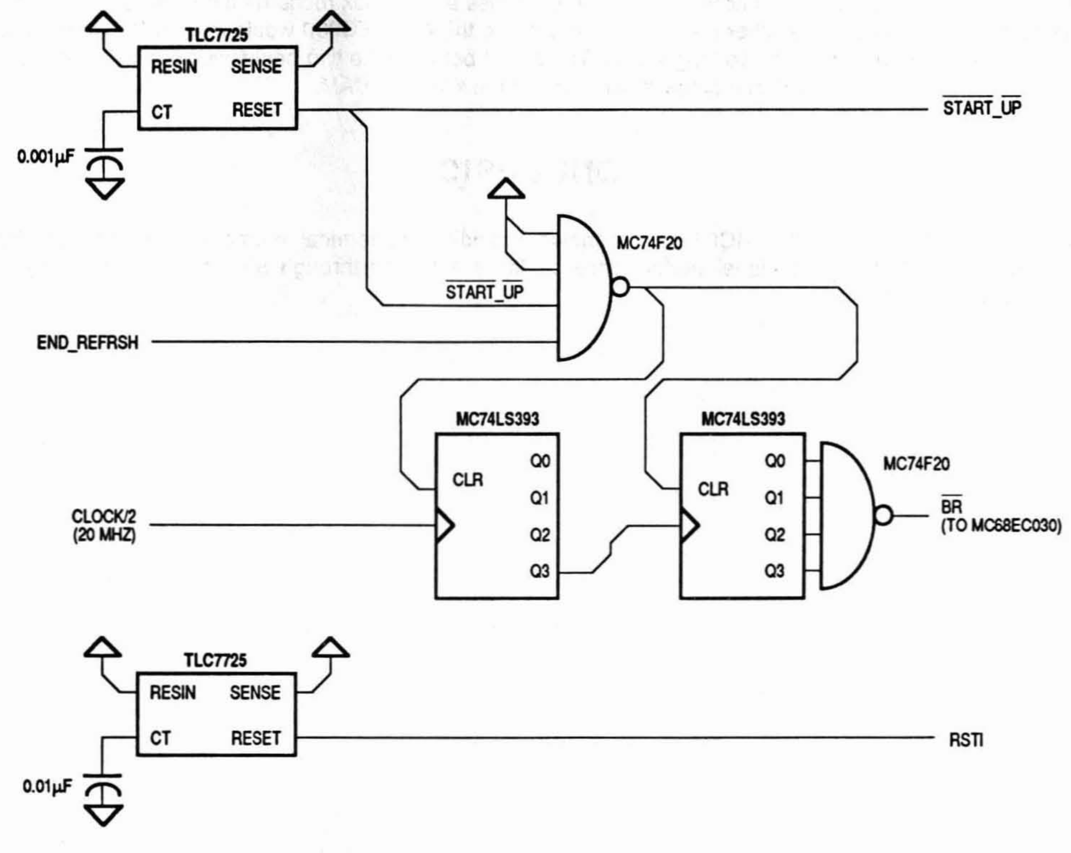

TLC7725
RESIN
SENSE
CT
RESET
0.001µF
$\overline{\text{START\_UP}}$
MC74F20
$\overline{\text{START\_UP}}$
END_REFRSH
MC74LS393
CLR
Q0
Q1
Q2
Q3
CLOCK/2
(20 MHZ)
MC74LS393
CLR
Q0
Q1
Q2
Q3
MC74F20
$\overline{\text{BR}}$
(TO MC68EC030)
TLC7725
RESIN
SENSE
CT
RESET
0.01µF
RSTI

Figure 9. Refresh Control Logic

The DRAM requires eight active cycles to establish the proper bias voltage, 200 μs after power-up. Two power-up reset signals provide this DRAM initialization. The first one negates 200 μs after power-up and the second one, to the processor, negates 350 μs after power-up. This ensures that the normal DRAM refresh logic provides at least the 8 active cycles required and guarantees the MC68EC030 40 MHz power-up reset timing requirement.

PERFORMANCE

The DRAM design shown here would provide approximately 2/3 to 3/4 of the performance of a no-wait-state-SRAM design at a significantly lower price. The DRAM design has a 5 clock initial access, 2 clock burst access and 2 clock recovery time. The recovery time affects the MC68EC030 only on back to back transfers (i.e., access followed immediately by another access, without any intervening bus idle clock periods). The MC68EC030 is not very likely to make back to back read accesses after a burst because of the on-board caches. Faster DRAMs would not increase the performance directly, just provide more setup margin. This increased margin could be used by multiplexing two banks of DRAM. This would double the amount of memory, provide 5 clock initial access, 1 clock burst access and 2 clock recharge time. One bank would be designated as even and the other odd. While the burst to the MC68EC030 would remain four long words, each bank would only provide two long words. The select between the two banks would correspond to the lower order column address (MA0) of the multiplexed address to the DRAM.

CONCLUSION

The DRAM interface to the MC68EC030 shown provides economical memory with relatively high performance. While slightly higher performance could be achieved through SRAM, the cost per byte is significantly higher.

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN1202

Battery Backup of Self-Refreshing Dynamic Random Access Memory

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INTRODUCTION

In today's information-dependent society, the need for maintaining the integrity of data and program status during a power outage is becoming increasingly important. Even though data files may be stored frequently during a session, in the event of a power failure, any changes since the last save would be lost, and the program would have to initialize and reload the required data. In applications where data loss would be costly in terms of dollars and time spent re-entering data, the use of battery backup circuits in conjunction with robust software can ensure that a power failure would be at most an annoying delay, requiring no user intervention upon the restoration of power.

SELF-REFRESHING DYNAMIC RANDOM ACCESS MEMORY

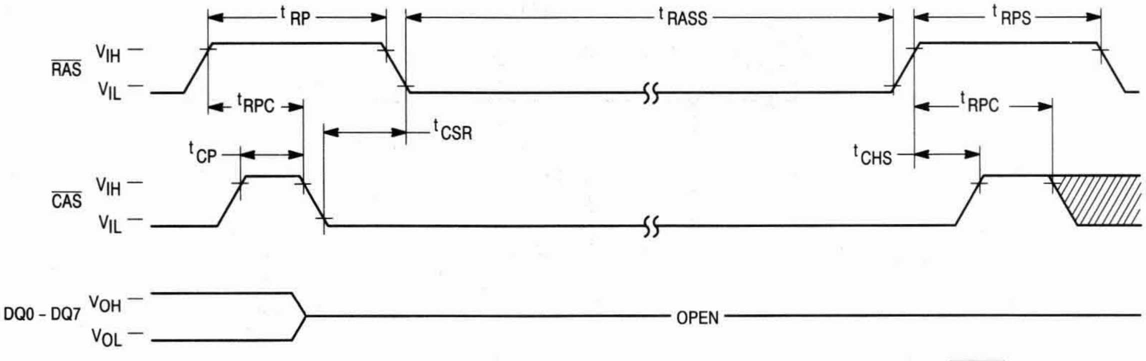
In the past, the best protection of volatile random access memory (RAM) data against a power loss was provided through the use of static RAMs (SRAMs) in the memory array because of the ease of interfacing with the rest of the system. SRAMs require none of the complex cycle and power consuming refresh circuitry associated with dynamic RAMs (DRAMs), because of their direct addressing and static cell. This has now changed with the introduction of Motorola's newest very low power 512K x 8 DRAM, the MCM5V4800A. Use of self-refreshing DRAMs allows battery backup of an increased memory size at a competitive price.

In addition to the usual methods of DRAM refresh (any read or write cycle, a $\overline{RAS}$-only refresh, a $\overline{CAS}$ before $\overline{RAS}$ refresh, or a hidden refresh), the MCM5V4800A also incorporates a **self-refresh** operation, previously found only on pseudo-static RAMs (PSRAMs). This self-refresh feature removes the need to have the DRAM control circuitry on the battery backup node, and is expected to be a standard feature on future generations of DRAMs.

The self-refresh operation is entered just as a normal $\overline{CAS}$ before $\overline{RAS}$ refresh, but $\overline{CAS}$ and $\overline{RAS}$ are held low for a period greater than t_{RASS} min (>100 µs), as shown in Figure 1. After this time, the DRAMs internal timer starts, and a new row is refreshed approximately every 130 µs. When the refresh pulse is generated by the internal timer, the I_{CC} current may peak to 120 mA, but the current I_{CCS} during the self-refresh is guaranteed to be a maximum of 200 µA, as shown in Figure 2.

The MCM5V4800A CMOS processing makes it particularly well suited for use in battery backup systems because of the inherent advantages of CMOS technology: superior noise immunity, faster switching speeds, low standby power dissipation, and a wide operating range.

For battery backup applications, chief among these advantages is the low standby power dissipation. Due to the series connection of P and N channel devices in CMOS designs, current is only drawn during switching. Thus, when the DRAM is in the self-refresh mode, the only current drawn is due to surface, junction, and channel leakage and the operation of the internal refresh timer.



NOTE: Din, $\overline{W}$, $\overline{G}$, A0 – A8, A9R = "H" or "L"

▨ "H" or "L"

Figure 1. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle for the MCM5V4800A

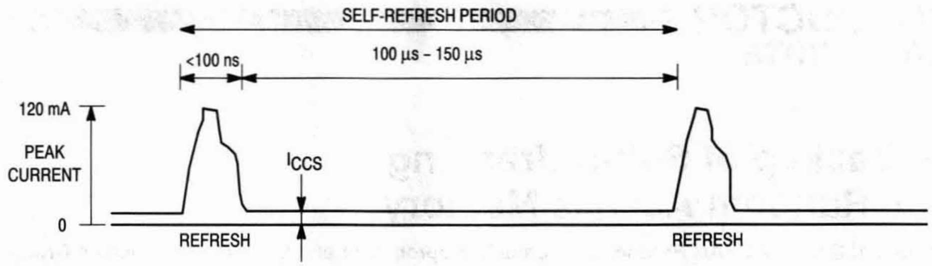


Figure 2. Power Supply Current of the MCM5V4800A During Self-Refresh

Pull-down resistors should be placed on the $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ pins to ensure that the DRAM stays in the self-refresh mode during the battery backup period. All other pins (addresses, data inputs/outputs, output enable, and write enable) should use pull-ups or pull-downs so that they do not float, creating undesirable current paths that would shorten battery life and possibly destroy data. (The use of pull-up and pull-down resistors to terminate each transmission line in the memory's bus is a wise practice with many inherent advantages. This topic is discussed in more detail in Motorola Application Notes AN971 and AN973. Although these notes specifically address Fast Static RAM applications, the principals generally can be applied to all volatile memories.)

BATTERY BACK-UP SYSTEM REQUIREMENTS

It is desirable after the occurrence of a power failure to be able to recover after power is restored and resume operation as if only a delay had occurred. This process is called fault recovery. Figure 3 shows the dc power bus for a system utilizing a low power processor, such as Motorola's MC68300 family of processors.

Note that besides the memory array, the processor and power failure detection circuit are also on the battery backup node. The MC68300 family is capable of low power standby necessary for battery backup operation. Having a low power processor greatly simplifies the circuitry and software required for fault recovery, because the processor itself can now store internal registers and keep track of the power state, without the need of external control logic comprising a finite state machine.

BATTERY BACKUP CIRCUIT

The battery backup circuit is one of the key components of the system. Its function is to supply power to the memory array, processor, and power failure detection circuit during a power failure. This is usually accomplished through the use of the trickle charge circuit illustrated in Figure 3, although numerous variations on this circuit exist. System interconnects are not shown in order to clarify the power connections.

In this circuit, diode D1 isolates the battery E1 from all but the system's RAM array, processor, and power failure detection circuit when the dc power supply has failed. The processor and power failure detection circuit must also have the battery backup in order to detect when the main power is restored and to keep track of whether the system is in the battery backup mode or normal operating mode. When the dc power supply is active, diode D2 and current limiting resistor R1 allow a small amount of current to be diverted into recharging the battery. If a non-rechargeable battery is used, resistor R1 can be eliminated. In order to prevent the battery from discharging during a scheduled power shutdown, a switch should be in series with the battery so that the backup circuit is disconnected when the system is deliberately powered off after all critical data has been written to some less volatile storage medium (e.g., floppy disk, hard disk, tape).

POWER FAILURE DETECTION CIRCUIT

The function of the power failure detection circuit is to monitor the ac power source. If the main power fails, this circuit generates an ACFAIL interrupt signal to the processor, which will store its internal status and put the memory in the

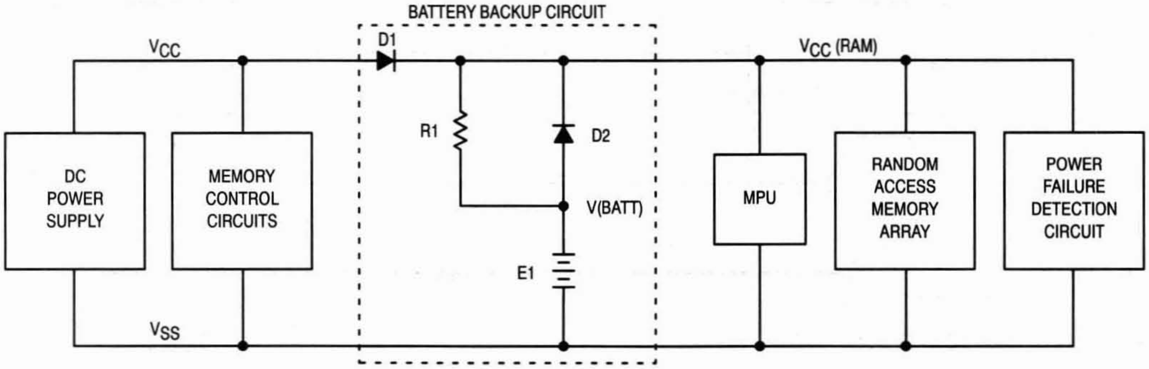


Figure 3. DC Power Bus for Complete System
Showing the Processor, Memory Array, and Power Failure Detection Circuit on the Battery Backup Node

self-refresh mode. Because of the necessary urgency in the event of a power failure, the signal issued to the processor in such an event is a non-maskable interrupt (NMI) of the highest priority.

Just as with the battery backup circuit, a wide variety of circuits exist for power failure detection. A simple power failure detection circuit is shown in Figure 4. It is recommended that the signal from the power supply into the power failure detection circuit be drawn from a separate winding of the transformer than that going to V_{CC}. This will avoid possible interference with the voltage regulation of the system.

In this circuit, the zener diode provides the reference level to the Schmitt trigger inverter, which fires if the ac power drops below a certain threshold. Resistor R1 and the zener reference voltage $V_{(REF)}$ should be chosen so that there is enough margin to the minimum system operating voltage for the power fail code to complete processing before the power loss propagates through the dc power supply, and V_{CC} falls below the system operating voltage. This margin must be greater than the execution time of the power fail code, which is on the order of 15 μs for the code illustrated in the following section. Concerns about this propagation delay can be dispelled through the use of an uninterruptable power supply (UPS), which can provide system power for a short time. An R-C network may also be included in parallel with the zener diode to prevent system shutdown if the ac power source goes down for only a few cycles. The trigger will then only fire if the power fails for more than a time constant. The hysteresis of the Schmitt trigger supplies additional margin.

Since the power failure detection circuit must continue to function during a power failure, its components need to have an operating range from the backup battery voltage to the normal system operating voltage and should also be of low power to minimize battery drain. Motorola's high performance Schmitt trigger inverter, the MC74HC9014, fulfills these requirements. If a high-to-low transition is required for the processor to begin the battery backup sequence, then a non-inverting Schmitt trigger should be used, such as the MC74HC9015.

SOFTWARE CONSIDERATIONS

The system's operating software must include code to accomplish the fault recovery process. From the standpoint of the processor, it is essential to save enough information to be able to return to the same point in program execution when power is restored. With the advent of components with low power standby modes, not only can essential data be saved, but also all variables and parameters may be recovered on return to normal operation.

Upon receipt of the ACFAIL signal from the power failure detection circuit, the processor will prepare the system for the battery backup operation. A low power processor from the MC68300 family will store its registers internally, send the memory array into the self-refresh mode, and make note that the system is now in the standby mode. Additional power can be saved by disabling circuitry that will be unused during the backup operation, such as the periodic interrupt timer, voltage controlled oscillator (VCO), and phase-locked loop (PLL).

Upon restoration of power, the ACFAIL signal is reset and the processor begins the fault recovery process. After the internal status of the processor is restored and the power to the external logic (especially the memory control circuits) reaches an operational level, the memory array can then return to the normal operating state. It is prudent to perform a refresh of the memory array as a part of the fault recovery process in order to ensure that no refresh parameters are violated.

As system complexity grows (for example when an operating system is being used), more complex measures must be taken to ensure proper fault recovery than if all software is written in assembly language. When the ACFAIL is detected, the operating system must shut down active processes and close files in an orderly fashion for full recovery after power is restored. Likewise, systems that implement some functions of operating systems like multitasking and scheduling, or access files on permanent storage devices, must close those processes or files to ensure proper recovery after the fault is repaired. The shutdown software must also keep a record of the status of the processes and files before the fault so that

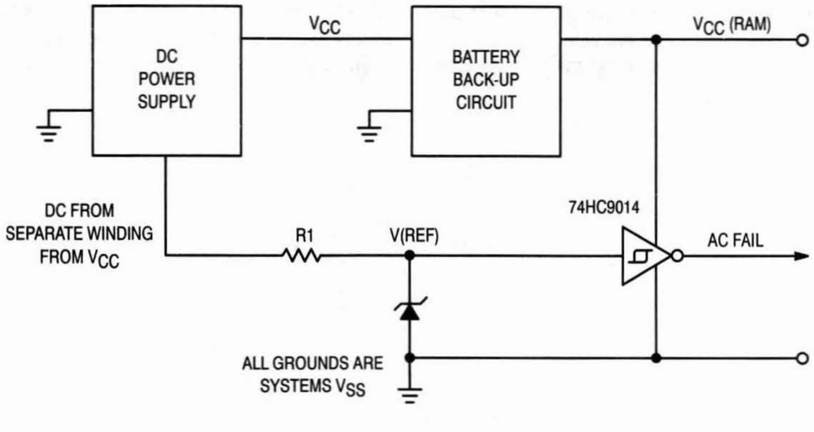


Figure 4. A Simple Power Failure Detection Circuit
(Note that the Schmitt trigger is also powered by the backup battery when the main power is down.)

they can be reopened on recovery. Consideration of the software or firmware necessary for such tasks is beyond the scope of this application note, but the user must take them into account nonetheless.

The code to perform a simple fault recovery for the MC68xxx family of processors follows. On reception of a power failure interrupt, the processor should execute, at a minimum, code similar to the following:

```
MOVEM.L        A0-A7,D0-D7,FAILREGS          Save regular registers and supervisor stack pointer.
                                             Note that the number of registers may vary
                                             depending on the type of processor being used.
MOVE.W         SR,FAILSR                     Save status register.
MOVE.L         USP,A0                        Get user stack pointer
MOVE.L         A0,FAILUSP                    and now save it.
RESET                                        Reset all system peripherals.
STOP                                         The CPU is now waiting to be reset
                                             for the duration of the power failure.
```

When the ac fault disappears, the fault recovery routine should contain code at the end of the routine similar to the following:

```
TAS            FAILSAVE                      Get value of state register and clear it through
                                             an indivisible read-modify-write cycle, while
                                             setting the Z bit of the CCR.
BEQ            JMP                           Skip if OK.
MOVE.L         FAILUSP,A0                    Load user stack pointer
MOVE.L         A0,USP                        and put in register.
MOVE.W         FAILSR,SR                     Reload status register.
MOVEM.L        FAILREGS,A0-A7,D0-D7          Reloading the registers causes the CPU to
RTE                                          reload the stack frame that was saved on the
                                             power fail interrupt; program execution
                                             continues as if no fault occurred.
JMP            CLR.W FAILSAVE                Clear semaphore in state register and continue
                                             power up code.
```

Note that the above code is generic for the MC68xxx family, and the number of internal status registers may vary. A low power processor from the MC68300 family can greatly simplify this code and shorten execution time, since it can store the status registers internally and initiate a low power stop.

SUMMARY

When critical data is being stored in a volatile RAM array, it is important to retain that data in the event of a power failure by having the RAM powered by a backup battery. It is also desirable after the occurrence of a power failure to be able to recover after power is restored through the process of fault recovery. From the standpoint of the processor, it is essential to save enough information to be able to return to the same point in program execution when power is restored. With the advent of self-refreshing DRAMs and processors with low power standby, not only can essential data be saved, but also all variables and parameters can be recovered, and the system returned to normal operation.

For a system to accomplish a fault recovery, additional circuitry is required beyond that of a system with no backup. A battery backup circuit switches between the main power and the battery; a power failure detection circuit senses a power loss and initiates the interrupt to the processor sending the system into the standby mode. The power failure detection circuit and processor must also be powered by the backup battery during a fault.

A wide variety of circuits exist for these additional requirements, and this application note has touched on only a few. As battery backup systems become more common, vendors are responding by including many of these requirements in their systems. For example, the VME bus specification defines an implementation of power failure detection. In the event that the power supply used in an application does not include the circuitry for battery backup operation, the required components can be obtained through Motorola.

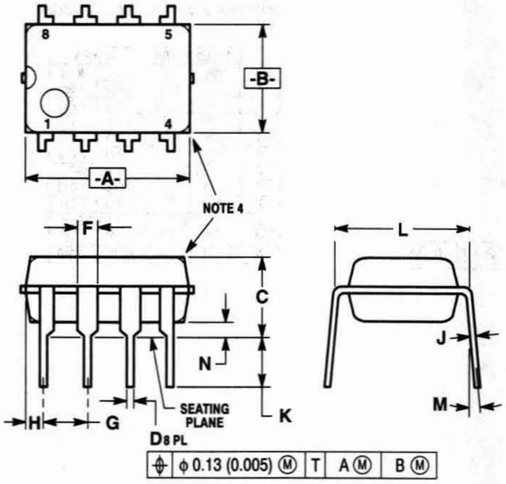
Mechanical Data

10

Package availability and ordering information are given on the individual data sheets.

8-LEAD PACKAGES

300 MIL PLASTIC
CASE 626-04

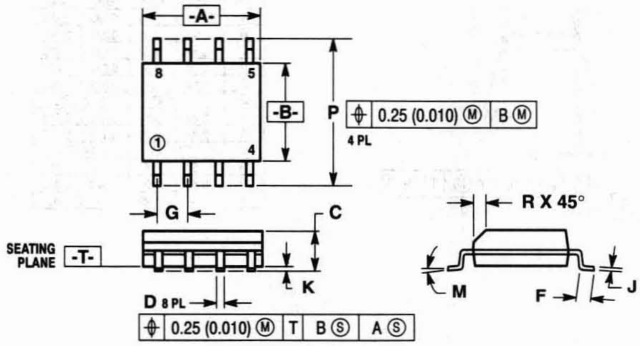


STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC - IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

NOTES:
1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.51	0.76	0.020	0.030

150 MIL SOG
CASE 751-03

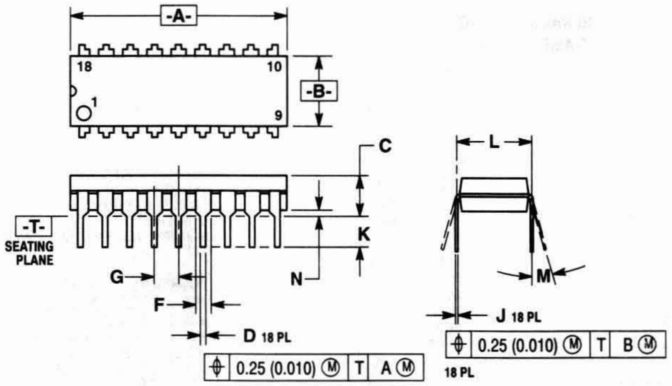


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIM: MILLIMETER.
3. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751-01 AND -02 OBSOLETE, NEW STANDARD 751-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

18-LEAD PACKAGES

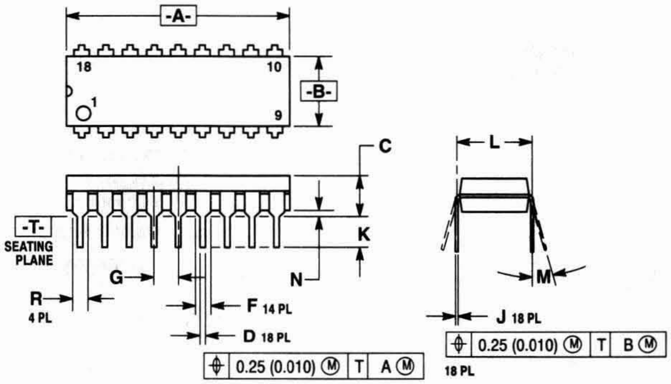
300 MIL PLASTIC
CASE 707A-01


-A-
18
10
1
9
-B-
C
L
-T-
SEATING PLANE
K
G
N
M
F
J 18 PL
D 18 PL
0.25 (0.010) Ⓜ T B Ⓜ
18 PL
0.25 (0.010) Ⓜ T A Ⓜ

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	21.85	22.35	0.860	0.880
B	7.12	7.49	0.280	0.295
C	3.56	4.57	0.140	0.180
D	0.36	0.55	0.014	0.022
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.30	0.008	0.012
K	2.93	3.42	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

300 MIL PLASTIC
CASE 707B-01

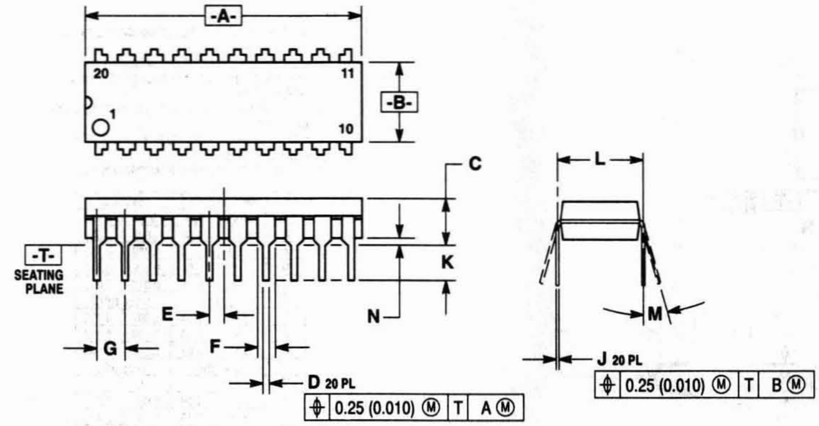

-A-
18
10
1
9
-B-
C
L
-T-
SEATING PLANE
K
G
N
M
R
4 PL
F 14 PL
J 18 PL
D 18 PL
0.25 (0.010) Ⓜ T B Ⓜ
18 PL
0.25 (0.010) Ⓜ T A Ⓜ

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	21.85	22.45	0.860	0.884
B	6.96	7.49	0.274	0.295
C	3.56	5.08	0.140	0.200
D	0.36	0.58	0.014	0.023
F	1.14	1.52	0.045	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.36	0.008	0.014
K	2.92	3.76	0.115	0.148
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.50	1.01	0.020	0.040
R	—	1.29	—	0.051

20-LEAD PACKAGES

300 MIL PLASTIC
CASE 738A-01

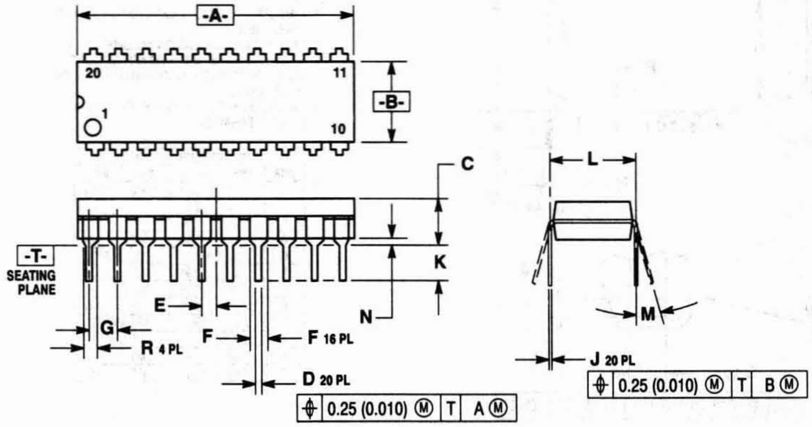

-A-
20
11
1
10
-B-
C
L
-T-
SEATING PLANE
K
E
N
M
G
F
J 20 PL
D 20 PL
0.25 (0.010) Ⓜ T B Ⓜ
0.25 (0.010) Ⓜ T A Ⓜ

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	24.39	24.89	0.960	0.980
B	7.12	7.49	0.280	0.295
C	3.69	4.44	0.145	0.175
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

300 MIL PLASTIC
CASE 738C-01


-A-
20
11
1
10
-B-
C
L
-T-
SEATING PLANE
K
E
N
M
G
R 4 PL
F
F 16 PL
J 20 PL
D 20 PL
0.25 (0.010) Ⓜ T B Ⓜ
0.25 (0.010) Ⓜ T A Ⓜ

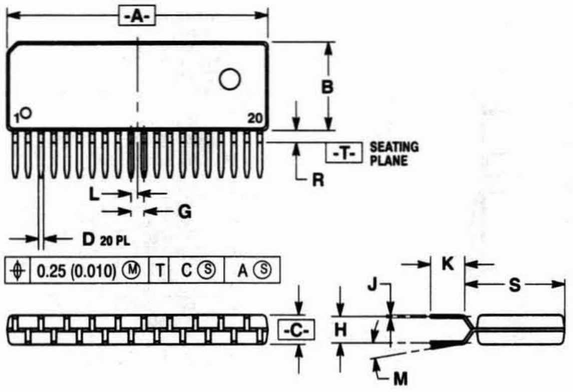
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	24.39	24.99	0.960	0.984
B	6.96	7.49	0.274	0.295
C	3.56	5.08	0.140	0.200
D	0.38	0.56	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.14	1.52	0.045	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.76	0.110	0.148
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.50	1.01	0.020	0.040
R	---	1.29	---	0.051

20-LEAD PACKAGES (Continued)

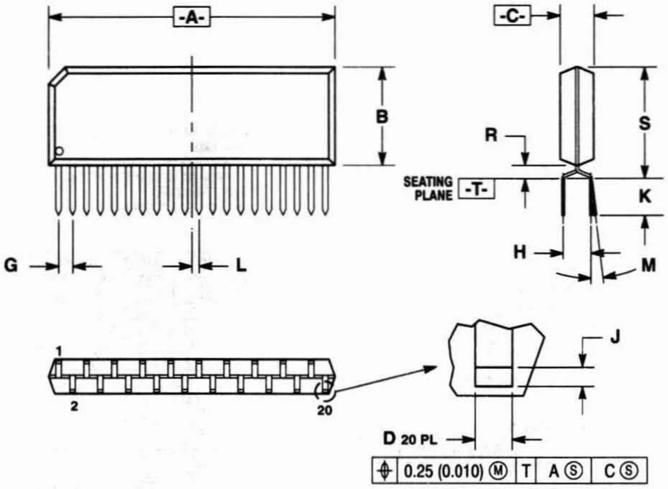
PLASTIC ZIP
CASE 836-02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "H" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS "A", "B", AND "S" DO NOT INCLUDE MOLD PROTRUSION.
5. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010).
6. 836-01 OBSOLETE, NEW STANDARD 836-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.53	25.90	1.005	1.020
B	8.59	8.89	0.338	0.350
C	2.75	2.94	0.108	0.116
D	0.45	0.55	0.018	0.022
G	1.27 BSC		0.050 BSC	
H	2.44	2.64	0.097	0.103
J	0.23	0.33	0.009	0.013
K	3.18	3.55	0.125	0.140
L	0.64 BSC		0.025 BSC	
M	0°	4°	0°	4°
R	0.89	1.39	0.035	0.055
S	9.66	10.16	0.380	0.400

PLASTIC ZIP
CASE 836A-01

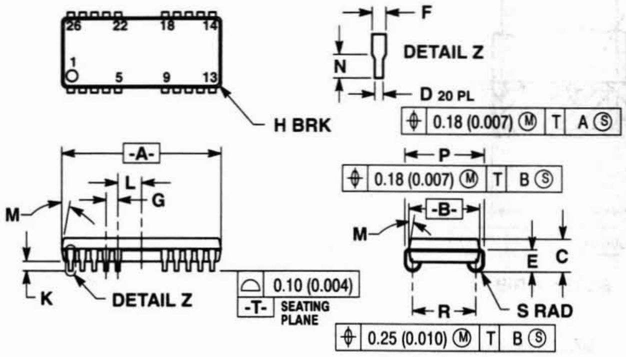


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A, B, AND S DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010).
4. DIMENSION H TO CENTER OF LEAD WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.53	26.11	1.006	1.027
B	8.31	8.89	.328	.350
C	2.75	2.94	.109	.115
D	0.42	0.62	.017	.024
G	1.27 BASIC		.050 BASIC	
H	2.14	2.94	.085	.115
J	0.20	0.35	.008	.092
K	2.80	3.75	.111	.147
L	0.635 BASIC		.025 BASIC	
M	0°	7°	0°	7°
R	0.53	—	.021	—
S	8.89	10.16	.350	.400

20/26-LEAD PACKAGES

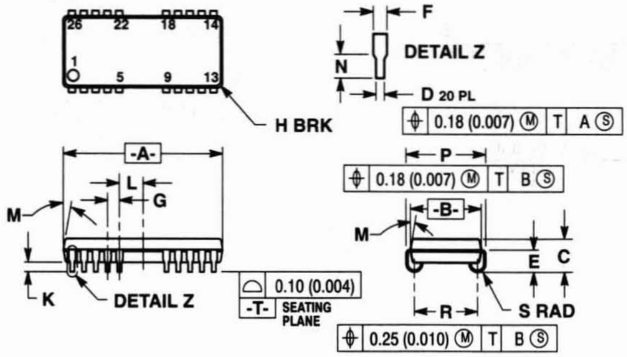
300 MIL SOJ
CASE 822-03


26
22
18
14
1
5
9
13
H BRK
-A-
L
G
M
K
DETAIL Z
F
DETAIL Z
N
D 20 PL
0.18 (0.007) Ⓜ T A Ⓢ
P
0.18 (0.007) Ⓜ T B Ⓢ
-B-
M
E
C
0.10 (0.004)
-T- SEATING PLANE
R
S RAD
0.25 (0.010) Ⓜ T B Ⓢ

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIM R TO BE DETERMINED AT DATUM -T-.
5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 6, 7, 8, 19, 20, & 21 ARE NOT USED.
6. 822-01 AND -02 OBSOLETE, NEW STANDARD 822-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.02	17.27	0.670	0.680
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	2.54 BSC		0.100 BSC	
M	0°	10°	0°	10°
N	0.89	1.14	0.035	0.045
P	8.39	8.63	0.330	0.340
R	6.61	6.98	0.260	0.275
S	0.77	1.01	0.030	0.040

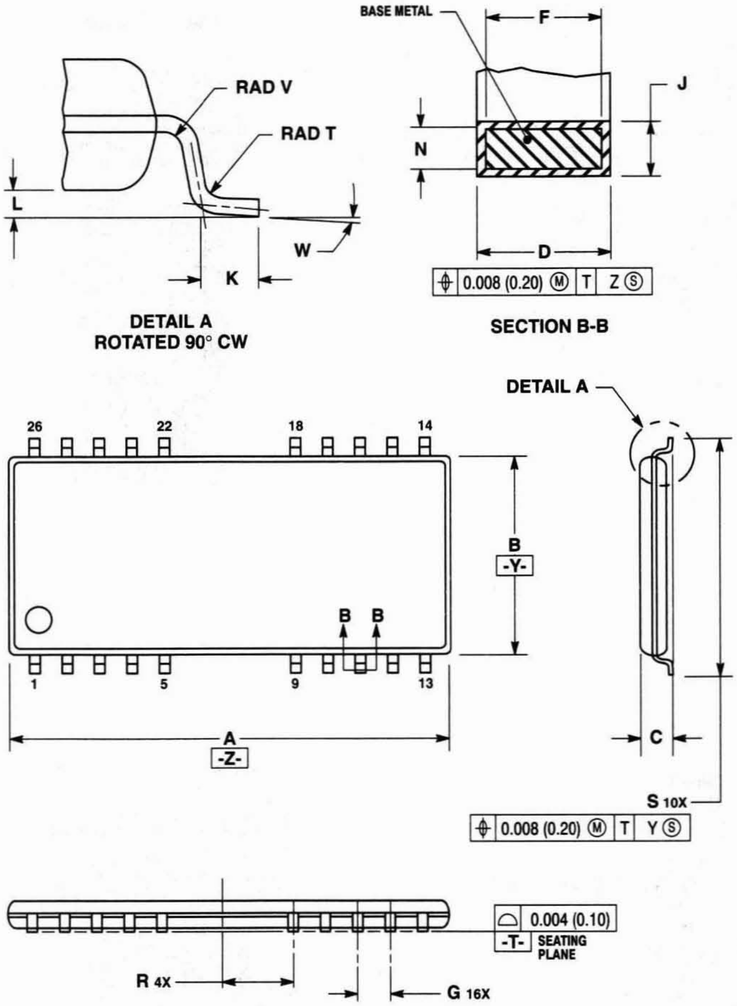
300 MIL SOJ
CASE 822B-01


26
22
18
14
1
5
9
13
H BRK
-A-
L
G
M
K
DETAIL Z
F
DETAIL Z
N
D 20 PL
0.18 (0.007) Ⓜ T A Ⓢ
P
0.18 (0.007) Ⓜ T B Ⓢ
-B-
M
E
C
0.10 (0.004)
-T- SEATING PLANE
R
S RAD
0.25 (0.010) Ⓜ T B Ⓢ

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIM R TO BE DETERMINED AT DATUM -T-.
5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 6, 7, 8, 19, 20, & 21 ARE NOT USED.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	16.79	17.27	0.661	0.680
B	7.50	7.74	0.295	0.305
C	3.25	3.76	0.128	0.148
D	0.38	0.53	0.015	0.021
E	2.16	2.61	0.085	0.103
F	0.66	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.63	1.14	0.025	0.045
L	2.54 BSC		0.100 BSC	
M	0°	20°	0°	20°
N	0.89	1.50	0.035	0.059
P	8.39	8.63	0.330	0.340
R	6.60	6.98	0.260	0.275
S	0.69	1.02	0.027	0.040

300 MIL TSOP
CASE 892-01


BASE METAL
F
J
N
D
0.008 (0.20) Ⓜ T Z Ⓢ
SECTION B-B
RAD V
RAD T
L
W
K
DETAIL A
ROTATED 90° CW
DETAIL A
26
22
18
14
1
5
9
13
B
-Y-
B B
A
-Z-
C
S 10X
0.008 (0.20) Ⓜ T Y Ⓢ
0.004 (0.10)
-T- SEATING PLANE
R 4X
G 16X

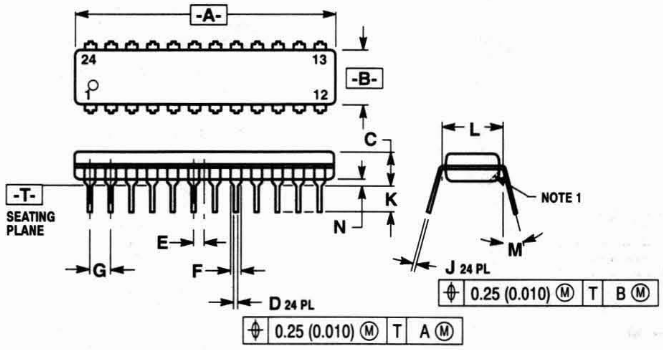
NOTES:

1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.006 (0.15) PER SIDE.
4. DIMENSION D DOES NOT INCLUDE DAM BAR PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.007 (0.18), TOTAL, IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.05	17.25	0.671	0.679
B	7.52	7.72	0.296	0.304
C	—	1.27	—	0.050
D	0.33	0.48	0.013	0.019
F	0.33	0.43	0.013	0.017
G	1.27 BSC		0.050 BSC	
J	0.12	0.20	0.005	0.008
K	0.41	0.58	0.016	0.023
L	0.02	0.18	0.001	0.007
N	0.11	0.16	0.004	0.006
R	2.54 BSC		0.100 BSC	
S	9.05	9.39	0.356	0.370
T	0.10 REF		0.004 REF	
V	0.10 REF		0.004 REF	
W	0°	5°	0°	5°

24-LEAD PACKAGE

300 MIL PLASTIC
CASE 724-03

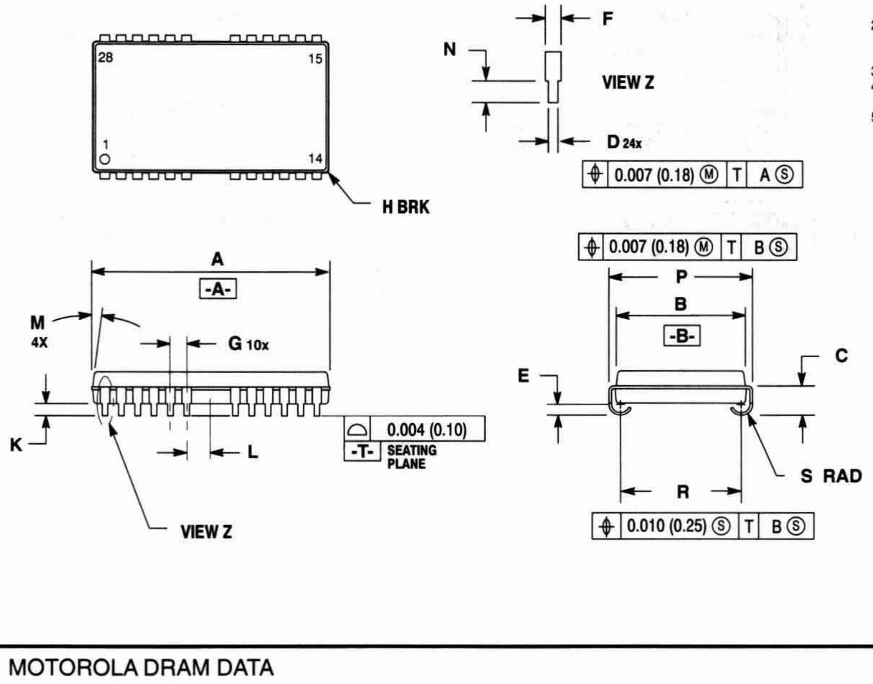

-A-
24
13
-B-
1
12
C
-T-
SEATING PLANE
K
N
E
G
F
D 24 PL
0.25 (0.010) Ⓜ T A Ⓜ
L
NOTE 1
M
J 24 PL
0.25 (0.010) Ⓜ T B Ⓜ

NOTES:
1. CHAMFERRED CONTOUR OPTIONAL.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

24/28-LEAD PACKAGE

400 MIL SOJ
CASE 810C-01

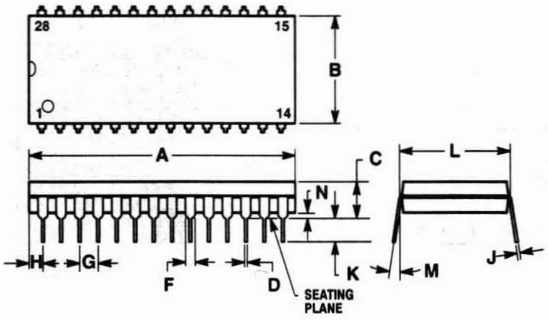

28
15
1
14
H BRK
F
N
VIEW Z
D 24x
0.007 (0.18) Ⓜ T A Ⓢ
0.007 (0.18) Ⓜ T B Ⓢ
A
-A-
M
4X
G 10x
K
L
0.004 (0.10)
-T- SEATING PLANE
VIEW Z
P
B
-B-
E
C
S RAD
R
0.010 (0.25) Ⓢ T B Ⓢ

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006 (0.15) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIMENSION A AND B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.
5. TO BE DETERMINED AT PLANE -T-

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.29	18.54	0.720	0.730
B	10.04	10.28	0.395	0.405
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.66	0.81	0.026	0.032
G	1.27 BASIC		0.050 BASIC	
H	---	0.50	---	0.020
K	0.89	1.14	0.035	0.045
L	1.905 BASIC		0.075 BASIC	
M	0°	5°	0°	5°
N	0.76	1.14	0.030	0.045
P	10.93	11.30	0.430	0.445
R	9.15	9.65	0.360	0.380
S	0.77	1.01	0.030	0.040

28-LEAD PACKAGES

600 MIL PLASTIC
CASE 710-02

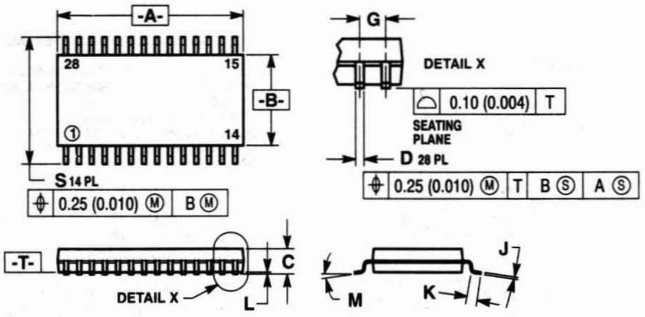


28
15
B
1
14
A
C
N
L
H
G
F
D
SEATING PLANE
K
M
J

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. 710-01 OBSOLETE, NEW STANDARD 710-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

300 MIL SOG
CASE 751H-02



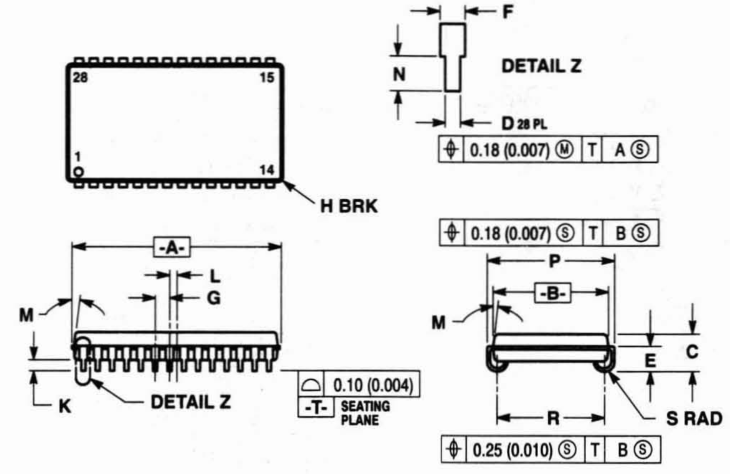
-A-
28
15
-B-
①
14
S 14 PL
0.25 (0.010) Ⓜ B Ⓜ
G
DETAIL X
0.10 (0.004) T
SEATING PLANE
D 28 PL
0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ
-T-
C
DETAIL X
L
M
K
J

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIM: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751H-01 OBSOLETE, NEW STANDARD 751H-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.70	18.50	0.697	0.728
B	8.23	8.90	0.324	0.350
C	2.04	2.50	0.080	0.098
D	0.35	0.50	0.014	0.020
G	1.27 BSC		0.050 BSC	
J	0.14	0.25	0.0060	0.0098
K	0.40	1.27	0.016	0.050
L	0.05	0.20	0.002	0.008
M	0°	8°	0°	8°
S	11.50	12.10	0.453	0.476

28-LEAD PACKAGES (Continued)

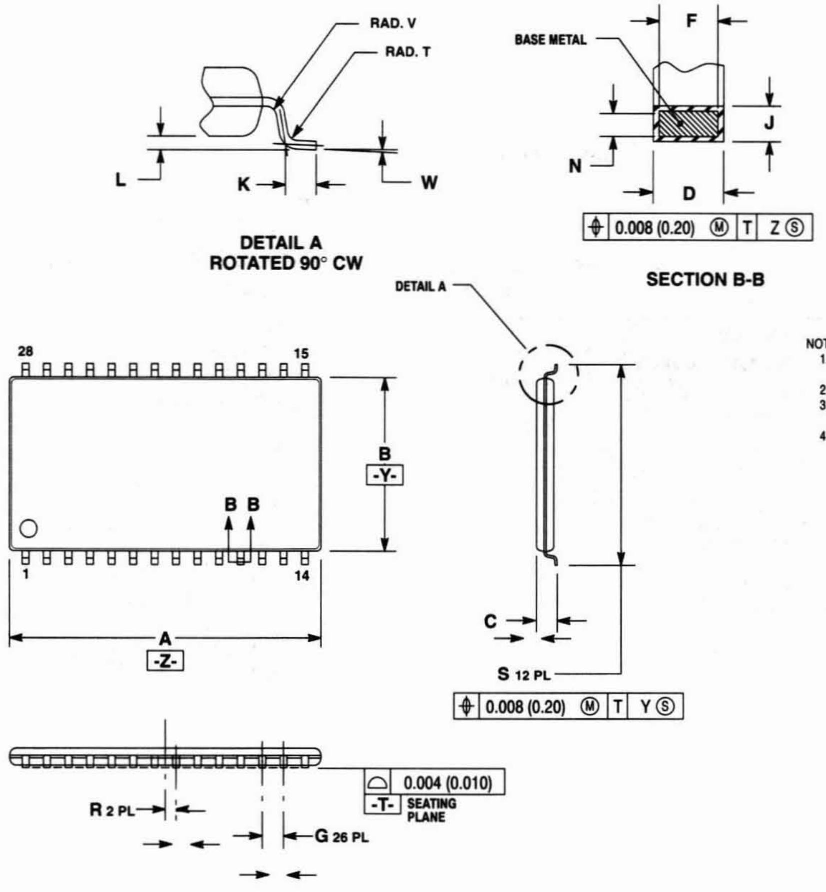
400 MIL SOJ
CASE 810-03


F
N
DETAIL Z
D 28 PL
⌖ 0.18 (0.007) Ⓜ T A Ⓢ
28
15
1
14
H BRK
⌖ 0.18 (0.007) Ⓢ T B Ⓢ
-A-
L
G
M
P
-B-
M
E
C
K
DETAIL Z
⌓ 0.10 (0.004)
-T- SEATING PLANE
R
S RAD
⌖ 0.25 (0.010) Ⓢ T B Ⓢ

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.
5. 810-01 AND -02 OBSOLETE, NEW STANDARD 810-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.29	18.54	0.720	0.730
B	10.04	10.28	0.395	0.405
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	5°	0°	5°
N	0.76	1.14	0.030	0.045
P	11.05	11.30	0.435	0.445
R	9.15	9.65	0.360	0.380
S	0.77	1.01	0.030	0.040

400 MIL TSOP
CASE 899-01

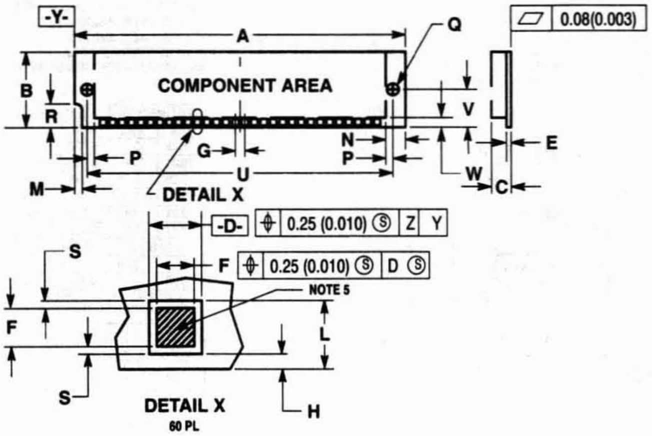

RAD. V
RAD. T
L
K
W
DETAIL A
ROTATED 90° CW
BASE METAL
F
J
N
D
⌖ 0.008 (0.20) Ⓜ T Z Ⓢ
SECTION B-B
DETAIL A
28
15
B
-Y-
B B
1
14
A
-Z-
C
S 12 PL
⌖ 0.008 (0.20) Ⓜ T Y Ⓢ
⌓ 0.004 (0.010)
-T- SEATING PLANE
R 2 PL
G 26 PL

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION IS .006 (0.15) PER SIDE.
4. DIMENSION D DOES NOT INCLUDE DAM BAR PROTRUSIONS. ALLOWABLE PROTRUSION IS .007 (0.18), TOTAL, IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.34	18.52	0.721	0.729
B	10.05	10.26	0.396	0.404
C	—	1.27	—	0.050
D	0.33	0.48	0.013	0.019
F	0.33	0.43	0.013	0.017
G	1.27 BASIC		0.050 BASIC	
J	0.12	0.20	0.005	0.008
K	0.41	0.58	0.016	0.023
L	0.02	0.18	0.001	0.007
N	0.11	0.16	0.004	0.006
R	0.635 BASIC		0.025 BASIC	
S	11.59	11.93	0.456	0.470
T	0.10 BASIC		0.004 REF	
V	0.10 BASIC		0.004 REF	
W	0°	5°	0°	5°

30-LEAD PACKAGES

CASE 839-01

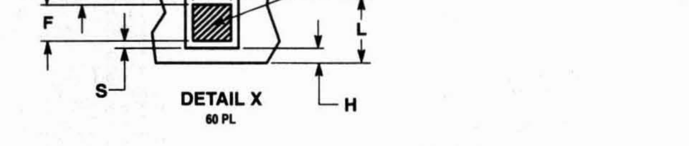

-Y-
A
Q
0.08(0.003)
B
R
COMPONENT AREA
V
E
N
P
G
P
U
W
C
M
DETAIL X
-D-
0.25 (0.010) Ⓢ Z Y
S
F
0.25 (0.010) Ⓢ D Ⓢ
NOTE 5
F
L
S
DETAIL X
60 PL
H

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TABS TO BE ELECTRICALLY CONNECTED BOTH SIDES OF CARD.
4. DIMENSION E INCLUDES PLATING AND/OR METALIZATION.
5. CONTACT ZONE MUST BE FREE OF HOLES.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	88.78	89.02	3.495	3.505
B	20.20	20.44	0.795	0.805
C	—	5.28	—	0.208
D	1.66	1.90	0.065	0.075
E	1.20	1.34	0.047	0.053
F	1.15	1.39	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	—	0.25	—	0.010
L	2.04	—	0.080	—
M	1.91	2.15	0.075	0.085
N	3.26	3.50	0.128	0.138
P	1.15	—	0.045	—
Q	3.13	3.22	0.123	0.127
R	6.23	6.47	0.245	0.255
S	0.13	0.38	0.005	0.015
U	82.02	82.27	3.229	3.239
V	10.04	10.28	0.395	0.405
W	2.54	—	0.100	—

CASE 839A-01


-Y-
Q
A
0.08 (0.003)
B
R
COMPONENT AREA
V
-Z-
E
N
P
G
P
U
W
C
M
DETAIL X
-D-
0.25 (0.010) Ⓢ Z Y
S
F
0.25 (0.010) Ⓢ D Ⓢ
NOTE 5
F
L
S
DETAIL X
60 PL
H

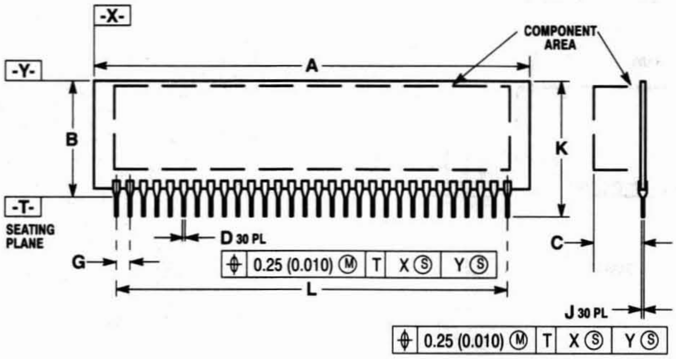
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TABS TO BE ELECTRICALLY CONNECTED BOTH SIDES OF CARD.
4. DIMENSION E INCLUDES PLATING AND/OR METALIZATION.
5. CONTACT ZONE MUST BE FREE OF HOLES.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	88.78	89.02	3.495	3.505
B	13.85	14.09	0.545	0.555
C	—	5.28	—	0.208
D	1.66	1.90	0.065	0.075
E	1.20	1.34	0.047	0.053
F	1.15	1.39	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	—	0.25	—	0.010
L	2.04	—	0.080	—
M	1.91	2.15	0.075	0.085
N	3.26	3.50	0.128	0.138
P	1.15	—	0.045	—
Q	3.13	3.22	0.123	0.127
R	6.23	6.47	0.245	0.255
S	0.13	0.38	0.005	0.015
U	82.02	82.27	3.229	3.239
V	10.04	10.28	0.395	0.405
W	2.54	—	0.100	—

30-LEAD PACKAGES (Continued)

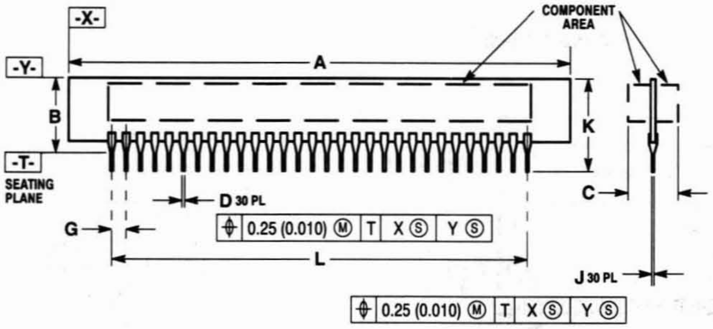
CASE 852-01


-X-
-Y-
A
COMPONENT AREA
B
K
-T-
SEATING PLANE
D 30 PL
G
C
L
J 30 PL
⊕ 0.25 (0.010) Ⓜ T X Ⓢ Y Ⓢ
⊕ 0.25 (0.010) Ⓜ T X Ⓢ Y Ⓢ

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	81.81	82.42	3.221	3.245
B	—	22.60	—	0.890
C	—	5.28	—	0.208
D	0.41	0.61	0.016	0.024
G	2.54 BSC		0.100 BSC	
J	0.10	0.40	0.004	0.016
K	—	25.60	—	1.008
L	73.66 BSC		2.900 BSC	

CASE 852A-02

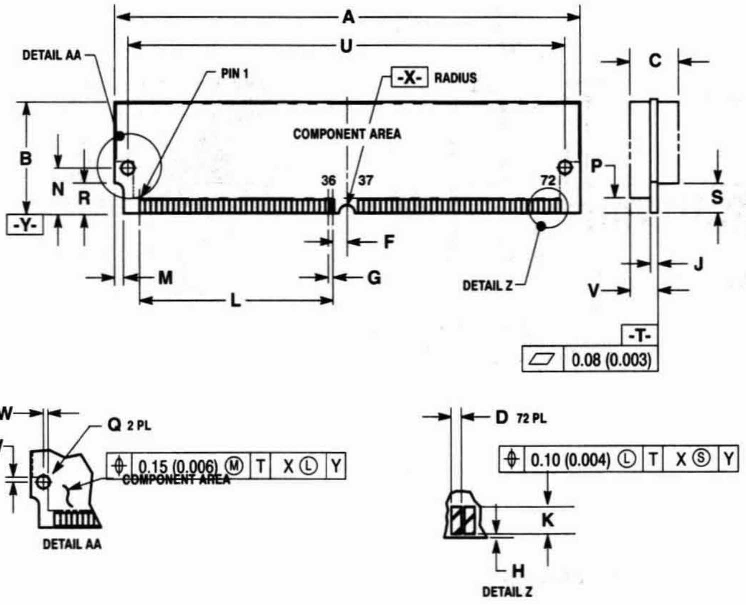

-X-
-Y-
A
COMPONENT AREA
B
K
-T-
SEATING PLANE
D 30 PL
G
C
L
J 30 PL
⊕ 0.25 (0.010) Ⓜ T X Ⓢ Y Ⓢ
⊕ 0.25 (0.010) Ⓜ T X Ⓢ Y Ⓢ

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 8520-01 OBSOLETE, NEW STANDARD 852A-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	88.39	89.41	3.480	3.520
B	—	13.21	—	0.520
C	—	8.89	—	0.350
D	0.41	0.61	0.016	0.024
G	2.54 BSC		0.100 BSC	
J	0.10	0.40	0.004	0.016
K	—	16.38	—	0.64
L	73.66 BSC		2.900 BSC	

72-LEAD PACKAGES

CASE 866-02

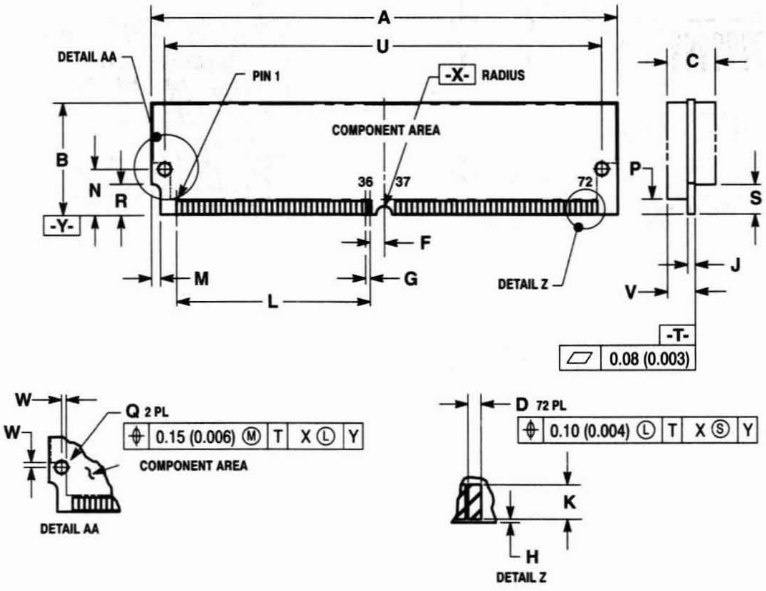


A
U
DETAIL AA
PIN 1
-X-
RADIUS
COMPONENT AREA
C
B
N
R
-Y-
36
37
72
P
S
F
M
G
L
DETAIL Z
J
V
-T-
0.08 (0.003)
W
Q 2 PL
0.15 (0.006) Ⓜ T X Ⓛ Y
COMPONENT AREA
DETAIL AA
D 72 PL
0.10 (0.004) Ⓛ T X Ⓢ Y
K
H
DETAIL Z

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.
4. 866-01 IS OBSOLETE, NEW STANDARD 866-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	107.82	108.08	4.245	4.255
B	25.27	25.53	0.995	1.005
C	—	9.14	—	0.360
D	1.02	1.07	0.040	0.042
F	3.18 BSC		0.125 BSC	
G	1.27 BSC		0.050 BSC	
H	—	0.25	—	0.010
J	1.19	1.37	0.047	0.054
K	0.25	—	0.100	—
L	44.45 REF		1.750 REF	
M	1.90	2.16	0.075	0.085
N	10.16 BSC		0.400 BSC	
P	3.18	—	0.125	—
Q	3.12	3.22	0.123	0.127
R	6.22	6.48	0.245	0.255
S	5.72	—	0.225	—
U	101.19 BSC		3.984 BSC	
V	—	5.28	—	0.208
W	1.12	—	0.044	—
X	1.52	1.63	0.060	0.064

CASE 866A-02



A
U
DETAIL AA
PIN 1
-X-
RADIUS
COMPONENT AREA
C
B
N
R
-Y-
36
37
72
P
S
F
M
G
L
DETAIL Z
J
V
-T-
0.08 (0.003)
W
Q 2 PL
0.15 (0.006) Ⓜ T X Ⓛ Y
COMPONENT AREA
DETAIL AA
D 72 PL
0.10 (0.004) Ⓛ T X Ⓢ Y
K
H
DETAIL Z

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.
4. 866A-01 IS OBSOLETE, NEW STANDARD 866A-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	107.82	108.08	4.245	4.255
B	31.62	31.88	1.245	1.255
C	—	9.14	—	0.360
D	1.02	1.07	0.040	0.042
F	3.18 BSC		0.125 BSC	
G	1.27 BSC		0.050 BSC	
H	—	0.25	—	0.010
J	1.19	1.37	0.047	0.054
K	0.25	—	0.100	—
L	44.45 REF		1.750 REF	
M	1.90	2.16	0.075	0.085
N	10.16 BSC		0.400 BSC	
P	3.18	—	0.125	—
Q	3.12	3.22	0.123	0.127
R	6.22	6.48	0.245	0.255
S	5.72	—	0.225	—
U	101.19 BSC		3.984 BSC	
V	—	5.28	—	0.208
W	1.12	—	0.044	—
X	1.52	1.63	0.060	0.064

Tape and Reel Data for MOS Memory Surface Mount Devices

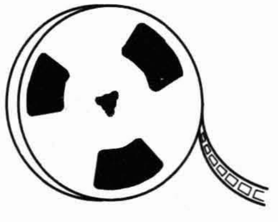
Embossed Tape and Reel

Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the "peel-back" cover tape.

- 13-Inch Reel
- Used For Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA-481
- SOJ: 24, 20/26, 24/26, 28, 32
- SOIC: 28, 32
- PLCC: 44, 52

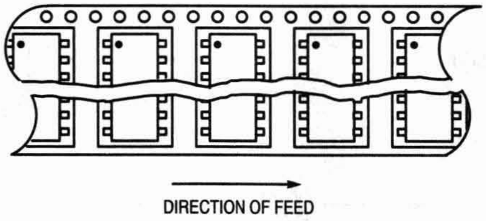
PACKAGES

SOJ: 24, 20/26, 24/26, 28, 32
SOIC: 28, 32
PLCC: 44, 52



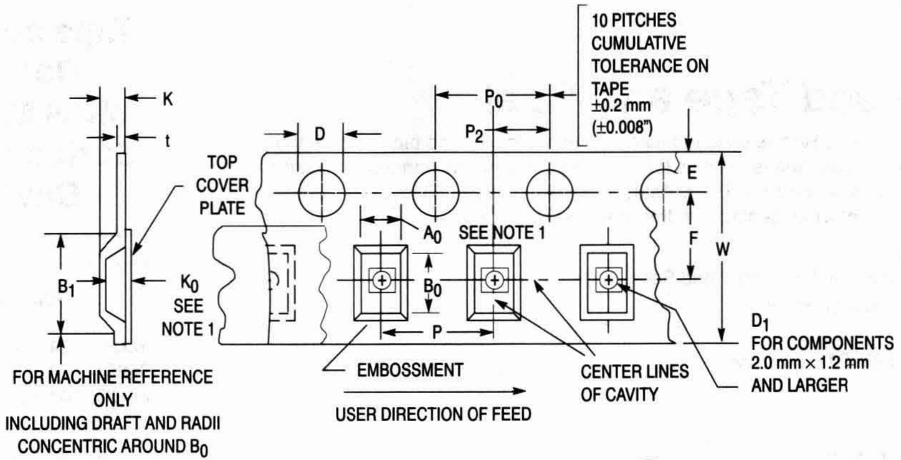
Ordering Information

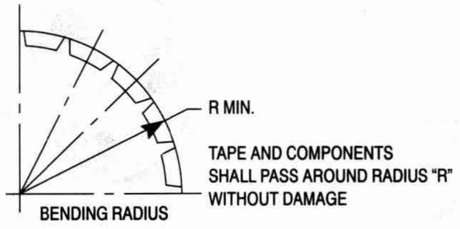
Use the standard device title and add the required suffix R2. Note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.

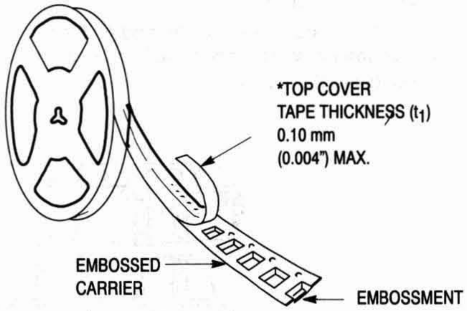


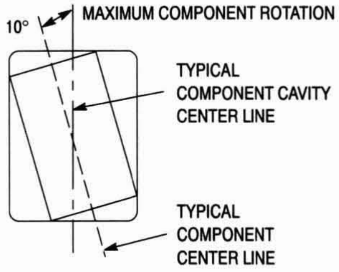
Package	Lead Count	Package Width (mils)	Tape Width (mm)	Reel Size	Devices Per Reel	Minimum Lot Size	Tape and Reel Suffix
SOJ	24	300	24	13"	1000	1000	R2
	20/26	300	24	13"	1000	1000	R2
	20/26	350	24	13"	1000	1000	R2
	24/26	300	24	13"	1000	1000	R2
	28	300	24	13"	1000	1000	R2
	28	400	24	13"	1000	1000	R2
	32	300	32	13"	1000	1000	R2
	32	400	32	13"	1000	1000	R2
SOIC (Gull Wing)	28	350	24	13"	1000	1000	R2
	32	450	32	13"	1000	1000	R2
PLCC	44	650/656	32	13"	500	500	R2
	52	750/756	32	13"	450	450	R2

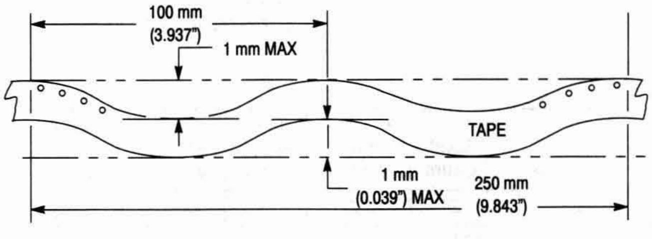
CARRIER TAPE SPECIFICATIONS


10 PITCHES CUMULATIVE TOLERANCE ON TAPE ±0.2 mm (±0.008")
K
t
P_0
P_2
D
TOP COVER PLATE
E
F
W
A_0
SEE NOTE 1
B_1
K_0 SEE NOTE 1
B_0
P
D_1 FOR COMPONENTS 2.0 mm × 1.2 mm AND LARGER
FOR MACHINE REFERENCE ONLY INCLUDING DRAFT AND RADII CONCENTRIC AROUND B_0
EMBOSSMENT
CENTER LINES OF CAVITY
USER DIRECTION OF FEED


R MIN.
TAPE AND COMPONENTS SHALL PASS AROUND RADIUS "R" WITHOUT DAMAGE
BENDING RADIUS


*TOP COVER TAPE THICKNESS (t_1) 0.10 mm (0.004") MAX.
EMBOSSED CARRIER
EMBOSSMENT


10°
MAXIMUM COMPONENT ROTATION
TYPICAL COMPONENT CAVITY CENTER LINE
TYPICAL COMPONENT CENTER LINE


100 mm (3.937")
1 mm MAX
TAPE
1 mm (0.039") MAX
250 mm (9.843")

CAMBER (TOP VIEW)
ALLOWABLE CAMBER TO BE 1 mm/100 mm NONACCUMULATIVE OVER 250 mm

DIMENSIONS

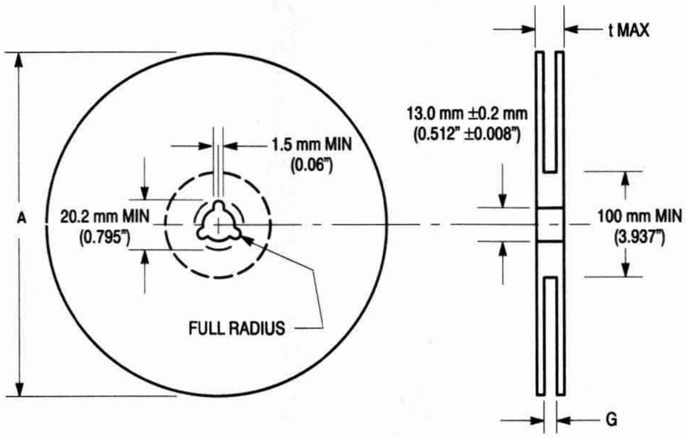
Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R Min	t Max	W
24 mm	19.4 mm (0.764")	1.5+0.1 mm −0.0 (0.059+0.004" −0.0)	2.0 mm Min (0.079")	1.75 ±0.1 mm (0.069 ±0.004")	11.5 ±0.1 mm (0.453 ±0.004")	4.0 mm (0.157")	12.0–16.0 ±0.10 mm (0.472–0.630 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.05 mm (0.079 ±0.002")	50 mm (1.968")	0.400 mm (0.016")	24 ±0.2 mm (0.945 ±0.008")
32 mm	23.0 mm (0.906")	1.5+0.1 mm −0.0 (0.059+0.004" −0.0)	2.0 mm Min (0.079")	1.75 ±0.1 mm (0.069 ±0.004")	14.2 ±0.1 mm (0.559 ±0.004")	10.0 mm (0.394")	16.0–24.0 ±0.10 mm (0.630–0.945 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.05 mm (0.079 ±0.002")	50 mm (1.968")	0.500 mm (0.020")	32 ±0.3 mm (1.26 ±0.012")

Metric Dimensions Govern–English are in parentheses for reference only.

NOTE 1: A_0, B_0, and K_0 are determined by compnent size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

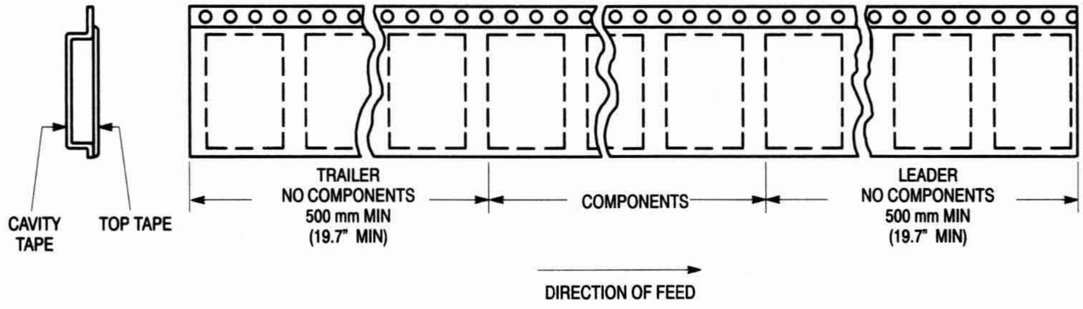
REEL DIMENSIONS

Metric Dimensions Govern–English are in Parentheses for Reference only.


t MAX
13.0 mm ±0.2 mm
(0.512" ±0.008")
1.5 mm MIN
(0.06")
A
20.2 mm MIN
(0.795")
100 mm MIN
(3.937")
FULL RADIUS
G

Size	A Max	G	t Max
24 mm	330 mm (12.992")	24.400 mm, +2.0 mm, –0.0 (0.961", +0.079", –0.00)	30.4 mm (1.197")
32 mm	330 mm (12.992")	32.4 mm, +2.0 mm, –0.0 (1.276", +0.079", –0.00)	38.4 mm (1.51")

TAPE ENDS


CAVITY TAPE
TOP TAPE
TRAILER
NO COMPONENTS
500 mm MIN
(19.7" MIN)
COMPONENTS
LEADER
NO COMPONENTS
500 mm MIN
(19.7" MIN)
DIRECTION OF FEED

1/4/93

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	Hall-Mark Electronics	(205)837-8700
	Time Electronics	(205)721-1133

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Tempe	Arrow/Schweber Electronics	(602)431-0030
	Time Electronics	(602)967-2000

CALIFORNIA

Agoura Hills	Time Electronics Corporate	(818)707-2890
Belmont	Richardson Electronics	(415)592-9225
Calabassas	Arrow/Schweber Electronics	(818)880-9686
	Wyle Laboratories	(818)880-9000
Chatsworth	Future Electronics	(818)772-6240
	Hall-Mark Electronics	(818)773-4500
	Time Electronics	(818)998-7200
Costa Mesa	Hamilton/Avnet Electronics	(714)754-6092
Culver City	Hamilton/Avnet Corporate	(213)558-2000
Gardena	Hamilton/Avnet Electronics	(213)516-6498
Irvine	Arrow/Schweber Electronics	(714)587-0404
	Future Electronics	(714)250-4141
	Hall-Mark Electronics	(714)727-6000
	Wyle Laboratories Corporate	(714)753-9953
	Wyle Laboratories	(714)863-9953
Mountain View	Richardson Electronics	(415)960-6900
Rocklin	Hall-Mark Electronics	(916)624-9781
Sacramento	Hamilton/Avnet Electronics	(916)925-2216
	Wyle Laboratories	(916)638-5282
San Diego	Arrow/Schweber Electronics	(619)565-4800
	Future Electronics	(619)278-5020
	Hall-Mark Electronics	(619)268-1201
	Hamilton/Avnet Electronics	(619)571-8730
	Wyle Laboratories	(619)565-9171
San Jose	Arrow/Schweber Electronics	(408)441-9700
	Arrow/Schweber Electronics	(408)428-6400
	Future Electronics	(408)434-1122
	Hall-Mark Electronics	(408)432-4000
Santa Clara	Wyle Laboratories	(408)727-2500
Sunnyvale	Hamilton/Avnet Electronics	(408)743-3300
	Time Electronics	(408)734-9888
Torrance	Time Electronics	(310)320-0880
Tustin	Time Electronics	(714)669-0100
Woodland Hills	Hamilton/Avnet Electronics	(818)594-0404
	Richardson Electronics	(615)594-5600

COLORADO

Broomfield	Future Electronics	(303)421-0123
Englewood	Arrow/Schweber Electronics	(303)799-0258
	Hall-Mark Electronics	(303)790-1662
	Hamilton/Avnet Electronics	(303)740-1000
	Time Electronics	(303)721-8882
Thornton	Wyle Laboratories	(303)457-9953

CONNECTICUT

Bethel	Future Electronics	(203)743-9594
Cheshire	Hall-Mark Electronics	(203)271-2844
Danbury	Hamilton/Avnet Electronics	(203)743-6077
Southbury	Time Electronics	(203)271-3200
Wallingfort	Arrow/Schweber Electronics	(203)265-7741

FLORIDA

Altamonte Springs	Future Electronics	(407)767-8414
Casselberry	Hall-Mark Electronics	(407)830-5855
Clearwater	Future Electronics	(813)530-1222
	Hall-Mark Electronics	(813)541-7440
Deerfield Beach	Arrow/Schweber Electronics	(305)429-8200
Ft. Lauderdale	Hamilton/Avnet Electronics	(305)767-6377
	Time Electronics	(305)484-1778
Lake Mary	Arrow/Schweber Electronics	(407)333-9300
Orlando	Hamilton/Avnet Electronics	(407)628-3888
	Time Electronics	(407)841-6565
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